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(12) **United States Patent**  
**You**(10) **Patent No.:** **US 8,356,152 B2**  
(45) **Date of Patent:** **Jan. 15, 2013**(54) **INITIATIVE WEAR LEVELING FOR  
NON-VOLATILE MEMORY**(75) Inventor: **Guangqing You**, Shanghai (CN)(73) Assignee: **Intel Corporation**, Santa Clara, CA  
(US)(\*) Notice: Subject to any disclaimer, the term of this  
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Zafman LLP(51) **Int. Cl.**  
**G06F 12/00** (2006.01)(52) **U.S. Cl.** ..... 711/165; 711/103; 711/173(58) **Field of Classification Search** ..... 711/103,  
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See application file for complete search history.

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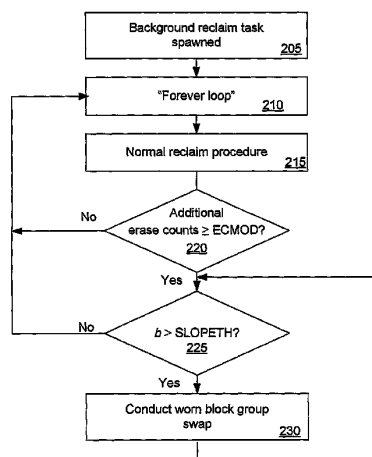
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**ABSTRACT**

A method and apparatus for initiative wear leveling for non-volatile memory. An embodiment of a method includes counting erase cycles for each of a set of multiple memory blocks of a non-volatile memory, the counting of erase cycles for each memory block including incrementing a first count for a physical block address of the memory block, and if the memory block is not a spare memory block, incrementing a second count for a logical block address of the memory block. The method also includes determining whether the non-volatile memory has uneven wear of memory blocks based at least in part on the counting of the erase cycles of the plurality of memory blocks.

**16 Claims, 9 Drawing Sheets**

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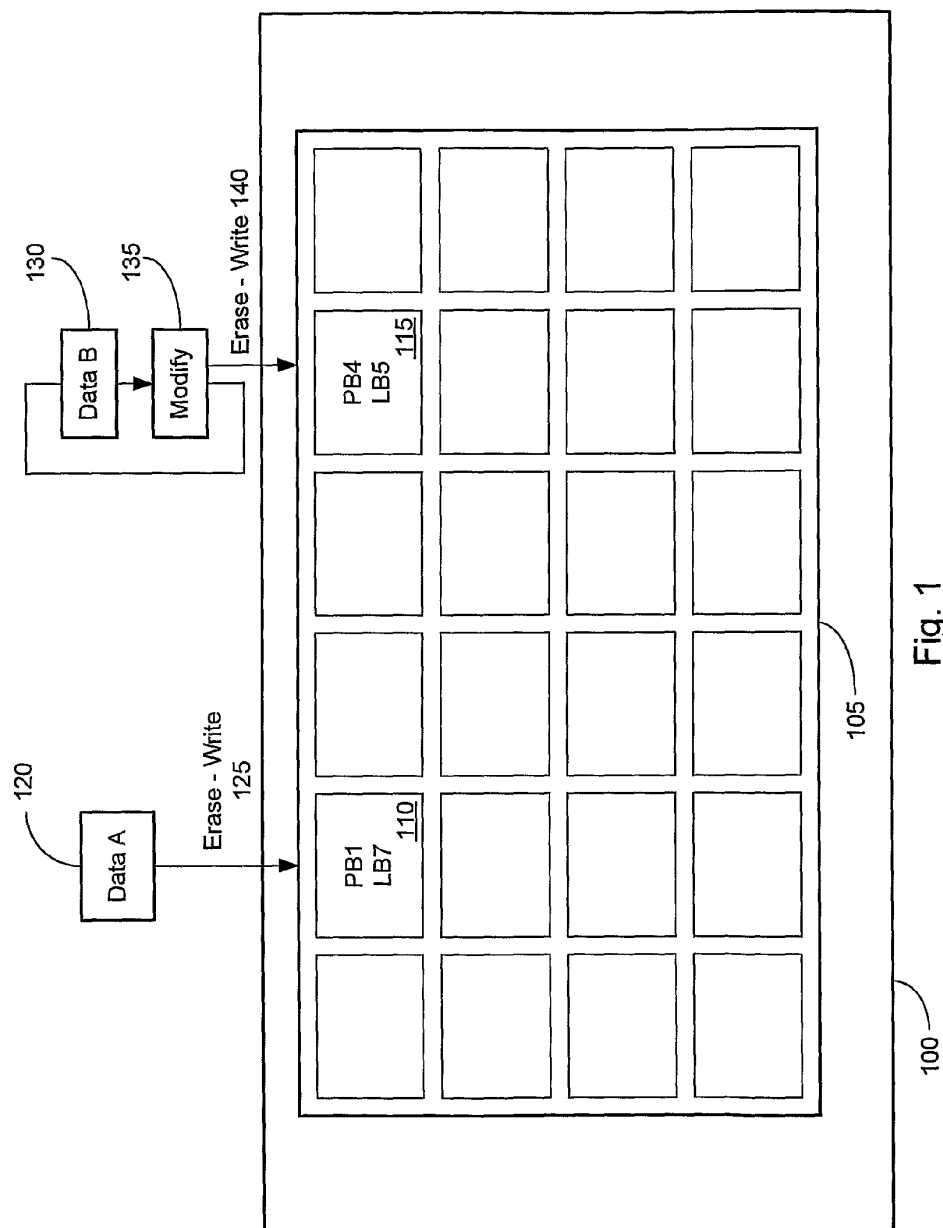


Fig. 1

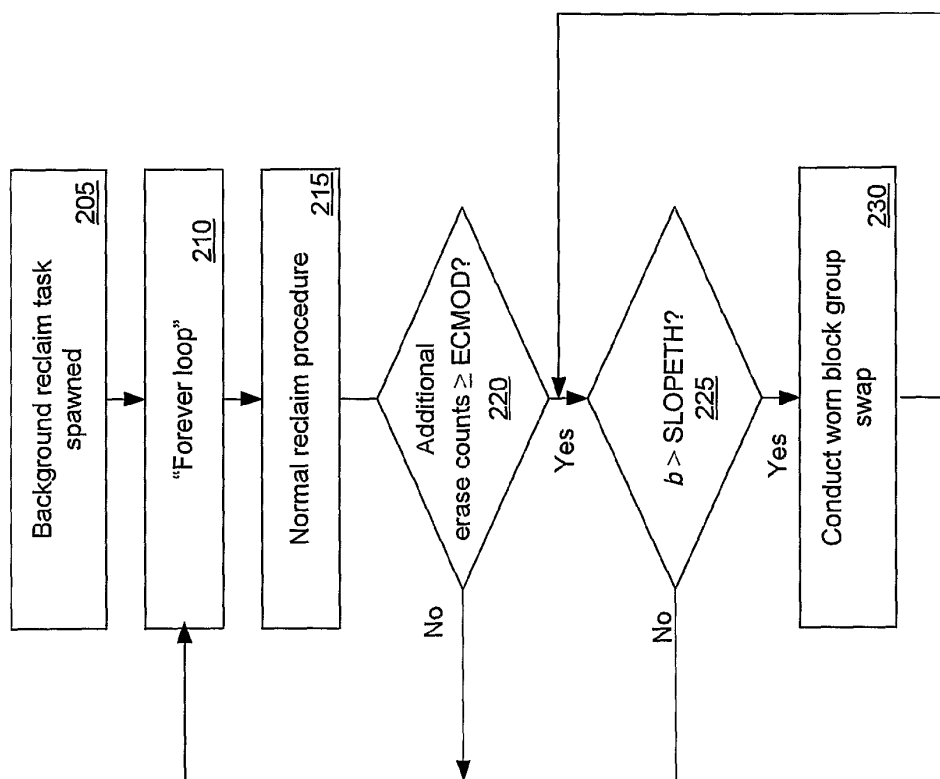


Fig. 2

Fig. 3A

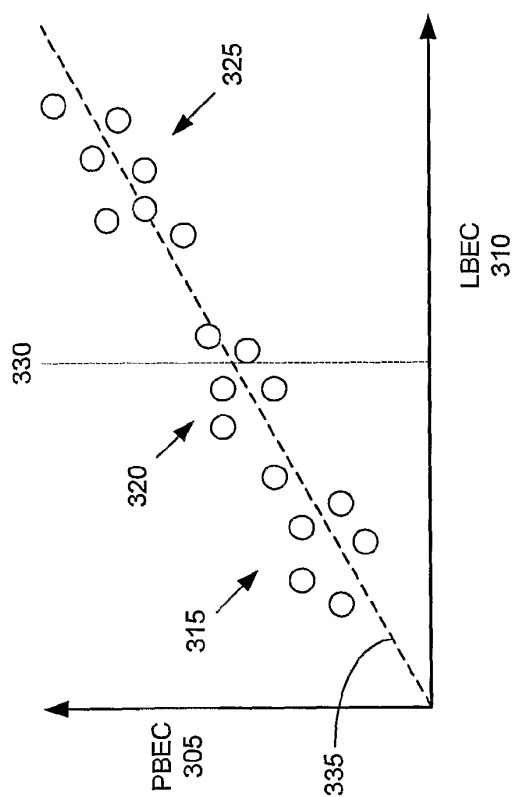
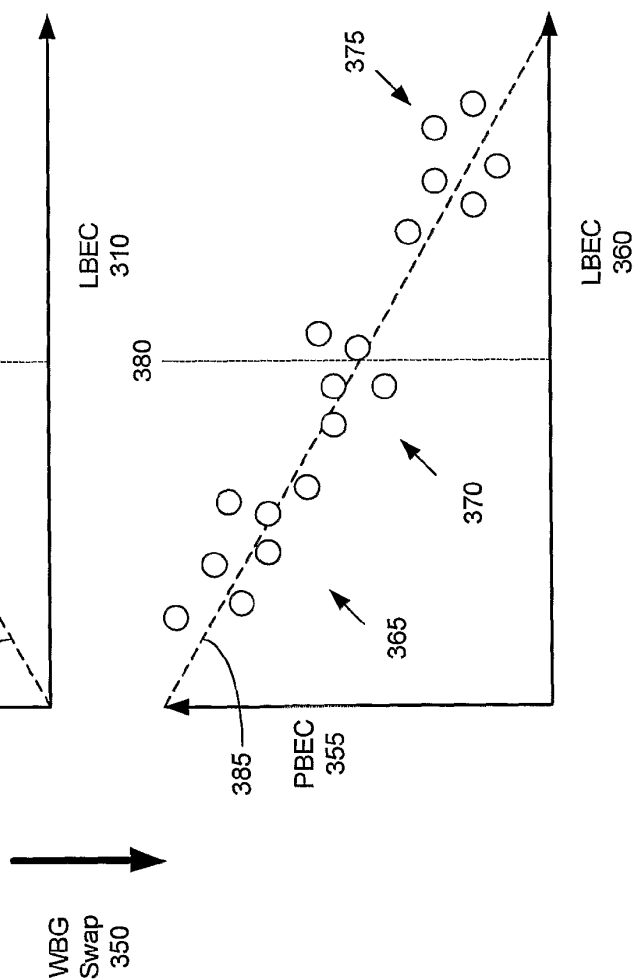


Fig. 3B



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