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You

(10) **Patent No.:** **US 8,356,152 B2**
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- (54) **INITIATIVE WEAR LEVELING FOR NON-VOLATILE MEMORY**
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- (73) Assignee: **Intel Corporation**, Santa Clara, CA (US)
- (*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 580 days.

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- (51) **Int. Cl.**
G06F 12/00 (2006.01)

- (52) **U.S. Cl.** **711/165; 711/103; 711/173**

- (58) **Field of Classification Search** **711/103, 711/165, 173**

See application file for complete search history.

(57) **ABSTRACT**

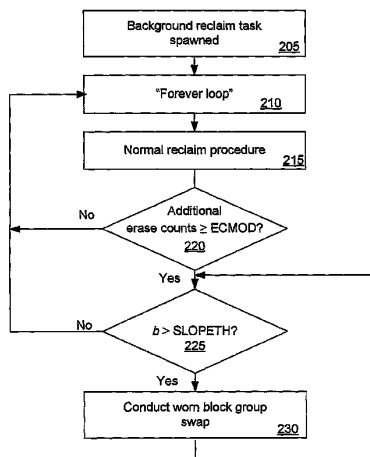
A method and apparatus for initiative wear leveling for non-volatile memory. An embodiment of a method includes counting erase cycles for each of a set of multiple memory blocks of a non-volatile memory, the counting of erase cycles for each memory block including incrementing a first count for a physical block address of the memory block, and if the memory block is not a spare memory block, incrementing a second count for a logical block address of the memory block. The method also includes determining whether the non-volatile memory has uneven wear of memory blocks based at least in part on the counting of the erase cycles of the plurality of memory blocks.

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16 Claims, 9 Drawing Sheets



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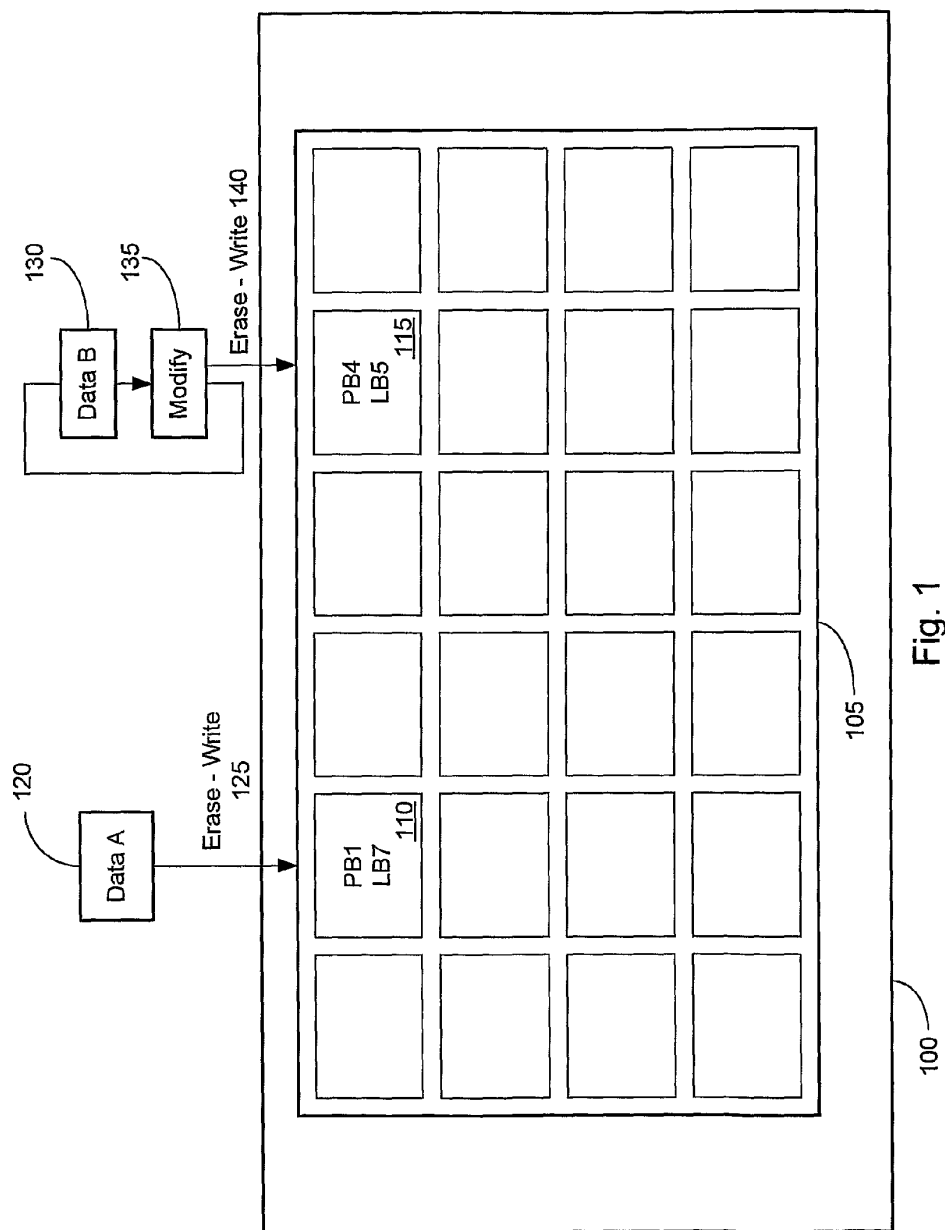


Fig. 1

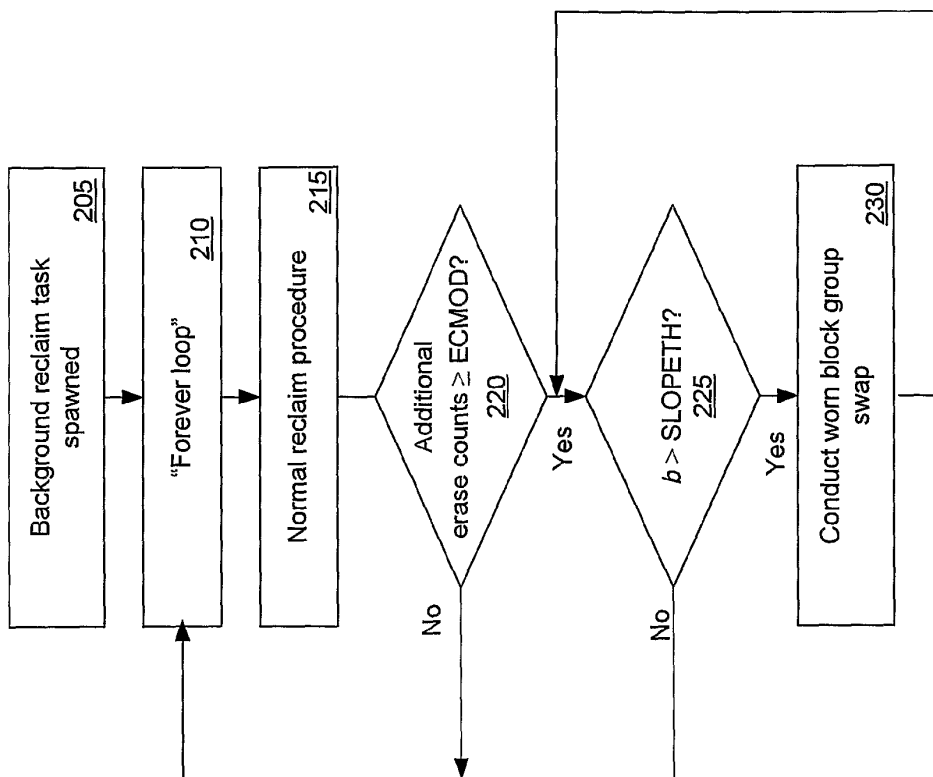


Fig. 2

Fig. 3A

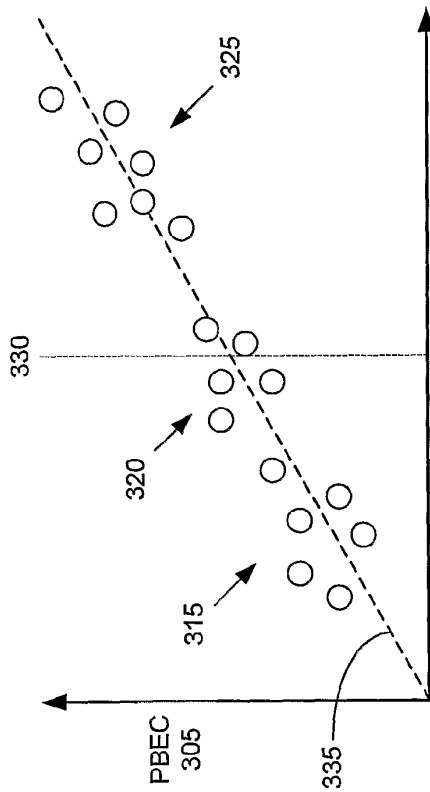
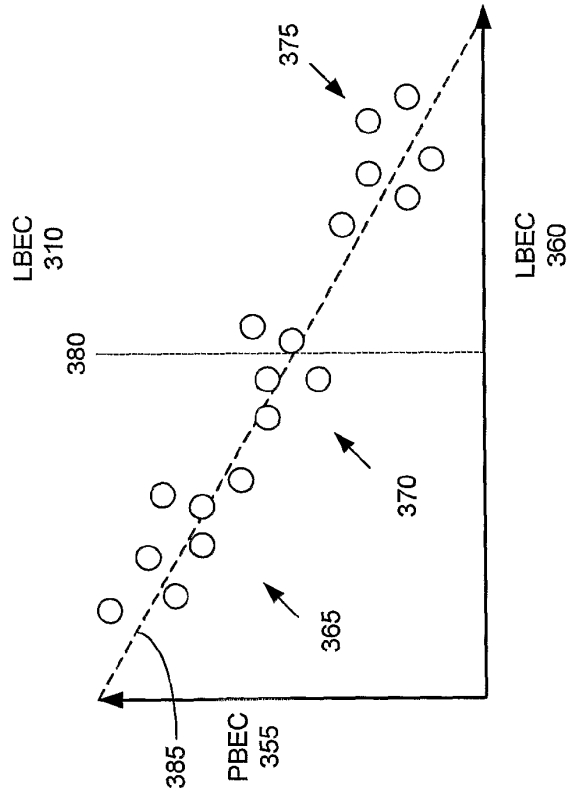


Fig. 3B



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