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(54) **WEAR LEVELING METHOD FOR NON-VOLATILE MEMORY DEVICE HAVING SINGLE AND MULTI LEVEL MEMORY CELL BLOCKS**

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(57) **ABSTRACT**

A method of executing a wear leveling operation within a non-volatile memory including a single-level memory cell block (SLC) and a multi-level memory cell block (MLC) is disclosed. The method includes calculating an average erase point in relation to a number of programming/erase (P/E) operations applied to a logical block address (LBA), a SLC mode usage point in relation to a number of the P/E operations applied to the SLC, a MLC mode usage point in relation to a number of the P/E operations applied to the MLC, and a wear value in relation to the average erase point, the SLC mode usage point, and the MLC mode usage point; and then if the wear value exceeds a defined threshold value, performing the wear leveling operation.

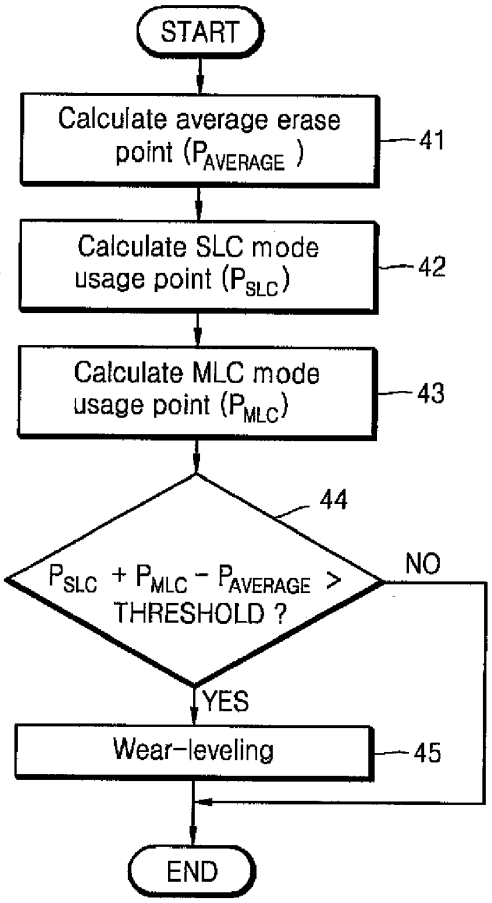

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FIG. 1 (PRIOR ART)

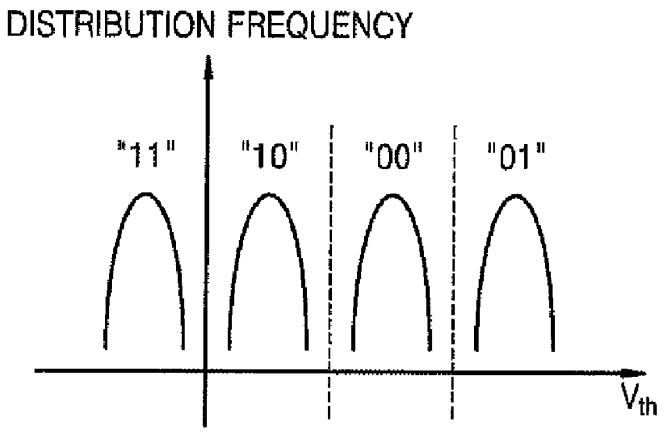

FIG. 2

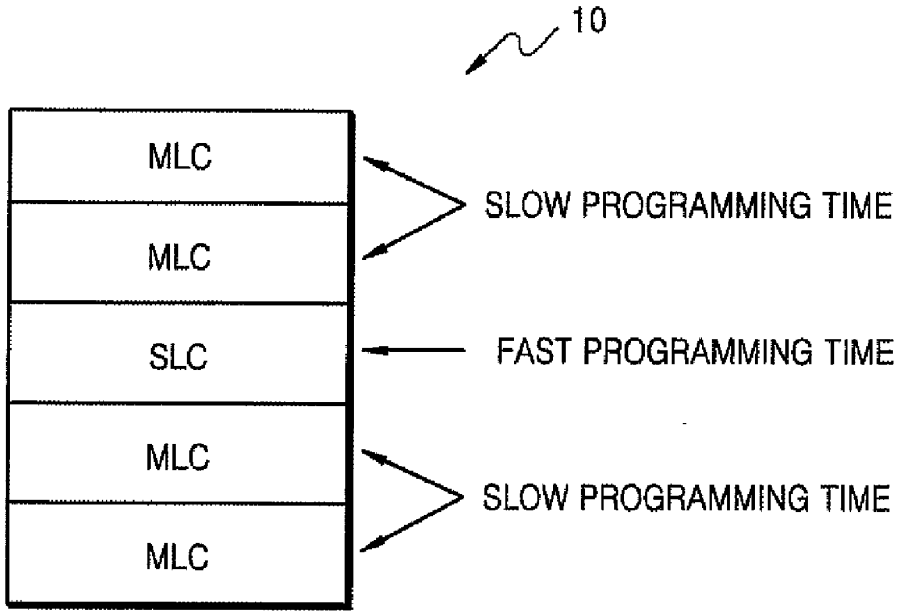

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FIG. 3A

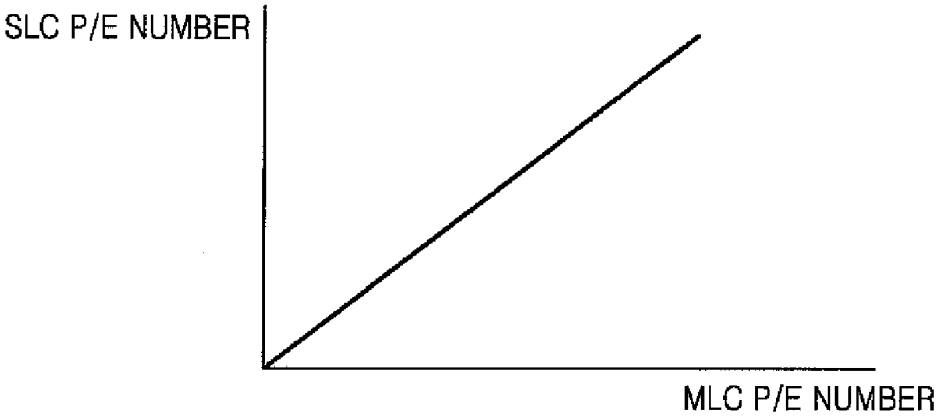

FIG. 3B

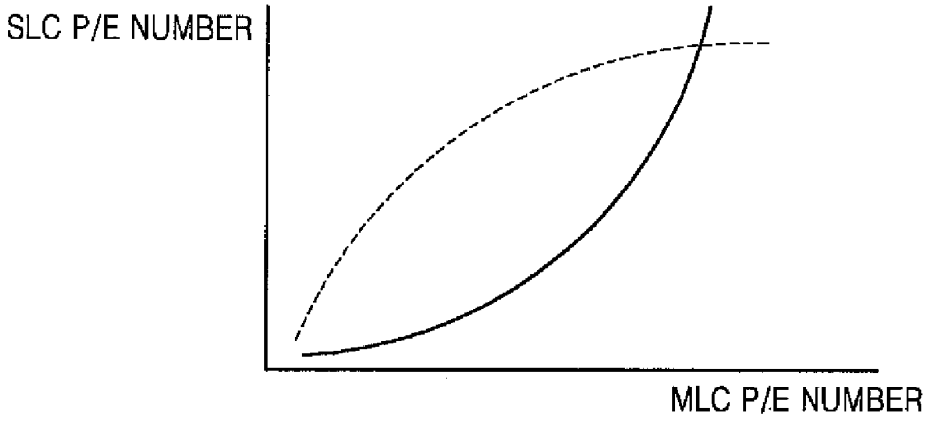

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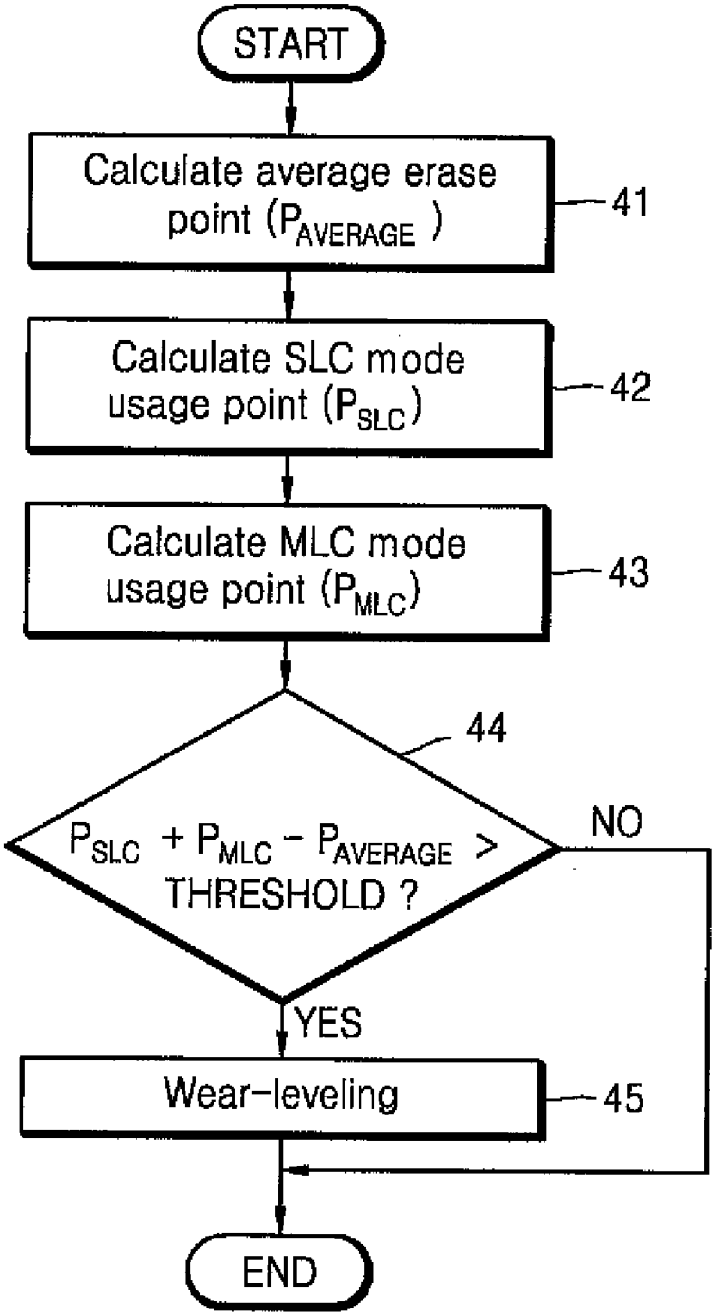
FIG. 4



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WEAR LEVELING METHOD FOR NON-VOLATILE MEMORY DEVICE HAVING SINGLE AND MULTI LEVEL MEMORY CELL BLOCKS

CROSS-REFERENCE TO RELATED APPLICATION

[0001] This application claims the benefit of Korean Patent Application No. 10-2008-0109467 filed on Nov. 5, 2008, the subject matter of which is hereby incorporated by reference.

BACKGROUND

[0002] The inventive concept relates generally to non-volatile memory devices. More particularly, the inventive concept relates to non-volatile memory devices including both single level and multi level memory cell blocks, wherein a wear leveling method is performed.

[0003] Due to their compact size and excellent performance characteristics, contemporary memory systems requiring repetitive reprogramming capabilities and non-volatile data storage are increasingly implemented with non-volatile memory cells, such as those found in conventional flash memory. Flash memory was initially implemented with single level memory cells configured to store one bit of information (i.e., data values of "0" and "1") using a single memory cell transistor. However, as data storage demands have increased over time, flash memory has increasingly been implemented with so-called multi level memory cells capable of storing two or more bits of information using a single memory cell transistor.

[0004] A threshold voltage distribution (Vth) for a two bit multi level memory cell having four stored data states is illustrated in Figure (FIG. **1**. The four data states equate respectively to data values of "01", "00", "10", or "11". In this manner, two bits of information may be stored in the multi level memory cell. The storage capacity of the illustrated two bit, multi level memory cell essentially allows a doubling of the storage capacity of a constituent memory cell array without greatly enlarging the area occupied by the array, as compared with the use of single bit memory cells.

[0005] Unfortunately, the data programming (or write) speed of the multi level memory cell is markedly slower than that of the single level memory cell. This reduced write speed is tolerable for much of the data commonly written to a contemporary memory system, but there are certain types of data requiring frequent update that benefit from the higher write speed afforded by single level memory cells. This being the case, it is not uncommon to find memory system including both multi level and single level memory blocks. For example, certain "fast programming time" memory blocks intended to receive relatively high speed data (e.g., data requiring frequent update) are implemented with single level memory cells. In contrast, other "slow programming time" memory blocks intended to receive relatively slow speed data (e.g., bulk payload data or data not normally requiring frequent update) are implemented with multi level memory cells. In this manner, a hybrid memory system of sorts provides a large data storage capacity due to the presence of the multi level memory cell (fast) blocks and high speed data access due to the presence of the single level memory (slow) blocks.

[0006] During operation, both the fast and slow memory blocks are repeatedly programmed and erased. It is well known that only a certain number of erase operations may be executed in relation to each flash memory block and/or corresponding physical memory cells before the constituent memory cells become too worn to ensure reliable operation. In other words, the operative lifespan of each memory block is defined in terms of a maximum number of programming and/or erase cycles. For conventional multi level memory cell (slow) blocks, this maximum number is currently defined in terms of about ten thousand erase operations. For conventional single level memory cell (fast) blocks, this maximum number is defined in terms of between one hundred thousand and a million erase operations. However defined, once a flash memory block has exceeded its maximum number of use cycles, it must be withdrawn from or replaced in operation within the constituent memory system. Otherwise, the integrity of the flash memory system can not be assured and the loss of user data or host device failure becomes a very real possibility.

[0007] Thus, the "wear" placed upon a flash memory block (or the physical memory array location of memory cells functionally implementing the memory block) will vary according to its use (i.e., a number of programming, erase, etc., operations executed in relation to the memory block). Recognizing that flash memory cell wear is a function of physically exercising a memory cell (or memory cell block), it should also be recognized that any operation performed in relation to a particular memory cell is performed in relation to a so-called logic block address (LBA). The LBA is used by the host device incorporating the flash memory system to indicate one or more memory cells to be programmed or erased, for example. Assuming a static relationship between a LBA and corresponding portion of the flash memory array, repeated commands by the host device directed to the same LBA will ultimately wear the memory cells associated with the corresponding physical location.

[0008] As noted above, uneven wear of some memory cells to the point of lifespan exhaustion may well impair the performance of the entire flash memory system. That is, a single overly worn memory block may cause the memory system to fail.

[0009] In order to extend the operative life of the memory system, therefore, and to ensure that the plurality of flash memory blocks are evenly worn, a wear leveling operation is often performed. In one approach, a wear leveling operation changes the mapping relationship between a given LBA (i.e., a frequently used LBA) and the physical location of corresponding memory cells (or a memory block) within flash memory. In this manner, repeated commands to a frequently used LBA will not result in the uneven wear of memory cells in a particular physical location. By rotating physical locations under the same frequently used LBA, a collection of flash memory blocks will wear much more evenly, thereby extending the overall lifespan of the entire memory system.

SUMMARY

[0010] Embodiments of the inventive concept provide a wear leveling method operable within a non-volatile memory device including at least one single level memory cell block and a plurality of multi level memory cell blocks.

[0011] In one embodiment, a method of executing a wear leveling operation within a non-volatile memory including a single-level memory cell block (SLC) and a multi-level memory cell block (MLC) includes; calculating an average erase point in relation to a number of programming/erase

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