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Li et al.

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(54) **MULTILEVEL PHASE-CHANGE MEMORY ELEMENT AND OPERATING METHOD**

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(51) **Int. Cl.**
GI1C 11/34 (2006.01)

(52) **U.S. Cl.** 365/185.03; 365/163

(58) **Field of Classification Search** 365/161,
365/163, 185.03, 46, 148; 257/1, 2
See application file for complete search history.

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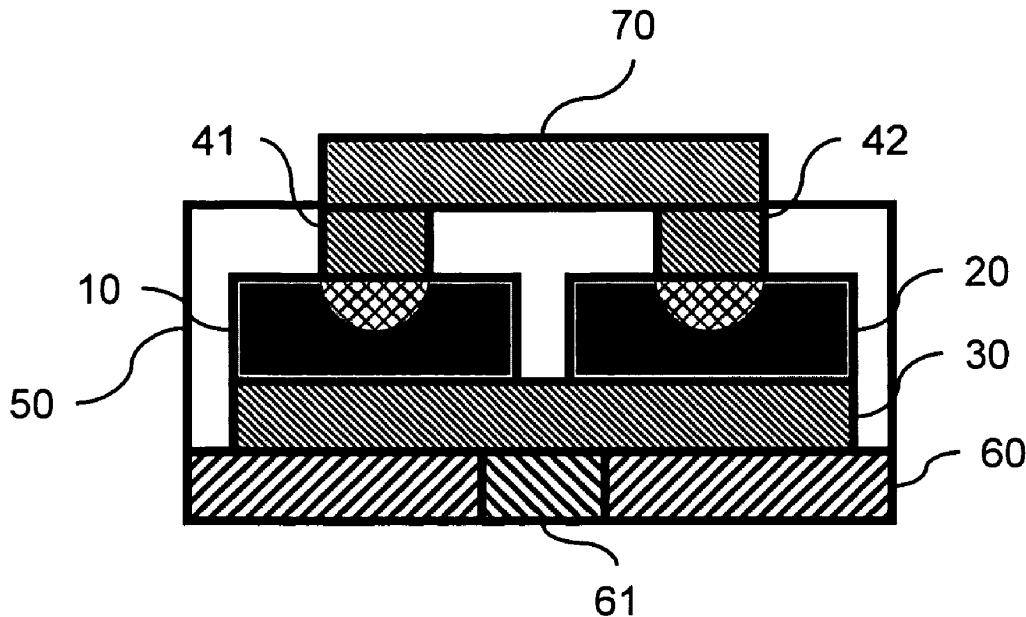
* cited by examiner

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(57) **ABSTRACT**

A multilevel phase change memory element and operating method and electrodes, which are configured in a parallel structure to form a memory cell. A voltage-drive mode is employed to control and drive the memory element such that multilevel memory states may be achieved by imposing different voltage levels. The provided multilevel phase-change memory element has more bits and higher capacity than that of a memory element with a single phase-change layer.

23 Claims, 13 Drawing Sheets



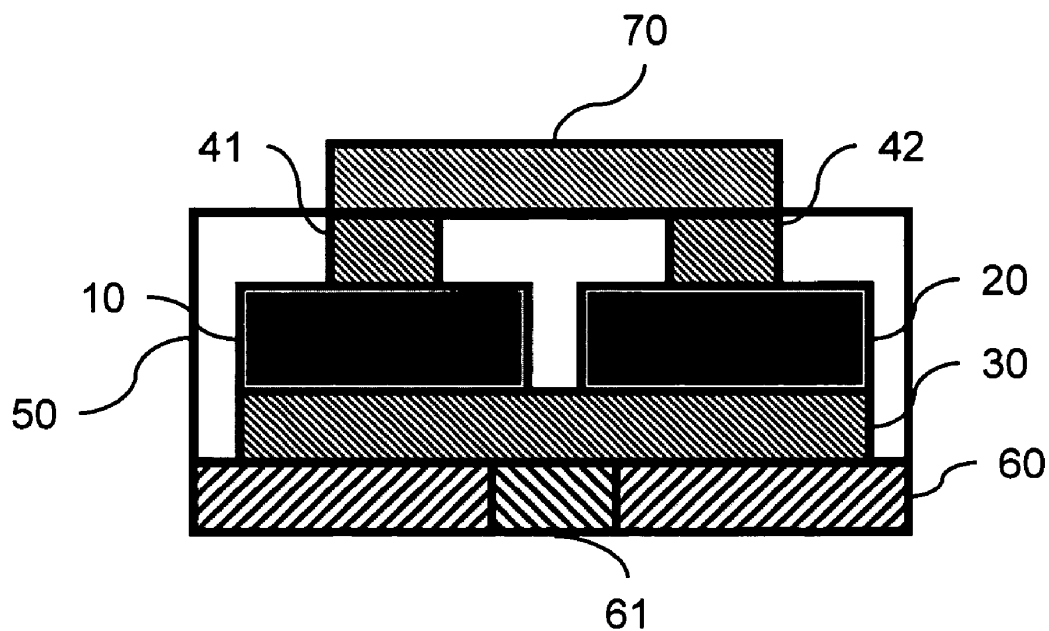


FIG. 1

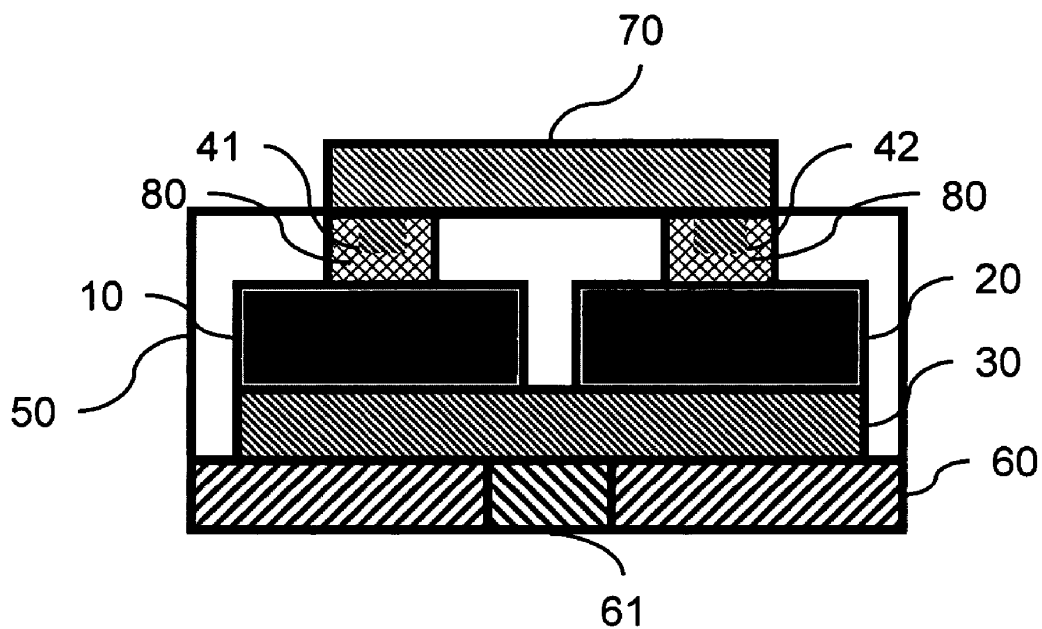


FIG. 2

FIG. 3A

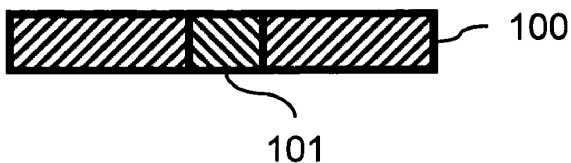


FIG. 3B

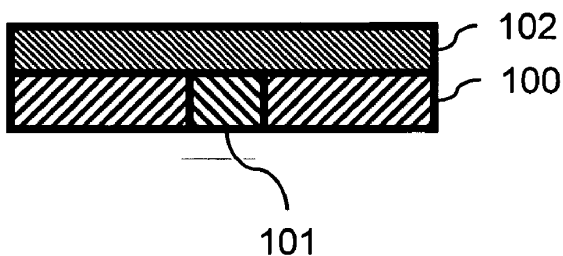


FIG. 3C

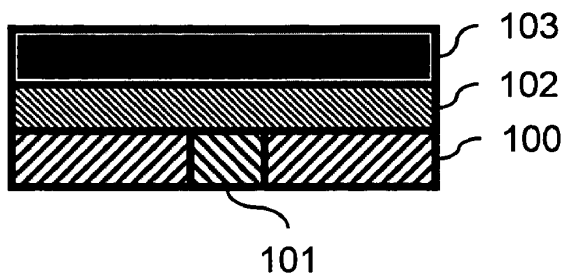


FIG. 3D

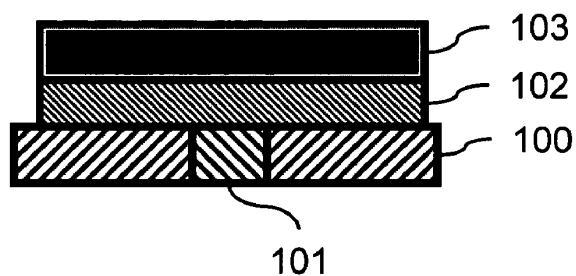
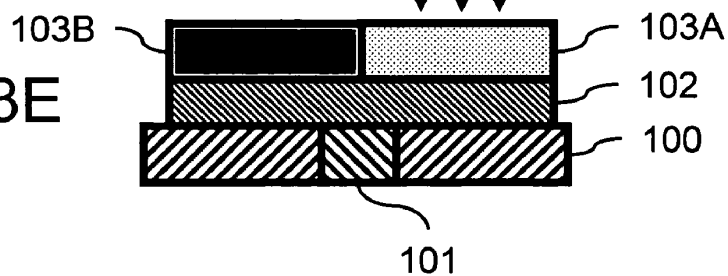
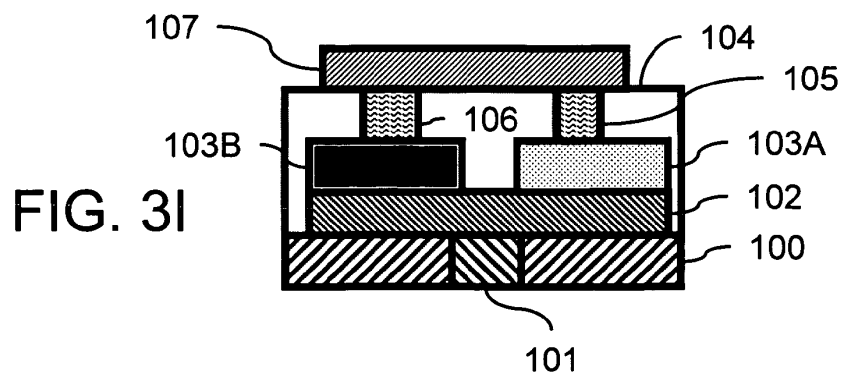
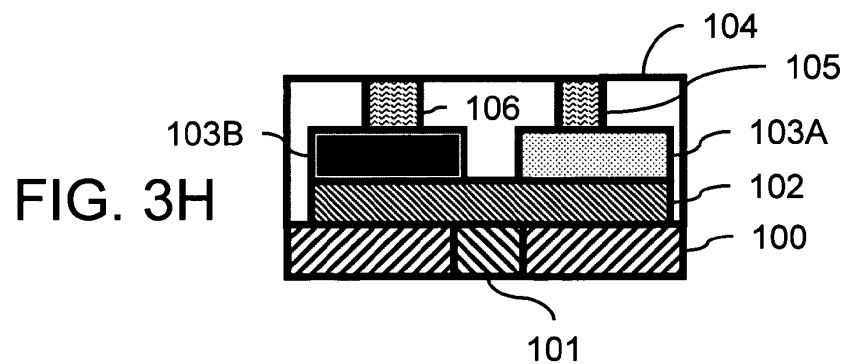
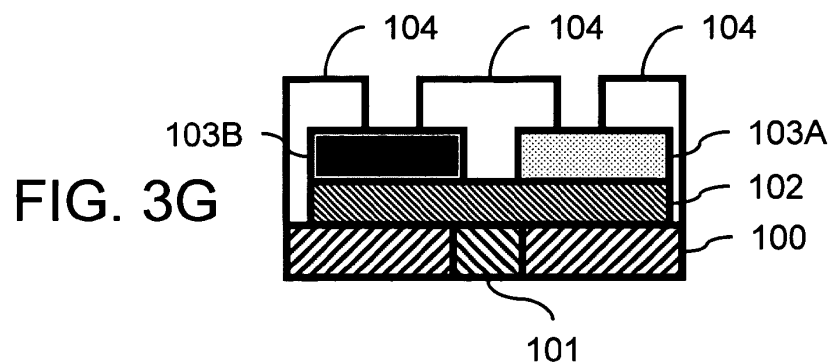
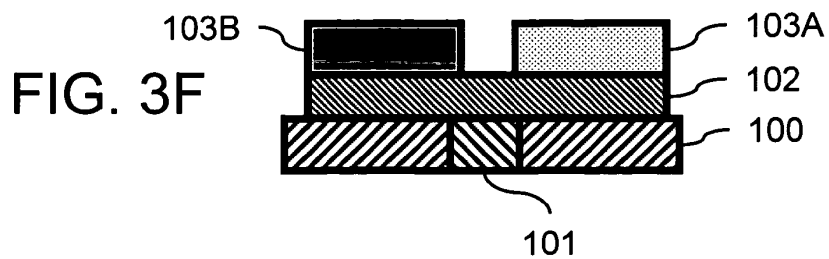


FIG. 3E





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