

**UNITED STATES PATENT AND TRADEMARK OFFICE**

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**BEFORE THE PATENT TRIAL AND APPEAL BOARD**

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MICRON TECHNOLOGY, INC.,  
Petitioner

v.

VERVAIN,LLC,  
Patent Owner

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Case No.: IPR2021-01547  
U.S. Patent No. 8,891,298  
Original Issue Date: November 18, 2014

Title: LIFETIME MIXED LEVEL NON-VOLATILE MEMORY SYSTEM

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**DECLARATION OF DR. DAVID LIU**

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c.	[1.B] “at least one SLC non-volatile memory module comprising a plurality of individually erasable blocks; and” .....	85
d.	[1.C] “a controller coupled to the at least one MLC non-volatile memory module and the at least one SLC non-volatile memory module wherein the controller is adapted to:” .....	87

e. [1.D] “maintain an address map of at least one of the MLC and SLC non-volatile memory modules, the address map comprising a list of logical address ranges accessible by a computer system, the list of logical address ranges having a minimum quanta of addresses, wherein each entry in the list of logical address ranges maps to a similar range of physical addresses within either the at least one SLC non-volatile memory module or within the at least one MLC non-volatile memory module;” .....89

f. [1.E] “determine if a range of addresses listed by an entry and mapped to a similar range of physical addresses within the at least one MLC non-volatile memory module, fails a data integrity test, and, in the event of such a failure, the controller remaps the entry to the next available equivalent range of physical addresses within the at least one SLC non-volatile memory module;” .....93

g. [1.F] “determine which of the blocks of the plurality of the blocks in the MLC and SLC non-volatile memory modules are accessed most frequently by maintaining a count of the number of times each one of the blocks is accessed” .....93

h. [1.G] “allocate those blocks that receive the most frequent writes by transferring the respective contents of those blocks to the at least one SLC non-volatile memory module;” .....96

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