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(54) **BALANCED PERFORMANCE FOR ON-CHIP FOLDING OF NON-VOLATILE MEMORIES**

Publication Classification

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(57) **ABSTRACT**

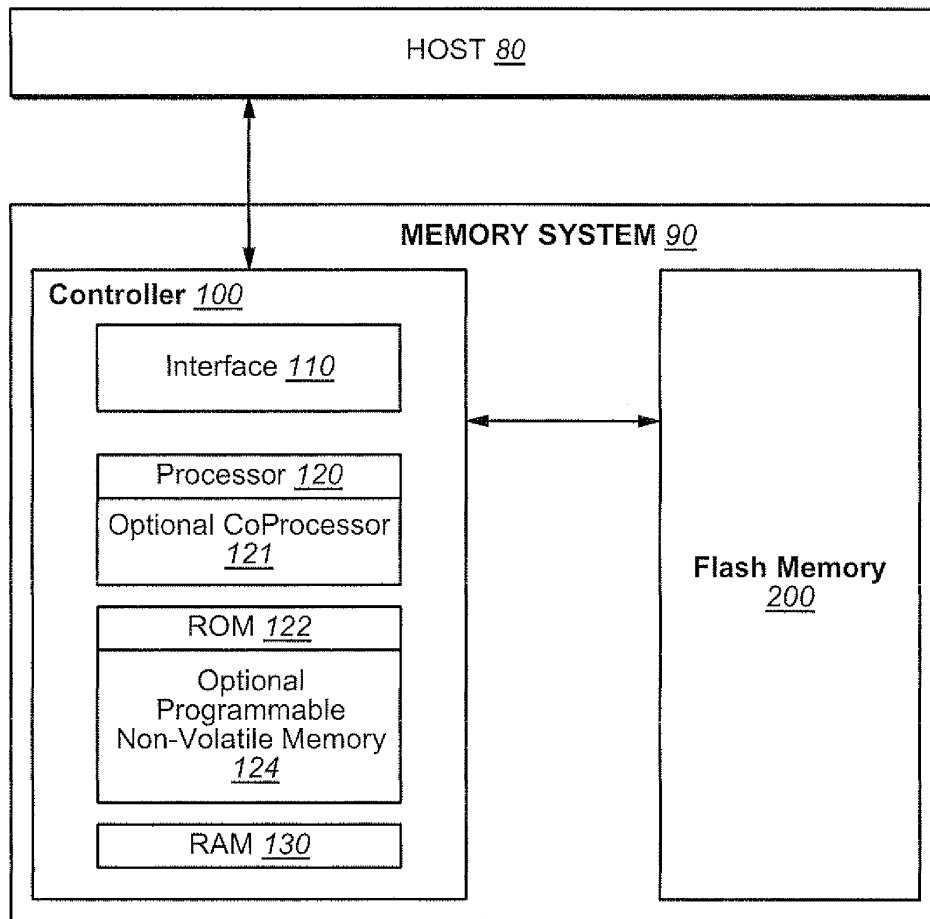
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A non-volatile memory system receives and stores host data. As the memory system receives host data, it initially writes the data in a binary format and then subsequently performs an on-chip folding operation on the data, storing the data in a multi-state format. The memory system interleaves the phases of the folding operations so that performance is made more uniform across allocation units, where the host stores data according to allocation units. The memory system also can perform the binary and subsequent on-chip folding operations on multiple memory planes in parallel, where the controller also balances the operations so that performance is made more uniform between planes with respect to allocation units as the data is received from the host. To further maintain performance, the memory system uses a free block list having a reserve portion that is only accessible for a specified set of commands.

Related U.S. Application Data

(63) Continuation-in-part of application No. 12/642,611, filed on Dec. 18, 2009, Continuation-in-part of application No. 12/642,649, filed on Dec. 18, 2009, now Pat. No. 8,144,512.

(60) Provisional application No. 61/495,053, filed on Jun. 9, 2011.



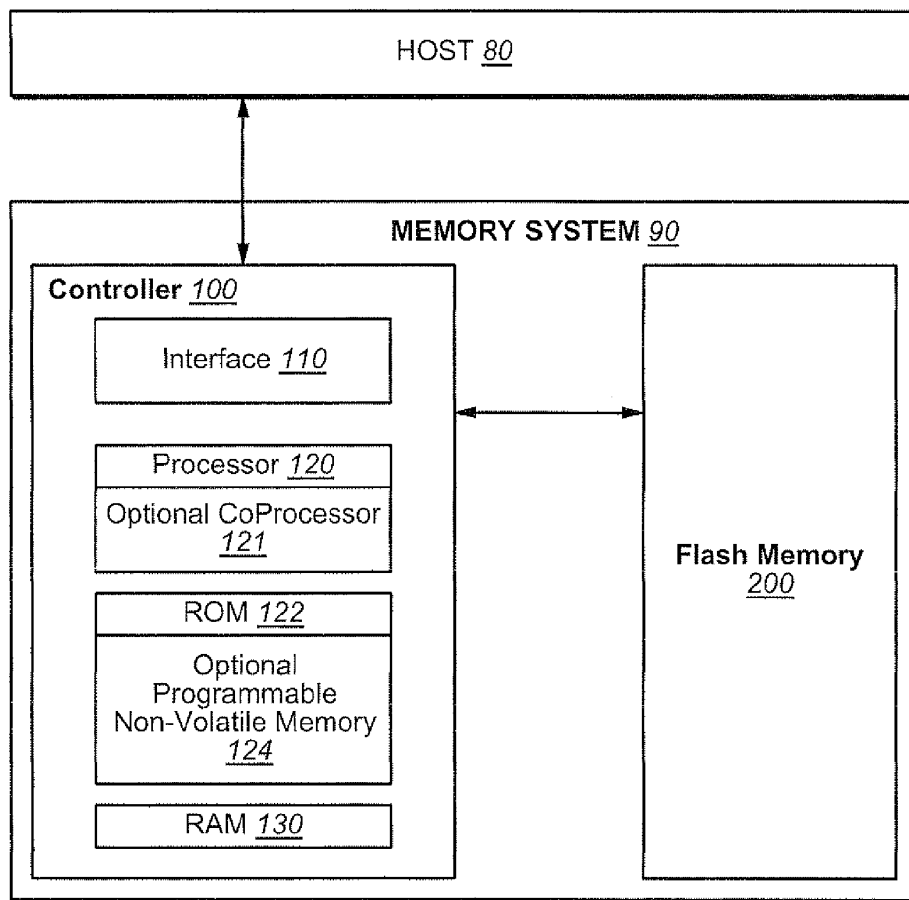


FIG. 1

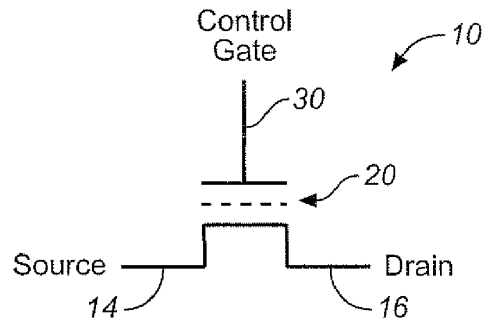


FIG. 2

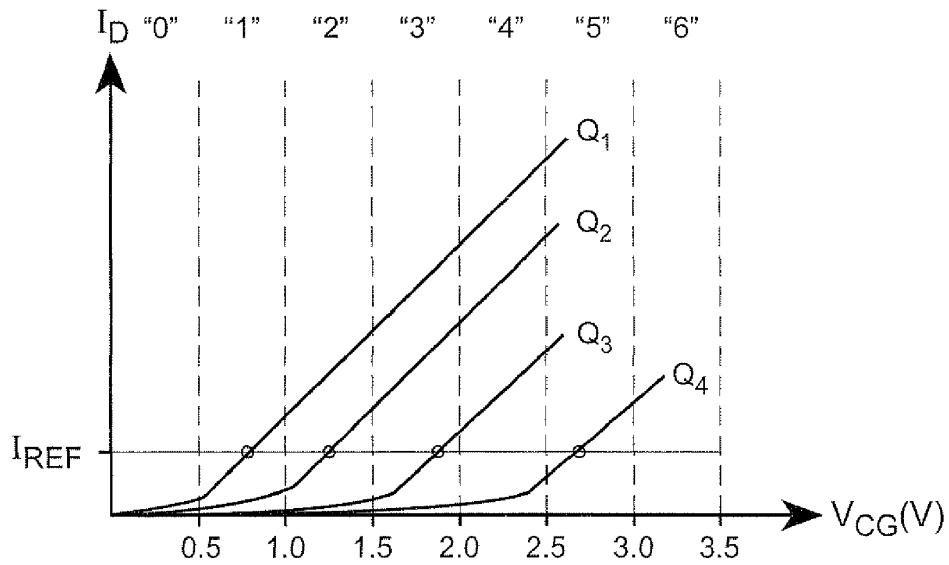


FIG. 3

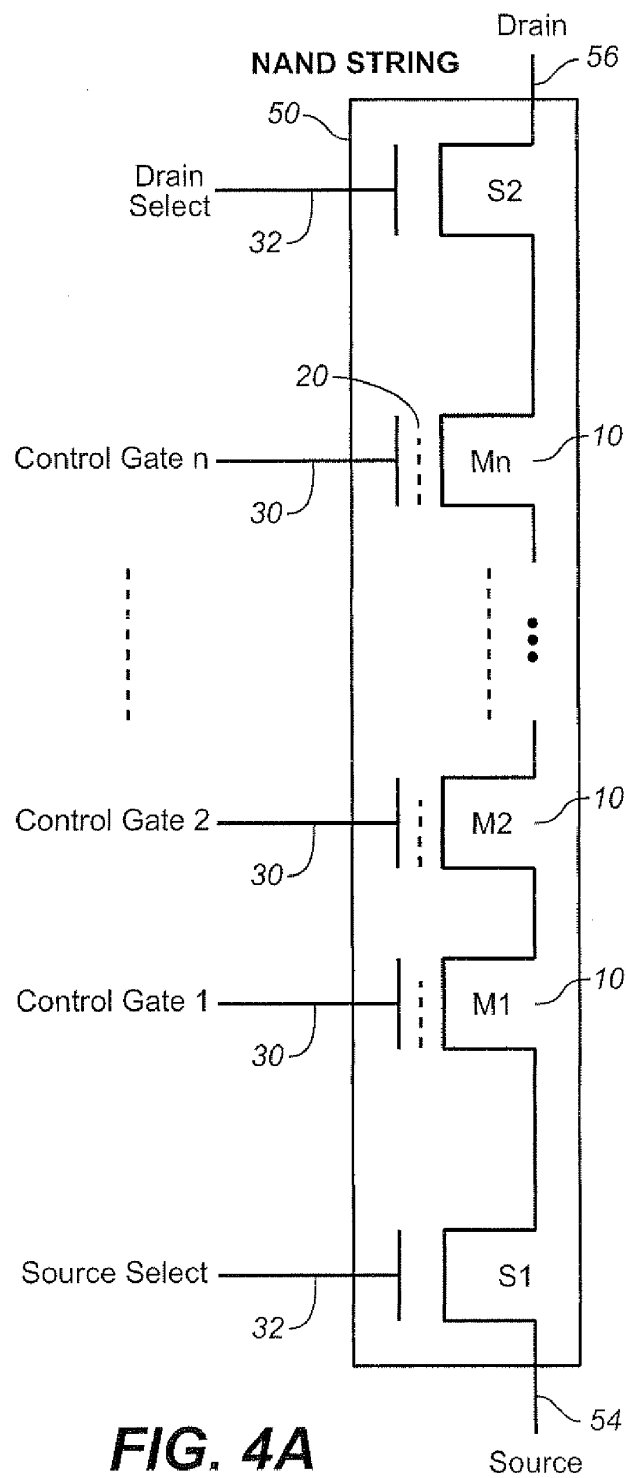


FIG. 4A

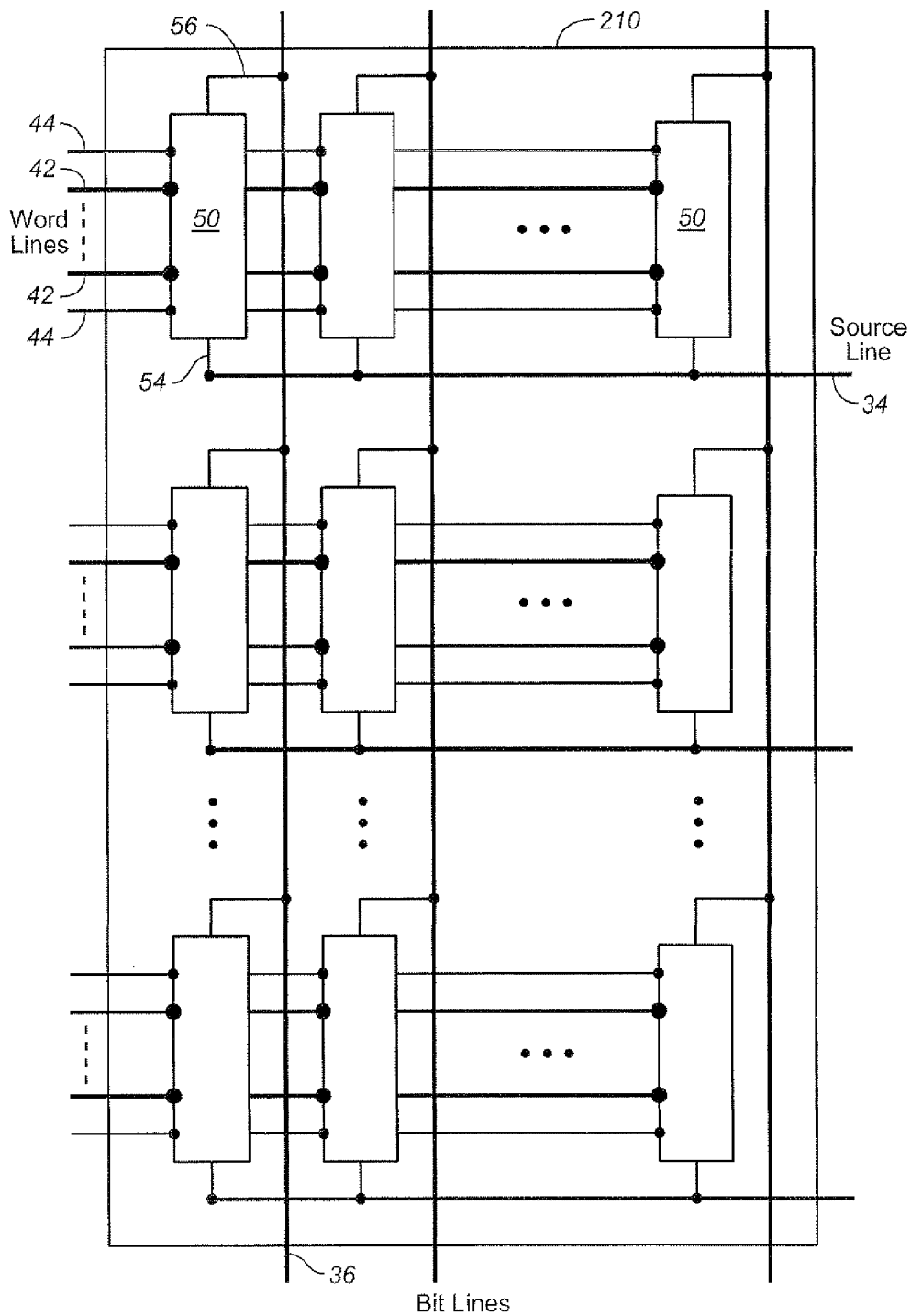


FIG. 4B

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