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(54) **NON-VOLATILE MEMORY AND METHOD WITH ACCELERATED POST-WRITE READ TO MANAGE ERRORS**

(52) **U.S. Cl. .... 365/185.09; 365/185.17; 365/185.03**

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(57) **ABSTRACT**

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Data errors in non-volatile memory inevitably increase with usage and with higher density of bits stored per cell. The memory is configured to have a first portion operating with less error but of lower density storage, and a second portion operating with a higher density but less robust storage. An error management provides reading and checking the copy after copying to the second portion. If the copy has excessive error bits, it is repeated in a different location either in the second or first portion. The reading and checking of the copy is accelerated by reading only a sample of it. The sample is selected from a subset of the copy having its own ECC and estimated to represent a worst error rate among the copy it is sampling. One embodiment has the sample taken from one bit of each multi-bit memory cell of a group.

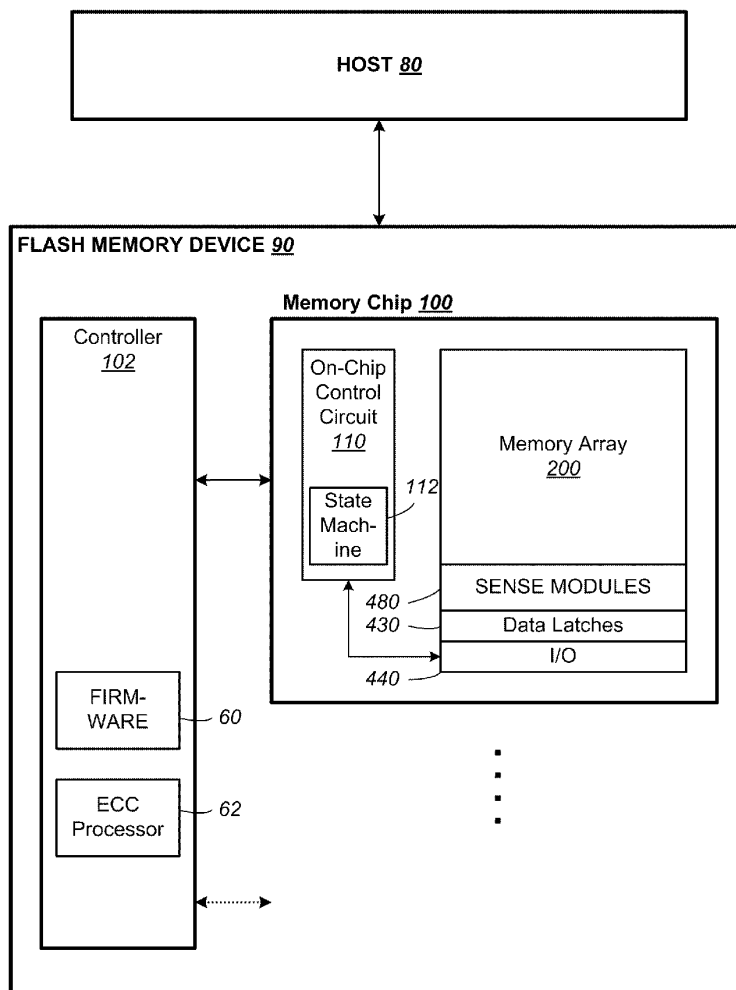
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**Related U.S. Application Data**

(63) Continuation-in-part of application No. 12/642,728, filed on Dec. 18, 2009, which is a continuation-in-part of application No. 12/607,522, filed on Oct. 28, 2009.

**Publication Classification**

(51) **Int. Cl. GIIC 16/06 (2006.01)**



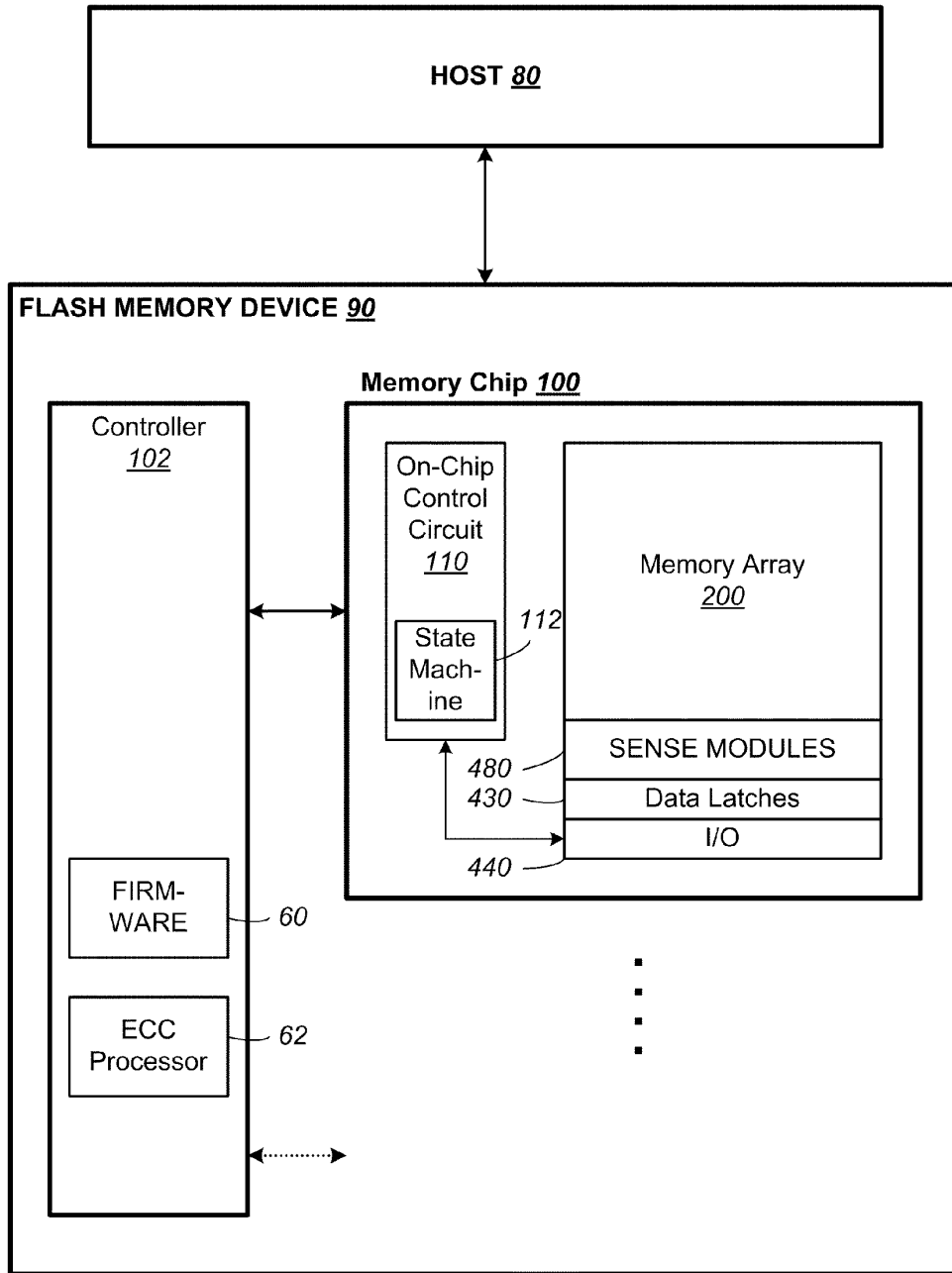
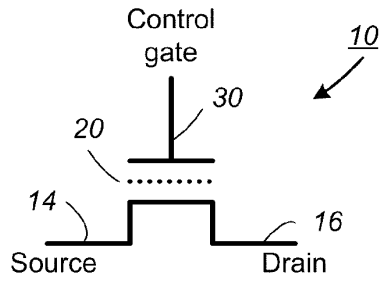
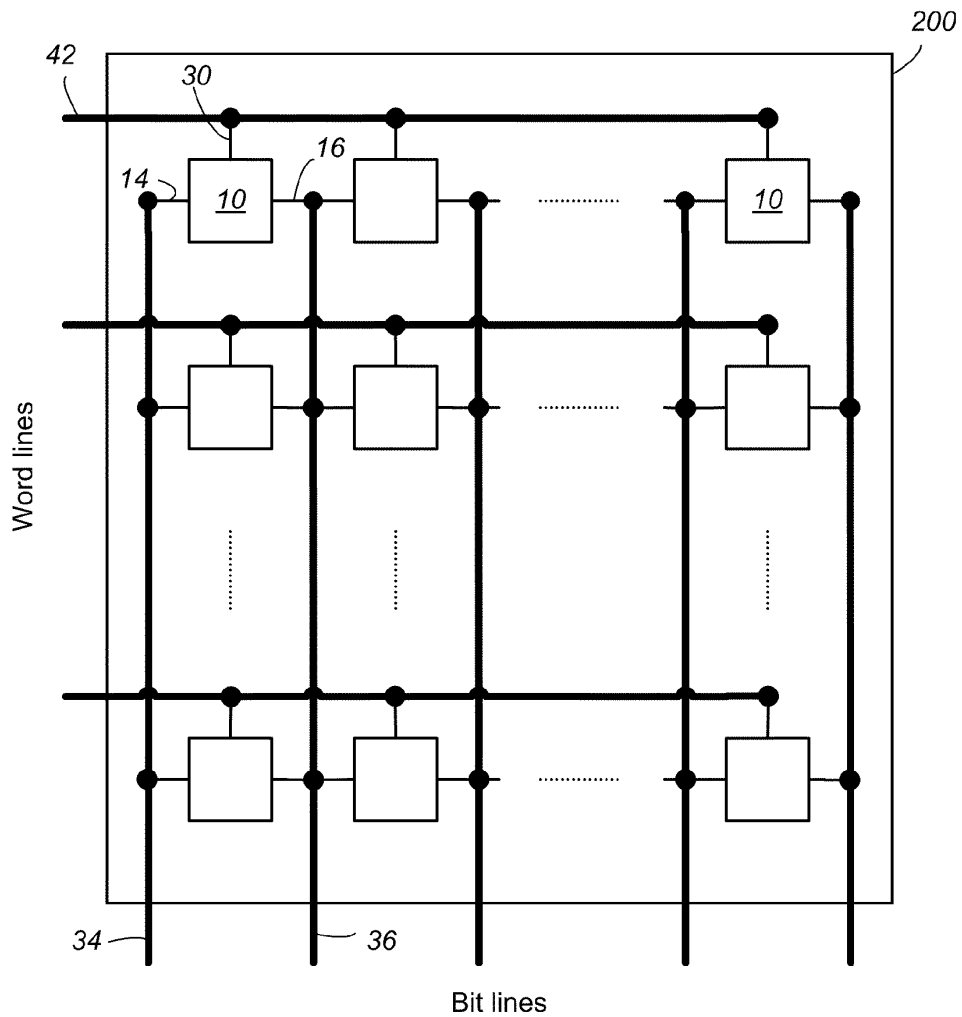


FIG. 1



**FIG. 2**



**FIG. 3**

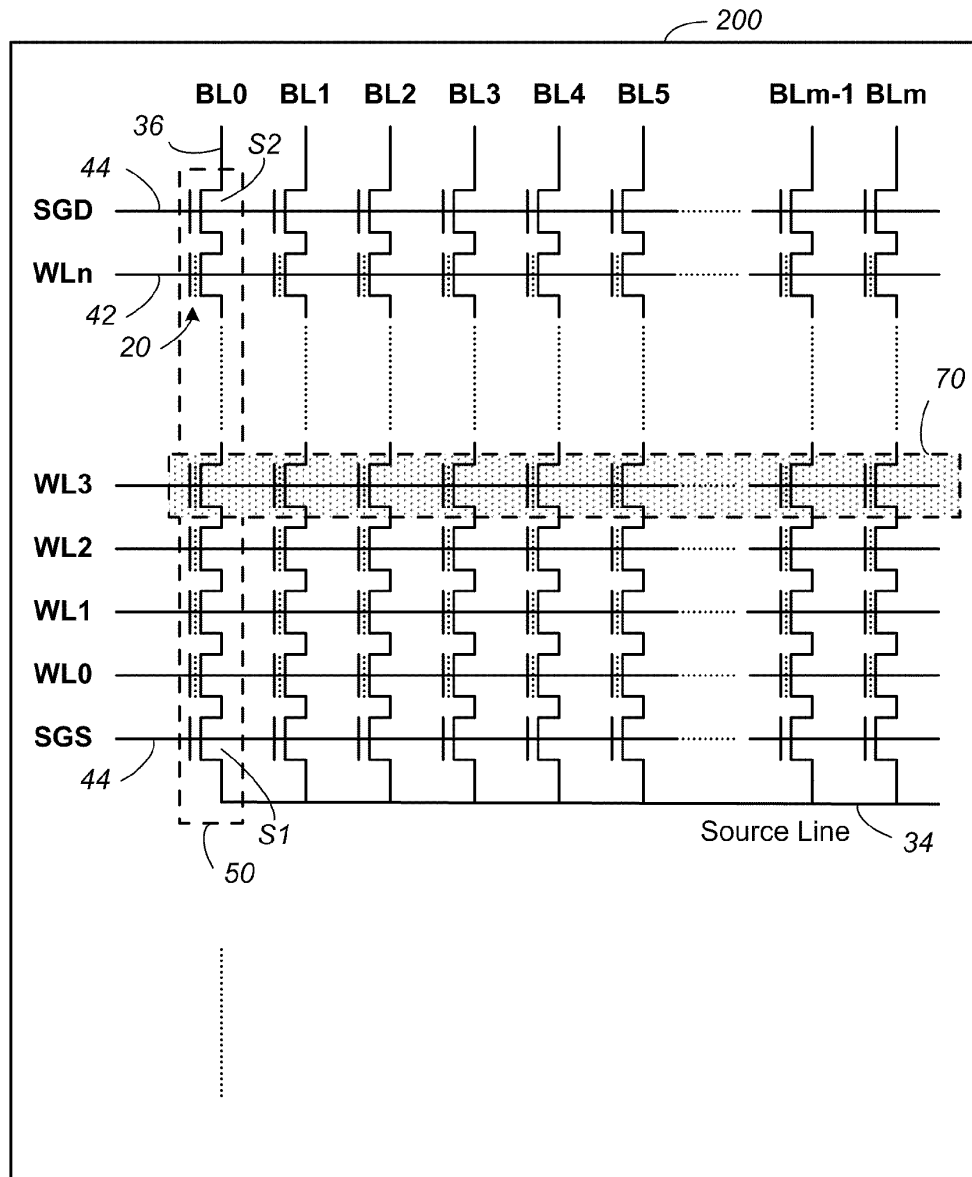


FIG. 4

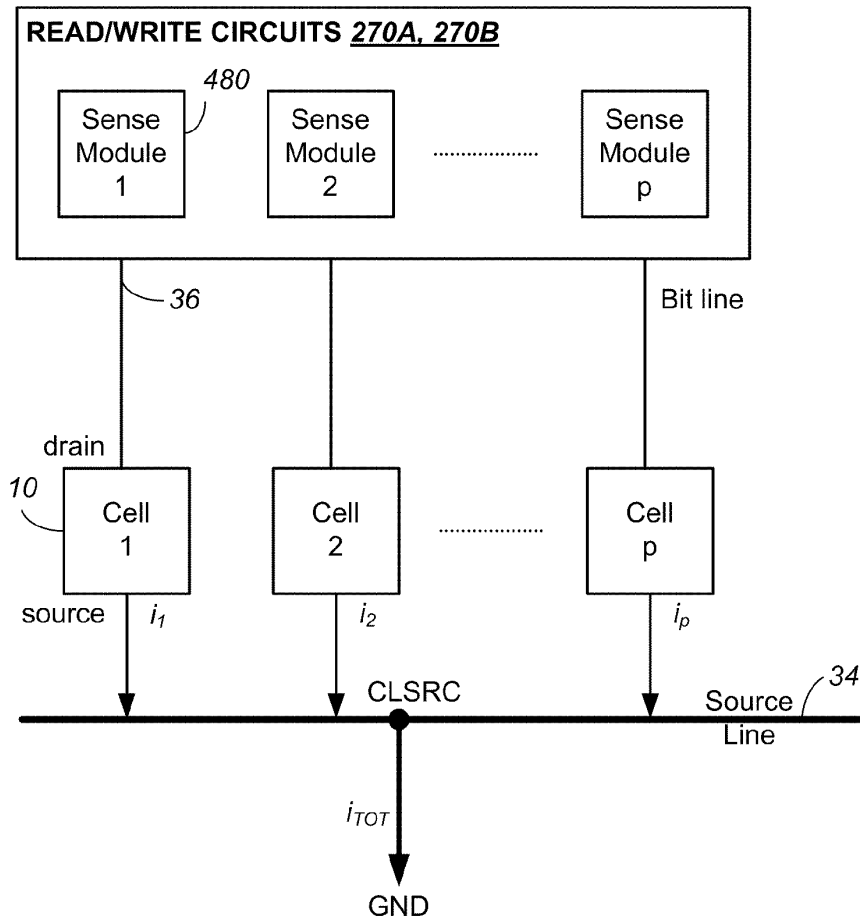


FIG. 5A

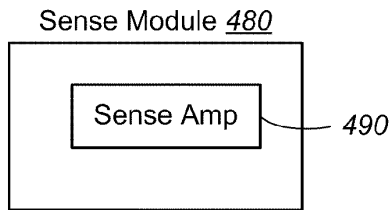


FIG. 5B

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