

IN THE UNITED STATES DISTRICT COURT  
FOR THE WESTERN DISTRICT OF TEXAS  
WACO DIVISION

VERVAIN, LLC,  
*Plaintiff*

-v-

MICRON TECHNOLOGY, INC.,  
MICRON SEMICONDUCTOR  
PRODUCTS, INC., MICRON  
TECHNOLOGY TEXAS, LLC  
*Defendants*

W-21-CV-00487-ADA

VERVAIN, LLC,  
*Plaintiff*

-v-

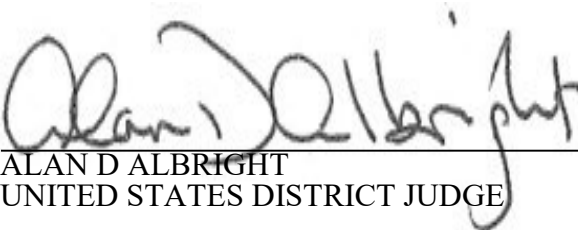
WESTERN DIGITAL  
CORPORATION, WESTERN  
DIGITAL TECHNOLOGIES, INC.,  
HGST, INC.  
*Defendants*

W-21-cv-00488-ADA

**CLAIM CONSTRUCTION ORDER**

The Court held a *Markman* hearing on January 24, 2022. During that hearing, the Court provided its final constructions. The Court now enters those claim constructions.

SIGNED this 24th day of January, 2022.

  
ALAN D ALBRIGHT  
UNITED STATES DISTRICT JUDGE

Term	Plaintiff's Proposed Construction	Defendants' Proposed Construction	C C
<p>#1: "SLC non-volatile memory"</p> <p>U.S. Patent No. 8,891,298, Claims 1, 5; U.S. Patent No. 9,196,385, Claims 1, 5; U.S. Patent No. 9,997,240, Claims 1, 6; U.S. Patent No. 10,950,300, Claims 1, 3, 4, 7, 12</p> <p>Proposed by Western Digital</p>	<p>Plain and ordinary meaning, where the plain and ordinary meaning is "nonvolatile memory that stores one bit of information per cell"</p>	<p>Western Digital: "non-volatile memory where each cell is capable of storing no more than one bit of information per cell"</p>	<p>Plain and where the meaning is memory th informatio</p>
<p>#2: "MLC non-volatile memory"</p> <p>U.S. Patent No. 8,891,298, Claims 1, 4; U.S. Patent No. 9,196,385, Claims 1, 4; U.S. Patent No. 9,997,240, Claims 1, 6; U.S. Patent No. 10,950,300, Claims 1, 3, 4, 12</p> <p>Proposed by Western Digital</p>	<p>Plain and ordinary meaning, where the plain and ordinary meaning is "nonvolatile memory that stores multiple bits of information per cell"</p>	<p>Western Digital: "non-volatile memory where each cell is capable of storing multiple bits of information per cell"</p>	<p>Plain and where the meaning is memory th bits of inf</p>

Term	Plaintiff's Proposed Construction	Defendants' Proposed Construction	C C
<p>#3: "data integrity test"</p> <p>U.S. Patent No. 8,891,298, Claim 1; U.S. Patent No. 9,196,385, Claim 1; U.S. Patent No. 9,997,240, Claim 1; U.S. Patent No. 10,950,300, Claims 1, 7, 12</p> <p>Proposed by Micron</p>	<p>Plain and ordinary meaning</p>	<p>Micron: Plain and ordinary meaning, which is "testing data for errors after the data has been written to flash"</p>	<p>Plain-and-</p>
<p>#4: "comparing the stored data to the retained data in the random access volatile memory"</p> <p>U.S. Patent No. 10,950,300, Claims 1, 7, 12</p> <p>Proposed by Defendants</p>	<p>Plain and ordinary meaning</p>	<p>"comparing the data obtained by reading the nonvolatile memory space to the data retained as part of a Write access operation, wherein both sets of the data are in the same random access volatile memory"</p>	<p>Plain-and-</p>
<p>#5: "to achieve enhanced endurance"</p> <p>U.S. Patent No. 10,950,300, Claims 1, 7, 12</p> <p>Proposed by Micron</p>	<p>"Plain and ordinary meaning"</p>	<p>Micron: Plain and ordinary meaning, which is "to achieve endurance (i.e., lifetime) superior to that of the MLC nonvolatile memory element"</p>	<p>Plain-and-</p>

Term	Plaintiff's Proposed Construction	Defendants' Proposed Construction	C C
<p>#6: "the list of logical address ranges having a minimum quanta of addresses"</p> <p>U.S. Patent No. 8,891,298, Claim 1;                      U.S. Patent No. 9,196,385, Claim 1;                      U.S. Patent No. 9,997,240, Claims 1, 6</p> <p>Proposed by Western Digital</p>	<p>Plain and ordinary meaning</p>	<p>Western Digital: Indefinite</p>	<p>Not indefinite ordinary m</p>

<p>#7: “wherein the controller is further adapted to determine which of the blocks of the plurality of the blocks in the MLC and SLC non-volatile memory modules are accessed most frequently and wherein the controller segregates those blocks that receive frequent writes into the at least one SLC non-volatile memory module and those blocks that receive infrequent writes into the at least one MLC nonvolatile module, and maintain a count value of the blocks in the MLC non-volatile memory module determined to have received frequent writes and that are accessed most frequently on a periodic basis when the count value is a predetermined count value, transfer the contents of the counted blocks in the MLC non-volatile memory module determined to have received frequent writes after reaching the predetermined count value to the SLC non-volatile memory module and which determined blocks in the SLC are determined in accordance with the next equivalent range</p>	<p>Plain and ordinary meaning</p>	<p>Indefinite.</p> <p>Although it is possible for a person of ordinary skill (“POSA”) to identify some embodiments that fall within the scope of the claim, a POSA would not be reasonably certain of the full scope of the claim.</p>	<p>Not indefinite ordinary m</p>
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