UNITED STATES PATENT AND TRADEMARK OFFICE

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BEFORE THE PATENT TRIAL AND APPEAL BOARD

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MICRON TECHNOLOGY, INC.,
Petitioner,

v.

VERVAIN, LLC,
Patent Owner.

———————

IPR2021-01547
Patent 8,891,298 B2

———————

Before SALLY C. MEDLEY, STACEY G. WHITE, and
ROBERT J. WEINSCHENK, *Administrative Patent Judges*.

MEDLEY, *Administrative Patent Judge*.

DECISION
Granting Institution of *Inter Partes* Review
35 U.S.C. § 314

I. INTRODUCTION

Micron Technology, Inc. ("Petitioner") filed a Petition for *inter partes* review of claims 1–5, 8, 9, and 11 of U.S. Patent No. 8,891,298 B2 (Ex. 1001, "the '298 patent"). Paper 1 ("Pet."). Vervain, LLC ("Patent Owner") filed a Preliminary Response. Paper 10 ("Prelim. Resp."). Institution of an *inter partes* review is authorized by statute when "the information presented in the petition . . . and any response . . . shows that there is a reasonable likelihood that the petitioner would prevail with respect to at least 1 of the claims challenged in the petition." 35 U.S.C. § 314(a). Upon consideration of the Petition, the Preliminary Response, and the evidence of record, we determine that Petitioner has established a reasonable likelihood of prevailing with respect to the unpatentability of at least one claim of the '298 patent. Accordingly, for the reasons that follow, we institute an *inter partes* review of claims 1–5, 8, 9, and 11 of the '298 patent.

A. Real Parties in Interest

Petitioner lists "Micron Technology, Inc.—along with its subsidiaries" as the real parties-in-interest. Pet. 4.

Patent Owner lists Vervain, LLC as the real party-in-interest. Paper 4, 2.

B. Related Matters

The parties identify a related district court litigation, *Vervain, LLC v. Micron Technology, Inc.*, No. 6:21-cv-00487 (W.D. Tex.) ("underlying litigation"). Pet. 4; Paper 4, 2. The parties further identify a district court litigation in which Patent Owner asserted the '298 patent against third parties, *Vervain, LLC v. Western Digital Corp. et al.*, No. 6:21-cv-00488 (W.D. Tex.). *Id.* The parties also identify the following *inter partes* review

petitions for other patents asserted in the underlying litigation: IPR2021-01548, involving U.S. Patent No. 9,196,385; IPR2021-01549, involving U.S. Patent No. 9,997,240; and IPR2021-01550, involving U.S. Patent No. 10,950,300. Pet. 4; Paper 4, 2–3.

C. The '298 Patent

The '298 patent relates to "reliable storage through the use of non-volatile memories." Ex. 1001, 1:25–26. In particular, the '298 patent describes "a system and method of increasing the reliability and lifetime of a NAND flash storage system, module, or chip through the use of a combination of single-level cell (SLC) and multi-level cell (MLC) NAND flash storage." *Id.* at 1:27–31. The '298 patent observes that "MLC NAND flash enjoys greater density than SLC NAND flash, at the cost of a decrease in access speed and lifetime (endurance)," and so the patent describes using one bank of "economical MLC NAND flash" and another bank of "high endurance SLC NAND flash." *See id.* at 3:19–21; 4:51–55.

Figure 1 illustrates a computer system for implementing an embodiment of the '298 patent, and is reproduced below.
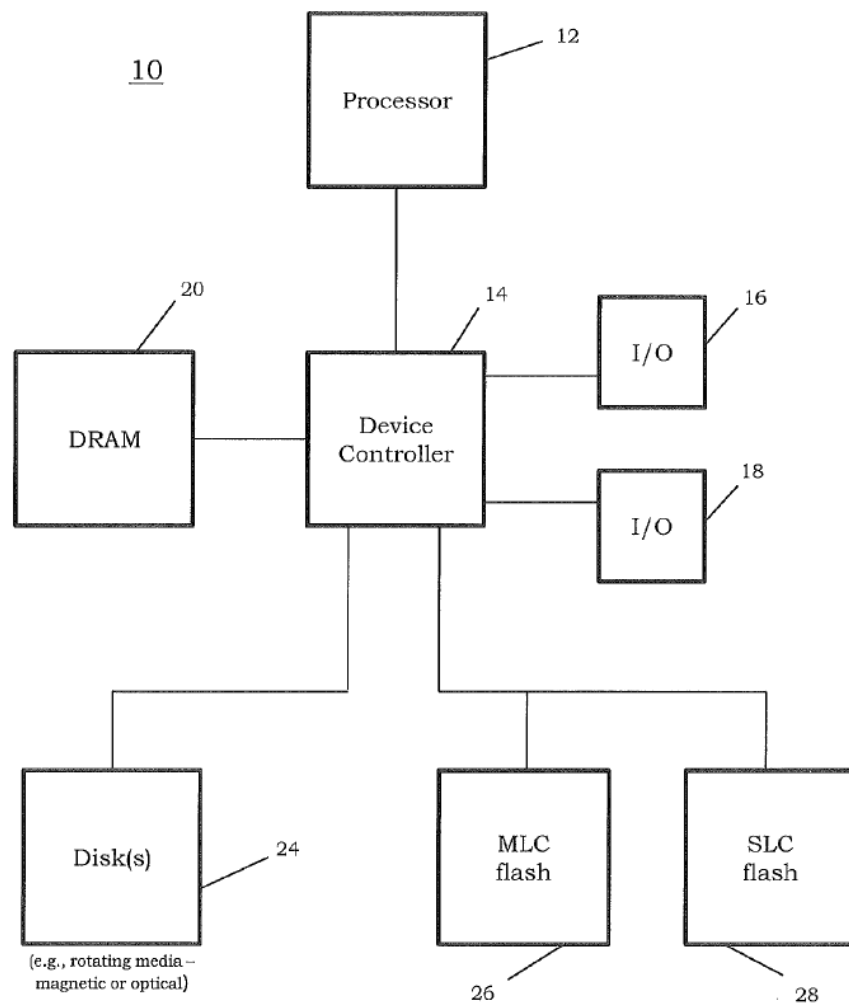
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FIG. 1

Figure 1 shows computer system 10 as including device controller 14 for controlling access to MLC NAND flash memory module 26 and SLC NAND flash memory module 28. *Id.* at 4:64–5:15. Device controller 14 maintains a translation table for mapping logical addresses to physical addresses in each of flash memory modules 26 and 28. *Id.* at 5:20–23. Initially, the translation table maps all logical addresses to MLC NAND flash memory module 26, because "MLC flash memory is less expensive than SLC flash memory, on a cost per bit basis." *Id.* at 5:24–27. For data

integrity purposes, device controller 14 may read data from an address range
after each write to an address within that range. *Id.* at 5:34–37. "If a data
integrity test fails, the address range is remapped from the MLC NAND
flash memory module 26 to the next available address range in the SLC
NAND flash memory module 28." *Id.* at 5:37–40.

      Figures 2a and 2b illustrate a failed data integrity test, and are
reproduced below.

LOGICAL ADDRESS RANGE	PHYSICAL ADDRESS RANGE
R0	MLC/Block 0
R1	MLC/Block 1
R2	MLC/Block 2
R3	MLC/Block 3
R4	MLC/Block 4
RN	MLC/Block N

Failed Data Integrity Test → R2

FIG. 2a

LOGICAL ADDRESS RANGE	PHYSICAL ADDRESS RANGE
R0	MLC/Block 0
R1	MLC/Block 1
R2	SLC/Block 0
R3	MLC/Block 3
R4	MLC/Block 4
RN	MLC/Block N

Remapping to SLC flash module → R2

FIG. 2b

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