EXHIBIT A-20
INVALIDITY CLAIM CHART FOR THE '298 PATENT
BASED ON U.S. PATENT APPLICATION PUB. NO. 2009/0327591 ("Moshayedi App.")

U.S. Patent Application Publication No. 2009/0327591 ("Moshayedi App.") was filed on June 25, 2009 and published on December 31, 2009. Moshayedi App. is prior art to the '298 patent under at least 35 U.S.C. § 102(a), (b), and (e) (pre-AIA). The asserted claims of the '298 patent are anticipated by Moshayedi App. expressly and/or inherently or rendered obvious, either alone or in combination with other references, as set forth in the cover pleading for Micron's Initial Invalidity Contentions and as further explained in the chart below.

This chart is based on Defendants' present understanding of Plaintiff's apparent positions as to the scope of the asserted claims. By including prior art that invalidates the claims of the patent based on Plaintiff's claim construction and infringement positions, Defendants are neither adopting nor acceding in any manner to Plaintiff's claim construction and infringement positions. Furthermore, nothing stated herein shall be treated as an admission or suggestion that Defendants agree with Plaintiff regarding either the scope of any of the asserted claims or the claim constructions Plaintiff advances in its infringement allegations or anywhere else. Nor shall anything in this chart be treated as an admission that any of Defendants' accused technology meets any limitations of the claims.

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Claim 1	**Disclosure in Moshayedi App.**
[1.Pre] A system for storing data comprising:	To the extent the preamble is limiting, Moshayedi App. discloses and/or renders obvious a system for storing data. *See, e.g.,* • Figure 1 • Abstract
[1.A] at least one MLC non-volatile memory module comprising a plurality of individually erasable blocks;	Moshayedi App. discloses and/or renders obvious at least one MLC non-volatile memory module comprising a plurality of individually erasable blocks. *See, e.g.,* • Figure 1 • [0026] • [0038]

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	• [0005] • [0030]
[1.B] at least one SLC non-volatile memory module comprising a plurality of individually erasable blocks; and	Moshayedi App. discloses and/or renders obvious at least one SLC non-volatile memory module comprising a plurality of individually erasable blocks. *See, e.g.,* • Figure 1 • [0026] • [0038] • [0005] • [0030]
[1.C] a controller coupled to the at least one MLC non-volatile memory module and the at least one SLC non-volatile memory module	Moshayedi App. discloses and/or renders obvious a controller coupled to the at least one MLC non-volatile memory module and the at least one SLC non-volatile memory module. *See, e.g.,* • Figure 1 • [0036] • [0026] (controller communicating with modules)
[1.D.i] wherein the controller is adapted to: (a) maintain an address map of at least one of the MLC and SLC non-	Moshayedi App. discloses and/or renders obvious wherein the controller is adapted to maintain an address map of at least one of the MLC and SLC non-volatile memory modules, the address map comprising a list of logical address ranges accessible by a computer system.

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volatile memory modules, the address map comprising a list of logical address ranges accessible by a computer system	*See, e.g.,* • [0006] • [0037] • [0047] • Abstract (using "logical" instead of "virtual")
[1.D.ii] the list of logical address ranges having a minimum quanta of addresses	Moshayedi App. discloses and/or renders obvious the list of logical address ranges having a minimum quanta of addresses. *See, e.g.,* • [0006] • [0037] • [0047]
[1.D.iii] wherein each entry in the list of logical address ranges maps to a similar range of physical addresses within either the at least one SLC non-volatile memory module or within the at least one MLC non-volatile memory module	Moshayedi App. discloses and/or renders obvious wherein each entry in the list of logical address ranges maps to a similar range of physical addresses within either the at least one SLC non-volatile memory module or within the at least one MLC non-volatile memory module. *See, e.g.,* • [0006] • [0037] • [0047]
[1.E.i] b) determine if a	Moshayedi App. discloses and/or renders obvious wherein the controller is adapted to determine if a

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range of addresses listed by an entry and mapped to a similar range of physical addresses within the at least one MLC non-volatile memory module, fails a data integrity test	range of addresses listed by an entry and mapped to a similar range of physical addresses within the at least one MLC non-volatile memory module, fails a data integrity test. *See, e.g.,* • [0031] (data errors) • [0033] • [0061]-[0064]
[1.E.ii] in the event of such a failure, the controller remaps the entry to the next available equivalent range of physical addresses within the at least one SLC non-volatile memory module	Moshayedi App. discloses and/or renders obvious in the event of such a failure, the controller remaps the entry to the next available equivalent range of physical addresses within the at least one SLC non-volatile memory module. *See, e.g.,* • [0006] • [0036]
[1.F] c) determine which of the blocks of the plurality of the blocks in the MLC and SLC non-volatile memory modules are accessed most frequently by maintaining a count of the number of times each one of the blocks is accessed	Moshayedi App. discloses and/or renders obvious wherein the controller is adapted to determine which of the blocks of the plurality of the blocks in the MLC and SLC non-volatile memory modules are accessed most frequently by maintaining a count of the number of times each one of the blocks is accessed. *See, e.g.,* • [0009] • [0024] • [0071] (describing tracking the number of times that actual NAND block is written to) • [0032] • [0049]

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[1.G] d) allocate those blocks that receive the most frequent writes by transferring the respective contents of those blocks to the at least one SLC non-volatile memory module	Moshayedi App. discloses and/or renders obvious wherein the controller is adapted to allocate those blocks that receive the most frequent writes by transferring the respective contents of those blocks to the at least one SLC non-volatile memory module. *See, e.g.,* • [0024] • [0032] • [0049]
Claim 3	**Disclosure in Moshayedi App.**
[3] The system of claim 1, wherein the minimum quanta of addresses is equal to one page.	Moshayedi App. discloses and/or renders obvious the system of claim 1, wherein the minimum quanta of addresses is equal to one page. *See, e.g.,* • [0046] ("virtual page number … according the LBA address received from host")
Claim 4	**Disclosure in Moshayedi App.**
[4] The system of claim 1, wherein the MLC non-volatile memory module is NAND flash memory.	Moshayedi App. discloses and/or renders obvious the system of claim 1, wherein the MLC non-volatile memory module is NAND flash memory. *See, e.g.,* • [0026] (MLC is "NAND flash")
Claim 5	**Disclosure in Moshayedi App.**
[5] The system of claim 1, wherein the SLC non-volatile	Moshayedi App. discloses and/or renders obvious the system of claim 1, wherein the SLC non-volatile memory module is NAND flash memory.

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