EXHIBIT A-18
INVALIDITY CLAIM CHART FOR THE '298 PATENT
BASED ON U.S. PATENT APPLICATION PUB. NO. US 2008/0140918 ("Sutardja")

U.S. Patent Application Publication No. US 2008/0140918 ("Sutardja") was filed on December 7, 2007 and published on June 12, 2008. Sutardja is prior art to the '298 patent under at least 35 U.S.C. §§ 102(a), (b), (e) (pre-AIA). The asserted claims of the '298 patent are anticipated by Sutardja expressly and/or inherently or rendered obvious, either alone or in combination with other references, as set forth in the cover pleading for Micron's Initial Invalidity Contentions and as further explained in the chart below.

This chart is based on Defendants' present understanding of Plaintiff's apparent positions as to the scope of the asserted claims. By including prior art that invalidates the claims of the patent based on Plaintiff's claim construction and infringement positions, Defendants are neither adopting nor acceding in any manner to Plaintiff's claim construction and infringement positions. Furthermore, nothing stated herein shall be treated as an admission or suggestion that Defendants agree with Plaintiff regarding either the scope of any of the asserted claims or the claim constructions Plaintiff advances in its infringement allegations or anywhere else. Nor shall anything in this chart be treated as an admission that any of Defendants' accused technology meets any limitations of the claims.

U.S. Pat. No. 8,891,298	
Claim 1	**Disclosure in Sutardja**
[1.Pre] A system for storing data comprising:	To the extent the preamble is limiting, Sutardja discloses and/or renders obvious a system for storing data. *See, e.g.*, • FIGs. 1-3 • [0011] • [0108]
[1.A] at least one MLC non-volatile memory module comprising a plurality of individually erasable blocks;	Sutardja discloses and/or renders obvious at least one MLC non-volatile memory module comprising a plurality of individually erasable blocks. *See, e.g.*, • FIG. 3 • [0013] • [0108]

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	• [0121] • [0011]
[1.B] at least one SLC non-volatile memory module comprising a plurality of individually erasable blocks; and	Sutardja discloses and/or renders obvious at least one SLC non-volatile memory module comprising a plurality of individually erasable blocks. *See, e.g.*, • [0108] • [0011]
[1.C] a controller coupled to the at least one MLC non-volatile memory module and the at least one SLC non-volatile memory module	Sutardja discloses and/or renders obvious a controller coupled to the at least one MLC non-volatile memory module and the at least one SLC non-volatile memory module. *See, e.g.*, • FIGs. 1-7 • [0105] • [0107] • [0118] • [0129]-[1030] *See also* Claim limitations [1.A-B] and accompanying citations.
[1.D.i] wherein the controller is adapted to: (a) maintain an address map of at least one of the MLC and SLC non-volatile memory modules, the address map comprising a	Sutardja discloses and/or renders obvious wherein the controller is adapted to maintain an address map of at least one of the MLC and SLC non-volatile memory modules, the address map comprising a list of logical address ranges accessible by a computer system. *See, e.g.*,

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list of logical address ranges accessible by a computer system	• [0042] • [0105] • [0118] • [0149] • [0150] • FIG. 7C • [0011]-[0012] (controller performs logical to physical mapping) • [0047] • [0107]
[1.D.ii] the list of logical address ranges having a minimum quanta of addresses	Sutardja discloses and/or renders obvious the list of logical address ranges having a minimum quanta of addresses. *See, e.g.*, • [0018]-[0019] (block addressing) • [0027]-[0028] • [0036]-[0037] • [0111] • [0121]-[0123]
[1.D.iii] wherein each entry in the list of logical address ranges maps to a similar range of physical addresses within either the at least one SLC non-volatile memory module or within the at least one MLC non-volatile memory module	Sutardja discloses and/or renders obvious wherein each entry in the list of logical address ranges maps to a similar range of physical addresses within either the at least one SLC non-volatile memory module or within the at least one MLC non-volatile memory module. *See, e.g.*, • [0042] • [0111]-[0112] • [0118]

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	• [0126] • [0149]-[0150] • [0167]
[1.E.i] b) determine if a range of addresses listed by an entry and mapped to a similar range of physical addresses within the at least one MLC non-volatile memory module, fails a data integrity test	Sutardja discloses and/or renders obvious wherein the controller is adapted to determine if a range of addresses listed by an entry and mapped to a similar range of physical addresses within the at least one MLC non-volatile memory module, fails a data integrity test. *See, e.g.*, • [0108] • [0111] • [0105] • [0118] • [0123] • [0135]-[0137] (degradation module)
[1.E.ii] in the event of such a failure, the controller remaps the entry to the next available equivalent range of physical addresses within the at least one SLC non-volatile memory module	Sutardja discloses and/or renders obvious in the event of such a failure, the controller remaps the entry to the next available equivalent range of physical addresses within the at least one SLC non-volatile memory module. *See, e.g.*, • [0108] • [0111] • [0105] • [0118] • [0123] • [0138] (wear leveling adjusted based on degradation)

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[1.F] c) determine which of the blocks of the plurality of the blocks in the MLC and SLC non-volatile memory modules are accessed most frequently by maintaining a count of the number of times each one of the blocks is accessed	Sutardja discloses and/or renders obvious wherein the controller is adapted to determine which of the blocks of the plurality of the blocks in the MLC and SLC non-volatile memory modules are accessed most frequently by maintaining a count of the number of times each one of the blocks is accessed. *See, e.g.*, • [0106] • [0108] • Claim 37 (MLC and SLC) • [0111], [0121] (storing count) • [0118] (controller includes wear leveling module) • [0146] (receive "write frequencies for logical addresses" from the host) • [0147] (tracking actual counts)
[1.G] d) allocate those blocks that receive the most frequent writes by transferring the respective contents of those blocks to the at least one SLC non-volatile memory module	Sutardja discloses and/or renders obvious wherein the controller is adapted to allocate those blocks that receive the most frequent writes by transferring the respective contents of those blocks to the at least one SLC non-volatile memory module. *See, e.g.*, • [0108] • [0111] • [0121] • [0123] • [0146]-[0148] • [0149] • [0167]
Claim 3	**Disclosure in Sutardja**
[3] The system of claim 1,	Sutardja discloses and/or renders obvious the system of claim 1, wherein the minimum quanta of

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