EXHIBIT A-3
INVALIDITY CLAIM CHART FOR THE '298 PATENT
BASED ON U.S. PATENT APPLICATION PUB. NO. 2011/0099460 ("Dusija")

U.S. Patent Application Publication No. 2011/0099460 ("Dusija") was filed on December 18, 2009 and published on April 28, 2011. Dusija is prior art to the '298 patent under at least 35 U.S.C. §§ 102(a), (e) (pre-AIA). The asserted claims of the '298 patent are anticipated by Dusija expressly and/or inherently or rendered obvious, either alone or in combination with other references, as set forth in the cover pleading for Micron's Initial Invalidity Contentions and as further explained in the chart below.

This chart is based on Defendants' present understanding of Plaintiff's apparent positions as to the scope of the asserted claims. By including prior art that invalidates the claims of the patent based on Plaintiff's claim construction and infringement positions, Defendants are neither adopting nor acceding in any manner to Plaintiff's claim construction and infringement positions. Furthermore, nothing stated herein shall be treated as an admission or suggestion that Defendants agree with Plaintiff regarding either the scope of any of the asserted claims or the claim constructions Plaintiff advances in its infringement allegations or anywhere else. Nor shall anything in this chart be treated as an admission that any of Defendants' accused technology meets any limitations of the claims.

U.S. Pat. No. 8,891,298	
Claim 1	**Disclosure in Dusija**
[1.Pre] A system for storing data comprising:	To the extent the preamble is limiting, Dusija discloses and/or renders obvious a system for storing data. *See, e.g.*, • [0059] • FIG. 1
[1.A] at least one MLC non-volatile memory module comprising a plurality of individually erasable blocks;	Dusija discloses and/or renders obvious at least one MLC non-volatile memory module comprising a plurality of individually erasable blocks. *See, e.g.*, • FIGs. 6, 14A • [0109] • [0079]

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[1.B] at least one SLC non-volatile memory module comprising a plurality of individually erasable blocks; and	Dusija discloses and/or renders obvious at least one SLC non-volatile memory module comprising a plurality of individually erasable blocks. *See, e.g.*, • [0109] • [0077]-[0079] • FIGs. 6, 14A
[1.C] a controller coupled to the at least one MLC non-volatile memory module and the at least one SLC non-volatile memory module	Dusija discloses and/or renders obvious a controller coupled to the at least one MLC non-volatile memory module and the at least one SLC non-volatile memory module. *See, e.g.*, • FIG. 1 • [0060] • [0117] • [0062] *See also* Claim limitations [1.A-B] and accompanying citations.
[1.D.i] wherein the controller is adapted to: (a) maintain an address map of at least one of the MLC and SLC non-volatile memory modules, the address map comprising a list of logical address ranges accessible by a computer	Dusija discloses and/or renders obvious wherein the controller is adapted to maintain an address map of at least one of the MLC and SLC non-volatile memory modules, the address map comprising a list of logical address ranges accessible by a computer system. *See, e.g.*, • [0117] • [0129]

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system	• [0138] • [0060], [0117], [0129], [0138] (examples of mapping) • [0164]-[0167] (example of mapping physical to "logical addresses")
[1.D.ii] the list of logical address ranges having a minimum quanta of addresses	Dusija discloses and/or renders obvious the list of logical address ranges having a minimum quanta of addresses. *See, e.g.*, • [0060] (logical sector) • [0111] (incoming "page") • [0166]-[0168] (logical blocks) • [0061]
[1.D.iii] wherein each entry in the list of logical address ranges maps to a similar range of physical addresses within either the at least one SLC non-volatile memory module or within the at least one MLC non-volatile memory module	Dusija discloses and/or renders obvious wherein each entry in the list of logical address ranges maps to a similar range of physical addresses within either the at least one SLC non-volatile memory module or within the at least one MLC non-volatile memory module. *See, e.g.*, • [0060] (mapping sectors to corresponding physical data unit) • [0117], [0129], [0138] (examples of mapping to different physical addresses in MLC and SLC) • [0164]-[0167] (noting that a "block" can correspond to a "group of logical addresses") • [0061]
[1.E.i] b) determine if a range of addresses listed by an entry and mapped to a similar range of physical	Dusija discloses and/or renders obvious wherein the controller is adapted to determine if a range of addresses listed by an entry and mapped to a similar range of physical addresses within the at least one MLC non-volatile memory module, fails a data integrity test.

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addresses within the at least one MLC non-volatile memory module, fails a data integrity test	*See, e.g.*, • [0111]-[0117] • [0119]-[0124] *See also* Claim limitation [1.A] and accompanying citations ("second portion" is MLC) *See also* Claim limitation [1.D] and accompanying citations (explaining logical-to-physical mapping)
[1.E.ii] in the event of such a failure, the controller remaps the entry to the next available equivalent range of physical addresses within the at least one SLC non-volatile memory module	Dusija discloses and/or renders obvious in the event of such a failure, the controller remaps the entry to the next available equivalent range of physical addresses within the at least one SLC non-volatile memory module. *See, e.g.*, • [0116] • [0117] • [0119]-[0125] • [0203] • FIG. 14B • [0153]-[0154] • [0060] (controller "controls" and "manages" memory operations); [0087]-[0088] (controller performs ECC); [0117] (controller remaps); [0118] (controller includes wear-leveling module) *See also* Claim limitation [1.B] and accompanying citations ("first portion" is the SLC memory module)
[1.F] c) determine which of the blocks of the plurality of the blocks in the MLC and	Dusija discloses and/or renders obvious wherein the controller is adapted to determine which of the blocks of the plurality of the blocks in the MLC and SLC non-volatile memory modules are accessed most frequently by maintaining a count of the number of times each one of the blocks is accessed.

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SLC non-volatile memory modules are accessed most frequently by maintaining a count of the number of times each one of the blocks is accessed	*See, e.g.*, • [0027] • [0051] • [0101] • [0107] • [0153]-[0159] (hot count) • [0204]
[1.G] d) allocate those blocks that receive the most frequent writes by transferring the respective contents of those blocks to the at least one SLC non-volatile memory module	Dusija discloses and/or renders obvious wherein the controller is adapted to allocate those blocks that receive the most frequent writes by transferring the respective contents of those blocks to the at least one SLC non-volatile memory module. *See, e.g.*, • [0027] • [0101] • [0153] • [0159] • [0204]
Claim 3	**Disclosure in Dusija**
[3] The system of claim 1, wherein the minimum quanta of addresses is equal to one page.	Dusija discloses and/or renders obvious the system of claim 1, wherein the minimum quanta of addresses is equal to one page. *See, e.g.*, • [0166]-[0168] • [0163]

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