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Rao

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(54) **LIFETIME MIXED LEVEL NON-VOLATILE MEMORY SYSTEM**

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G06F 12/02 (2006.01)
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See application file for complete search history.

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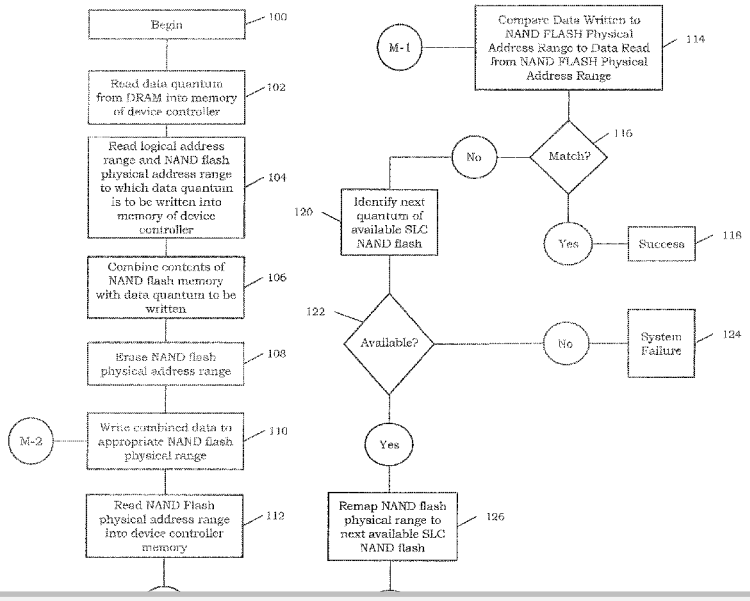
(57) **ABSTRACT**

A flash controller for managing at least one MLC non-volatile memory module and at least one SLC non-volatile memory module. The flash controller is adapted to determine if a range of addresses listed by an entry and mapped to said at least one MLC non-volatile memory module fails a data integrity test. In the event of such a failure, the controller remaps said entry to an equivalent range of addresses of said at least one SLC non-volatile memory module. The flash controller is further adapted to determine which of the blocks in the MLC and SLC non-volatile memory modules are accessed most frequently and allocating those blocks that receive frequent writes to the SLC non-volatile memory module and those blocks that receive infrequent writes to the MLC non-volatile memory module.

12 Claims, 5 Drawing Sheets



Related U.S. Application Data

continuation of application No. 14/525,411, filed on Oct. 28, 2014, now Pat. No. 9,196,385, which is a division of application No. 13/455,267, filed on Apr. 25, 2012, now Pat. No. 8,891,298.

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G11C 29/00	(2006.01)
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(52) **U.S. Cl.**

CPC ***G06F 12/0246*** (2013.01); ***G11C 11/5621*** (2013.01); ***G11C 11/5678*** (2013.01); ***G11C 16/16*** (2013.01); ***G11C 16/3495*** (2013.01); ***G11C 29/52*** (2013.01); ***G11C 29/76*** (2013.01); *G06F 2212/7202* (2013.01); *G11C 2211/5641* (2013.01)

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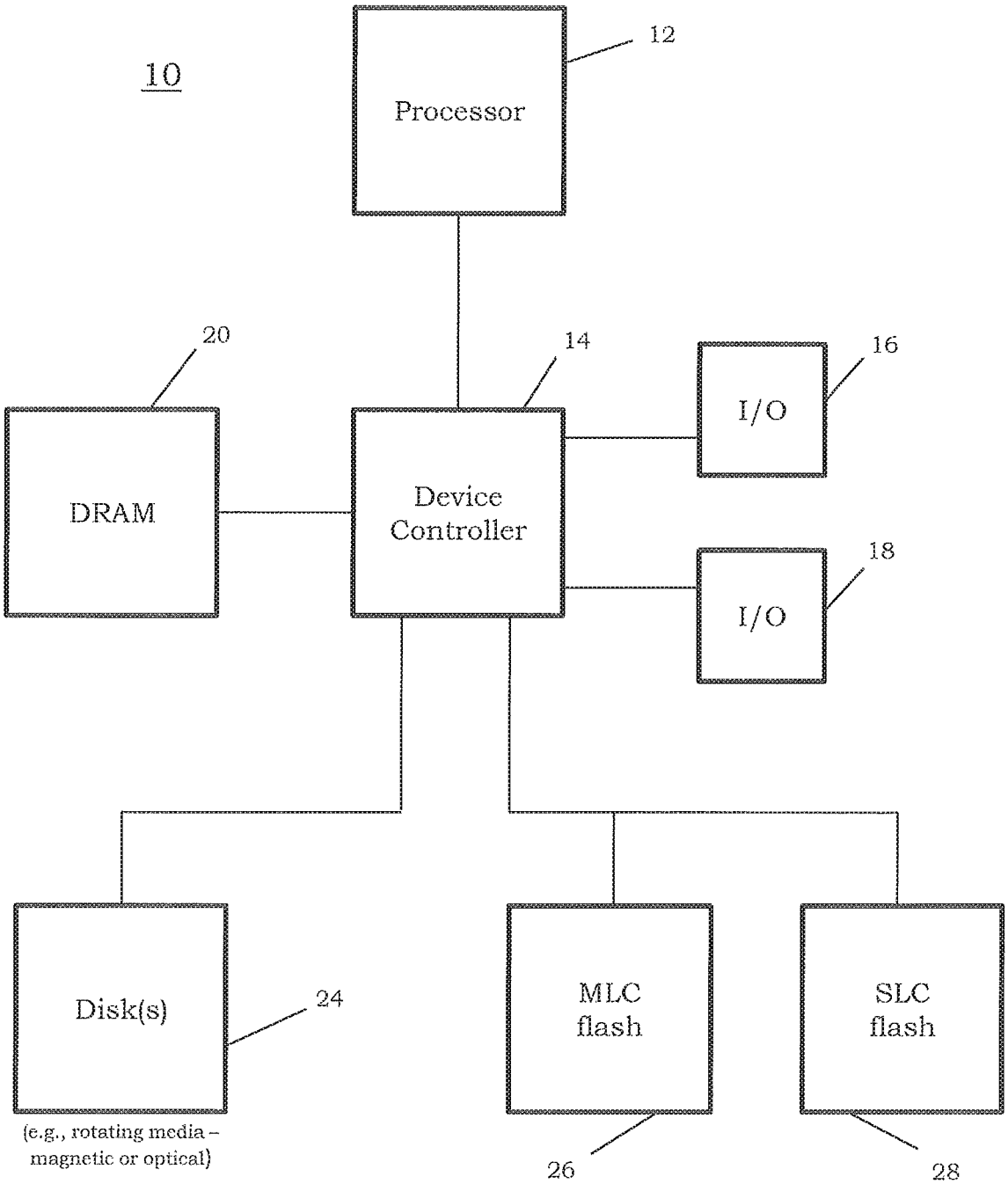

FIG. 1

Failed Data Integrity Test →

LOGICAL ADDRESS RANGE	PHYSICAL ADDRESS RANGE
R0	MLC/Block 0
R1	MLC/Block 1
R2	MLC/Block 2
R3	MLC/Block 3
R4	MLC/Block 4
RN	MLC/Block N

FIG. 2A

Remapping to SLC flash module →

LOGICAL ADDRESS RANGE	PHYSICAL ADDRESS RANGE
R0	MLC/Block 0
R1	MLC/Block 1
R2	SLC/Block 0
R3	MLC/Block 3
R4	MLC/Block 4
RN	MLC/Block N

FIG. 2B

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