UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

APPLE INC.
Petitioner

v.

FUTURE LINK SYSTEMS, LLC
Patent Owner

Case No. IPR2021-01488
U.S. Patent No. 6,807,505

PETITION FOR *INTER PARTES* REVIEW
OF U.S. PATENT NO. 6,807,505

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I. INTRODUCTION

Petitioner Apple Inc. ("Petitioner") requests an *Inter Partes* Review ("IPR") of claims 1, 6, and 8 (the "Challenged Claims") of U.S. Patent No. 6,807,505 ("the '505 Patent").

II. SUMMARY OF THE '505 PATENT

A. The '505 Patent's Alleged Invention

The '505 Patent describes an alleged improvement to existing boundary scan circuit testing. *'505 Patent* (Ex. 1001), 2:17-24. Boundary scan circuit testing was developed in the 1980s by a group of manufacturers called the "Joint Test Action Group," or JTAG, who in 1990 codified a testing technique in Institute of Electrical and Electronics Engineers ("IEEE") Standard 1149.1 that has since evolved into a family of related standards published as recently as 2013. *See JTAG boundary-scan, firmly based on IEEE standards,*" JTAG Technologies, (last visited Sep. 1, 2021), https://www.jtag.com/jtag-boundary-scan-firmly-based-on-ieee-standards/ (explaining the history and evolution of the original IEEE 1149.1 standard) (Ex. 1002). The '505 Patent describes the standard by citing to an article co-authored by inventor Franciscus G. M. De Jong ("De Jong Article"). *'505 Patent* (Ex. 1001), 1:24-28. Figure 1-19 of that article depicts the IEEE standard for boundary scan circuitry on an integrated circuit ("IC"):

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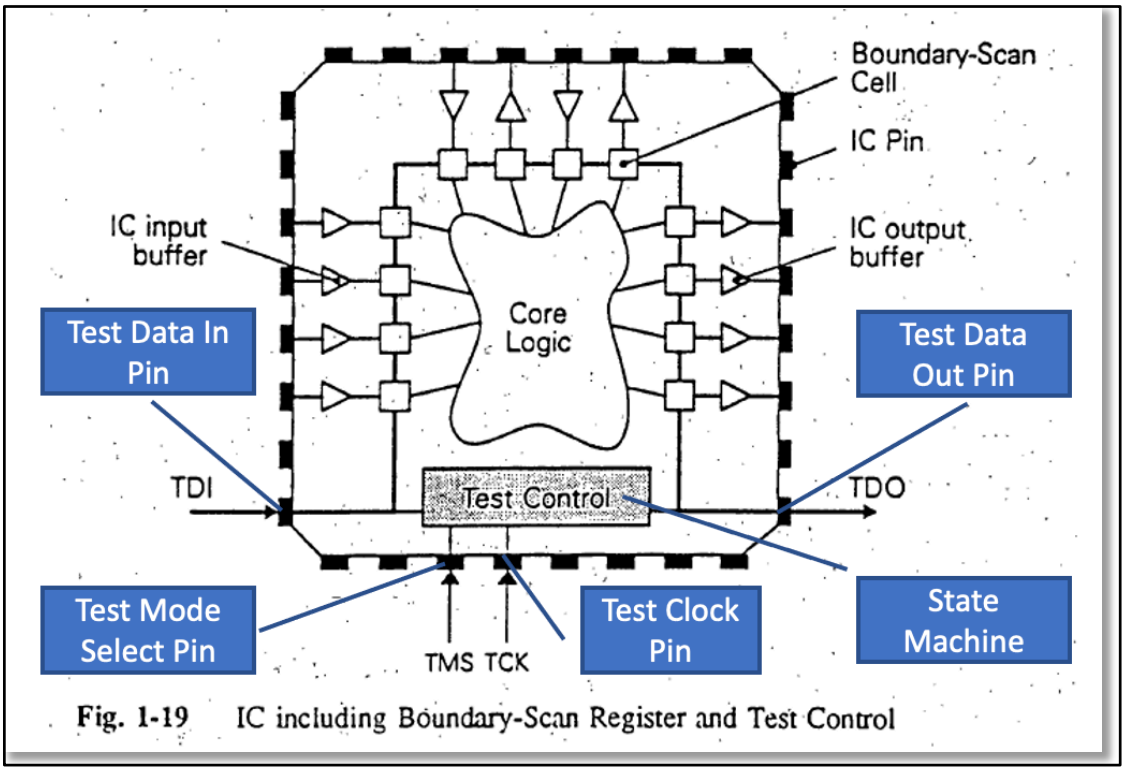

Fig. 1-19 IC including Boundary-Scan Register and Test Control

De Jong Article (Ex. 1003), 13 (annotated). As depicted in the figure, the typical boundary scan circuity is designed to test interconnects (*i.e.,* buses)[1] that feed information to and from a circuit using four dedicated testing pins collectively referred to as the Test Access Port to the circuit and a test controller (also called a

[1] A POSITA would have considered buses to be interconnects. *Liu Dec.* (Ex. 1004), ¶ 33 (explaining that the '505 Patent at 1:7-15 and 2:25-49 describes its object as testing interconnects between electronic circuits, which the patent specifies as the address and data buses between them at 6:18-7:25 and 7:26-54).

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state machine) that controls the serial shift of test data through boundary-scan cells connected to the input and output ("I/O") nodes of a circuit. *'505 Patent* (Ex. 1001), 1:28-61.

According to the '505 Patent, synchronous dynamic random access memory ("SDRAM") devices had "highly standardised pin lay-out[s]" incompatible with the dedicated TDI, TDO, TMS, and TCK test pins required in a conventional boundary scan architecture. *Id.* at 5:56-6:1 (describing the structured pin layout[2] of an SDRAM device obstructed by typical boundary scan test pins); *see also id.* at 4:19-24 (describing pin count and compatibility constraints). To avoid the need for these additional test pins, the '505 Patent proposes an "alternative" to the traditional boundary scan testing standard that replaces its state machine and dedicated test pins for a "low complexity memory" that can be used to accomplish much of the same interconnect testing. *Id.* at 2:25-44 (describing interacting with such low-complexity

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[2] A POSITA would have recognized circuit pins as circuit input and output nodes. *Liu Dec.* (Ex. 1004), ¶ 34 (explaining that the '505 Patent at Fig. 1 and 5:46-59 discloses an SDRAM device "pin lay-out" that also "schematically shows which I/O nodes are generally present on an SDRAM device" and concluding the '505 Patent refers to pins and I/O nodes interchangeably).

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