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PTO/SB/05 (03-01)
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# UTILITY PATENT APPLICATION TRANSMITTAL

*(Only for new nonprovisional applications under 37 C.F.R. 1.53(b))*

| | |
|---|---|
| *Attorney Docket No.* | PHN 17,203A |
| *First Inventor* | Franciscus G. DeJong |
| *Title* | CIRCUIT WITH INTERCONNECT TEST UNIT AND METHOD OF TESTING INTERCONNECTS BETWEEN A FIRST AND A SECOND ELECTRONIC CIRCUIT |
| *Express Mail Label No.* | EV312014124US 7/16/03 |

## APPLICATION ELEMENTS

*See MPEP chapter 600 concerning utility patent application contents.*

*ADDRESS TO:* Assistant Commissioner for Patents, Box Patent Application, Alexandria, VA 22313-1450

1. ☒ Fee Transmittal Form (e.g., PTO/SB/17) *(Submit an original and a duplicate for fee processing)*
2. ☐ Applicant claims small entity status. See 37 CFR 1.27.
3. ☒ Specification [*Total Pages* 21 ]
   *(preferred arrangement set forth below)*
   - Descriptive title of the Invention
   - Cross Reference to Related Applications
   - Statement Regarding Fed sponsored R & D
   - Reference to sequence listing, a table, or a computer program listing appendix
   - Background of the Invention
   - Brief Summary of the Invention
   - Brief Description of the Drawings *( if filed)*
   - Detailed Description
   - Claim(s)
   - Abstract of the Disclosure
4. ☒ Drawing(s) (*35 U.S.C.113*) [*Total Sheets* 3 ]
5. Oath or Declaration [*Total Pages* ]
   a. ☐ Newly executed (original or copy)
   b. ☒ Copy from a prior application (37 CFR 1.63 (d))
   *(for a continuation/divisional with Box 18 completed)*
   i. ☐ DELETION OF INVENTOR(S)
   Signed statement attached deleting inventor(s) named in the prior application, see 37 CFR 1.63(d)(2) and 1.33(b).
6. ☐ Application Data Sheet. See 37 CFR 1.76
7. ☐ CD-ROM or CD-R in duplicate, large table or Computer Program *(Appendix)*
8. Nucleotide and/or Amino Acid Sequence Submission *(if applicable, all necessary)*
   a. ☐ Computer Readable Form (CRF)
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      i. ☐ CD-ROM or CD-R (2 copies); or
      ii. ☐ paper
   c. ☐ Statements verifying identity of above copies

16235 U.S. PTO 10/620202 07/16/03

### ACCOMPANYING APPLICATIONS PARTS

9. ☐ Assignment Papers (cover sheet & document(s))
10. ☐ 37 C.F.R.§3.73(b) Statement ☐ Power of Attorney *(when there is an assignee)*
11. ☐ English Translation Document *(if applicable)*
12. ☐ Information Disclosure Statement (IDS)/PTO-1449 ☒ Copies of IDS Citations
13. ☒ Preliminary Amendment
14. ☒ Return Receipt Postcard (MPEP 503) *(Should be specifically itemized)*
15. ☐ Certified Copy of Priority Document(s) *(if foreign priority is claimed)*
16. ☐ Nonpublication Request under 35 U.S.C. 122 (b)(2)(B)(i). Applicant must attach form PTO/SB/35 or its equivalent.
17. ☐ Other: ____

18. **If a CONTINUING APPLICATION,** *check appropriate box, and supply the requisite information below and in a preliminary amendment, or in an Application Data Sheet under 37 CFR 1.76:*

☐ Continuation ☒ Divisional ☐ Continuation-in-part (CIP) of prior application No: 09/ 402,154

*Prior application information:* *Examiner* Craig S. Miller *Group / Art Unit: 2857*

**For CONTINUATION or DIVISIONAL APPS only: The entire disclosure of the prior application, from which an oath or declaration is supplied under Box 5b, is considered a part of the disclosure of the accompanying or divisional application and is hereby incorporated by reference. The incorporation can only be relied upon when a portion has been inadvertently omitted from the submitted application parts.**

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07/16/03 160 U.S. PTO

# FEE TRANSMITTAL for FY 2002

*Patent fees are subject to annual revision.*

| Complete If Known | |
|---|---|
| Application Number | |
| Filing Date | |
| First Named Inventor | Franciscus G. DeJong |
| Examiner Name | |
| Group / Art Unit | |
| Attorney Docket No. | PHN 17,203A |

**TOTAL AMOUNT OF PAYMENT** ($) 750.00

## METHOD OF PAYMENT (check one)

1. ☒ The Commissioner is hereby authorized to charge indicated fees and credit any over payments to:

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☐ Applicant claims small entity status. See 37 CFR 1.27

2. ☐ Payment Enclosed:

☐ Check ☐ Credit card ☐ Money Order ☐ Other

## FEE CALCULATION

1. BASIC FILING FEE

| Large Entity Fee Code | Large Entity Fee ($) | Small Entity Fee Code | Small Entity Fee ($) | Fee Description | Fee Paid |
|---|---|---|---|---|---|
| 101 | 750 | 201 | 370 | Utility filing fee | 750 |
| 106 | 330 | 206 | 165 | Design filing fee | |
| 107 | 510 | 207 | 255 | Plant filing fee | |
| 108 | 740 | 208 | 370 | Reissue filing fee | |
| 114 | 160 | 214 | 80 | Provisional filing fee | |

SUBTOTAL (1) ($) 750

2. EXTRA CLAIM FEES

| | | | Extra Claims | | Fee from below | = | Fee Paid |
|---|---|---|---|---|---|---|---|
| Total Claims | | - ** = | 0 | X | | = | 0 |
| Independent Claims | | - ** = | 0 | X | | = | 0 |
| Multiple Dependent | | | | X | | = | 0 |

| Large Entity Fee Code | Large Entity Fee ($) | Small Entity Fee Code | Small Entity Fee ($) | Fee Description |
|---|---|---|---|---|
| 103 | 18 | 203 | 9 | Claims in excess of 20 |
| 102 | 84 | 202 | 42 | Independent claims in excess of 3 |
| 104 | 280 | 204 | 140 | Multiple dependent claim, if not paid |
| 109 | 84 | 209 | 42 | ** Reissue independent claims over original patent |
| 110 | 18 | 210 | 9 | ** Reissue claims in excess of 20 and over original patent |

SUBTOTAL (2) ($) 0

**or number previously paid, if greater; For Reissues, see above

## FEE CALCULATION (continued)

3. ADDITIONAL FEES

| Large Entity Fee Code | Large Entity Fee ($) | Small Entity Fee Code | Small Entity Fee ($) | Fee Description | Fee Paid |
|---|---|---|---|---|---|
| 105 | 130 | 205 | 65 | Surcharge - late filing fee or oath | |
| 127 | 50 | 227 | 25 | Surcharge - late provisional filing fee or cover sheet. | |
| 139 | 130 | 139 | 130 | Non-English specification | |
| 147 | 2,520 | 147 | 2,520 | For filing a request for reexamination | |
| 112 | 920* | 112 | 920* | Requesting publication of SIR prior to Examiner action | |
| 113 | 1,840* | 113 | 1,840* | Requesting publication of SIR after Examiner action | |
| 115 | 110 | 215 | 55 | Extension for reply within first month | |
| 116 | 400 | 216 | 200 | Extension for reply within second month | |
| 117 | 920 | 217 | 460 | Extension for reply within third month | |
| 118 | 1,440 | 218 | 720 | Extension for reply within fourth month | |
| 128 | 1,960 | 228 | 980 | Extension for reply within fifth month | |
| 119 | 320 | 219 | 160 | Notice of Appeal | |
| 120 | 320 | 220 | 160 | Filing a brief in support of an appeal | |
| 121 | 280 | 221 | 140 | Request for oral hearing | |
| 138 | 1,510 | 138 | 1,510 | Petition to institute a public use proceeding | |
| 140 | 110 | 240 | 55 | Petition to revive – unavoidable | |
| 141 | 1,280 | 241 | 640 | Petition to revive – unintentional | |
| 142 | 1,280 | 242 | 640 | Utility issue fee (or reissue) | |
| 143 | 460 | 243 | 230 | Design issue fee | |
| 144 | 620 | 244 | 310 | Plant issue fee | |
| 122 | 130 | 122 | 130 | Petitions to the Commissioner | |
| 123 | 50 | 123 | 50 | Processing fee under 37 CFR 1.17 (q) | |
| 126 | 180 | 126 | 180 | Submission of Information Disclosure Stmt | |
| 581 | 40 | 581 | 40 | Recording each patent assignment per property (times number of properties) | |
| 146 | 740 | 246 | 370 | Filing a submission after final rejection (37 CFR § 1.129(a)) | |
| 149 | 740 | 249 | 370 | For each additional invention to be examined (37 CFR § 1.129(b)) | |
| 179 | 740 | 279 | 370 | Request for Continued Examination (RCE) | |
| 169 | 900 | 169 | 900 | Request for expedited examination of a design application | |
| | | | | Other fee (specify) ____ | |

*Reduced by Basic Filing Fee Paid

SUBTOTAL (3) ($) 0

| SUBMITTED BY | | | | Complete (if applicable) | |
|---|---|---|---|---|---|
| Name (Print/Type) | Michael E Belk ~~Eric M. Bram~~ | Registration No. Attorney/Agent | 33,357 ~~37,285~~ | Telephone | 914-333-9535 |
| Signature | Michael E Belk | | | Date | 7/16/03 |

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CIRCUIT WITH INTERCONNECT TEST UNIT AND A METHOD OF TESTING INTERCONNECTS BETWEEN A FIRST AND A SECOND ELECTRONIC CIRCUIT

The invention relates to an electronic circuit comprising: a plurality of input/output (I/O) nodes for connecting the electronic circuit to a further electronic circuit via interconnects, a main unit for implementing a normal mode function of the electronic circuit, and a test unit for testing the interconnects, the electronic circuit having a normal mode in which the I/O nodes are logically connected to the main unit and a test mode in which the I/O nodes are logically connected to the test unit.

The invention further relates to a method of testing interconnects between a first electronic circuit and a second electronic circuit, the first electronic circuit comprising a main unit implementing a normal mode function of the first electronic circuit, and a test unit for testing the interconnects, the method comprising the steps of logically connecting the test unit to the interconnects, and putting test data on the interconnects by the second electronic circuit.

Such a circuit is known from "Boundary-scan test, a practical approach", H. Bleeker, P. van den Eijnden and F. de Jong, Kluwer, Boston, 1993, ISBN 0-7923-9296-5, Figures 1-19, which shows an integrated (IC) in accordance with the boundary-scan test standard IEEE Std. 1149.1. The known circuit has a main unit or core logic that is responsible for providing some arbitrary specified function in a normal mode of the circuit. The known circuit further has a test unit for in a test mode performing an interconnect test, i.e. a test whether the circuit is properly connected to a further circuit via its I/O nodes or IC pins. Efficient interconnect test of miniaturised and/or complex circuit assemblies is a necessary part of the production process of such assemblies. The boundary-scan test technique is accepted as standardised solution for interconnect test. It is available in most of the leading microprocessor families and is supported for in-house developed application specific ICs through automated tools in the IC design process.

The test unit of the known boundary-scan circuit includes a test control unit or Test Access Port controller and a shift register or boundary-scan register along the circuit boundary, cells of the shift register being connected to I/O nodes corresponding to the interconnects to be tested. The test control unit has a state machine controlling states of the shift register, examples of such states being a shift state for shifting in/out data into the shift register and a capture state for capturing data originating from the interconnects into the shift

register. The shift register is accessible from outside the circuit via a Test Data In (TDI) node and a Test Data Out (TDO) node. A Test Clock signal (TCK) and a Test Mode Select signal (TMS) are provided from outside the circuit to the test control unit for stepping through the various states. In the normal mode of the known circuit, the I/O nodes are logically connected to the main unit, thereby allowing the circuit to perform its normal mode function. In the test mode of the known circuit, the I/O nodes are logically connected to the test unit, thereby giving the test unit access to the interconnects.

Provided that also the further circuit is equipped with a test unit in accordance with the boundary-scan test standard, the interconnects between the two circuits can be tested according to the standard boundary-scan test method. Hereto, appropriate test data is first shifted into the shift registers of the two circuits and is subsequently applied to the interconnects. Then, response data originating from the interconnects is captured into the shift registers and subsequently shifted out of the shift registers for observation. From the response data it can be determined whether the circuits are properly interconnected. For a single interconnect this means that to one of its ends a signal is applied and at the other end it is observed whether that signal is transmitted. In this way, an open circuit in an interconnect can be found. Additionally, a number of test patterns will be applied to the interconnects in order to check for short-circuits between neighbouring interconnects, or between an interconnect and a power supply line. Essentially, interconnect testing comes down to applying test data to one end of an interconnect and observing response data at another end, in such a way that open circuits and short circuits are detected.

A problem with the boundary-scan approach is that for some circuits pin count and pin compatibility considerations inhibit the addition of extra pins to a circuit design for the TCK, TMS, TDI, TDO and the optional TRSTN signals. Moreover, the price-pressure in some semiconductor fields is such that it is considered to be too expensive to reserve area for interconnect test of the size as required by boundary-scan circuitry.

It is an object of the invention to provide a circuit as specified in the preamble, that allows interconnect testing with reduced overhead in terms of required I/O nodes and/or area. This object is achieved according to the invention in an electronic circuit, which is characterised in that in the test mode the test unit is operable as a low complexity memory via the I/O nodes. Low complexity memories are those memories that do not have to be put through a complex initialisation process before they can be accessed, and that have simple access protocols without dynamic restrictions. Such a test unit enables an alternative procedure

for applying test data to one end of an interconnect and observing response data at the other end. If the low complexity memory has a read-only character and holds pre-stored test data at a number of addresses, the test unit produces this pre-stored test data at its side of the interconnects when address data and appropriate control data are applied to it by the further circuit via the interconnects. The further circuit then receives response data, which should be identical to the pre-stored test data. In this way, both the interconnects that are used to carry the address and control data and the interconnects that are used to carry the pre-stored data itself are tested. It is important that particular input data for the test unit, i.e. the address, result in output data from the test unit that are known a priori, i.e. the stored data. If the low complexity memory allows both read and write access, the further circuit can apply test data to its side of the interconnects in a write mode of the test unit, thereby storing the test data in the test unit. In a subsequent read mode of the test unit, the further circuit can read back response data.

Whether the test unit has a read-only or a read/write behaviour, it does not need a state machine like the boundary-scan state machine and can therefore be implemented consuming less area. Moreover, the simple operation of the test unit allows less pins or even no pins at all to be reserved for controlling the test unit in the test mode. For both a read-only and a read/write test unit, a subset of the interconnects is used as a data bus for exchanging the storage data. At least in the case that the test unit has a read/write behaviour, a further subset of the interconnects is used as a control bus, including, for example, control lines for controlling the read and/or write process. At least in the case that the test unit has a read-only behaviour, a still further subset of the interconnects is used as an address bus for selecting the storage location to read from. An important aspect of the invention is that one is free how to map the data bus, the control bus and/or the address bus on the interconnects to be tested.

Access to the control bus, the address bus, and the data bus during test mode could be provided, for example, via boundary-scan circuitry of the further circuit. Then, with ordinary boundary-scan test equipment, data can be shifted in and out of the further circuit. In this way, data to be supplied to the control bus and/or the address bus and data returned by the test unit on the data bus can be handled. As a further example, if the further circuit is a programmed microprocessor or Application-Specific IC (ASIC), the further circuit could perform the interconnect test in a stand alone fashion, without the need for external equipment for feeding the further circuit with the test data and for evaluating the response data. It is noted that the further circuit alternatively could consist of two or more separate circuits, together operating the test unit as a low complexity memory.

An embodiment of the electronic circuit according to the invention is defined in Claim 2. A Read-Only Memory (ROM) is a suitable device for holding the data required by the interconnect test. When control data, in the form of an address and, if necessary, a limited number of further control signals, is applied to the circuit, the ROM outputs data pre-stored at that address on the data bus. It will be clear that in this way both the data bus, the address bus and, if present, the control bus are tested. A small number of test patterns pre-stored in the ROM would normally suffice for an interconnect test capable of detecting open circuits in interconnects and short circuits between interconnects. It will further be clear that for the test unit being operable as a low complexity memory, it is not required that the test unit is implemented as a real ROM table. Especially if only a small number of test patterns is used, the test unit could be implemented as a combinatorial circuit, leading to more efficient area usage.

An embodiment of the electronic circuit according to the invention is defined in Claim 3. In relation with such a read/write register, the control bus at least controls whether the register is in a read mode or in a write mode, and the data bus is used for both supplying the data to be written to the test unit and for receiving the data to be read back from the test unit. In this embodiment, no address bus is needed since only a single register is used.

An embodiment of the electronic circuit according to the invention is defined in Claim 5. The test circuit of this embodiment requires comparatively little area of the substrate on which it is manufactured. Furthermore, it enables to test the interconnects in a single type of test and with a very good test coverage, i.e. a small set of patterns suffices to detect the possible defects in the interconnects. Furthermore, the diagnostic resolution of the test is very good since almost all faults have a unique signature.

High complexity memory devices are those devices which have complex protocols for reading from and writing into their memory array. Therefore, as opposed to low complexity memories, high complexity memories are not suited as test units for interconnect testing, as the process of exchanging data is too complex and therefore takes too much time. Examples of high complexity memory devices are Synchronous Dynamic Random Access memories (SDRAMs) and non-volatile memory like flash memory devices. Besides complex access protocols, high complexity memories often need initialisation and have dynamic restrictions. The initialisation is troublesome for testing because (almost) all control lines and address lines have to be connected correctly to succeed in initialisation. Although interconnect problems with control and address lines can be detected because the failing initialisation will

block all access to the devices, the diagnosis of the failure, i.e. exactly which of the pins is not connected correctly has a very low resolution.

The dynamic restrictions of SDRAMs, usually identified by the refresh time and the maximum RAS pulse width, hamper interconnect test because the test patterns (i.e. writing into and reading from the memory array) have to meet the dynamic requirements. The speed of application of test patterns using a boundary-scan circuit is determined by the length of the boundary-scan register and the maximum test clock frequency. The test clock frequency is determined either by the circuit implementation of the boundary-scan circuit in the ICs on the board or by the maximum speed of the boundary-scan tester.

For these reasons, high complexity memories form a class of circuits that could very well benefit from adding a low complexity memory for enabling efficient interconnect testing. This is especially true because boundary-scan is hardly available in memory devices due to pin count and/or pin compatibility considerations.

An embodiment of the circuit according to the invention is described in Claim 6. This particular way of activating the test mode is possible because in most SDRAMs the first action to be performed after power up is prescribed to be a write action. Thus at power up, by utilising the read action for activating the test mode, the normal operation of the SDRAM is not effected. As an alternative, the circuit in accordance with the invention can be brought into test mode via a particular combination of input signals on the I/O nodes, or via a dedicated node that is dedicated to this function.

Non-volatile memories like flash memory devices hamper interconnect test, because writing into the memory array for test purposes is not allowed when the device is already pre-programmed. This test would destroy the functional data. An un-programmed device can be written into but has to be erased afterwards. Erasure of large memory blocks can take up to several seconds, lengthening considerably the board interconnect test.

By including a test unit in accordance with the invention, high complexity memories, including non-volatile memories, can undergo an efficient interconnect test. One could use the normal mode data bus, address bus and/or control bus for the test mode as well. To also test interconnects that provide signals that are specific for the high complexity memory functionality, and therefore are not needed to control the test unit in the test mode, either the data bus or the address bus can be extended with these interconnects. The invention enables interconnect testing using test patterns which take only milliseconds to execute and for which test pattern generators are commercially available.

Low complexity memory types like Static Random Access Memories (SRAMs) and (Programmable) ROMs can readily be tested for their connectivity using neighbouring circuits equipped with boundary-scan or neighbouring microprocessors and/or ASICs. For interconnect testing of such low complexity memories no extra measures in the form of added test units have to be taken.

It is a further object of the invention to provide a method as specified in the preamble, which performs the interconnect test with reduced overhead in terms of required I/O nodes and/or area. This object is achieved according to the invention in a method, which is characterised in that the putting step comprises operating the first electronic circuit as a low complexity memory by the second electronic circuit.

Although the invention is presented in the context of boundary-scan testing, which mainly applies to testing interconnects between ICs on a carrier, such as a printed circuit board (PCB), the principles of the invention are equally applicable to the testing of interconnects between any two circuits, such as interconnects between cores within a single IC or interconnects between ICs on distinct PCBs that are inserted into a cabinet.

The invention and its attendant advantages will be further elucidated with the aid of exemplary embodiments and the accompanying schematic drawings, whereby:

Figure 1 shows an embodiment of a circuit in accordance with the invention,

Figure 2 shows a way to provide access during interconnect test to a circuit that is testable in accordance with the invention,

Figure 3 shows a further way to provide access during interconnect test to a circuit that is testable in accordance with the invention,

Figure 4 shows an alternative embodiment of the invention,

Figure 5 schematically shows the test unit for five inputs and two outputs, and

Figure 6 schematically shows an alternative for the test unit for five inputs and two outputs.

Corresponding features in the various Figures are denoted by the same reference symbols.

Figure 1 shows an embodiment of a circuit 100 in accordance with the invention. The circuit 100 has I/O nodes 130, 140, through which the circuit 100 is connectable to external circuits. An I/O node may be an input node, i.e. a node only suitable to

receive signals, an output node, i.e. a node only suitable to send signals, or a bi-directional node, i.e. a node suitable to either receive or send signals. For performing its intended normal mode function, the circuit 100 has a main unit 110, which is, by way of example, assumed to be an SDRAM. Thus, the circuit 100 is in fact an SDRAM device. It is further assumed that the circuit 100 is part of an assembly, whereas interconnects between the circuit 100 and further parts of the assembly should be testable. Hereto, the circuit 100 has a test unit 120, which is connected to the main unit 110 via *n* parallel connections and to the I/O nodes 130. In a normal mode of the circuit 100, the test unit 120 is transparent, and signals can pass freely between the I/O nodes 130 and the main unit 110. In a test mode of the circuit 100, the main unit 110 is logically disconnected from the I/O nodes 130 and the test unit 120 is in control. It is noted that preferably, but not necessarily, all I/O nodes are arranged for interconnect testing. To indicate this, the I/O nodes 140 are not connected to the test unit 120, and therefore, the test unit 120 does not offer testability for interconnects corresponding to these I/O nodes 140.

SDRAM devices have a highly standardised pin lay-out. Figure 1 does not give an exact representation of such a pin-layout, but it schematically shows which I/O nodes are generally present on an SDRAM device. The circuit 100 has a data bus D0-D3, an address bus A0-A11, and a control bus including a Chip Select pin (CSn), an Output Enable pin (OEn), Write Enable pin (WEn), Clock pin (CLK), Clock Enable pin (CKE), Row Address Strobe pin (RAS), Column Address Strobe pin (CAS), and Data I/O Mask pins (DQML and DQMH). The precise functions of these pins are not relevant for the invention. However, the standardised pin lay-out obstructs the addition of boundary-scan circuitry because of the required extra pins. Another reason for not using boundary-scan for interconnect testing of devices like circuit 100 is the enormous pressure on cost. As a result, the IC area available for extra features like interconnect testing is very limited. In accordance with the invention, as an alternative to an ordinary boundary-scan test unit, the test unit 120 is operable as a low complexity memory. Such a test unit can be implemented very efficiently in terms of IC area and requires less or even zero extra pins.

A low complexity memory can have a read-only behaviour or a read/write behaviour. In accordance with the invention, a test unit has either kind of behaviour, or both kinds of behaviour in subsequent phases of an interconnect test. In the circuit 100, during a first part of a preferred interconnect test, the test unit 120 has a read-only behaviour and during a subsequent second part of the interconnect test, the test unit 120 has a read/write behaviour. This two-step approach enables a thorough interconnect test that is especially suited for

SDRAMs like the circuit 100. The first part of the interconnect test aims at testing the address bus of the circuit 100 and is functionally described by:

1. After power up of the circuit 100, a test mode is active which allows read access to the test unit 120. The test unit 120 is then operable as a ROM table. Alternatively, the test mode is activated by other means, such as a particular combination or sequence of signals applied to the I/O nodes 130, 140 of the circuit 100.

2. Read access to the test unit 120 is controlled by CSn=0, OEn=0 and WEn=1, and validated by a defined edge of the CLK and active level of the clock enable CKE.

3. The test unit's ROM table is addressed by the 'extended' address bus which is defined as the actual address bus, extended with the control signals RAS, CAS, DQML and DQMU.

4. The width of the ROM table is equal to the width of the data bus plus possible additional outputs of the circuit 100.

5. Each of the primary addresses (all but one address bits equal to '0', one address bit equal to '1') reads the all '1' data word. All other extended addresses read the all '0' data word.

The table below shows the contents of the ROM table for the SDRAM device of circuit 100, with 12 bit wide address bus, RAS, CAS, DQML and DQMU and four data pins.

| extended address bus | data bus |
|---|---|
| AAAAAAAAAAAARCDD<br>1198765432 10AAQQ<br>10 SSMM<br>LH | DDDD<br>3210 |
| 0000000000000001 | 1111 |
| 0000000000000010 | 1111 |
| 0000000000000100 | 1111 |
| 0000000000001000 | 1111 |
| 0000000000010000 | 1111 |
| 0000000000100000 | 1111 |
| 0000000001000000 | 1111 |
| 0000000010000000 | 1111 |
| 0000000100000000 | 1111 |
| 0000001000000000 | 1111 |
| 0000010000000000 | 1111 |
| 0000100000000000 | 1111 |
| 0001000000000000 | 1111 |
| 0010000000000000 | 1111 |
| 0100000000000000 | 1111 |
| 1000000000000000 | 1111 |
| 'any other address' | 0000 |

With the above described functional behaviour of the circuit 100 after power up, an efficient test for the extended address bits consist of just reading all primary addresses (16 in the above case) and one other address. The test sequence covers the following faults:

1. any stuck-at 1 on an extended address pin
2. any stuck-at 0 on an extended address pin
3. any 2-net AND-type short between any pair of address pins
4. any 2-net OR-type short between any pair of address pins
5. any stuck-at 1 on a data pin

6. any stuck-at 0 on a data pin

An interconnect with a stuck-at fault remains at either logic high or logic low, no matter what signals are applied to it. A 2-net AND-type short between a first and a second interconnect causes the two interconnects to carry the same logic value as determined by either one of the interconnects. A 2-net OR-type short between a first and a second interconnect causes the two interconnects to carry complementary logic values as determined by either one of the interconnects.

The above test sequence provides a diagnostic resolution down to a single pin. Note that this test concept is independent from the number of extended address lines or the number of data lines, nor is there any relation assumed between the two numbers.

The second part of the interconnect test aims at testing for shorts between the interconnects making up the data bus, and is functionally described by:

1. Write access is provided to a command register, which is loaded with the value of the (actual) address bus.
2. There will be a certain combination of address bits, which, after being loaded into the aforementioned command register, select a single write/read register that logically forms part of the test unit, with a width equal to the width of the data bus. This combination of address bits is to be determined by the manufacturer of the device and to be specified in the data sheet.

This single write/read register can then be used to write data and read data. Algorithms are available to generate a minimal set of test patterns which cover all AND-type and OR-type shorts between any pair of data lines. The table below shows a set of test patterns for a 16-bit wide data bus.

| DDDDDDDDDDDDDDDD<br>1111119876543210<br>543210 |
|---|
| 1111100000000000 |
| 0000011111100000 |
| 1110011100011000 |
| 1001011010010110 |
| 1100110011001100 |
| 0101010101010101 |

For dynamic memory devices, like the circuit 100, the above described two parts of the interconnect test have read and write access to the test unit which is not affected with any dynamic requirements. It will be clear that many variants can be imagined to either part. Moreover, one can also choose to implement only one of the above described two parts of the interconnect test. For flash devices, for example, the first part of the interconnect test is applicable for unprogrammed devices. The manufacturer may choose not to offer this facility for already programmed devices, to accomplish compatibility with EPROM devices (these access the main memory array when a first read is done after power up).

As mentioned above, the mechanism for switching the circuit from the normal mode into the test mode may be implemented in different ways. In the SDRAM embodiment, the circuit is brought into the test mode by performing a read action after power up. Such a read action after power up, is a special action which does not form part of the normal actions for the circuit and has been given the special meaning of a command for switching into the test mode. In general, any pattern or sequence of patterns applied to one or more I/O nodes of the circuit can be given the special meaning of a command for going into test mode, provided that this pattern or sequence is not used in the normal mode of the circuit. An alternative is to provide the circuit with a dedicated test control node, in addition to the I/O nodes, to control whether the circuit is to behave in the normal operational mode or in the test mode. The actual signal value on the test control node, in relation with predefined values corresponding to the respective modes, brings the circuit into the desired mode.

Figure 2 shows a way to provide access during interconnect test to a circuit 200 that is testable in accordance with the invention. The circuit 200 includes a test unit 205 that is operable as a low complexity memory. A neighbouring circuit 210, which has boundary-scan circuitry, can provide data to and receive data from the circuit 200 via a control and address bus 220 and a bi-directional data bus 230. Alternatively, when only a ROM behaviour is implemented in the test unit 205, the data bus 230 would be uni-directional, i.e. from the circuit 200 to the circuit 210.

A number of interconnects make up the control and address bus 220 and the data bus 230. The function of these interconnects during a normal mode is irrelevant for the invention. When the circuit 200 is a memory device, there will also be a 'normal mode data bus'. The 'test mode data bus' 230 could partly or completely coincide with the normal mode data bus. The same applies to the control and address bus 220.

Via a boundary-scan chain 240 data is shifted into circuit 210, that data making up read and/or write commands to be supplied to the circuit 200. After a read command, the

boundary-scan chain 240 captures data supplied to the data bus 230 by the circuit 200. That data subsequently are shifted out to be analysed externally.

Figure 3 shows a further way to provide access during interconnect test to a circuit 300 that is testable in accordance with the invention. The circuit 300 includes a test unit 305 that is operable as a low complexity memory via control and address bus 320 and data bus 330. A neighbouring circuit 310, which is a microprocessor, executes the program with the necessary read and write commands. The test program and the test data are stored in a memory 340 of the circuit 310. Preferably, the circuit 310 also analyses the data obtained from the circuit 300. The circuit 310 could alternatively be an ASIC.

The above presented design-for-test method does not require any additional pins to the device for test access, meeting pin count and pin compatibility requirements of this type of memories. Silicon area overhead is limited to the (small) ROM table, or functional equivalent, the read/write data register (possibly to be combined with existing logic) and the associated decoding logic. Standardisation of this approach by a body like EIS or JEDEC would ensure compatibility between devices from different manufacturers.

Boundary-scan is the preferred design-for-test method for testing interconnects on assemblies with ICs. It can be used to efficiently test all interconnects between devices with boundary-scan circuitry implemented. It can also be used directly to apply test patterns for low complexity memory devices. If the above described design-for-test method is implemented in complex memory devices, then also these devices can efficiently be tested using boundary scan access, without restrictions from dynamic requirements, initialisation issues and erasure issues for non-volatile devices. The described interconnect test approach does not need additional test pins, and only requires little silicon area.

Figure 4 shows an alternative embodiment of the invention. In the same way as described above, the circuit 402 of which the interconnects are to be tested has a main unit 404 and a test unit 406. The main unit 404 is active in the normal operational mode of the circuit and the test unit is active in the test mode of the circuit. The interconnect test in this embodiment is functionally described by:

1. After power-up of the circuit 100, the test mode can be activated, which allows read access to the test unit 120. The test unit 120 is then operable as a ROM table. Alternatively, the test mode is activated by other means, such as activating a particular pin. Alternatively, a particular combination or sequence of signals applied to the I/O nodes 130, 140 of the circuit 100 may activate the test mode.

2. Read access to the test unit 120 is controlled by CSn=0, CASn=0 and CKE=0, followed by CKE=1.

3. The test unit's ROM table function is addressed by the 'extended' address bus which is defined as the actual address bus, extended with the remaining control signal inputs (in case of a typical 64M SDRAM example: A0 – A12, RASn, CLK, Wen, DQM0 – DQM3).

4. The width of the output table is that of the extended data bus, all pins of the device which are used as output, when in test mode. (In case of a typical 64M SDRAM example: DQ0 – DQ31). (In case of a Flash device, Databus including the read/busy pin).

5. During test mode the respective extended data bus extended address bus may be changed.

6. Each of the primary addresses and the all '0' and all '1' input read an implementation defined data word. All other address values read results different from these.

For the purpose of the interconnect test, the pins of circuit 402 are divided into 3 groups: a control bus 408 of p bits wide, an input bus 410 of n bits wide and an output bus 412 of m bits wide. The control bus is used to set the circuit into the test mode. A single line control bus may be used, i.e. one pin whose actual signal value determines whether the circuit is set in the test mode or in the normal operational mode. Or a number of lines may be used, whereby a specific combination of signals applied on the respective pins sets the circuit into the test mode. The remaining input pins of the circuit are grouped into the input bus. The output pins of the circuit and the bi-directional pins of the circuit are grouped into the output bus. As an alternative, one or more of the bi-directional pins can be grouped into the input bus.

The test unit 406 of this embodiment is a combinatorial circuit between the input bus 410 and the output bus 412. This circuit implements the functionality of a ROM table. The design of the combinatorial circuit is based on the following rules:

1. Each output signal is an exclusive-nor function of two or more input signals;
2. There are no two output signals that depend on the same set of input signals;
3. Each input signal contributes to at least one exclusive-nor function forming an output signal.

The example below is a description of the test unit for an input bus of five bits and an output bus of two bits. The description is given in the standard language Verilog.

```
module en5_2 (o1, o2, i1, i2, i3, i4, i5);

        output o1, o2;
        input i1, i2, i3, i4, i5;

        xnor #1 (o1, i1, i2);
        xnor #1 (o2, i3, i4, i5);
endmodule
```

Example 1 A test unit with five inputs and two outputs

The first line indicates that a new module starts and specifies the signals of that module. The second and third line indicate the output and input signals respectively. The fourth line defines the relation between the output signal o1 and the input signals i1 and i2 by means of the Verilog primitive xnor, which implements the exclusive-nor function. The '#1' symbol indicates that the output of the xnor primitive is available after 1 cycle of a simulator simulating this module.

Figure 5 schematically shows the test unit for five inputs and two outputs. This figure corresponds with the example above. The test unit 406 has a two-input XNOR gate 502 which implements the required exclusive-nor function between o1 and i1 and i2. The test unit further has a three-input XNOR gate 504 which implements the exclusive-nor function between the input pins i3, i4 and i5 and the output pin o2.

Another example of the test unit is given below. In this example, the test unit has five inputs and five outputs.

```
module en5_5 (o1, o2, o3, O4, o5, i1, i2, i3, i4, i5);

        output o1, o2, o3, o4, o5;
        input i1, i2, i3, i4, i5;

        xnor #1 (o1, i1, i2);
        xnor #1 (o2, i1, i3);
        xnor #1 (o3, i1, i4);
        xnor #1 (o4, i1, i5);
        xnor #1 (o5, i2, i3);
endmodule
```

Example 2 A test unit with five inputs and five outputs

For a given test unit, there must be enough input pins to feed the outputs while adhering to the rules stated above. In the general case of n inputs, a theoretical number of $2^n$ possible combinations of exclusive-nor functions can be obtained. Given the purpose of testing the interconnects however, the n exclusive-nor functions with one input have to be excluded as well as the exclusive-nor function with zero inputs. This means that in order to feed m outputs, the following relation must be met:

$$m < 2^n - n$$

So for example five inputs are enough to feed as many as 26 outputs, while adhering to the rules for implementing the test unit according to this embodiment.

For performing the interconnect test as described above, the patterns that are applied to the inputs are the:

a pattern with all 0s

n patterns with a 'walking' 1

a pattern with all 1s

n patterns with a 'walking' 0

The following table gives the patterns for Example 1 and the required outputs.

| pattern number | iiiii 12345 | oo 12 |
|---|---|---|
| 1 | 00000 | 11 |
| 2 | 10000 | 01 |
| 3 | 01000 | 01 |
| 4 | 00100 | 10 |
| 5 | 00010 | 10 |
| 6 | 00001 | 10 |
| 7 | 11111 | 10 |
| 8 | 01111 | 00 |
| 9 | 10111 | 00 |
| 10 | 11011 | 11 |
| 11 | 11101 | 11 |
| 12 | 11110 | 11 |

So a combination of bits given in the second column of the table applied on the input pins of the test unit gives on the output pins a signal as specified in the corresponding element of the third column. The following table gives the input test patterns and the corresponding outputs for Example 2.

| pattern number | iiiii 12345 | ooooo 12345 |
|---|---|---|
| 1 | 00000 | 11111 |
| 2 | 10000 | 00001 |
| 3 | 01000 | 01110 |
| 4 | 00100 | 10110 |
| 5 | 00010 | 11011 |
| 6 | 00001 | 11101 |
| 7 | 11111 | 11111 |
| 8 | 01111 | 00001 |
| 9 | 10111 | 01110 |
| 10 | 11011 | 10110 |
| 11 | 11101 | 11011 |
| 12 | 11110 | 11101 |

A third example of the test unit similar to example 1 above, but now implemented with xor primitives is given below.

```
module ex5_2 (o1, o2, i1, i2, i3, i4, i5);

        output o1, o2;
        input i1, i2, i3, i4, i5;

        xor #1 (o1, i1, i2, i3);
        xor #1 (o2, i3, i4, i5);
endmodule
```

Example 3 A test unit with five inputs and two outputs using xor primitives

CLAIMS:

1. An electronic circuit (100) comprising:
a plurality of input/output (I/O) nodes (130) for connecting the electronic circuit to a further electronic circuit via interconnects,
a main unit (110) for implementing a normal mode function of the electronic circuit,
and a test unit (120) for testing the interconnects,
the electronic circuit having a normal mode in which the I/O nodes (130) are logically connected to the main unit (110) and a test mode in which the I/O nodes (130) are logically connected to the test unit (120),
characterised in that in the test mode the test unit (120) is operable as a low complexity memory via the I/O nodes (130).

2. An electronic circuit (100) as claimed in Claim 1, wherein the test unit (120) comprises a Read Only Memory (ROM).

3. An electronic circuit (100) as claimed in Claim 1, wherein the test unit (120) comprises a read/write register.

4. An electronic circuit (402) as claimed in Claim 1, wherein the test unit (406) comprises a combinatorial circuit (502) implementing an XNOR function and being connected to the I/O nodes.

5. An electronic circuit (402) as claimed in Claim 4, wherein a first selection (410) of the I/O nodes are arranged to carry respective input signals and a second selection (412) of the I/O nodes are arranged to carry respective output signals and wherein the test unit (406) is arranged according to the following rules:
each output signal results from an XNOR function having at least two input signals,
each output signal is dependent on a unique subset of the input signals,
each input signal contributes to at least one output signal via a particular XNOR function.

6. An electronic circuit (402) as claimed in Claim 1, wherein the test unit (406) comprises a combinatorial circuit (602) implementing an XOR function and connected to the I/O nodes.

7. An electronic circuit (100) as claimed in Claim 1, wherein the main unit (110) is arranged to bring the electronic circuit (100) into the test mode on receipt via a subset of the I/O nodes (130) of a predefined pattern or sequence of patterns.

8. An electronic circuit (100) as claimed in Claim 1, wherein the electronic circuit is provided with a test control node and wherein the electronic circuit is arranged to switch into the test mode on the basis of a signal value on the test control node.

9. An electronic circuit as claimed in Claim 1, wherein the main unit is a Synchronous Dynamic Random Access Memory (SDRAM) and the test mode is activatable by a read action following power up of the electronic circuit.

10. An electronic circuit (100) comprising:
a plurality of input/output (I/O) nodes (130) for connecting the electronic circuit to a further electronic circuit via interconnects,
a main unit (110) for implementing a normal mode function of the electronic circuit,
and a test unit (120) for testing the interconnects,
the electronic circuit having a normal mode in which the I/O nodes (130) are logically connected to the main unit (110) and a test mode in which the I/O nodes (130) are logically connected to the test unit (120),
characterised in that the test unit comprises at least one combinatorial circuit (502) implementing an XNOR function with at least two function inputs and a function output, the function inputs being connected to particular I/O nodes arranged to operate as input nodes of the test circuit and the function output being connected to a particular I/O node arranged to operate as output node of the test circuit.

11. A method of testing interconnects between a first electronic circuit (100) and a second electronic circuit (210), the first electronic circuit (100) comprising a main unit (110) implementing a normal mode function of the first electronic circuit, and a test unit (120) for testing the interconnects, the method comprising the steps of

logically connecting the test unit (120 ) to the interconnects, and

putting test data on the interconnects by the second electronic circuit (210),

characterised in that the putting step comprises operating the first electronic circuit (100) as a low complexity memory by the second electronic circuit.

12. A method as claimed in Claim 11, wherein the test data comprises an address, the method further comprising the step of generating response data on the interconnects by the first electronic circuit (100), the response data being previously stored in the first electronic circuit (100) at the address.

13. A method as claimed in Claim 12, wherein the test data comprises write data and the putting step comprises storing the write data in the first electronic circuit (100), the method further comprising the step of reading back the stored write data by the second electronic circuit.

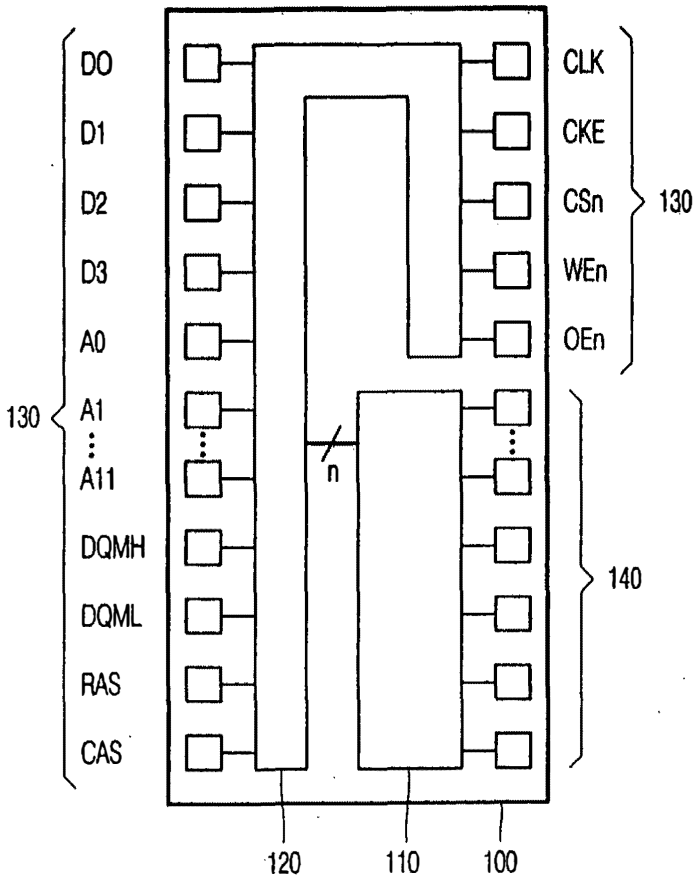
DO
D1
D2
D3
A0
A1
A11
DQMH
DQML
RAS
CAS
130
CLK
CKE
CSn
WEn
OEn
130
n
140
120
110
100

FIG. 1

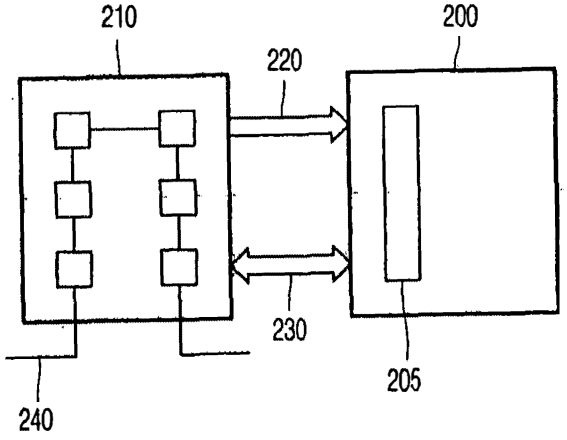
210
200
220
230
205
240

FIG. 2

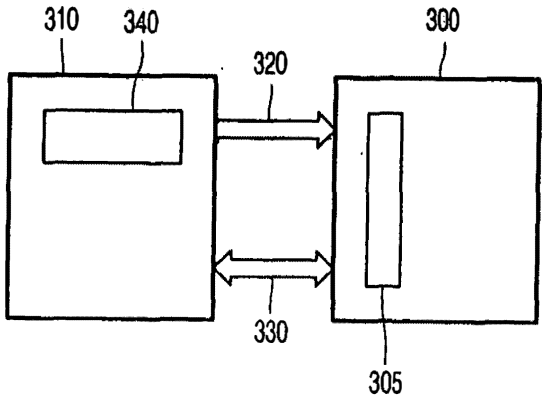
310
340
320
300
330
305

FIG. 3

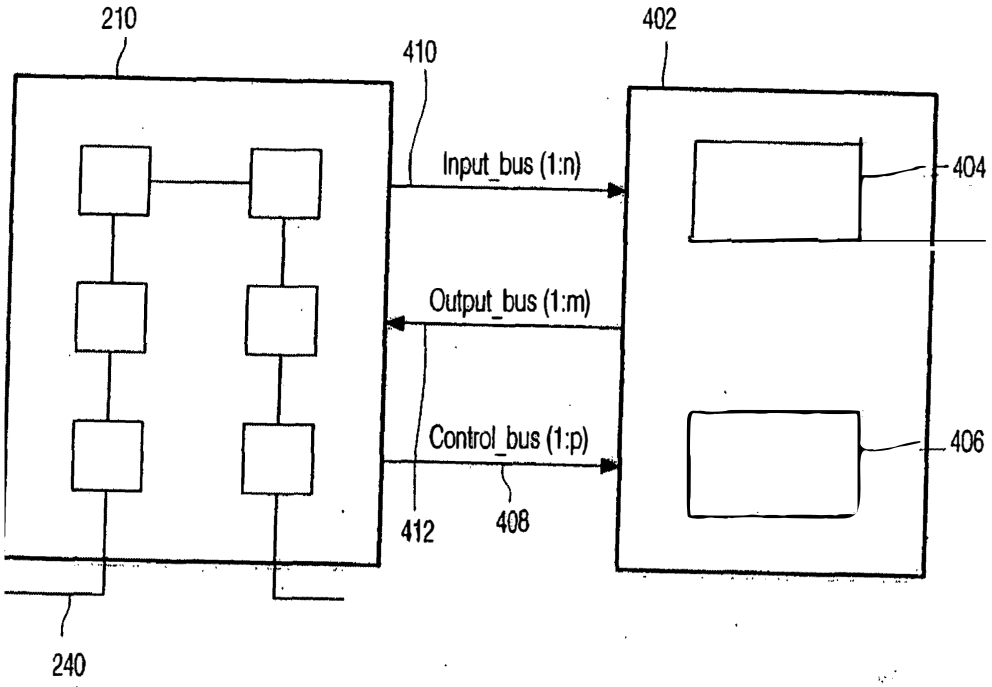
210
410
402
Input_bus (1:n)
404
Output_bus (1:m)
Control_bus (1:p)
406
412
408
240

FIG. 4

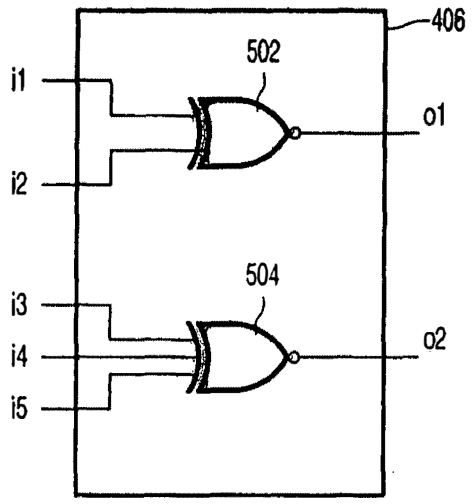


FIG. 5

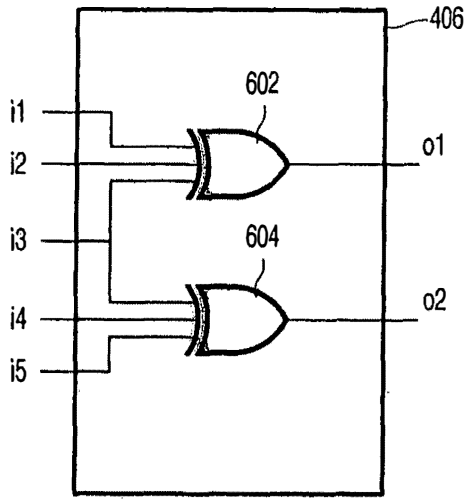


FIG. 6

COMBINED DECLARATION FOR PATENT APPLICATION AND POWER OF ATTORNEY
(Includes Reference to PCT International Applications)

ATTORNEY'S DOCKET NUMBER
PHN 17.203

As a below named inventor, I hereby declare that:

My residence, post office address and citizenship are as stated below next to my name.

I believe I am the original, first and sole inventor (if only one name is listed below) or an original, first and joint inventor (if plural names are listed below) of the subject matter which is claimed and for which a patent is sought on the invention entitled:

"Circuit with interconnect test unit and a method of testing interconnects between a first and a second electronic circuit"

the specification of which (check only one item below):

☐ is attached hereto.

☐ was filed as United States application

Serial No. _____

on _____.

and was amended

on _____ (if applicable).

☒ was filed as PCT international application

Number PCT/IB99/00172

on 29 January 1999

and was amended under PCT Article 19

on _____ (if applicable).

I hereby state that I have reviewed and understand the contents of the above-identified specification, including the claims, as amended by any amendment referred to above.

I acknowlege the duty to disclose information which is material to the examination of this application in accordance with Title 37, Code of Federal Regulations, §1.56(a).

I hereby claim foreign priority benefits under Title 35, United States Code, §119 of any foreign application(s) for patent or inventor's certificate or of any PCT international application(s) designating at least one country other than the United States of America listed below and have also identified below any foreign application(s) for patent or inventor's certificate or any PCT international application(s) designating at least one country other than the United States of America filed by me on the same subject matter having a filing date before that of the application(s) of which priority is claimed:

PRIOR FOREIGN/PCT APPLICATION(S) AND ANY PRIORITY CLAIMS UNDER 35 U.S.C. 119:

| COUNTRY (if PCT indicate PCT) | APPLICATION NUMBER | DATE OF FILING (day, month, year) | PRIORITY CLAIMED UNDER 35 USC 119 |
|---|---|---|---|
| Europe | 98200288.3 | February 02, 1998 | ☒ YES ☐ NO |
| Europe | 98204042.0 | November 30, 1998 | ☒ YES ☐ NO |
| Europe | 98201482.1 | May 06, 1998 | ☒ YES ☐ NO |
| | | | ☐ YES ☐ NO |
| | | | ☐ YES ☐ NO |

Combined Declaration For Patent Application and Power of Attorn y (Continued)
(Includes Reference to PCT International Applications)

ATTORNEY'S DOCKET NUMBER: PHN 17.203

POWER OF ATTORNEY: As a named inventor, I hereby appoint the following attorney(s) and/or agent(s) to prosecute this application and transact all business in the Patent and Trademark Office connected therewith. *(List name and registration number)*

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| | RESIDENCE & CITIZENSHIP | CITY | STATE OR FOREIGN COUNTRY | COUNTRY OF CITIZENSHIP |
| | POST OFFICE ADDRESS | POST OFFICE ADDRESS | CITY | STATE & ZIP CODE/COUNTRY |
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| | POST OFFICE ADDRESS | POST OFFICE ADDRESS | CITY | STATE & ZIP CODE/COUNTRY |

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under section 1001 of Title 18 of the United States Code, and that such willful false statements may jeopardize the validity of the application or any patent issuing thereon.

| SIGNATURE OF INVENTOR 201 | SIGNATURE OF INVENTOR 202 | SIGNATURE OF INVENTOR 203 |
|---|---|---|
| DATE: 24 August 1999 | DATE: 27 August 1999 | DATE: 31 August 1999 |
| SIGNATURE OF INVENTOR 204 | SIGNATURE OF INVENTOR 205 | SIGNATURE OF INVENTOR 206 |
| DATE: 6 September 1999 | DATE | DATE |

**IN THE UNITED STATES**
**PATENT AND TRADEMARK OFFICE**

| | | |
|---|---|---|
| Appl. No. | : | |
| Applicant(s) | : | DE JONG et al. |
| Filed | : | Herewith |
| TC/A.U. | : | 2857 (in parent) |
| Examiner | : | Craig MILLER (in parent) |
| Atty. Docket | : | N-17203-A |

Title: CIRCUIT WITH INTERCONNECT TEST UNIT AND A METHOD OF TESTING INTERCONNECTS BETWEEN A FIRST AND A SECOND ELECTRONIC CIRCUIT

**PRELIMINARY AMENDMENT**

Mail Stop **Non-Fee Amendment**
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

Preliminary to examination of the above-referenced application, please amend the application as follows.

**This paper includes** (each beginning on a separate sheet):

1. **Amendments to the specification;**
2. **Amendments to the claims; and**
3. **Remarks/Discussion of issues.**

**Amendments to the Specification:**

Please replace the title with the following rewritten title:

CIRCUIT WITH INTERCONNECT TEST UNIT ~~AND A METHOD OF TESTING INTERCONNECTS BETWEEN A FIRST AND A SECOND ELECTRONIC CIRCUIT~~

**Amendments to the Claims**:

A clean version of the entire set of pending claims (including amendments to the claims, if any) is submitted herewith per 37 CFR 1.121(c)(3). This listing of claims will replace all prior versions, and listings, of claims in the application.

**Listing of Claims**:

1. (Canceled)

2. (Currently amended) An electronic circuit ~~(100)~~ as ~~claimed in Claim 1~~ recited in claim 10, wherein the test unit ~~(120)~~ comprises a Read Only Memory (ROM).

3. (Currently amended) An electronic circuit ~~(100)~~ as ~~claimed in Claim 1~~ recited in claim 10, wherein the test unit ~~(120)~~ comprises a read/write register.

4. (Currently amended) An electronic circuit ~~(402)~~ as ~~claimed in Claim 1~~ recited in claim 10, wherein the test unit ~~(406)~~ comprises a combinatorial circuit ~~(502)~~ implementing an XNOR function and being connected to the I/O nodes.

5. (Currently amended) An electronic circuit ~~(402)~~ as ~~claimed in Claim~~ recited in claim 4, wherein a first selection ~~(410)~~ of the I/O nodes are arranged to carry respective input signals and a second selection ~~(412)~~ of the I/O nodes are arranged to carry respective output signals and wherein the test unit ~~(406)~~ is arranged according to the following rules:

each output signal results from an XNOR function having at least two input signals,

each output signal is dependent on a unique subset of the input signals,

each input signal contributes to at least one output signal via a particular XNOR function.

6. (Currently amended) An electronic circuit ~~(402)~~ as ~~claimed in Claim 1~~ recited in claim 10, wherein the test unit ~~(406)~~ comprises a combinatorial circuit ~~(602)~~ implementing an XOR function and connected to the I/O nodes.

7. (Currently amended) An electronic circuit ~~(100)~~ as ~~claimed in Claim 1~~ recited in claim 10, wherein the main unit ~~(110)~~ is arranged to bring the electronic circuit ~~(100)~~ into the test mode on receipt via a subset of the I/O nodes ~~(130)~~ of a predefined pattern or sequence of patterns.

8. (Currently amended) An electronic circuit ~~(100)~~ as ~~claimed in Claim 1~~ recited in claim 10, wherein the electronic circuit is provided with a test control node and wherein the electronic circuit is arranged to switch into the test mode on the basis of a signal value on the test control node.

9. (Currently amended) An electronic circuit as ~~claimed in Claim 1~~ recited in claim 10, wherein the main unit is a Synchronous Dynamic Random Access Memory

(SDRAM) and the test mode is activatable by a read action following power up of the electronic circuit.

10. (Currently amended) An electronic circuit ~~(100)~~ comprising:

a plurality of input/output (I/O) nodes ~~(130)~~ for connecting the electronic circuit to a further electronic circuit via interconnects,

a main unit ~~(110)~~ for implementing a normal mode function of the electronic circuit,

and a test unit ~~(120)~~ for testing the interconnects,

the electronic circuit having a normal mode in which the I/O nodes ~~(130)~~ are logically connected to the main unit ~~(110)~~ and a test mode in which the I/O nodes ~~(130)~~ are logically connected to the test unit ~~(120)~~,

~~characterised in that~~ wherein the test unit comprises at least one combinatorial circuit ~~(502)~~ implementing at least one of an XNOR function and an XOR function with at least two function inputs and a function output, the function inputs being connected to particular I/O nodes arranged to operate as input nodes of the test circuit and the function output being connected to a particular I/O node arranged to operate as output node of the test circuit.

11-13 (Canceled)

## REMARKS/DISCUSSION OF ISSUES

Claims 2-10 are pending in the application.

Claims 1-9 and 11-13 were elected in the parent application 09/402,154 following a restriction requirement, and were subsequently allowed. Accordingly, claims 1 and 11-13 are canceled as directed to the species elected in the parent application.

Dependent claims 2-9 are amended to depend from independent claim 10, the only claim nonelected in the parent application, and are not narrowed in scope except insofar as claims 2-9 now depend from claim 10 instead of from canceled claim 1. Claim 10 is amended for nonstatutory reasons, to broaden the claim in conformance with a corresponding amendment in the European application. All other changes to the claims are made merely to remove label numbers and otherwise put the claim language in conformance with U.S. patent practice, and not to address issues of patentability. No new matter is added.

The title is amended to reflect the cancellation of method claims 11-13.

This is a preliminary amendment; no Office action has yet been received. Examination of the application on its merits is now respectfully requested. If any points remain in issue that may best be resolved through a personal or telephonic interview, the Examiner is respectfully requested to contact the undersigned at the telephone number listed below.

Respectfully submitted,

Eric M. Bram
Reg. 37,285
Att'y for Applicant(s)
Philips Intellectual Property
& Standards

P.O. Box 3001
Briarcliff Manor, NY 10510-8001
Phone: (914) 333-9635
Fax: (914) 332-06150

PATENT APPLICATION SERIAL NO. _____

U.S. DEPARTMENT OF COMMERCE
PATENT AND TRADEMARK OFFICE
FEE RECORD SHEET

07/21/2003 WASFAW1 00000049 141270 10621002
01 FC:1001 750.00 DA

PTO-1556
(5/87)

*U.S. Government Printing Office: 2002 — 489-267/69033

# PATENT APPLICATION FEE DETERMINATION RECORD

Effective January 1, 2003

Application or Docket Number: PHN 17,203A

## CLAIMS AS FILED - PART I

| | (Column 1) | (Column 2) |
|---|---|---|
| TOTAL CLAIMS | 10 | |
| FOR | NUMBER FILED | NUMBER EXTRA |
| TOTAL CHARGEABLE CLAIMS | 10 minus 20= | * |
| INDEPENDENT CLAIMS | 1 minus 3 = | * |
| MULTIPLE DEPENDENT CLAIM PRESENT | | ☐ |

* If the difference in column 1 is less than zero, enter "0" in column 2

| SMALL ENTITY TYPE ☐ | | OR | OTHER THAN SMALL ENTITY | |
|---|---|---|---|---|
| RATE | FEE | | RATE | FEE |
| BASIC FEE | 375.00 | OR | BASIC FEE | 750.00 |
| X$ 9= | | OR | X$18= | |
| X42= | | OR | X84= | |
| +140= | | OR | +280= | |
| TOTAL | | OR | TOTAL | 750 |

## CLAIMS AS AMENDED - PART II

| | | (Column 1) CLAIMS REMAINING AFTER AMENDMENT | | (Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR | (Column 3) PRESENT EXTRA |
|---|---|---|---|---|---|
| AMENDMENT A | Total | * | Minus | ** | = |
| | Independent | * | Minus | *** | = |
| | FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM | | | | ☐ |

| SMALL ENTITY | | OR | OTHER THAN SMALL ENTITY | |
|---|---|---|---|---|
| RATE | ADDITIONAL FEE | | RATE | ADDITIONAL FEE |
| X$ 9= | | OR | X$18= | |
| X42= | | OR | X84= | |
| +140= | | OR | +280= | |
| TOTAL ADDIT. FEE | | OR | TOTAL ADDIT. FEE | |

| | | (Column 1) CLAIMS REMAINING AFTER AMENDMENT | | (Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR | (Column 3) PRESENT EXTRA |
|---|---|---|---|---|---|
| AMENDMENT B | Total | * | Minus | ** | = |
| | Independent | * | Minus | *** | = |
| | FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM | | | | ☐ |

| RATE | ADDITIONAL FEE | | RATE | ADDITIONAL FEE |
|---|---|---|---|---|
| X$ 9= | | OR | X$18= | |
| X42= | | OR | X84= | |
| +140= | | OR | +280= | |
| TOTAL ADDIT. FEE | | OR | TOTAL ADDIT. FEE | |

| | | (Column 1) CLAIMS REMAINING AFTER AMENDMENT | | (Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR | (Column 3) PRESENT EXTRA |
|---|---|---|---|---|---|
| AMENDMENT C | Total | * | Minus | ** | = |
| | Independent | * | Minus | *** | = |
| | FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM | | | | ☐ |

| RATE | ADDITIONAL FEE | | RATE | ADDITIONAL FEE |
|---|---|---|---|---|
| X$ 9= | | OR | X$18= | |
| X42= | | OR | X84= | |
| +140= | | OR | +280= | |
| TOTAL ADDIT. FEE | | OR | TOTAL ADDIT. FEE | |

* If the entry in column 1 is less than the entry in column 2, write "0" in column 3.
** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20."
***If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3."
The "Highest Number Previously Paid For" (Total or Independent) is the highest number found in the appropriate box in column 1.

# MULTIPLE DEPENDENT CLAIM FEE CALCULATION SHEET

SERIAL NO 10621002 | FILING DATE 07-16-03

APPLICANT(S)

CLAIMS

| | AS FILED | | AFTER 1ST AMENDMENT | | AFTER 2ND AMENDMENT | |
|---|---|---|---|---|---|---|
| | IND | DEP | IND | DEP | IND | DEP |
| 1 | | | | | | |
| 2 | | 1 | | | | |
| 3 | | 1 | | | | |
| 4 | | 1 | | | | |
| 5 | | 1 | | | | |
| 6 | | 1 | | | | |
| 7 | | 1 | | | | |
| 8 | | 1 | | | | |
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| 49 | | | | | | |
| 50 | | | | | | |
| TOTAL IND. | 1 | | | | | |
| TOTAL DEP. | 9 | | | | | |
| TOTAL CLAIMS | 10 | | | | | |

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|---|---|---|---|---|---|---|
| | IND | DEP | IND | DEP | IND | DEP |
| 51 | | | | | | |
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| 100 | | | | | | |
| TOTAL IND. | | | | | | |
| TOTAL DEP. | | | | | | |
| TOTAL CLAIMS | | | | | | |

PTO-1360 (12/02)

*MAY BE USED FOR ADDITIONAL CLAIMS OR AMENDMENTS

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P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

| APPLICATION NUMBER | FILING OR 371 (c) DATE | FIRST NAMED APPLICANT | ATTORNEY DOCKET NUMBER |
|---|---|---|---|
| 10/621,002 | 07/16/2003 | Franciscus G.M. De Jong | PHN 17,203A |

**CONFIRMATION NO. 9122**

24737
PHILIPS INTELLECTUAL PROPERTY & STANDARDS
P.O. BOX 3001
BRIARCLIFF MANOR, NY 10510

**FORMALITIES LETTER**

*OC000000011057765*

Date Mailed: 10/17/2003

## NOTICE TO FILE CORRECTED APPLICATION PAPERS

### *Filing Date Granted*

An application number and filing date have been accorded to this application. The application is informal since it does not comply with the regulations for the reason(s) indicated below. Applicant is given TWO MONTHS from the date of this Notice within which to correct the informalities indicated below. Extensions of time may be obtained by filing a petition accompanied by the extension fee under the provisions of 37 CFR 1.136(a).

The required item(s) identified below must be timely submitted to avoid abandonment:

- An abstract of the technical disclosure not exceeding 150 words in length and commencing on a separate sheet in compliance with 37 CFR 1.72(b) is required. An abstract was not provided for this application.

Replies should be mailed to: Mail Stop Missing Parts
Commissioner for Patents
P.O. Box 1450
Alexandria VA 22313-1450

***A copy of this notice MUST be returned with the reply.***

Customer Service Center
Initial Patent Examination Division (703) 308-1202
PART 3 - OFFICE COPY

**Abstract**

An electronic circuit comprises a plurality of input/output (I/O) nodes for connecting the electronic circuit to a further electronic circuit via interconnects. A main unit implements a normal mode function of the electronic circuit. A test unit tests the interconnects. The electronic circuit has a normal mode in which the I/O nodes are logically connected to the main unit and a test mode in which the I/O nodes are logically connected to the test unit. In the test mode the test unit is operable as a low complexity memory via the I/O nodes.

| | Search Text | DBs |
|---|---|---|
| 1 | "0588507" | DERWENT |
| 2 | "0588507" | DERWENT |
| 3 | "2278689" | DERWENT |
| 4 | miller$.xa. | DERWENT |
| 5 | miller$.xa. | USPAT |
| 6 | miller$.xa. and dut | USPAT |
| 7 | (("57841559") or ("6119256") or ("5894224") or ("5680407") or ("6297643") or ("5963038")).PN. | USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB |
| 8 | ((("57841559") or ("6119256") or ("5894224") or ("5680407") or ("6297643") or ("5963038")).PN.) or 5968191.pn. | USPAT |
| 9 | (interconnect and test and digital).ti,ab. | USPAT |
| 10 | ((((("57841559") or ("6119256") or ("5894224") or ("5680407") or ("6297643") or ("5963038")).PN.) or ((((("57841559") or ("6119256") or ("5894224") or ("5680407") or ("6297643") or ("5963038")).PN.) or 5968191.pn.) or ((interconnect and test and digital).ti,ab.) ) and ((logic or logical) and (operation or operator)) | USPAT |
| 11 | ((((("57841559") or ("6119256") or ("5894224") or ("5680407") or ("6297643") or ("5963038")).PN.) or ((((("57841559") or ("6119256") or ("5894224") or ("5680407") or ("6297643") or ("5963038")).PN.) or 5968191.pn.) or ((interconnect and test and digital).ti,ab.) ) and ((logic or logical) WITH (operation or operator)) | USPAT |
| 12 | (circuit and test and (connection or interconnection) ).ti,ab. | USPAT |

| | Search Text | DBs |
|---|---|---|
| 13 | ((circuit and test and (connection or interconnection) ).ti,ab.) and 702/(117-124).ccls. | USPAT |
| 14 | ((circuit and test and (connection or interconnection) ).ti,ab.) and 702/117-124.ccls. | USPAT |
| 15 | ((circuit and test and (connection or interconnection) ).ti,ab.) and 702.clas. | USPAT |
| 16 | ("2278689").PN. | USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB |
| 17 | ("0588507").PN. | USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB |
| 18 | ("ep588507").PN. | USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB |
| 19 | ("0588507").PN. | USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB |
| 20 | ("5819025").PN. | USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB |
| 21 | ("4791358" \| "4879717" \| "4963824" \| "5029166" \| "5084874" \| "5172377" \| "5175494" \| "5202625" \| "5222068" \| "5260649" \| "5260949" \| "5281864" \| "5329533" \| "5331274" \| "5442640").PN. | USPAT |
| 22 | 5442640.URPN. | USPAT |
| 23 | (("4791358" \| "4879717" \| "4963824" \| "5029166" \| "5084874" \| "5172377" \| "5175494" \| "5202625" \| "5222068" \| "5260649" \| "5260949" \| "5281864" \| "5329533" \| "5331274" \| "5442640").PN.) or 5442640.URPN. | USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB |

| | Search Text | DBs |
|---|---|---|
| 24 | ((("4791358" \| "4879717" \| "4963824" \| "5029166" \| "5084874" \| "5172377" \| "5175494" \| "5202625" \| "5222068" \| "5260649" \| "5260949" \| "5281864" \| "5329533" \| "5331274" \| "5442640").PN.) or 5442640.URPN.) and (connection or interconnection or (inter adj connection) ) and test | USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB |
| 25 | glucometer.ti. | USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB |
| 26 | glucometer | USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB |
| 27 | (("6119256") or ("6297643") or ("5680407") or ("5781559")).PN. | USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB |
| 28 | ((("6119256") or ("6297643") or ("5680407") or ("5781559")).PN.) and memory | USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB |
| 29 | ((boundary adj scan).ti,ab.) and memory.ti,ab. | USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB |
| 30 | (((boundary adj scan).ti,ab.) and memory.ti,ab.) and (test adj mode) | USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB |
| 31 | (("5819025") or ("5880595")).PN. | USPAT |
| 32 | (boundary adj scan).ti,ab. | USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB |
| 33 | ((boundary adj scan).ti,ab.) and ("xnor" and "xor") | USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB |
| 34 | ("0000172").PN. | DERWENT |
| 35 | ("$000172").PN. | DERWENT |
| 36 | ("98200288").PN. | USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB |
| 37 | 98200288.an. | USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB |
| 38 | "98200288" | USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB |

| | Search Text | DBs |
|---|---|---|
| 39 | (normal and test) WITH mode | USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB |
| 40 | ((normal and test) WITH mode) and (dut or (device adj under adj test)) | USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB |
| 41 | (((normal and test) WITH mode) and (dut or (device adj under adj test))) and (((normal and test) WITH mode) and ("xnor" and "xor")) | USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB |
| 42 | ((normal and test) WITH mode) and ("xnor" and "xor") | USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB |
| 43 | (((normal and test) WITH mode) and (dut or (device adj under adj test))) and (((normal and test) WITH mode) and ("xnor" and "xor")) | USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB |
| 44 | (((normal and test) WITH mode) and ("xnor" and "xor")) not ((((normal and test) WITH mode) and (dut or (device adj under adj test))) and (((normal and test) WITH mode) and ("xnor" and "xor"))) | USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB |
| 45 | ("5416409" \| "5781559" \| "5819025" \| "5880595" \| "5968191").PN. | USPAT |

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# NOTICE OF ALLOWANCE AND FEE(S) DUE

24737 7590 05/04/2004

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P.O. BOX 3001
BRIARCLIFF MANOR, NY 10510

| EXAMINER | |
|---|---|
| MILLER, CRAIG S | |
| ART UNIT | PAPER NUMBER |
| 2857 | |

DATE MAILED: 05/04/2004

| APPLICATION NO. | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. | CONFIRMATION NO. |
|---|---|---|---|---|
| 10/621,002 | 07/16/2003 | Franciscus G.M. De Jong | PHN 17203A | 9122 |

TITLE OF INVENTION: CIRCUIT WITH INTERCONNECT TEST UNIT

| APPLN. TYPE | SMALL ENTITY | ISSUE FEE | PUBLICATION FEE | TOTAL FEE(S) DUE | DATE DUE |
|---|---|---|---|---|---|
| nonprovisional | NO | $1330 | $300 | $1630 | 08/04/2004 |

**THE APPLICATION IDENTIFIED ABOVE HAS BEEN EXAMINED AND IS ALLOWED FOR ISSUANCE AS A PATENT. PROSECUTION ON THE MERITS IS CLOSED. THIS NOTICE OF ALLOWANCE IS NOT A GRANT OF PATENT RIGHTS. THIS APPLICATION IS SUBJECT TO WITHDRAWAL FROM ISSUE AT THE INITIATIVE OF THE OFFICE OR UPON PETITION BY THE APPLICANT. SEE 37 CFR 1.313 AND MPEP 1308.**

**THE ISSUE FEE AND PUBLICATION FEE (IF REQUIRED) MUST BE PAID WITHIN THREE MONTHS FROM THE MAILING DATE OF THIS NOTICE OR THIS APPLICATION SHALL BE REGARDED AS ABANDONED. THIS STATUTORY PERIOD CANNOT BE EXTENDED. SEE 35 U.S.C. 151. THE ISSUE FEE DUE INDICATED ABOVE REFLECTS A CREDIT FOR ANY PREVIOUSLY PAID ISSUE FEE APPLIED IN THIS APPLICATION. THE PTOL-85B (OR AN EQUIVALENT) MUST BE RETURNED WITHIN THIS PERIOD EVEN IF NO FEE IS DUE OR THE APPLICATION WILL BE REGARDED AS ABANDONED.**

**HOW TO REPLY TO THIS NOTICE:**

I. Review the SMALL ENTITY status shown above.

If the SMALL ENTITY is shown as YES, verify your current SMALL ENTITY status:
A. If the status is the same, pay the TOTAL FEE(S) DUE shown above.

B. If the status is changed, pay the PUBLICATION FEE (if required) and twice the amount of the ISSUE FEE shown above and notify the United States Patent and Trademark Office of the change in status, or

If the SMALL ENTITY is shown as NO:

A. Pay TOTAL FEE(S) DUE shown above, or

B. If applicant claimed SMALL ENTITY status before, or is now claiming SMALL ENTITY status, check the box below and enclose the PUBLICATION FEE and 1/2 the ISSUE FEE shown above.

☐ Applicant claims SMALL ENTITY status. See 37 CFR 1.27.

II. PART B - FEE(S) TRANSMITTAL should be completed and returned to the United States Patent and Trademark Office (USPTO) with your ISSUE FEE and PUBLICATION FEE (if required). Even if the fee(s) have already been paid, Part B - Fee(s) Transmittal should be completed and returned. If you are charging the fee(s) to your deposit account, section "4b" of Part B - Fee(s) Transmittal should be completed and an extra copy of the form should be submitted.

III. All communications regarding this application must give the application number. Please direct all communications prior to issuance to Mail Stop ISSUE FEE unless advised to the contrary.

**IMPORTANT REMINDER: Utility patents issuing on applications filed on or after Dec. 12, 1980 may require payment of maintenance fees. It is patentee's responsibility to ensure timely payment of maintenance fees when due.**



PTOL-85 (Rev. 11/03) Approved for use through 04/30/2004.

# PART B - FEE(S) TRANSMITTAL

**Complete and send this form, together with applicable fee(s), to: Mail** **Mail Stop ISSUE FEE**
**Commissioner for Patents**
**P.O. Box 1450**
**Alexandria, Virginia 22313-1450**

**or Fax** **(703) 746-4000**

INSTRUCTIONS: This form should be used for transmitting the ISSUE FEE and PUBLICATION FEE (if required). Blocks 1 through 4 should be completed where appropriate. All further correspondence including the Patent, advance orders and notification of maintenance fees will be mailed to the current correspondence address as indicated unless corrected below or directed otherwise in Block 1, by (a) specifying a new correspondence address; and/or (b) indicating a separate "FEE ADDRESS" for maintenance fee notifications.

CURRENT CORRESPONDENCE ADDRESS (Note: Legibly mark-up with any corrections or use Block 1)

24737 7590 05/04/2004

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BRIARCLIFF MANOR, NY 10510

Note: A certificate of mailing can only be used for domestic mailings of the Fee(s) Transmittal. This certificate cannot be used for any other accompanying papers. Each additional paper, such as an assignment or formal drawing, must have its own certificate of mailing or transmission.

**Certificate of Mailing or Transmission**

I hereby certify that this Fee(s) Transmittal is being deposited with the United States Postal Service with sufficient postage for first class mail in an envelope addressed to the Mail Stop ISSUE FEE address above, or being facsimile transmitted to the USPTO, on the date indicated below.

(Depositor's name)

(Signature)

(Date)

| APPLICATION NO. | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. | CONFIRMATION NO. |
|---|---|---|---|---|
| 10/621,002 | 07/16/2003 | Franciscus G.M. De Jong | PHN 17203A | 9122 |

TITLE OF INVENTION: CIRCUIT WITH INTERCONNECT TEST UNIT

| APPLN. TYPE | SMALL ENTITY | ISSUE FEE | PUBLICATION FEE | TOTAL FEE(S) DUE | DATE DUE |
|---|---|---|---|---|---|
| nonprovisional | NO | $1330 | $300 | $1630 | 08/04/2004 |

| EXAMINER | ART UNIT | CLASS-SUBCLASS |
|---|---|---|
| MILLER, CRAIG S | 2857 | 702-117000 |

1. Change of correspondence address or indication of "Fee Address" (37 CFR 1.363).

❑ Change of correspondence address (or Change of Correspondence Address form PTO/SB/122) attached.

❑ "Fee Address" indication (or "Fee Address" Indication form PTO/SB/47; Rev 03-02 or more recent) attached. **Use of a Customer Number is required.**

2. For printing on the patent front page, list (1) the names of up to 3 registered patent attorneys or agents OR, alternatively, (2) the name of a single firm (having as a member a registered attorney or agent) and the names of up to 2 registered patent attorneys or agents. If no name is listed, no name will be printed.

1 _____

2 _____

3 _____

3. ASSIGNEE NAME AND RESIDENCE DATA TO BE PRINTED ON THE PATENT (print or type)

PLEASE NOTE: Unless an assignee is identified below, no assignee data will appear on the patent. Inclusion of assignee data is only appropriate when an assignment has been previously submitted to the USPTO or is being submitted under separate cover. Completion of this form is NOT a substitute for filing an assignment.

(A) NAME OF ASSIGNEE (B) RESIDENCE: (CITY and STATE OR COUNTRY)

Please check the appropriate assignee category or categories (will not be printed on the patent); ❑ individual ❑ corporation or other private group entity ❑ government

4a. The following fee(s) are enclosed:

❑ Issue Fee

❑ Publication Fee

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| APPLICATION NO. | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. | CONFIRMATION NO. |
|---|---|---|---|---|
| 10/621,002 | 07/16/2003 | Franciscus G.M. De Jong | PHN 17203A | 9122 |

24737 7590 05/04/2004

PHILIPS INTELLECTUAL PROPERTY & STANDARDS
P.O. BOX 3001
BRIARCLIFF MANOR, NY 10510

| EXAMINER | |
|---|---|
| MILLER, CRAIG S | |

| ART UNIT | PAPER NUMBER |
|---|---|
| 2857 | |

DATE MAILED: 05/04/2004

**Determination of Patent Term Adjustment under 35 U.S.C. 154 (b)**
(application filed on or after May 29, 2000)

The Patent Term Adjustment to date is 0 day(s). If the issue fee is paid on the date that is three months after the mailing date of this notice and the patent issues on the Tuesday before the date that is 28 weeks (six and a half months) after the mailing date of this notice, the Patent Term Adjustment will be 0 day(s).

If a Continued Prosecution Application (CPA) was filed in the above-identified application, the filing date that determines Patent Term Adjustment is the filing date of the most recent CPA.

Applicant will be able to obtain more detailed information by accessing the Patent Application Information Retrieval (PAIR) system (http://pair.uspto.gov).

Any questions regarding the Patent Term Extension or Adjustment determination should be directed to the Office of Patent Legal Administration at (703) 305-1383. Questions relating to issue and publication fee payments should be directed to the Customer Service Center of the Office of Patent Publication at (703) 305-8283.

| Notice of Allowability | Application No. | Applicant(s) | |
|---|---|---|---|
| | 10/621,002 | DE JONG ET AL. | |
| | Examiner | Art Unit | |
| | Craig Miller | 2857 | |

***-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--***

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to *pre-amendment filed 7/16/03*.

2. ☒ The allowed claim(s) is/are *2-10 now renumbered 2-9 and 1, respectively*.

3. ☒ The drawings filed on *16 July 2003* are accepted by the Examiner.

4. ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
   a) ☒ All b) ☐ Some* c) ☐ None of the:
      1. ☒ Certified copies of the priority documents have been received.
      2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
      3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

   * Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
**THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.**

5. ☐ A SUBSTITUTE OATH OR DECLARATION must be submitted. Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL PATENT APPLICATION (PTO-152) which gives reason(s) why the oath or declaration is deficient.

6. ☐ CORRECTED DRAWINGS ( as "replacement sheets") must be submitted.
   (a) ☐ including changes required by the Notice of Draftsperson's Patent Drawing Review ( PTO-948) attached
      1) ☐ hereto or 2) ☐ to Paper No./Mail Date _____.
   (b) ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.

   **Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).**

7. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

**Attachment(s)**

1. ☒ Notice of References Cited (PTO-892)
2. ☐ Notice of Draftperson's Patent Drawing Review (PTO-948)
3. ☐ Information Disclosure Statements (PTO-1449 or PTO/SB/08), Paper No./Mail Date _____
4. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material
5. ☐ Notice of Informal Patent Application (PTO-152)
6. ☐ Interview Summary (PTO-413), Paper No./Mail Date _____.
7. ☐ Examiner's Amendment/Comment
8. ☒ Examiner's Statement of Reasons for Allowance
9. ☐ Other _____.

1. Claims 2-10, now renumbered 2-9 and 1, respectively, are allowable over the prior art of record.

2. The following is an examiner's statement of reasons for allowance:

The prior art of record neither discloses nor suggests normal and test interconnects wherein the test input unit includes at least one combinatorial circuit with at least two inputs and a function output, thus testing particular I/O nodes.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "*Comments on Statement of Reasons for Allowance.*"

3. The prior art made of record but not relied upon is deemed pertinent to applicant's disclosure.

Williams (EP pub. 0,588,507 A2) discloses testing IC interconnections.
Thatcher *et al.* (GB 2,278,689 A) discloses measuring passive elements during IC testing.
Whetsel (5,103,450) discloses test protocols for IC testing.
Hunter (5,416,409) discloses IC interconnect integrity.
Muris *et al.* (5,781,559) discloses a testable circuit with separate test mode interconnects.

4. Any inquiry concerning this communication or earlier communications from the Examiner should be directed to Craig Steven Miller whose telephone number is (571) 272-2219.

The Examiner can normally be reached on Mondays, Tuesdays and Thursdays from 07:00 am through 4:00 p.m. EDT.

If attempts to reach the Examiner by telephone are unsuccessful, the Examiner's Supervisor, Marc Hoff, can be reached at (571) 272-2216.

Any inquiry of a general nature or relating to the status of this application should be directed to the Group receptionist whose telephone number is (571) 272-2800.

Craig Steven Miller (ss)
21 April 2004

MARC S. HOFF
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2800

| Notice of References Cited | Application/Control No. 10/621,002 | Applicant(s)/Patent Under Reexamination DE JONG ET AL. | |
|---|---|---|---|
| | Examiner Craig Miller | Art Unit 2857 | Page 1 of 1 |

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| | B | US-5,416,409 | 05-1995 | Hunter, Paul W. | 324/158.1 |
| | C | US-5,781,559 | 07-1998 | Muris et al. | 714/726 |
| | D | US- | | | |
| | E | US- | | | |
| | F | US- | | | |
| | G | US- | | | |
| | H | US- | | | |
| | I | US- | | | |
| | J | US- | | | |
| | K | US- | | | |
| | L | US- | | | |
| | M | US- | | | |

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| * | | Document Number Country Code-Number-Kind Code | Date MM-YYYY | Country | Name | Classification |
|---|---|---|---|---|---|---|
| | N | EP 0588507a2 | 03-1994 | EPO | Williams | G01R 31/04 |
| | O | GB 2278689 A | 12-1994 | United Kingdom | THATCHER et al. | G01R 31/28 |
| | P | | | | | |
| | Q | | | | | |
| | R | | | | | |
| | S | | | | | |
| | T | | | | | |

**NON-PATENT DOCUMENTS**

| * | | Include as applicable: Author, Title Date, Publisher, Edition or Volume, Pertinent Pages) |
|---|---|---|
| | U | |
| | V | |
| | W | |
| | X | |

*A copy of this reference is not being furnished with this Office action. (See MPEP § 707.05(a).)
Dates in MM-YYYY format are publication dates. Classifications may be US or foreign.

(19) Europäisches Patentamt
European Patent Office
Office européen des brevets

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## (54) Method of testing interconnections between integrated circuits in a circuit.

(57) A method of testing the interconnections between integrated circuits in a circuit uses latches, respectively connected to the terminals of the integrated circuit, which are connectable in series as a shift register so that a test pattern of bits can be entered into the latches. The pattern of bits is transmitted through the interconnections to other latches and then shifted out of the circuit along the shift register. Discrepancies between the input and output patterns indicate malfunctioning interconnections. The method is extended to apply to a microprocessor in the circuit, the microprocessor having a program that enables it to use its RAM to act as the latches connected to the other integrated circuits. The program may be stored in on-chip memory in the microprocessor and where that memory is RAM, EPROM or EEPROM it may be erased therefrom after successful testing of the circuit.

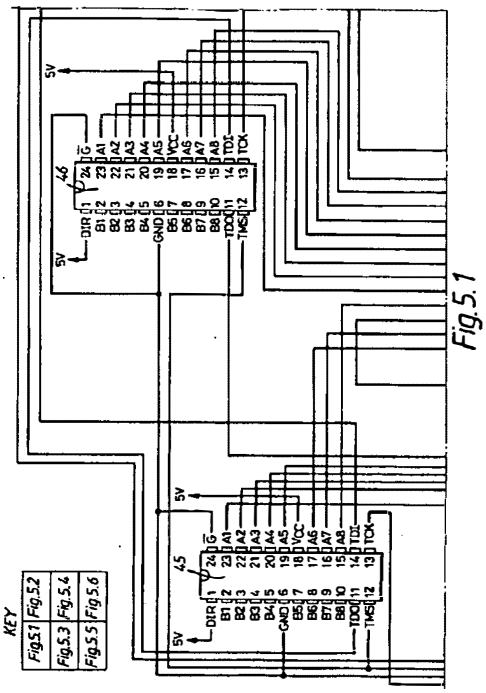


Fig.5.1

EP 0 588 507 A2

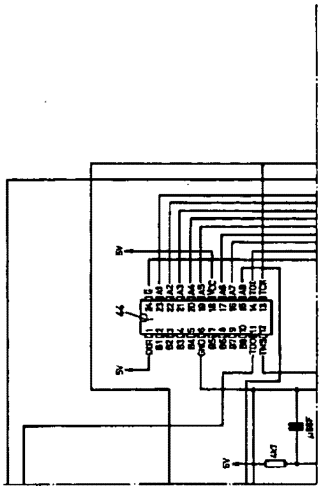

Fig 5.2

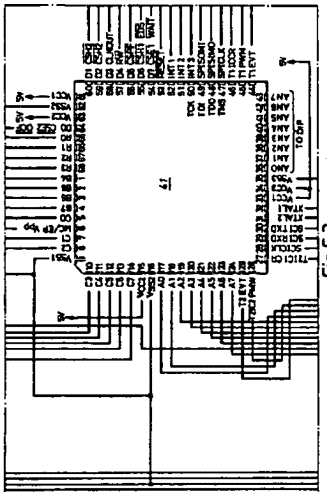

Fig 5.3

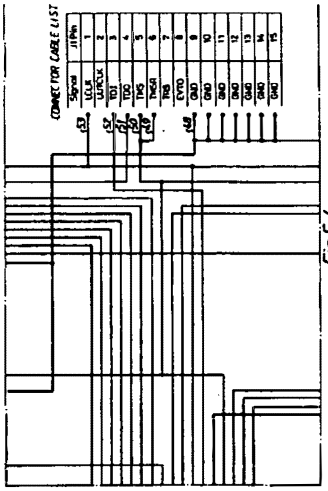

Fig 5.4

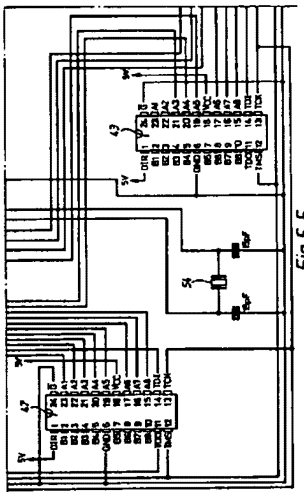

Fig 5.5

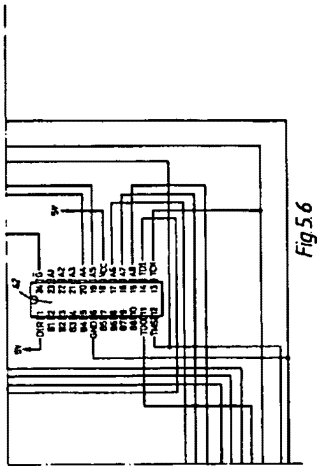

Fig 5.6

The present invention relates to the testing of circuit boards, in particular to the boundary scan testing of a circuit board including a microprocessor.

Manufacturers of electronic circuits commonly produce their circuits in the form of printed circuit boards having mounted on them a plurality of integrated circuits as well as other components. The components are interconnected by conductors or metallic tracks printed on the board with electrical contact between the leads or pins of the components and the tracks made using solder joints. The interconnections may be imperfect and may display short- or open-circuit connections that are erroneous, the errors possibly arising from faults of either the solder joints or the tracks.

Once a circuit board is completed it would, of course, be possible to operate the circuit as a method of testing it but with the complexity of many such boards it would be both difficult and time consuming to test it thoroughly to check that all interconnections were correctly made. Boundary scan testing is a method of testing the interconnections between integrated circuits on a circuit board which enables the test to be carried out more quickly. A system of boundary scan testing is defined by IEEE standard 11491.1-1990 "Standard Test Access Port and Boundary Scan Architecture" also known as JTAG. To support JTAG boundary scan testing an integrated circuit will have specially provided for each of a number of its pins a boundary scan cell, for example, an input latch, an output latch or both of those or a combined input-output latch, for transmitting and receiving signals via the particular pin. In addition a boundary scan cell may include a control latch. The latches may each comprise a shift register latch and a shadow latch. The shift register latches can be joined with others, from the same and other boundary scan cells, to form a long shift register joining up all the input and/or output terminals of the integrated circuits. The cells can therefore be loaded serially with data supplied to an dedicated test data input pin on each integrated circuit. Data already in the shift register latches is shifted out via a dedicated test data output pin of the integrated circuit when the shift register is operated. From time to time data can be transferred between the shift register latches and their corresponding shadow latches.

In a circuit having more than one JTAG integrated circuit the shift registers of each integrated circuit can be joined serially to form one long shift register known as the scan path.

To perform a test of the interconnections between integrated circuits on a circuit board test data appropriately interspersed with control data is fed along the scan path and is loaded into the input and output latches of the integrated circuits. Each boundary scan cell will either be an input cell or an output cell depending on the value loaded in its control latch if it has one; if a cell has no control latch then it will have been built as an input cell or an output cell. Next, each output cell transmits the test data held in its output latch over the interconnections via its pin and each input latch receives test data from the interconnections via its pin and stores it. The resulting pattern of data in the latches can then be shifted out along the scan path for analysis to find out whether the interconnections are functioning correctly. Note that the data held in the shadow latches actually determine whether the boundary scan cells are inputs or outputs and the values to be output on the cells' pins are directly responsive to data supplied to the pins.

Usually the test patterns are generated by a computer which also analyses the resulting patterns. Normally the computer is given a description of the integrated circuits on the scan path, for example which cells have input latches and which have output latches, and a description of the interconnections on the board between the pins. From those descriptions the computer generates a number of test patterns, and after running the test the resulting patterns are analysed to see whether the circuit board has the described interconnections and, if not, to indicate in what way it might be faulty.

Boundary scan testing does provide a quick and reliable method of testing a circuit board; however it does require that the integrated circuits are constructed to include the necessary hardware; this includes not only the latches described above but the means to join them in a shift register and the means responsive to the necessary control signals.

Boundary scan testing is at its simplest and most effective when all the integrated circuits on a circuit board support it. If only some of the integrated circuits support it, then there are a number of things that can be done. The manufacturer of the integrated circuits can redesign the integrated circuits to include the hardware to support boundary scan testing; this takes some time, increases the silicon areas of the devices and hence their cost, and means that the new integrated circuits will not be compatible with the old ones and hence cannot directly replace the old ones since dedicated control pins and test data pins must be provided on the new ones. The manufacturer of the circuit board can add buffers that do support boundary scan testing between the integrated circuits that do not and the rest of the circuit but that increases cost and may affect the performance and timing of the circuit, and will introduce further interconnections that cannot be tested. As a last resort the corrections to the non-supporting integrated circuits can be ignored by the test, so reducing the coverage of the testing; the effects of that can to some extent be reduced by more lengthy and elaborate boundary scan test procedures, such as those described by Robinson and Deshages in a paper entitled "Interconnect Testing of Boards with Partial Boundary Scan" published by Gen Rad, Inc., of 300 Baker Avenue, Concord, MA, USA.

The disadvantages of these approaches are increased when the non-supporting integrated circuit is a microprocessor, for example a microcontroller, since such devices are usually the centre of functionality of any circuit in which they are included and consequently are connected to many of the other components.

Addition of the necessary JTAG hardware to a microcontroller can involve a considerable amount of work due to the complexity, type and number of input and output pins normally associated with them. Consequently, there is a reluctance to modify existing microcontroller designs to incorporate this feature.

It is an object of the present invention to provide a method of boundary scan testing a circuit, which includes a microprocessor that overcomes at least the difficulties described above.

According to the present invention there is provided a method of testing interconnections of a circuit having a plurality of integrated circuits,

at least some of the integrated circuits including

storage elements respectively associated with some of the terminals of those integrated circuits and means for joining the storage elements into at least one shift register chain,

the method including

entering an initial test pattern of bits serially into the storage elements along the at least one shift register chain,

transferring certain of the bits of the initial test pattern from the storage elements into which they were entered, via the terminals and interconnections, to others of the storage elements,

retrieving the resulting pattern of bits serially from the storage elements along the at least one shift register chain, and

comparing the initial test pattern and resulting pattern to derive information about the interconnections, characterised in that

at least one of the plurality of integrated circuits is a microprocessor, there being stored in the circuit a test program which causes the microprocessor to perform a number of operations including

entering serially into the microprocessor part of the initial test pattern of bits and storing it in a memory,

reading certain of the bits stored in the memory and producing corresponding output signals on terminals of the microprocessor connected to particular interconnections,

reading bits via particular interconnections at terminals of the microprocessor and storing the received bits in the memory, and

producing as an output from the microprocessor in serial form the received bits stored in the memory, so as to enable interconnections connected to terminals of the microprocessor to be tested.

The JTAG standard will now be described with reference to Figures 1, 2 and 3, followed by a description of a method of boundary scan testing a circuit board including a microprocessor, by way of example only. Reference will be made to the accompanying drawings, of which:-

FIGURE 1 is a circuit diagram of a circuit having three integrated circuits, all of which support boundary scan testing according to the JTAG standard;

FIGURE 2 is a diagram of an integrated circuit that supports boundary scan testing according to the JTAG standard;

FIGURE 3 is a state diagram for the test access port controller of Figure 2;

FIGURE 4 is a block diagram of one example of a microcontroller; and

FIGURE 5 is a diagram of a circuit including the microcontroller of Figure 4 that can be arranged to provide for boundary scan testing.

Figure 1 is a circuit diagram of a circuit having three integrated circuits 21,22, 23 all of which support JTAG boundary scan testing. Each integrated circuit has twenty pins 1-20 of which 1 and 20 are connected respectively to test mode select (TMS) and test clock (TCK) signal lines of JTAG bus, pins 10 and 11 are connected to the power supply, and application pins 3-9 and 12-18 are connected via various of the interconnections 25,26,27,28 to pins of others of the integrated circuits 21,22,23 or to terminals 24. For each of the pins 3-9 and 12-18 there is provided in the integrated circuit a boundary scan cell 29 having a combined input/output latch and a control latch. The boundary scan cells of all the integrated circuits are on a scan path 30 which starts at the terminal TDI, enters integrated circuit 21 at pin 2, passing through the boundary scan cells of that integrated circuit, and then leaves via pin 19 continuing through the integrated circuits 21,22 in a similar way in turn and finishing at terminal TDO. The scan path 30 can operate as a shift register driven by clock signals TCK.

To test, for example, the interconnects 26 between the pins 12-18 of the integrated circuit 21 and the pins 3-9 of the integrated circuit 22, test data and interspersed control data is passed along the scan path 30, under the control of the signals on the TMS and TCK lines, into the input and output latches of the boundary scan cells 29. The input and output latches of the cells for pins 12-18 of the integrated circuit 21 are set up to be outputs and those for pins 3-9 of the integrated circuit 22 set up to be inputs. The important values of the test

data are those provided for the pins 12 to 18 of the integrated circuit 21 since it is these that are transferred across to the input latches of the integrated circuit 22, once all the data has been shifted in along the scan path. The data latched across are subsequently shifted out and analysed to check whether the interconnections 26 are all functioning correctly.

As a particular example, a test pattern might be LOW in all of the output latches for pins 12 to 18 except for a HIGH in the latch for pin 15. In the diagram it can be seen that if there were no fault a HIGH would be latched across to the input latch of pin 8 of the integrated circuit 22, the others of pins 3-9 receiving LOWs. If, for example, the interconnect from pin 15 to pin 8 was shorted to that from pin 14 to pin 4, then a HIGH would be received at the latch for pin 4, assuming that the latch for pin 15 was able to drive those interconnections HIGH while the latch for pin 14 was trying to drive them LOW. This extra HIGH in the resulting pattern shifted out along the scan path 30 would be detected by the computer performing the test which would produce an output indicating the nature of the fault detected.

It is clear that to test fully the interconnections for open and short circuits many operations of shifting in data, latching across and shifting out will be required. Test patterns are normally generated by the computer running the test under the control of software, such as the ASSET system of Texas Instruments Incorporated. More complicated interconnects than the one pin to one pin interconnects 26, for example the interconnects 27, can also be tested. Interconnects to terminals 24 could be tested by connecting them to other integrated circuits supporting JTAG off the circuit board under test, but included in the scan path.

Figure 2 is a diagram of an integrated circuit 39 that supports JTAG similar to those of Figure 1. In addition to boundary scan cells 29 on the scan path 30, the application pins 31 and pins 2,19 to connect to the scan path 30, pins 1,20 to receive the control signals, TMS, TCK and pins 10,11 to connect to the power supply, Figure 2 shows application circuitry 32, a test access port (TAP) controller 33, a bypass register 34, an instruction register 35, multiplexers 36,37 and a tristate latch 38. In the JTAG standard the bypass register and the set of boundary scan cells are known as data registers. In a full implementation of the standard there are other data registers provided but their operation is not relevant to the present invention and they will not be described.

The application circuitry provides the normal functions of the integrated circuit when it is not in test mode. During those times it communicates freely with other components via the application pins 31 unhindered by the latches of the boundary scan cells. Note that in practice it may be required that the inputs and outputs of the application circuitry are latched and in that case the latches of the boundary scan cells could be used for that purpose.

The bypass register 34 and the instruction register are alternative scan paths to the boundary scan cells through the integrated circuit 39. Multiplexers 36 and 37 recombine those paths into a single one and latch 38 simply increases the length of each path by one step. The test access port controller is responsive to the TCK and TMS signals of the test bus and also to the value stored in the instruction register; it controls the operation of the rest of the test logic.

The bypass register 34 and the instruction register 35 like the boundary scan cells not only have latches which form a shift register when data is scanned through them but also latches shadowing those latches to and from which values can be transferred from time to time.

Figure 3 shows a state diagram for the test access port controller 33 of Figure 2, which conforms to the JTAG standard. The test access port controller examines the TMS signal at each positive going edge of TCK and changes to a new state depending on the value of TMS. This is shown in the diagram by arrows labelled 1 and 0 indicating the values of the TMS signal. The two parts of the diagram enclosed in dotted rectangles are for manipulating respectively a data register and the instruction register and are marked DR-SCAN 40 and IR-SCAN 39. The particular data register manipulated depends on the value held in the instruction register. It should be noted, then, that the selection of the scan path change through the integrated circuit 39 involves both the control signals, TMS and TCK, and the value in the instruction register 35. Moving around the state diagram allows boundary scan tests such as those described above to be carried out.

A full description of the functions of these states can be found in the JTAG standard. Some functions are not implemented in the device described below and only a brief description of the relevant states will be given.

The TEST-LOGIC-RESET state is the state on power up. In this state the test logic is inactive and the integrated circuit 39 performs its normal function using the application circuitry 32.

The RUN-TEST/IDLE state is used in the full standard for some special test functions; those are not implemented in the device described below but the state is provided to allow the states to change in the standard way in response to the TMS and TCK signals.

The SELECT-DR-SCAN and SELECT-IR SCAN states perform no function other than allowing other states to be reached from them.

In the CAPTURE-IR state the instruction register is loaded with a 10000001 pattern and is sent along the scan path. If the TEST-LOGIC-RESET state has been passed through since the last scan operation, the latch

38 which drives the TDO (test data output) pin 19 is enabled to output a LOW or zero, otherwise it is enabled to output the same as that which it was outputting the last time it was enabled.

In the SHIFT-IR state data is advanced through the instruction register, one step per cycle of TCK, from the TDI (test data input) pin 2 to the TDO pin 19. The 10000001 pattern in the register in the CAPTURE-IR state is shifted out and can be used to confirm that the instruction register is connected in the scan path.

EXIT1-IR and EXIT2-IR perform no operation; they allow the shifting operation to be ended.

PAUSE-IR performs no operation; the test access port controller 33 can be held in this state to allow the shifting operation to be suspended for a period of time.

In the state UPDATE-IR the value in the shift register latches of the instruction register are transferred to the shadow latches.

The functions of the states for manipulating the data registers depend on the particular register to be manipulated. They are as follows:-

CAPTURE-DR; the data register selected by the value in the instruction register is placed on the scan path, and the latch 38 that drives the TDO pin 19 is enabled in a similar manner as it is by the CAPTURE-IR instruction, except that when the bypass register is selected the latch 38 is enabled to output a low or zero level. In the case of the boundary scan cells it is during this state that the values present on the input pins and received by the shadow input latches from other boundary scan cells via the interconnects 26,27 are latched, along with data held in the other shadow latches, into the shift register latches.

In the SHIFT-DR state data held in the shift register latches of the selected register is shifted through the integrated circuit 39 from the TDI pin 2 to the TDO pin 19 one bit per cycle of TCK. In the case of the data register the data shifted will include control data as well as test data. In the case of the bypass register bits of the data are shifted through the integrated circuit rapidly since the register is only one bit long. This register is used, for example, when it is desired to use the boundary scan cells of other integrated circuits but not those of the particular integrated circuit.

The EXIT-DR, EXIT2-DR and PAUSE-DR states have similar functions to the corresponding IR states.

In the UPDATE-DR state the latches shadowing the shift register latches are updated from those latches. In the case of the boundary scan cells the control data latches and the output latches are given their new values.

Thus to perform the test of interconnects such as the interconnect 26,27 described above it is necessary to pass through the IR-SCAN state 39 once to shift into the instruction register an instruction which puts the boundary scan cells 29 on the scan path, and to pass through the DR-SCAN state 40 twice, once to shift into the boundary scan cells the test data and the control data and to transfer those values into the shadow latches and once more to latch across test data from other boundary scan cells to the input shadow latches, then into the shift register latches and to shift the resulting pattern out of the boundary scan shift register.

The present invention relates to enabling a boundary scan test to be performed so as to include a microprocessor, for example a microcontroller, on the scan path when the microprocessor or microcontroller does not have special circuitry to support boundary scan testing. The approach of the present invention to this problem is to program the microprocessor so that it simulates the behaviour of a JTAG integrated circuit such as those of Figures 1 and 2 in response to test bus and test data signals making use of the resources of the microprocessor as they are without providing any additional circuitry on the microprocessor.

In the present invention the simulation is carried outunder the control of software and the application of the invention to microcontrollers is particularly simple because many microcontrollers have, on chip, an amount of ROM or EPROM or EEPROM in which the software can be stored. Also many microcontrollers have, on chip, an amount of RAM in which the data manipulated by the software can be stored. The resulting device is therefore self-contained.

If the memory in which the test software is stored is of a kind as to permit it, for example if it is RAM or EPROM or EEPROM, the test software could be erased after a JTAG test has been successfully completed so as to release the memory space occupied by the test software for other uses.

By writing software which causes a microprocessor to simulate the hardware and protocol of the JTAG standard, a device, conforming to the standard, can be incorporated into a boundary scan test without any modifications to the device itself. In this way, no costly reengineering of an existing microprocessor is required and microprocessor-based systems can easily be made compatible with existing JTAG test and support hardware.

To simulate the bahaviour of a JTAG circuit the software will have to manipulate the input and output to and from the microprocessor chip via its pins. Microcontrollers usually provide flexible methods of controlling the input and output including having pins which are individually programmable which simplifies the task of writing the software.

One example of a microcontroller, according to the present invention will now be described. Figure 4 is a

block diagram of a TMS370 CX5X microcontroller manufactured by Texas Instruments. A full description of this device can be found in the data sheet published by Texas Instruments. The program used to enable the microcontroller to support boundary scan testing is appended to this specification. The program is written in TMS 370 assembly language. The program is stored in the program memory of the microcontroller, which may be either ROM or EPROM. To simulate the JTAG boundary scan test mode the program expects the microcontroller to be operated in its single chip microcomputer mode which is achieved by applying a LOW signal level input to its MC pin. In this mode the microcontroller defaults to its unexpanded mode with its ports A,B,C,D configured as general purpose input/output ports rather than address, data and control bus connections. The program leaves the microcontroller in this mode.

The program expects the TCK, TMS, TDI signals of the JTAG test bus to be respectively applied to the INT3, SPICLK and SPISOMI pins of the microcontroller and produces the TDO output signal on the SPISIMO pin; of these pins, INT3, is configured to function as a maskable interrupt input and the other pins which are those of the serial peripheral interface are configured as general purpose input/output pins. Of the remaining pins of the microcontroller INT1 and INT2, those of the serial communications interface and those of the timers are configured as general purpose input/output pins and the analogue port is configured as a general purpose digital input port.

The program simulates the functions of the usual JTAG circuitry and in particular it simulates the functions of the test access port controller 33 and its progress through the JTAG state diagram (Figure 3). To do this the program maintains two registers in the RAM memory of the microcontroller, which indicate the next state, one for HIGH values of TMS and one for LOW. Since the JTAG test access port controller and hence the program start off in the TEST-LOGIC-RESET state the program initialises those two registers to indicate TEST-LOGIC-RESET and RUN-TEST/IDLE respectively as the next states. The program then sets up INT3 to generate interrupts at the positive going edges of TCK. On interrupt, an interrupt handling routine checks the value of the TMS signal to see if it is LOW or HIGH and then calls one of a number of routines which perform the functions of the next state, the particular routine chosen being that indicated by the appropriate next state register. In addition to the functions of their state those routines update the next state register appropriately, so that on subsequent interrupts the states are traversed in the manner shown in Figure 3.

Some of the states require action on the negative going edges of TCK, such action being in particular the outputting of the TDO signal ready for it to be received by another integrated circuit on the next positive going edge. The state routines handle this by resetting INT3 to generate interrupts on negative going edges and waiting for an interrupt. When an interrupt occurs the interrupt handling routine outputs the next bit of the TDO signal and restores INT3 to generating interrupts on positive going edges.

The program maintains a register in the RAM of the microcontroller for simulating the instruction register. This register is manipulated by the state routines for the states of the IR-SCAN box 39 of Figure 3 in a similar manner to that applied to the instruction register 35 of the JTAG circuitry. The value or instruction code in this register is then available to the state routines for the states of the DR-SCAN box 40 of Figure 3 so that they can modify their actions accordingly.

JTAG circuitry may in general support all or only some of the instructions specified in the standard. The program appended to this specification supports only the EXTEST and BYPASS instructions. If codes for other instructions are found in the instructions register then the BYPASS instruction is performed.

When the code for the EXTEST instruction is in the instruction register maintained by the program the DR-SCAN 40 state routine manipulates a data register.

The data register occupies seventeen consecutive eight-bit registers of the RAM memory of the microcontroller. A table given in the comment lines at the beginning of the appended program shows how the data register is organised. This data register corresponds to the shift register latches of the boundary scan cells 29 of integrated circuits with special JTAG circuitry provided. The register that corresponds to the shadow latches consists of the latches of the ports of the microcontroller that already exist. Those latches exist in the portion of the memory map of the microcontroller known as the peripheral file. In order that transfers between the data register and the port latches, which transfers correspond to transfers between the shadow latches and their shift register latches respectively, can be made simply, the organisation of the data register reflects that of the port latches in the memory map. Such an organisation has no disadvantages for test pattern generation and analyses systems, such as the ASSET system mentioned above, since they require no particular ordering of input/output latches control data latches and the like, but they do require that the order of these latches and the boundary scan cell or pin to which they belong, are specified to them. Therefore, to test a TMS370 CX5X microcontroller having the appended program using a system such as ASSET, that information as contained in the table will have to be specified to the system.

The transfers made between the data register and the existing port latches are made by the DR-CAPTURE and DR-UPDATE state routines. Respectively, these routines transfer data from the existing port latches to

the data register and in the reverse direction. The shifting of the data register is carried out by the SHIFT-DR routine in which the bit present at the TDI pin 2 is shifted into bit 135 of the data register (see the table at the start of the appended program), data bits already in the register are moved down one bit and bit 0 is set up to be output at the TDO pin 19 at the next negative going edge of the TCK signal by placing it in a register in the RAM called OUTREG in the program. The bit held in OUTREG is set up by the program on the TDO pin on a negative going edge of TCK; in this way the function of the latch 38 of JTAG integrated circuits is simulated.

From the table it can be seen that pins of the microcontroller included on the scan path variously have combined input/output latches, separate input and/or output latches and possibly a control latch. For each of those latches there is a bit of the data register. However, there are some bits of the data register marked by a dash in the "definition" column of the table that are not intended to have corresponding shadow latches. These bits lengthen the shift register and so should be specified to the pattern generation and analysis system as being present but containing no information when read by the analysis system. These bits when the other bits of the data register are transferred into their shadow latches will also, of course, be written into the peripheral file into whatever latch, if any, happens to be at that location. In the present example this has no undesired effects. However in other examples perhaps running other microprocessors this may not be so. A remedy would be to mask out these bits with appropriate values as they are written to the peripheral file or its equivalents.

When the code for the BYPASS instruction is in the instruction register the DR-SCAN 40 state routines simulate the operation of a JTAG integrated circuit having its bypass register on the scan path. In fact all instruction codes other than that for EXTEST will be treated as a BYPASS instruction. The simulation is achieved in the following way:-

In the CAPTURE-DR state routine , a Low or zero is placed in OUTREG ready to be set up on the TDO pin on the next negative going edge of TCK. In the SHIFT-DR state routine the value present at the TDI pin is read and is placed in OUTREG ready to be set up on the TDO pin. In the UPDATE-DE state routine no operation other than to update the next state registers is performed.

The DR-SCAN 40 state routine also makes allowance, for both the BYPASS and EXTEST instructions, for the pipelining of the TMS signal.

It will be appreciated that the method of simulating the behaviour of a JTAG integrated circuit employed by the program described above is not the only possibility. For example, instead of being interrupt driven the program could poll the TCK signal, the data register could be organised differently or a different selection of the pins to which the test bus (TCK,TMS,TDI,TDO) is connected could be made. As another example, a similar program might be written for a microprocessor whose equivalents of ports A,B,C,D of the TMS 370CX5X can only be configured as ports for data, address and control busses. In such a program it would not be so straightforward to produce the desired outputs on those pins, since for example the instruction set of the microprocessor might not allow the pins for the address and data busses to be programmed separately. However, there will be an instruction which writes a data value to a certain address and using this instruction with the desired values could be used to program the ports together. Since these values would possibly only remain on the pins for a few cycles of the microprocessor's clock, allowances would have to be made so that the period during which the data was set up on the pins included the time at which it was latched by other JTAG integrated circuits. Programming the control port at the same time as the address and data busses might not be possible, and the interconnects connected to those pins would have to be tested at different times, with allowance made for that in the test pattern generation and analysis system.

It is not necessary that the software be stored in memory internal to the microprocessor. The JTAG simulation software can be stored in many places, depending on the configuration of the system. If external ROM or PROM or EPROM is used for example, the software could reside there and be a minimal overhead to the total system memory. Conveniently the software could be transferred as a block from the external ROM or PROM or EPROM to the internal RAM of the microprocessor and run from there. Alternatively, a removable test ROM or PROM or EPROM could be used, and replaced by application software after successful testing of the printed circuit board. Many microcontrollers are intended for embedded control in mass-produced end applications. Such devices frequently use on chip masked ROM or EPROM. In the case of EPROM, the device could be erased and reprogrammed by the application software following a successful test.

A particularly advantageous solution can be achieved with microcontrollers such as the TMS370 family, which have on chip EEPROM (non-volatile memory). The JTAG software can be embedded in the device EEPROM before shipment to the manufacturer of the end equipment, and the application software provided by him on ROM or PROM or EPROM (either on-or off-chip) can read a check byte in the EEPROM at power-up which forces execution of the JTAG software.

Following a successful test, the JTAG software can be erased by the microcontroller itself, perhaps after receiiving a special command word in the simulated instruction register. In this way, the JTAG software leaves

no trace of its existence following the test, and the resources it had used are available to the application software in normal use. The special command word could be one of the unused codes of the JTAG standard. The EEPROM of the TMS370 family has the ability to be written to our erased by the microcontroller itself, the 12.6 volts required being generated from the supply rails by an on-chip charge pump.

If the software or the data it manipulates is not stored within the microprocessor but rather off-chip in some other memory then certain of the input and output pins of the microprocessor will be required for transferring instruction words or data words between the microprocessor and that memory. The lines required for the TMS370CX5X microcontroller of Figure 4, would include ports A to D. These lines would not, therefore, be available for direct JTAG testing. However some indication of their functioning would still be provided by a JTAG test since if the program or data was not correctly transferred the test pattern generation and analysis system would not receive a proper response from the microprocessor thus indicating a fault with those lines.

Although the simulation described produces a microprocessor that conforms to the JTAG protocol for boundary scan testing systems, the present invention could be applied to other systems, protocols or standards of boundary scan testing.

Figure 5 is a diagram of a circuit including a TMS 370C756 microcontroller which has stored in its EPROM memory the program appended to this patent specification. Figure 5 demonstrates the use in boundary scan testing of the circuit and its subsequent use in the application that the circuit was designed for.

The circuit has at its centre the TMS 370C756 microcontroller 41. The analogue port pins AN0 ... AN7 of the microcontroller 41 are connected to a set of eight DIP switches not shown, providing, depending on their positions, either a HIGH or LOW level to the respective pins of the analogue port. Many of the other pins are connected to various of the pins of the A ports of the six octal buffers, 42 to 47 of the type SN74BCT8245. These buffers have special circuitry provided to support JTAG boundary scan testing.

The circuit has terminals 48 to 53 for a JTAG connector cable which connects the circuit to a test pattern generation and analysis system. In particular there are four terminals 50-53 for connection of the test bus signals TMS,TDO,TDI,TCK. The TMS terminal 50 is connected to the TMS input pin of each of the octal buffers 42-27 and to the SPICLK pin of the microcontroller 41 which serves as its TMS pin. The TCK terminal 53 is connected to the TCK input pin of each of the octal buffers 42-47 and to the INT3 pin of the microcontroller 41 which serves as its TCK pin. Also provided in the circuit is a scan path; this starts at the TDI terminal 52 and passes into the microcontroller 41 at its SPISOMI pin, which serves as its TCK pin. The scan path then continues on through each of the octal buffers 42-47 in turn, passing into each at its TDI pin and passing out at its TDO pin, to arrive finally at the TDO terminal 52.

The octal buffers 42-47 and the microcontroller 41 have suitable connections to a power supply, not shown. The microcontroller is suitably connected to a crystal 54 for controlling the frequency of its internal clock. The reset pin of the microcontroller 41 is connected through an RC network to a HIGH signal level, so that the reset pin is held at its active LOW level for a few moments after the power supply is turned on, before rising to a HIGH level and allowing the microcontroller 41 to start operating. The octal buffers 42-47 have their DIR pins connected to a HIGH level, so that the buffers are configured with their A port pins as inputs and their B port pins as outputs. Various of the B port output pins of the octal buffers 42-47 are connected to driver circuits not shown which, depending on the levels of the signal outputs of the buffer, illuminate light emitting diodes, not shown.

The microcontroller 41 having the appended program stored in its EPROM makes the testing of all the interconnections of the circuit with a JTAG test pattern generator and analysis system a straightforward matter. Firstly, the test pattern generator and analysis system is given a description of the circuit in terms of the interconnections between the integrated circuits, those being those between the octal buffers 42-47 and the microcontroller 41, and in terms of the order of, and the latches contained on, the boundary scan cells of the integrated circuits. For the microcontroller the boundary scan cells are simulated by the appended program and the information required is given in the table at the start of the program. The circuit can then be connected to the test pattern generator and analysis system.

In trials of the microcontroller with the appended program it was found that the test bus clock signal TCK could be operated at a rate of up to about 4 kHz.

The full JTAG standard requires, for an integrated circuit to conform to that standard, that the integrated circuit can be clocked at any speed from 0Hz to several MHz. Although clearly the maximum clock rate of 4kHz achieved by the microcontroller in the trial does not conform to the wide ranging speed requirement of the standard, the microcontroller does conform to the JTAG protocol and therefore enables the circuit interconnections to be tested. Since the test as described above does not require redesign of the microcontroller to enable the test to be executed, the microcontroller can retain compatibility with its earlier versions.

The test now proceeds, as described above in relation to Figure 1, with the test pattern generator generating test patterns which are fed to the integrated circuits of the circuit along the scan path. Certain of the bits

of the test pattern after being latched into the integrated circuits are transferred via the circuit interconnections to other latches of the integrated circuits. The resulting pattern of bits is output along the scan path to the analysis system for analysis.

The appended program as it stands does not terminate and expects the testing to continue indefinitely. However it could be modified so that if there were an application program also resident in the EPROM of the microcontroller this could be executed while the appended program was waiting in the TEST-LOGIC-RESET state.

The appended program can be used in the following way. The program is stored in the EPROM of the microcontroller by the manufacturer of the microcontroller before the device is shipped to the manufacturer of a circuit into which it is to be assembled, for example that of Figure 5, who installs the microcontroller in the circuit and tests the circuit wiring using boundary scan testing as described above. Once the test has been successfully completed, the program is of no further use (except perhaps if the circuit is returned for servicing by its end user), and consequently the storage space in the EPROM is wasted. The manufacturer of the assembled circuit can, if he wishes, erase the program in the EPROM and use the space to store at least part of an application program required to operate the circuit. In that way, all of the EPROM storage space can be used for application programs after the test program has been erased. In the case of the circuit of Figure 5 such an application program might illuminate the light emitting diodes in a sequence which depends on the setting of the DIP switches.

Such rewriting of the EPROM means that a JTAG testable microcontroller has been provided not only without special circuitry being added to the design of the microcontroller but also without permanently using any of the resources of the microcontroller except for the four pins used for connection to the test bus. The latter is not a serious disadvantage because very few circuits including a microcontroller require the use of all of their pins and the program can easily be rewritten so that connection of the test bus is made to otherwise unused pins. If necessary it might be possible after testing of the circuit to reconnect the pins connected to the test bus to other interconnections by moving links or with other means.

APPENDIX

```
;
; THE DATA REGISTER DEFINITIONS FOLLOW :-
;
;   BIT NUMBER     PIN No.   DEFINITION      REGISTER   BIT No.    PFILE
;
;       0            17        A0 DATA         R100        0        P022
;       1            18        A1 DATA                     1
;       2            19        A2 DATA                     2
;       3            20        A3 DATA                     3
;       4            21        A4 DATA                     4
;       5            22        A5 DATA                     5
;       6            23        A6 DATA                     6
;       7            24        A7 DATA                     7
;       8            --        A0 DDR          R101        0        P023
;       9            --        A1 DDR                      1
;       10           --        A2 DDR                      2
;       11           --        A3 DDR                      3
;       12           --        A4 DDR                      4
;       13           --        A5 DDR                      5
;       14           --        A6 DDR                      6
;       15           --        A7 DDR                      7
;       16           65        B0 DATA         R102        0        P026
;       17           66        B1 DATA                     1
;       18           67        B2 DATA                     2
;       19           68        B3 DATA                     3
;       20            1        B4 DATA                     4
;       21            2        B5 DATA                     5
;       22            3        B6 DATA                     6
;       23            4        B7 DATA                     7
;       24           --        B0 DDR          R103        0        P027
;       25           --        B1 DDR                      1
;       26           --        B2 DDR                      2
;       27           --        B3 DDR                      3
;       28           --        B4 DDR                      4
;       29           --        B5 DDR                      5
;       30           --        B6 DDR                      6
;       31           --        B7 DDR                      7
;       32            5        C0 DATA         R104        0        P02A
;       33            7        C1 DATA                     1
;       34            8        C2 DATA                     2
;       35           10        C3 DATA                     3
;       36           11        C4 DATA                     4
;       37           12        C5 DATA                     5
;       38           13        C6 DATA                     6
;       39           14        C7 DATA                     7
;       40           --        C0 DDR          R105        0        P02B
;       41           --        C1 DDR                      1
;       42           --        C2 DDR                      2
;       43           --        C3 DDR                      3
;       44           --        C4 DDR                      4
;       45           --        C5 DDR                      5
;       46           --        C6 DDR                      6
;       47           --        C7 DDR                      7
;       48           64        D0 DATA         R106        0        P02E
;       49           60        D1 DATA                     1
;       50           59        D2 DATA                     2
;       51           58        D3 DATA                     3
;       52           57        D4 DATA                     4
;       53           56        D5 DATA                     5
;       54           55        D6 DATA                     6
;       55           54        D7 DATA                     7
;       56           --        D0 DDR          R107        0        P02F
;       57           --        D1 DDR                      1
;       58           --        D2 DDR                      2
```

```
;   59   --   D3 DDR                    3
;   60   --   D4 DDR                    4
;   61   --   D5 DDR                    5
;   62   --   D6 DDR                    6
;   63   --   D7 DDR                    7
;   64   --   T1EVT DDR        R108     0      P04D
;   65   --   --                        1
;   66   44   T1EVT DATA OUT             2
;   67   44   T1EVT DATA IN              3
;   68   --   --                        4
;   69   --   --                        5
;   70   --   --                        6
;   71   --   --                        7
;   72   --   T1CR DDR          R109     0      P04E
;   73   --   --                        1
;   74   46   T1CR DATA OUT              2
;   75   46   T1CR DATA IN               3
;   76   --   T1PWM DDR                 4
;   77   --   --                        5
;   78   45   T1PWM DATA OUT             6
;   79   45   T1PWM DATA IN              7
;   80   --   T2EVT DDR        R110     0      P06D
;   81   --   --                        1
;   82   25   T2EVT DATA OUT             2
;   83   25   T2EVT DATA IN              3
;   84   --   --                        4
;   85   --   --                        5
;   86   --   --                        6
;   87   --   --                        7
;   88   --   T2CR DDR          R111     0      P06E
;   89   --   --                        1
;   90   27   T2CR DATA OUT              2
;   91   27   T2CR DATA IN               3
;   92   --   T2PWM DDR                 4
;   93   --   --                        5
;   94   26   T2PWM DATA OUT             6
;   95   26   T2PWM DATA IN              7
;   96   --   SCICLK DDR       R112     0      P05D
;   97   --   --                        1
;   98   28   SCICLK DATA OUT            2
;   99   28   SCICLK DATA IN             3
;  100   --   --                        4
;  101   --   --                        5
;  102   --   --                        6
;  103   --   --                        7
;  104   --   SCIRXD DDR       R113     0      P05E
;  105   --   --                        1
;  106   29   SCIRXD DATA OUT            2
;  107   29   SCIRXD DATA IN             3
;  108   --   SCITXD DDR                4
;  109   --   --                        5
;  110   30   SCITXD DATA OUT            6
;  111   30   SCITXD DATA IN             7
;  112   36   AN 0             R114     0      P07D
;  113   37   AN 1                       1
;  114   38   AN 2                       2
;  115   39   AN 3                       3
;  116   40   AN 4                       4
;  117   41   AN 5                       5
;  118   42   AN 6                       6
;  119   43   AN 7                       7
;  120   --   --               R115     0      P017
;  121   --   --                        1
;  122   --   --                        2
```

```
;       123         --      --                          3
;       124         --      --                          4
;       125         --      --                          5
;       126         52      INT1 DATA IN                6
;       127         --      --                          7
;       128         --      --              R116        0       P018
;       129         --      --                          1
;       130         --      --                          2
;       131         51      INT2 DATA OUT               3
;       132         --      INT2 DDR                    4
;       133         --      --                          5
;       134         51      INT2 DATA IN                6
;       135         --      --                          7
;
;
;       TDI = SPISOMI     PIN 49
;
;       TDO = SPISIMO     PIN 48
;
;       TMS = SPICLK      PIN 47
;
;       TCK = INT3        PIN 50
;
;       INTERNAL REGISTER ALLOCATION FOLLOWS :-
;
;        STACK            R20  (14H)
;
;        OUTREG           R50  (32H)   DATA REGISTER OUTPUT LATCH
;
;        BYPASS REGISTER  R51  (33H)   not used
;
;        STATE_L REG      R52  (34H)   HOLDS MSB OF NEXT STATE IF TMS=0
;
;        STATE_L REG      R53  (35H)   HOLDS LSB OF NEXT STATE IF TMS=0
;
;        STATE_H REG      R54  (36H)   HOLDS MSB OF NEXT STATE IF TMS=1
;
;        STATE_H REG      R55  (37H)   HOLDS LSB OF NEXT STATE IF TMS=1
;
;        INSTRUCTION REG  R56  (38H)
;
;        TMS_DELAY        R57  (39H)   DELAY FLAG FOR TMS PIPELINE
;
;        DATA REGISTER    R100 TO R116  (64H)  (74)
;
;
;
;
;
;
;
;
;
;
;
;
;
```

```
        .text
        .GLOBAL DR_CAPTURE
        .GLOBAL DR_SHIFT
        .GLOBAL DR_EXIT1
        .GLOBREG STATE_H
        .GLOBREG STATE_L
        .GLOBREG INSTRUCT_REG
        .GLOBREG OUTREG
        .GLOBREG TMS_DELAY
;
DR_CAPTURE      MOV     #01H,TMS_DELAY      ;
;
                CMP     #00H,INSTRUCT_REG   ; CHECK INSTRUCTION REGISTER
                JNZ     BYPASS_C            ; IF NOT 00, ASSUME BYPASS
;
;
; INSTRUCTION=0, SO MODE MUST BE XTEST
; LOAD ALL I/O INTO RAM BASED SHIFT REGISTER
;
                MOV     P022,R100     ;     PORT A I/O
                MOV     P023,R101     ;     PORT A DDR
                MOV     P026,R102     ;     PORT B I/O
                MOV     P027,R103     ;     PORT B DDR
                MOV     P02A,R104     ;     PORT C I/O
                MOV     P02B,R105     ;     PORT C DDR
                MOV     P02E,R106     ;     PORT D I/O
                MOV     P02F,R107     ;     PORT D DDR
                MOV     P04D,R108     ;     TIMER 1 I/O
                MOV     P04E,R109     ;     TIMER 1 I/O
                MOV     P06D,R110     ;     TIMER 2 I/O
                MOV     P06E,R111     ;     TIMER 2 I/O
                MOV     P05D,R112     ;     SCI I/O
                MOV     P05E,R113     ;     SCI I/O
                MOV     P07D,R114     ;     A-D I/P
                MOV     P017,R115     ;     INT1 I/O
                MOV     P018,R116     ;     INT2 I/O
;
;
CAPTURE_NEXT    MOVW    #DR_SHIFT,STATE_L       ; NEXT STATE IS DR_SHIFT
                MOVW    #DR_EXIT1,STATE_H       ; NEXT STATE IS DR_EXIT1
                RTS
;
BYPASS_C        MOV     #010H,OUTREG            ; LOAD '0' INTO OUTPUT REGIST
                JMP     CAPTURE_NEXT
;
                .END
```

```
        .text
        .GLOBAL DR_EXIT1
        .GLOBAL DR_PAUSE
        .GLOBAL DR_UPDATE
        .GLOBAL DR_SHIFT1
        .GLOBAL BYPASS_S1
        .GLOBREG STATE_H
        .GLOBREG STATE_L
        .GLOBREG TMS_DELAY
        .GLOBREG INSTRUCT_REG
;
SPIPC2  .EQU    P03E
;
;
DR_EXIT1        BTJO    #01,TMS_DELAY,NO_DELAY1
                MOV     #01,TMS_DELAY
;
DELAY1          CMP     #00H,INSTRUCT_REG  ; CHECK INSTRUCTION REGISTER
                JNZ     BYPASS_DELAY       ; IF NOT 00H, ASSUME BYPASS
;
SHIFT_DELAY     CALL    DR_SHIFT1
                JMP     NO_DELAY1
;
BYPASS_DELAY    CALL    BYPASS_S1
;
NO_DELAY1       MOVW    #DR_PAUSE,STATE_L       ; NEXT STATE IS DR_PAUSE
                MOVW    #DR_UPDATE,STATE_H      ; NEXT STATE IS DR_UPDATE
                RTS
;
                .END
```

```
        .text
        .GLOBAL DR_EXIT2
        .GLOBAL DR_SHIFT
        .GLOBAL DR_UPDATE
        .GLOBREG STATE_H
        .GLOBREG STATE_L
;
DR_EXIT2        MOVW    #DR_SHIFT,STATE_L       ; NEXT STATE IS DR_SHIFT
                MOVW    #DR_UPDATE,STATE_H      ; NEXT STATE IS DR_UPDATE
                RTS
;
                .END
```

```
        .text
        .GLOBAL DR_EXIT2
        .GLOBAL DR_PAUSE
        .GLOBREG STATE_H
        .GLOBREG STATE_L
;
DR_PAUSE        MOVW    #DR_PAUSE,STATE_L       ; NEXT STATE IS PAUSE
                MOVW    #DR_EXIT2,STATE_H       ; NEXT STATE IS DR_UPDATE
                RTS
;
                .END
```

```
        .text
        .GLOBAL IR_SCAN
        .GLOBAL DR_SCAN
        .GLOBAL DR_CAPTURE
        .GLOBREG STATE_L
        .GLOBREG STATE_H
;
SPIPC2  .EQU    P03E
;
;
DR_SCAN         MOVW    #DR_CAPTURE,STATE_L     ; NEXT STATE IS DR_SHIFT
                MOVW    #IR_SCAN,STATE_H        ; NEXT STATE IS IR_SCAN
                RTS
;
                .END
```

```
        .text
        .GLOBAL DR_EXIT1
        .GLOBAL DR_SHIFT
        .GLOBAL DR_SHIFT1
        .GLOBAL BYPASS_S1
        .GLOBREG STATE_L
        .GLOBREG STATE_H
        .GLOBREG OUTREG
        .GLOBREG INSTRUCT_REG
        .GLOBREG OUTREG
        .GLOBREG TMS_DELAY
SPIPC2          .EQU    P03E
INT3CTL         .EQU    P019


DR_SHIFT        CMP     #00H,INSTRUCT_REG  ; CHECK INSTRUCTION REGISTER
                JNZ     BYPASS_S           ; IF NOT 00H, ASSUME BYPASS
;
                BTJO    #01H,TMS_DELAY,OUTPUT   ; IS THIS THE FIRST TIME
                CALL    DR_SHIFT1               ; INTO DR_SHIFT ? IF SO,
                JMP     OUTPUT                  ; DON'T SHIFT !
;
;
;
; SHIFT REGISTER ROUTINE, BY ROTATING THROUGH CARRY THE LEAST SIGNIFICANT
; BIT OF EACH REGISTER CAN BE INPUT TO THE NEXT REGISTER IN THE CHAIN
; AUTOMATICALLY.
;
DR_SHIFT1       BTJO    #08H,SPIPC2,IN_ONE      ; COPY TDI (SPISOMI) TO CARRY
IN_ZERO         CLRC
                JMP     ROTATE
IN_ONE          SETC
ROTATE          RRC     R116                    ; SHIFT STATE OF SPISOMI INTO
                RRC     R115                    ; R116 AND SHIFT ALL REGISTER
                RRC     R114                    ; TOWARDS LSB.
                RRC     R113
                RRC     R112
                RRC     R111
                RRC     R110
                RRC     R109
                RRC     R108
                RRC     R107
                RRC     R106
                RRC     R105
                RRC     R104
                RRC     R103
                RRC     R102
                RRC     R101                    ; LAST SHIFT FEEDS LSB
                RRC     R100                    ; INTO CARRY
                RTS
;
OUTPUT          BTJO    #01H,R100,OUT_ONE       ; PRE-LOAD OUTPUT REG WITH
OUT_ZERO        MOV     #010H,OUTREG            ; LSB AND TDO ENABLE BIT
                JMP     WAIT_NEG1               ; READY FOR -VE TCK EDGE
OUT_ONE         MOV     #050H,OUTREG            ;
;
WAIT_NEG1       MOV     #00H,TMS_DELAY
                MOV     #01H,INT3CTL            ; ENABLE TCK (INT3) FOR
                EINTH                           ; -VE EDGE DETECTION
                IDLE
;
                MOVW    #DR_SHIFT,STATE_L       ; NEXT STATE IS DR_SHIFT
                MOVW    #DR_EXIT1,STATE_H       ; NEXT STATE IS DR_EXIT1
                RTS
```

```
;
BYPASS_S        BTJO    #01H,TMS_DELAY,WAIT_NEG1 ; IS THIS THE FIRST TIME
                CALL    BYPASS_S1                ; INTO BYPASS ? IF SO,
                JMP     WAIT_NEG1                ; DON'T SHIFT !
;
;
;
BYPASS_S1       BTJO    #08H,SPIPC2,IN_ONE2      ; READ TDI (SPISOMI)
;
IN_ZERO2        MOV     #010H,OUTREG             ; LOAD '0' INTO OUTPUT REGIST
                RTS
;
IN_ONE2         MOV     #050H,OUTREG             ; LOAD '1' INTO OUTPUT REGIST
                RTS
;
                .END


        .text
        .GLOBAL DR_SCAN
        .GLOBAL RUN_TEST
        .GLOBAL DR_UPDATE
        .GLOBREG STATE_H
        .GLOBREG STATE_L
        .GLOBREG INSTRUCT_REG
;
SPIPC2  .EQU    P03E
;
;
DR_UPDATE       MOV     #00,SPIPC2    ; TRI-STATE TDO
;
                CMP     #00H,INSTRUCT_REG  ; CHECK INSTRUCTION REGISTER
                JNZ     BYPASS             ; IF NOT 00H, ASSUME BYPASS
;
                MOV     R100,P022     ;     PORT A I/O
                MOV     R101,P023     ;     PORT A DDR
                MOV     R102,P026     ;     PORT B I/O
                MOV     R103,P027     ;     PORT B DDR
                MOV     R104,P02A     ;     PORT C I/O
                MOV     R105,P02B     ;     PORT C DDR
                MOV     R106,P02E     ;     PORT D I/O
                MOV     R107,P02F     ;     PORT D DDR
                MOV     R108,P04D     ;     TIMER 1 I/O
                MOV     R109,P04E     ;     TIMER 1 I/O
                MOV     R110,P06D     ;     TIMER 2 I/O
                MOV     R111,P06E     ;     TIMER 2 I/O
                MOV     R112,P05D     ;     SCI I/O
                MOV     R113,P05E     ;     SCI I/O
                MOV     R114,P07D     ;     A-D I/P
                MOV     R115,P017     ;     INT1 I/O
                MOV     R116,P018     ;     INT2 I/O
;
;
BYPASS          MOVW    #RUN_TEST,STATE_L       ; NEXT STATE IS RUN_TEST
                MOVW    #DR_SCAN,STATE_H        ; NEXT STATE IS DR_SCAN
                RTS
;
                .END
```

```
        .text
        .GLOBAL IR_CAPTURE
        .GLOBAL IR_SHIFT
        .GLOBAL IR_EXIT1
        .GLOBREG STATE_H
        .GLOBREG STATE_L
        .GLOBREG INSTRUCT_REG
        .GLOBREG TMS_DELAY
;
IR_CAPTURE      MOV     #01H,TMS_DELAY
;
                MOV     #01H,INSTRUCT_REG       ; LOAD INSTRUCTION REG
                                                ; WITH 0000 0001
;
                MOVW    #IR_SHIFT,STATE_L       ; NEXT STATE IS IR_SHIFT
                MOVW    #IR_EXIT1,STATE_H       ; NEXT STATE IS IR_EXIT1
                RTS
;
                .END


        .text
        .GLOBAL IR_EXIT1
        .GLOBAL IR_PAUSE
        .GLOBAL IR_UPDATE
        .GLOBAL IR_SHIFT1
        .GLOBREG STATE_H
        .GLOBREG STATE_L
        .GLOBREG TMS_DELAY
;
SPIPC2  .EQU    P03E
;
;
IR_EXIT1        BTJO    #01,TMS_DELAY,NO_DELAY
EXIT1_DELAY     MOV     #01,TMS_DELAY
                CALL    IR_SHIFT1
;
NO_DELAY        MOVW    #IR_PAUSE,STATE_L       ; NEXT STATE IS IR_PAUSE
                MOVW    #IR_UPDATE,STATE_H      ; NEXT STATE IS IR_UPDATE
                RTS
;
                .END


         .text
         .GLOBAL IR_EXIT2
         .GLOBAL IR_SHIFT
         .GLOBAL IR_UPDATE
         .GLOBREG STATE_H
         .GLOBREG STATE_L
 ;
 IR_EXIT2       MOVW    #IR_SHIFT,STATE_L       ; NEXT STATE IS IR_SHIFT
                MOVW    #IR_UPDATE,STATE_H      ; NEXT STATE IS IR_UPDATE
                RTS
 ;
                .END


         .text
         .GLOBAL IR_EXIT2
         .GLOBAL IR_PAUSE
         .GLOBREG STATE_H
         .GLOBREG STATE_L
 ;
 IR_PAUSE       MOVW    #IR_PAUSE,STATE_L       ; NEXT STATE IS IR_PAUSE
                MOVW    #IR_EXIT2,STATE_H       ; NEXT STATE IS IR_UPDATE
                RTS
 ;
                .END
```

```
        .text
        .GLOBAL IR_SCAN
        .GLOBAL TL_RESET
        .GLOBAL IR_CAPTURE
        .GLOBREG STATE_L
        .GLOBREG STATE_H
        .GLOBREG TMS_DELAY
TMS_DELAY       .EQU    R57
;
SPIPC2  .EQU    P03E
;
;
IR_SCAN         MOVW    #IR_CAPTURE,STATE_L     ; NEXT STATE IS IR_SHIFT
                MOVW    #TL_RESET,STATE_H       ; NEXT STATE IS TL_RESET
                RTS
;
                .END
```

```
        .text
       .GLOBAL IR_EXIT1
        .GLOBAL IR_SHIFT
        .GLOBAL IR_SHIFT1
        .GLOBREG STATE_L
        .GLOBREG STATE_H
        .GLOBREG OUTREG
        .GLOBREG INSTRUCT_REG
        .GLOBREG TMS_DELAY
;
SPIPC2          .EQU    P03E
INT3CTL         .EQU    P019
;
;
IR_SHIFT        BTJO    #01H,TMS_DELAY,OUTPUT1  ; IS THIS THE FIRST TIME
                CALL    IR_SHIFT1               ; INTO IR_SHIFT ? IF SO,
                JMP     OUTPUT1                 ; DON'T SHIFT !
;
;
IR_SHIFT1       BTJO    #08H,SPIPC2,IN_ONE1     ; COPY TDI (SPISOMI) TO CARRY
IN_ZERO1        CLRC
                JMP     ROTATE_IR
IN_ONE1         SETC
ROTATE_IR       RRC     INSTRUCT_REG            ; SHIFT STATE OF TDI (SPISOMI
                RTS                             ; INTO INSTRUCTION REGISTER R
;                                                 TOWARDS LSB.
;
OUTPUT1         BTJO    #01H,INSTRUCT_REG,OUT_ONE1  ; STATE OF IR LSB ?
;
OUT_ZERO1       MOV     #010H,OUTREG                ; COPY LSB TO O/P REG
                JMP     WAIT_NEG
OUT_ONE1        MOV     #050H,OUTREG
;
WAIT_NEG        MOV     #00H,TMS_DELAY          ; CLEAR TMS_DELAY
                MOV     #01H,INT3CTL            ; ENABLE TCK (INT3) FOR
                EINTH                           ; -VE EDGE DETECTION
                IDLE
;
                MOVW    #IR_SHIFT,STATE_L       ; NEXT STATE IS IR_SHIFT
                MOVW    #IR_EXIT1,STATE_H       ; NEXT STATE IS IR_EXIT1
                RTS
;
                .END
```

```
        .text
        .GLOBAL DR_SCAN
        .GLOBAL RUN_TEST
        .GLOBAL IR_UPDATE
        .GLOBREG STATE_H
        .GLOBREG STATE_L
;
SPIPC2  .EQU    P03E
;
IR_UPDATE       MOV     #00,SPIPC2              ; TRI-STATE TDO
;
                MOVW    #RUN_TEST,STATE_L       ; NEXT STATE IS RUN_TEST
                MOVW    #DR_SCAN,STATE_H        ; NEXT STATE IS IR_SCAN
                RTS
;
                .END
```

```
        .text
        .GLOBAL RUN_TEST
        .GLOBAL DR_SCAN
        .GLOBREG STATE_H
        .GLOBREG STATE_L
;
;
RUN_TEST        MOVW    #RUN_TEST,STATE_L       ; NEXT STATE IS RUN_TEST
                MOVW    #DR_SCAN,STATE_H        ; NEXT STATE IS DR_SCAN
                RTS
;
                .END
```

```
        .text
        .GLOBAL START
        .GLOBAL TCK
        .GLOBAL TL_RESET
        .GLOBAL RUN_TEST
        .GLOBREG STATE_H
        .GLOBREG STATE_L
        .GLOBREG OUTREG
        .GLOBREG INSTRUCT_REG
        .GLOBREG BYPASS_REG
;
INT3CTL         .EQU    P019
ADENA           .EQU    P07E
STATE_L         .EQU    R53
STATE_H         .EQU    R55
OUTREG          .EQU    R50
BYPASS_REG      .EQU    R51
INSTRUCT_REG    .EQU    R56
;
        .SECT   ROMCODE                 ; THIS TEST RESIDES IN ROM
;       SOME KIND OF JTAG ENTRY TEST IS REQUIRED HERE
START   NOP
        NOP                             ; ALL I/O ASSUMED TRI-STATE
        NOP
        NOP
        BR      JTAG                    ; BRANCH TO JTAG CODE IN EEPROM
;
        .TEXT                           ; EEPROM STARTING ADDRESS ???
JTAG    MOV     #0FFH,ADENA             ; ENABLE A-D INPUTS
        MOVW    #TL_RESET,STATE_H       ; INITILISE STATE TO TL_RESET
        MOVW    #RUN_TEST,STATE_L
        MOV     #014H,B
        LDSP                            ; INITIALISE STACK POINTER AT R20
        MOV     #00,P017                ; DISABLE ALL UNUSED INTS
        MOV     #00,P018
        MOV     #00,P04B
        MOV     #00,P06B
        MOV     #00,P055
        MOV     #00,P054
        MOV     #00,P031
        MOV     #00,P071
        MOV     #05H,INT3CTL            ; ENABLE TCK (INT3) +VE EDGE
        EINTH
WAIT    IDLE
        BR      WAIT                    ; WAIT FOR NEXT TCK
;
;
        .SECT  VECTORS
        .WORD    TCK                    ; INT3 VECTOR FOR TCK 7FF8,7FF9
        .WORD    START                  ; INT2 VECTOR UNUSED
        .WORD    START                  ; INT1 VECTOR UNUSED
        .WORD    START                  ; RESET VECTOR TO ROM 7FFE,7FFF
;
        .END
```

```
        .text
        .GLOBAL TCK
        .GLOBREG OUTREG
        .GLOBREG STATE_L
        .GLOBREG STATE_H
;
SPIPC1  .EQU    P03D
SPIPC2  .EQU    P03E
INT3CTL .EQU    P019
;
TCK             MOV     #05H,INT3CTL            ; CLEAR INT3
                BTJZ    #040H,INT3CTL,TCK_NEG   ; +VE OR -VE EDGE ON TCK (INT
;
TCK_POS         BTJO    #08H,SPIPC1,TMS_HI      ; CHECK STATE OF TMS (SPICLK)
;
TMS_LO          CALL    @STATE_L
                RTI
;
TMS_HI          CALL    @STATE_H                ; CALL NEXT STATE ROUTINE
                RTI
;
TCK_NEG         MOV     OUTREG,SPIPC2           ; OUTPUT BIT TO TDO (SPISIMO)
;
                MOV     #05,INT3CTL             ; RE-ARM TCK FOR +VE EDGE
                RTI
;
               .END
```

```
        .text
        .GLOBAL TL_RESET
        .GLOBAL RUN_TEST
        .GLOBREG STATE_L
        .GLOBREG STATE_H
        .GLOBREG INSTRUCT_REG
;
SPIPC2  .EQU    P03E
;
TL_RESET        MOV     #00,SPIPC2              ; TRI-STATE TDO
;
                MOV     #0FFH,INSTRUCT_REG      ; DEFAULT BY-PASS MODE

                MOVW    #RUN_TEST,STATE_L       ; NEXT STATE IS RUN_TEST
                MOVW    #TL_RESET,STATE_H       ; NEXT STATE IS TL_RESET
                RTS
;
                .END
```

```
SETUP.OBJ
STATE.OBJ
TL_RESET.OBJ
RUNTEST.OBJ
DR_CAPT.OBJ
DR_EXIT1.OBJ
DR_EXIT2.OBJ
DR_PAUSE.OBJ
DR_SCAN.OBJ
DR_SHIFT.OBJ
DR_UPDAT.OBJ
IR_CAPT.OBJ
IR_EXIT1.OBJ
IR_EXIT2.OBJ
IR_PAUSE.OBJ
IR_SCAN.OBJ
IR_SHIFT.OBJ
IR_UPDAT.OBJ

-o JTAG.OUT
-m JTAG.MAP

MEMORY
{
  RFILE:  origin =   02h  length = 0FEh
  ROM:    origin = 7000h  length = 1000h
  EEPROM: origin = 01F00h length = 0100h
}
SECTIONS
{
    ROMCODE 07000h : { } > ROM
    .text 07700h : { } > ROM            /* WILL BE EEPROM !! */
    VECTORS 07FF8h : {} > ROM
}
```

```
*******************************************************
TMS370 COFF Linker          , Version 3.40
*******************************************************
Mon Mar 26 21:21:10 1990

OUTPUT FILE NAME:   <JTAG.OUT>
ENTRY POINT SYMBOL: 0


MEMORY CONFIGURATION

          name      origin     length     attributes
        --------   --------   ---------   ----------
        RFILE      00000002   0000000fe      RWIX
        EEPROM     00001f00   000000100      RWIX
        ROM        00007000   000001000      RWIX


SECTION ALLOCATION MAP

 output                                  attributes/
section   page    origin      length       input sections
--------  ----  ----------  ----------   ----------------
ROMCODE     0    00007000    00000007
                   00007000    00000007     SETUP.OBJ (ROMCODE)

.text       0    00007700    0000020b
                   00007700    0000002f     SETUP.OBJ (.text)
                   0000772f    00000018     STATE.OBJ (.text)
                   00007747    0000000f     TL_RESET.OBJ (.text)
                   00007756    00000009     RUNTEST.OBJ (.text)
                   0000775f    00000049     DR_CAPT.OBJ (.text)
                   000077a8    0000001d     DR_EXIT1.OBJ (.text)
                   000077c5    00000009     DR_EXIT2.OBJ (.text)
                   000077ce    00000009     DR_PAUSE.OBJ (.text)
                   000077d7    00000009     DR_SCAN.OBJ (.text)
                   000077e0    0000006c     DR_SHIFT.OBJ (.text)
                   0000784c    00000044     DR_UPDAT.OBJ (.text)
                   00007890    0000000f     IR_CAPT.OBJ (.text)
                   0000789f    00000013     IR_EXIT1.OBJ (.text)
                   000078b2    00000009     IR_EXIT2.OBJ (.text)
                   000078bb    00000009     IR_PAUSE.OBJ (.text)
                   000078c4    00000009     IR_SCAN.OBJ (.text)
                   000078cd    00000032     IR_SHIFT.OBJ (.text)
                   000078ff    0000000c     IR_UPDAT.OBJ (.text)

VECTORS     0    00007ff8    00000008
                   00007ff8    00000008     SETUP.OBJ (VECTORS)

.data       0    00000000    00000000     UNINITIALIZED

.bss        0    00000000    00000000     UNINITIALIZED


GLOBAL SYMBOLS

address  name                            address  name
-------- ----                            -------- ----
00000000 .bss                            00000000 edata
00000000 .data                           00000000 .data
00007700 .text                           00000000 end
00000033 BYPASS_REG                      00000000 .bss
00007840 BYPASS_S1                       00000032 OUTREG
0000775f DR_CAPTURE                      00000033 BYPASS_REG
```

```
000077a8 DR_EXIT1
000077c5 DR_EXIT2
000077ce DR_PAUSE
000077d7 DR_SCAN
000077ee DR_SHIFT1
000077e0 DR_SHIFT
0000784c DR_UPDATE
00000038 INSTRUCT_REG
00007890 IR_CAPTURE
0000789f IR_EXIT1
000078b2 IR_EXIT2
000078bb IR_PAUSE
000078c4 IR_SCAN
000078d6 IR_SHIFT1
000078cd IR_SHIFT
000078ff IR_UPDATE
00000032 OUTREG
00007756 RUN_TEST
00007000 START
00000037 STATE_H
00000035 STATE_L
0000772f TCK
00007747 TL_RESET
00000039 TMS_DELAY
00000000 edata
00000000 end
0000790b etext

[33 symbols]
```

```
00000035 STATE_L
00000037 STATE_H
00000038 INSTRUCT_REG
00000039 TMS_DELAY
00007000 START
00007700 .text
0000772f TCK
00007747 TL_RESET
00007756 RUN_TEST
0000775f DR_CAPTURE
000077a8 DR_EXIT1
000077c5 DR_EXIT2
000077ce DR_PAUSE
000077d7 DR_SCAN
000077e0 DR_SHIFT
000077ee DR_SHIFT1
00007840 BYPASS_S1
0000784c DR_UPDATE
00007890 IR_CAPTURE
0000789f IR_EXIT1
000078b2 IR_EXIT2
000078bb IR_PAUSE
000078c4 IR_SCAN
000078cd IR_SHIFT
000078d6 IR_SHIFT1
000078ff IR_UPDATE
0000790b etext
```

## Claims

1. A method of testing interconnections of a circuit having a plurality of integrated circuits,
at least some of the integrated circuits including
storage elements respectively associated with some of the terminals of those integrated circuits and means for joining the storage elements into at least one shift register chain,
the method including
entering an initial test pattern of bits serially into the storage elements along the at least one shift register chain,
transferring certain of the bits of the initial test pattern from the storage elements into which they were entered, via the terminals and interconnections, to others of the storage elements,
retrieving the resulting pattern of bits serially from the storage elements along the at least one shift register chain, and
comparing the initial test pattern and resulting pattern to derive information about the interconnections,
characterised in that
at least one of the plurality of integrated circuits is a microprocessor, there being stored in the circuit a test program which causes the microprocessor to perform a number of operations including
entering serially into the microprocessor part of the initial test pattern of bits and storing it in a memory,
reading certain of the bits stored in the memory and producing corresponding output signals on terminals of the microprocessor connected to particular interconnections,
reading bits via particular interconnections at terminals of the microprocessor and storing the received bits in the memory, and
producing as an output from the microprocessor in serial form the received bits stored in the memory, so as to enable interconnections connected to terminals of the microprocessor to be tested.

2. A method according to claim 1 wherein the microprocessor has internal memory including a read-write memory, the bits of the part of the initial test pattern being stored in that read-write memory.

3. A method according to claim 1 or claim 2, wherein the microprocessor has internal memory including a

non-volatile memory, the test program being stored in the non-volatile memory.

4. A method according to claim 1 or claim 2, wherein the test program is stored in non-volatile memory external to the microprocessor, the program being transferred from that memory to a read-write memory internal to the microprocessor, the program being executed from that internal memory.

5. A method according to claim 3 or claim 4, wherein after a successful test of the interconnections of the circuit, the test program is deleted from that non-volatile memory in which it is stored, thereby releasing that memory for re-use.

6. A method according to claim 3 or claim 4 or claim 5, wherein the non-volatile memory is EEPROM.

7. A method according to any one of the preceding claims in which control signals are applied to the integrated circuits to regulate the operations on the bits of the initial test pattern and the bits derived therefrom, wherein the test program in the microprocessor either polls inputs to which the control signals are applied or is interrupted by the control signals so as to cause the test program to execute operations corresponding to those performed by the other integrated circuits in response to the control signals.

8. A method according to claim 7, wherein the control signals are test mode select (TMS), test clock (TCK), test data input (TDI) and test data output (TDO), and are conveyed by a test bus to all of the integrated circuits.

9. A method according to any one of the preceding claims wherein the microprocessor is a microcontroller.

10. A method according to claim 9 wherein the microcontroller is used in a single chip microcomputer mode.

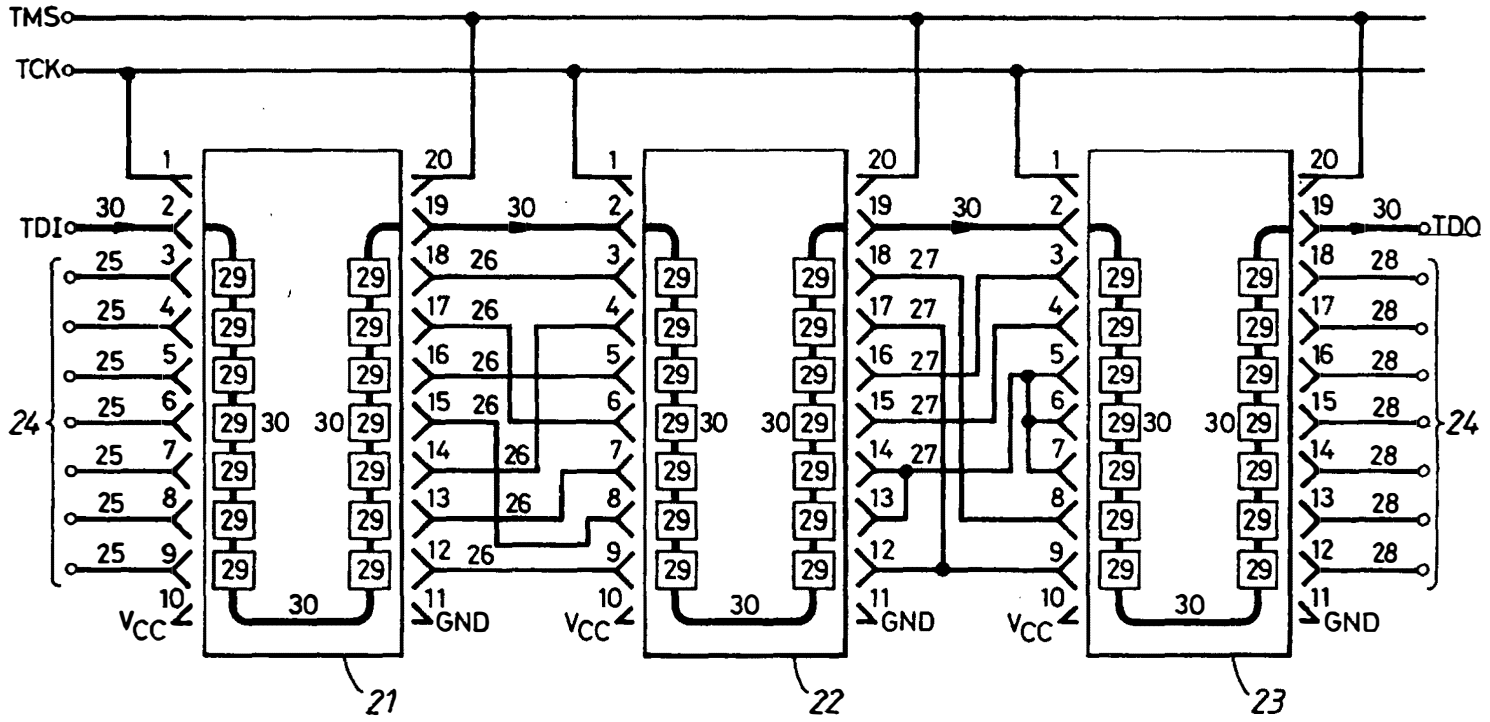


Fig.1

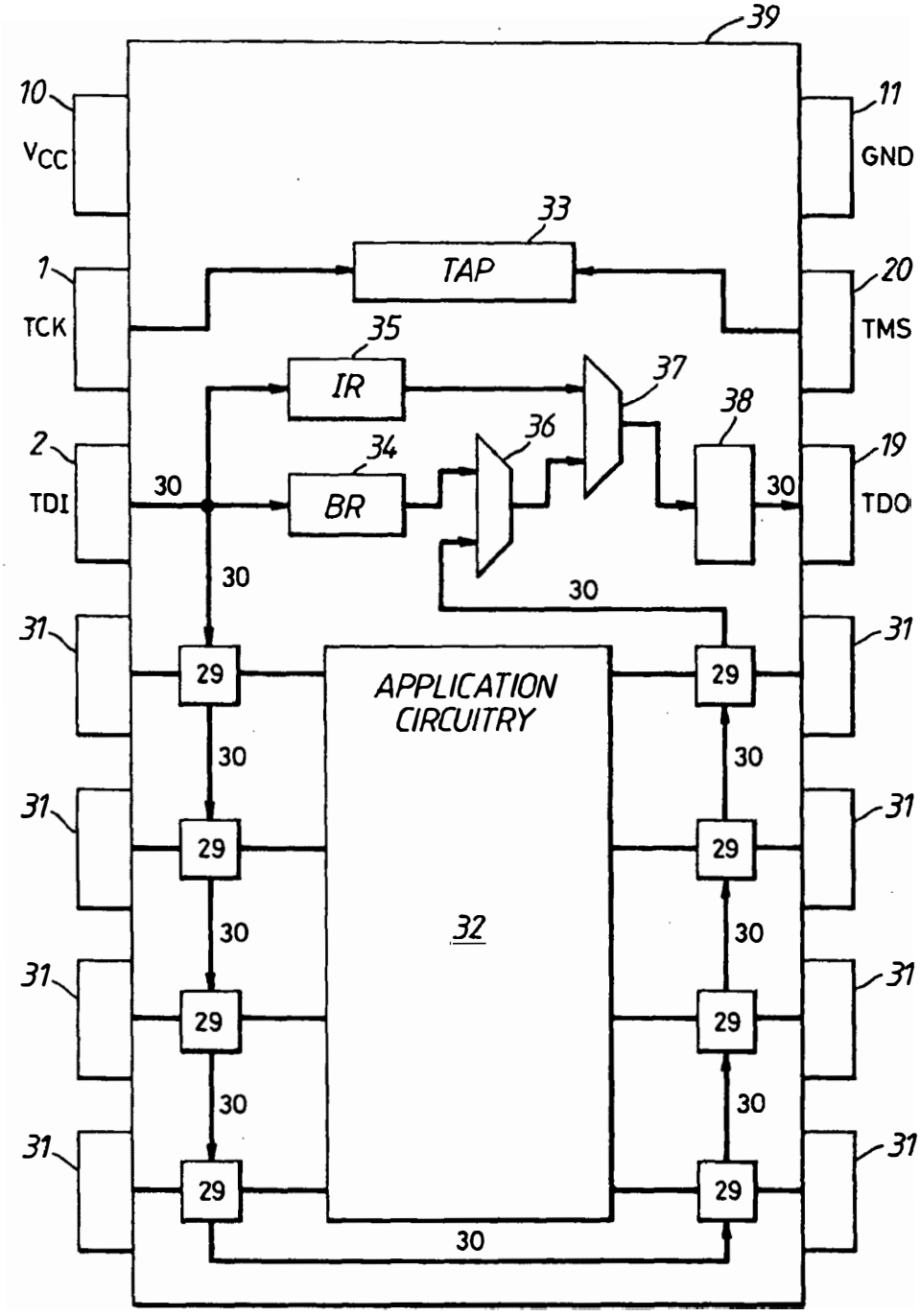


Fig.2

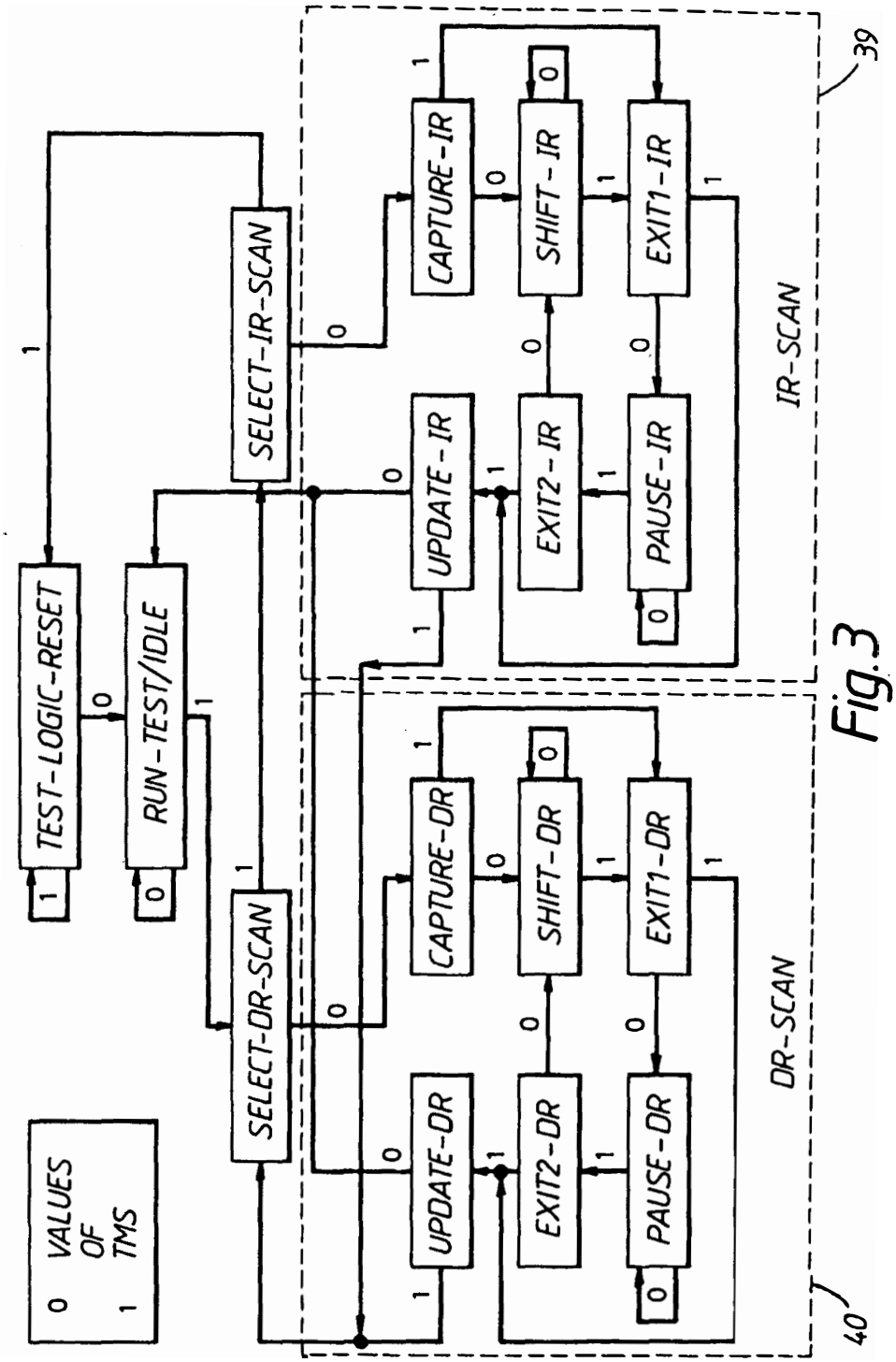


Fig.3

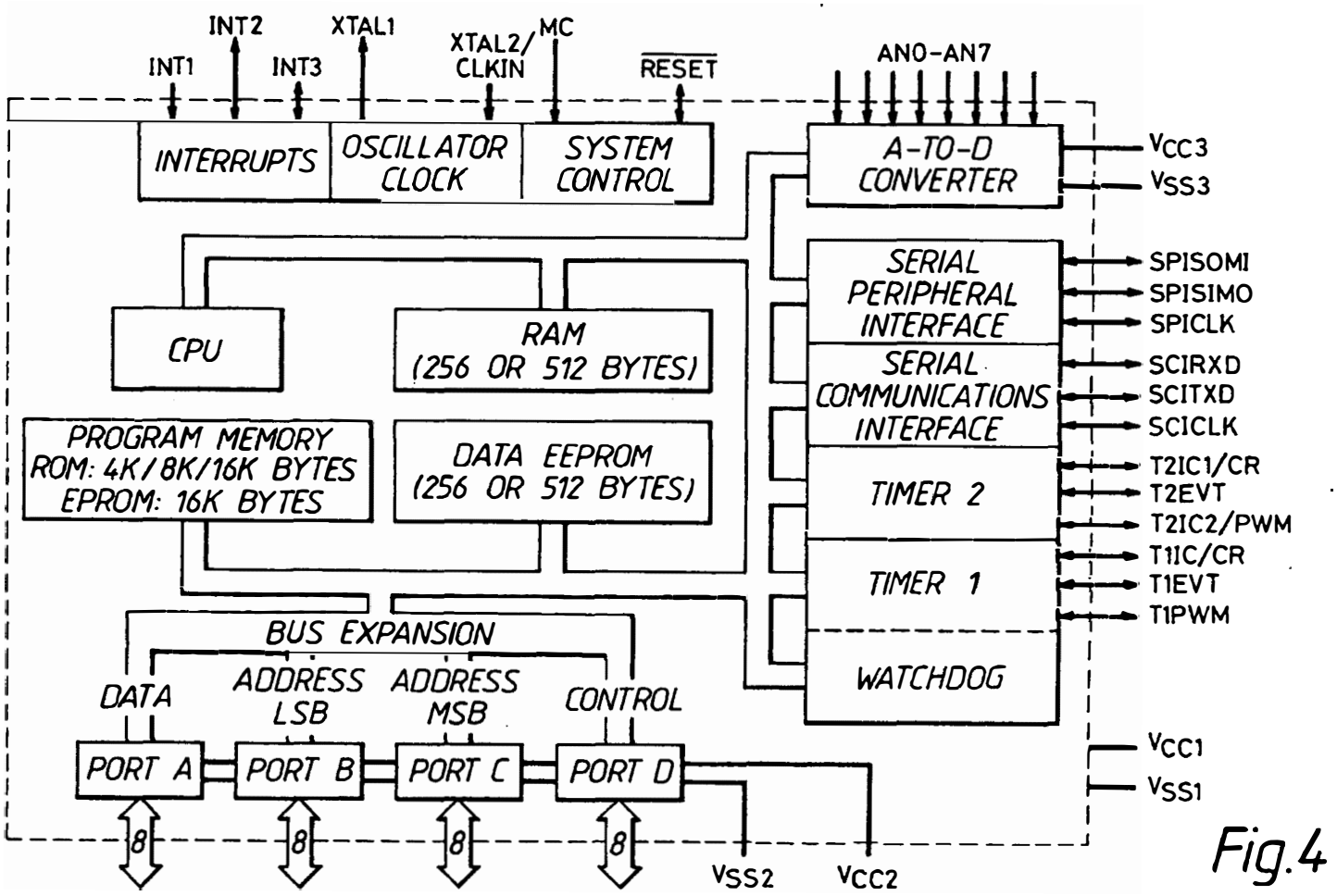


Fig.4

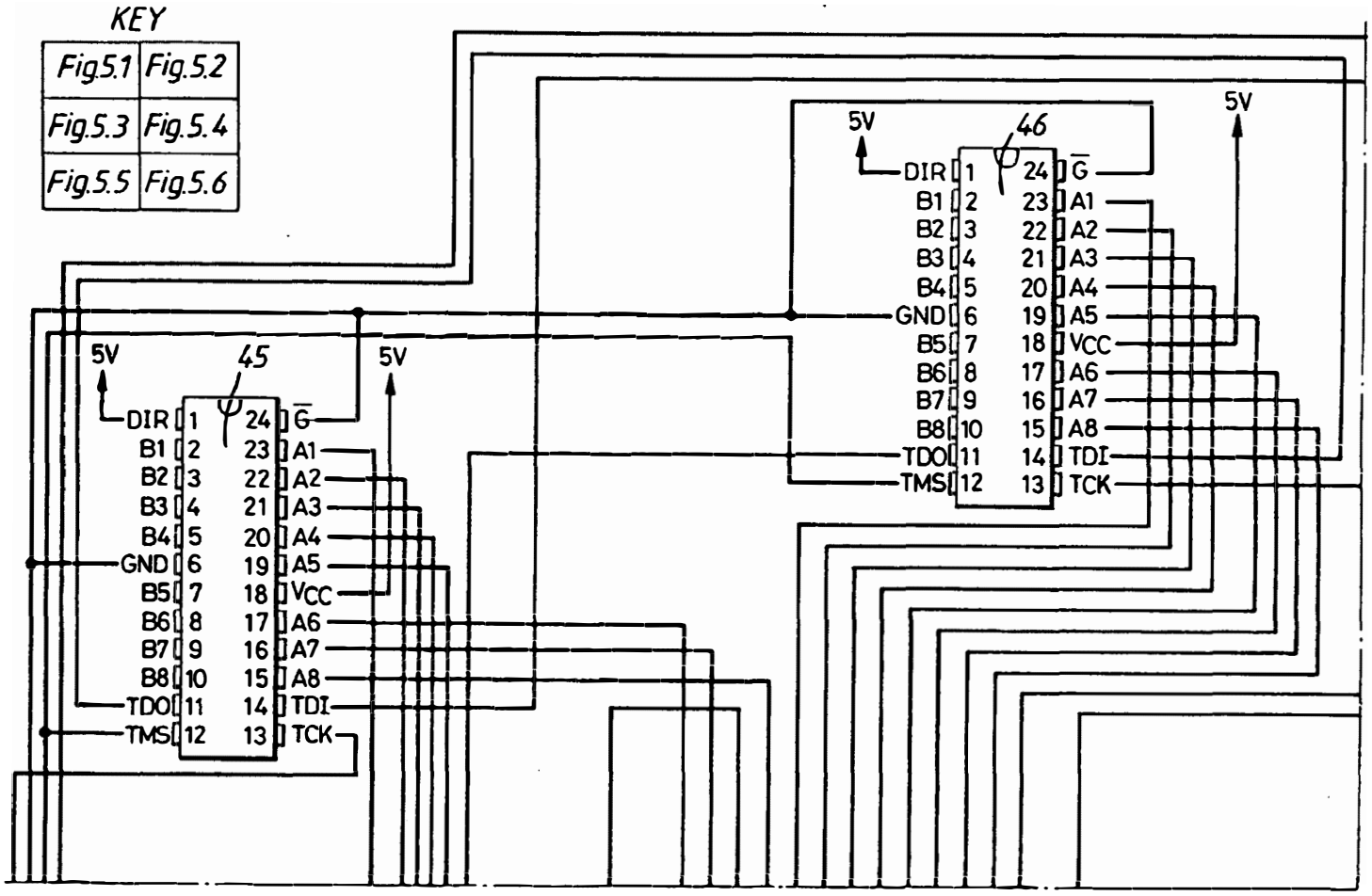


Fig.5.1

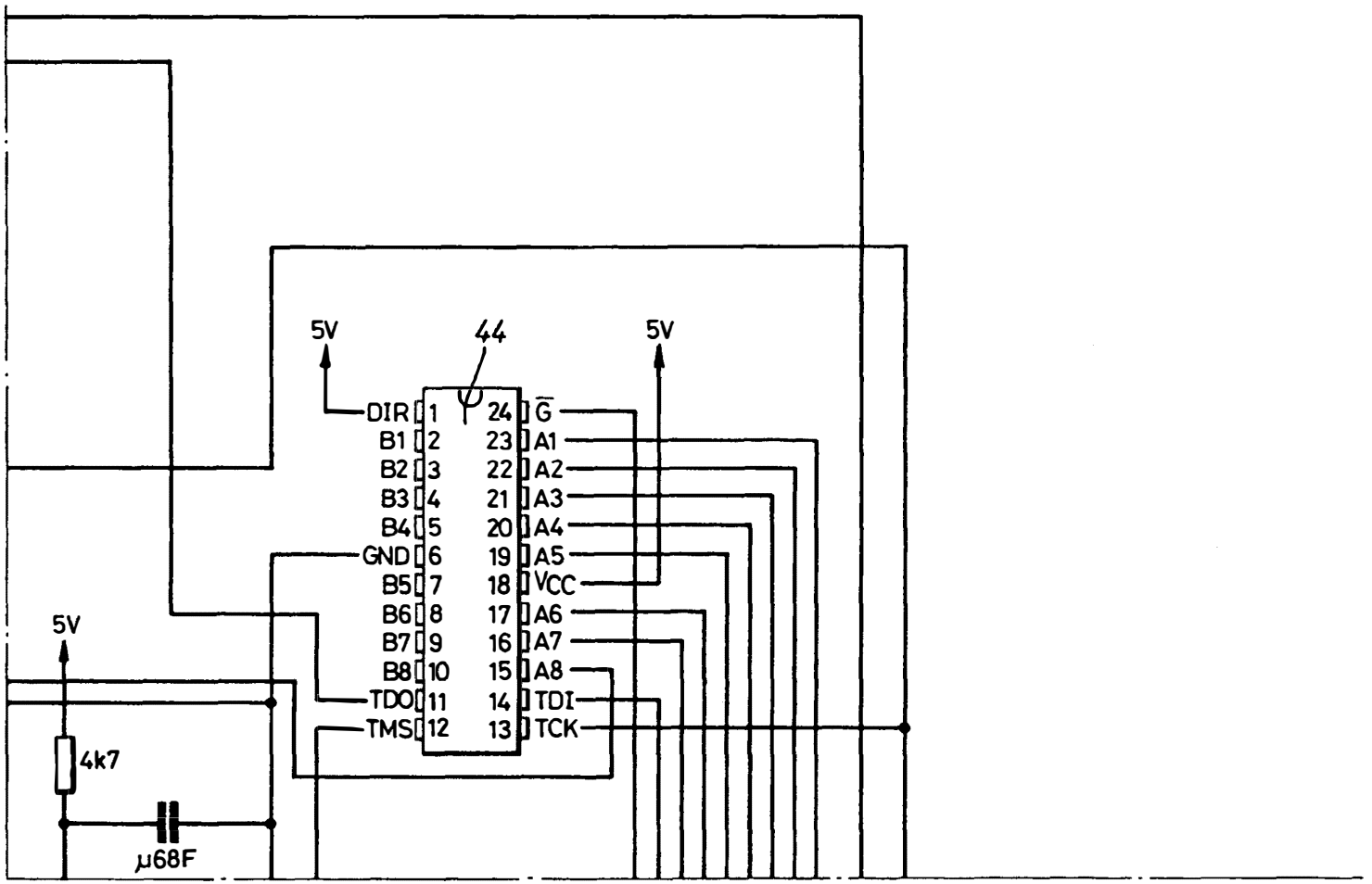


Fig. 5.2

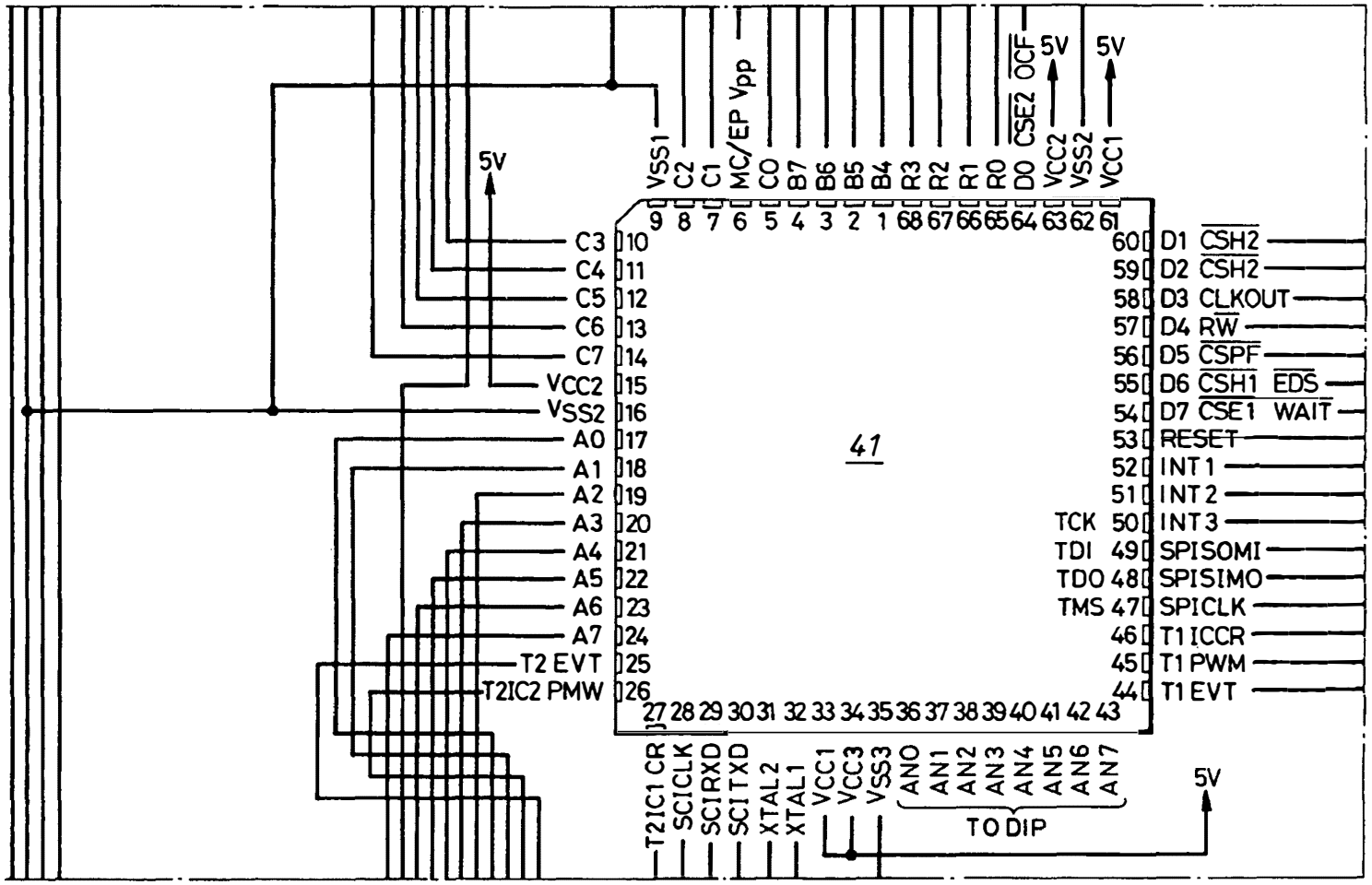


Fig.5.3

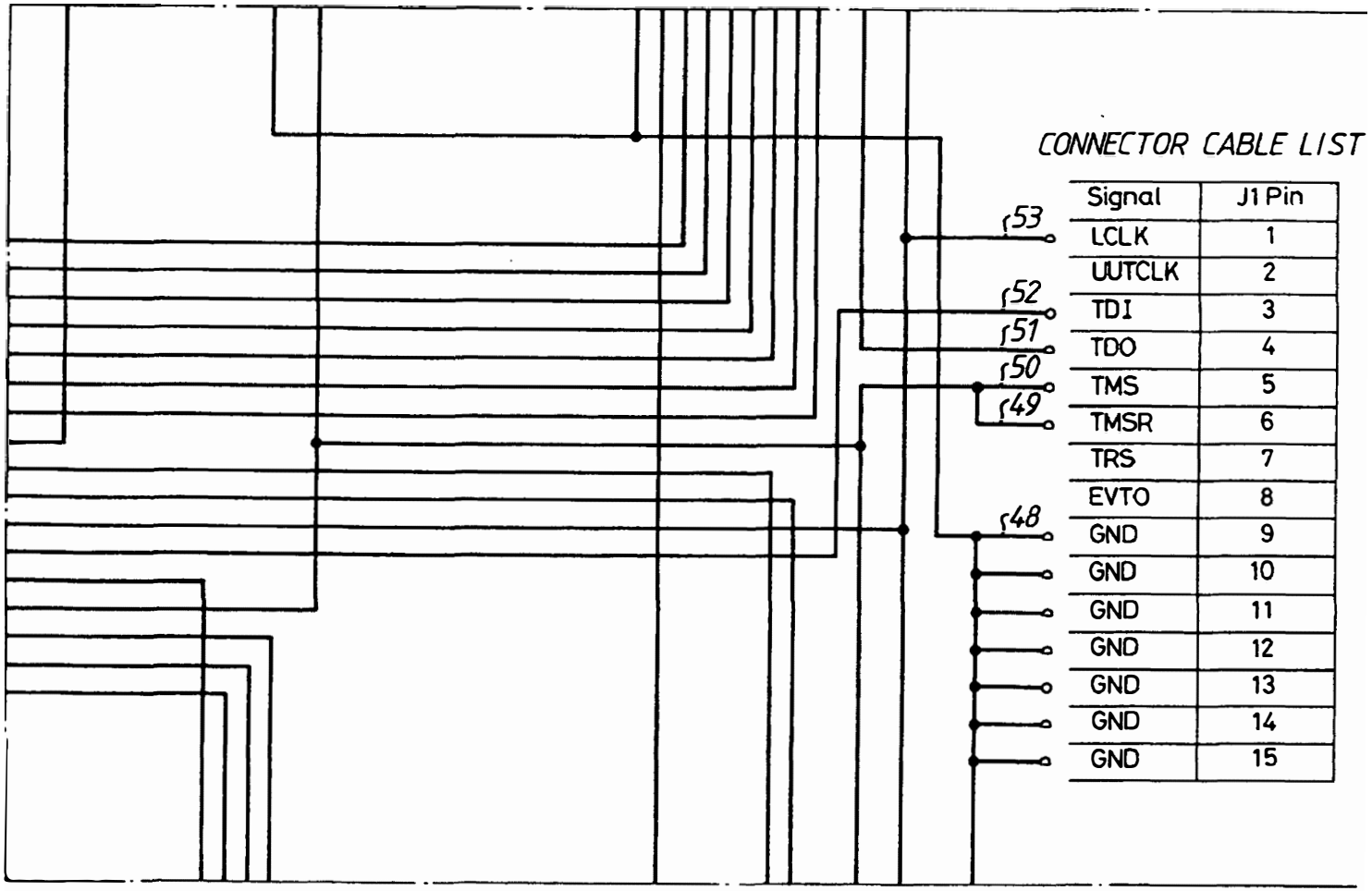


Fig.5.4

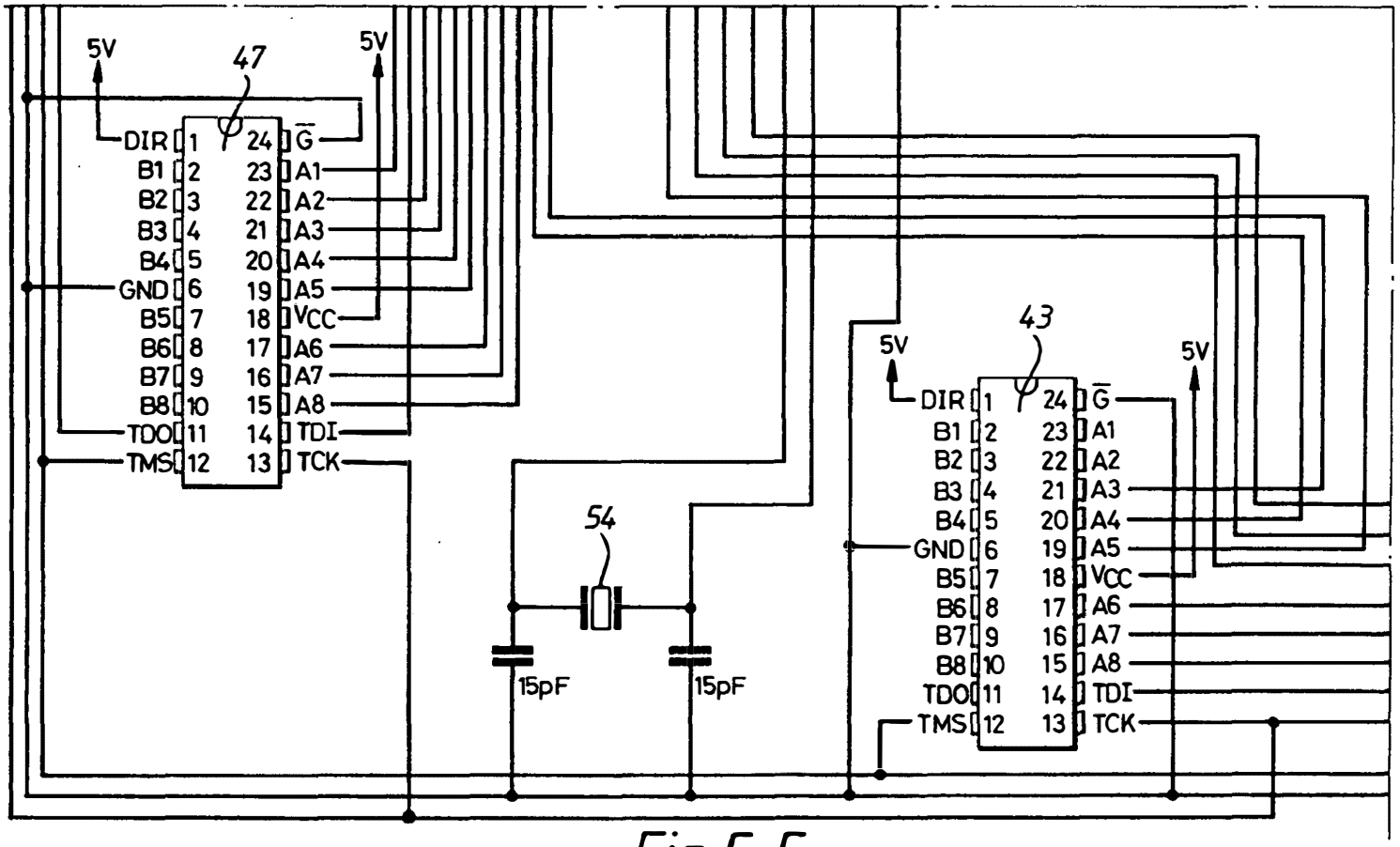


Fig. 5. 5

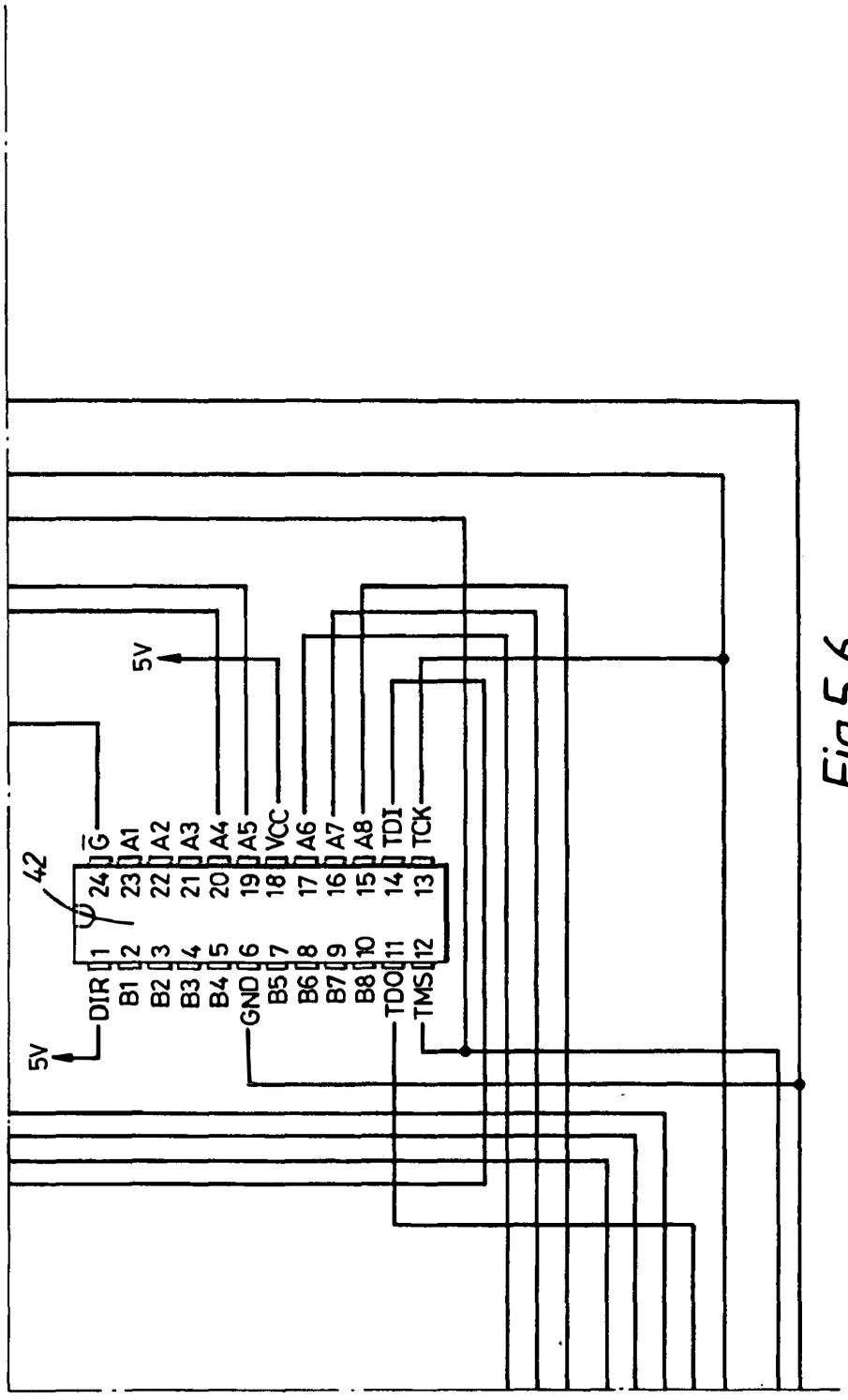


Fig.5.6

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G01R 31/28

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G1U UR3128

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# (54) Method and apparatus for testing integrated circuits

(57) A method and apparatus is disclosed for testing integrated circuit interconnect and measuring the value of passive components interconnecting the IC's (16, 18). Each IC (16, 18) includes both analog (20, 22) and digital circuitry and is provided with a test access port (24, 26) and boundary scan architecture for selectively connecting components to an analog test bus (102, 104) and for testing for the integrity of interconnections. When connected with the test bus (102, 104), a constant current is supplied to the component and the resulting voltage developed across the bus is used for identifying the value of the component. In a second embodiment (Fig 4 not shown) each IC includes a pair of buses (130, 132) which permits measurement of the impedance of the switches connecting the components to the test bus.

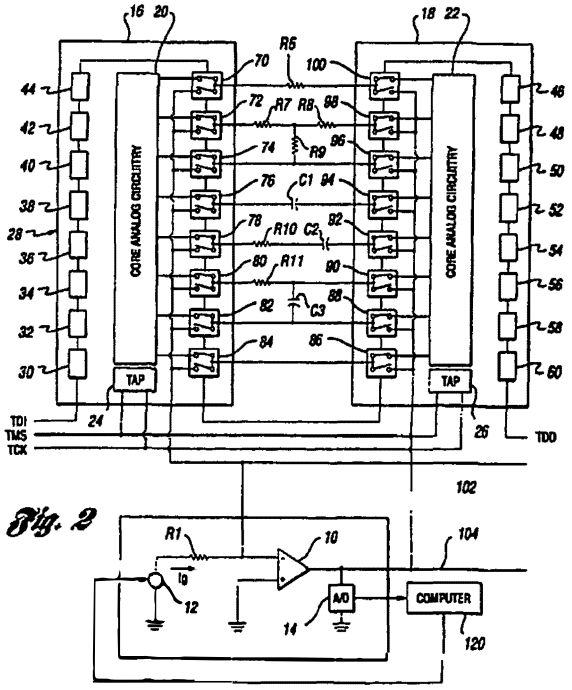
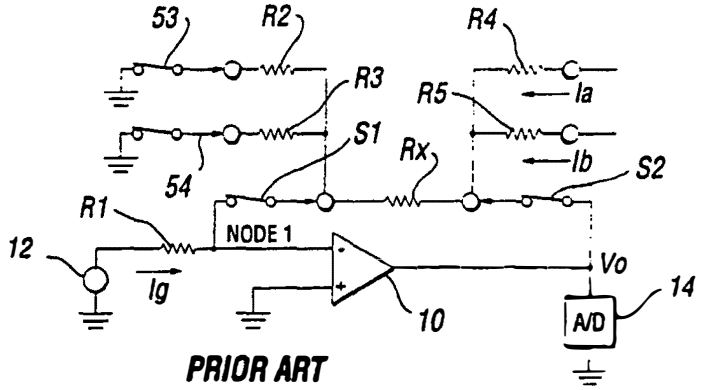



Fig. 2

GB 2 278 689 A

Fig. 1




PRIOR ART

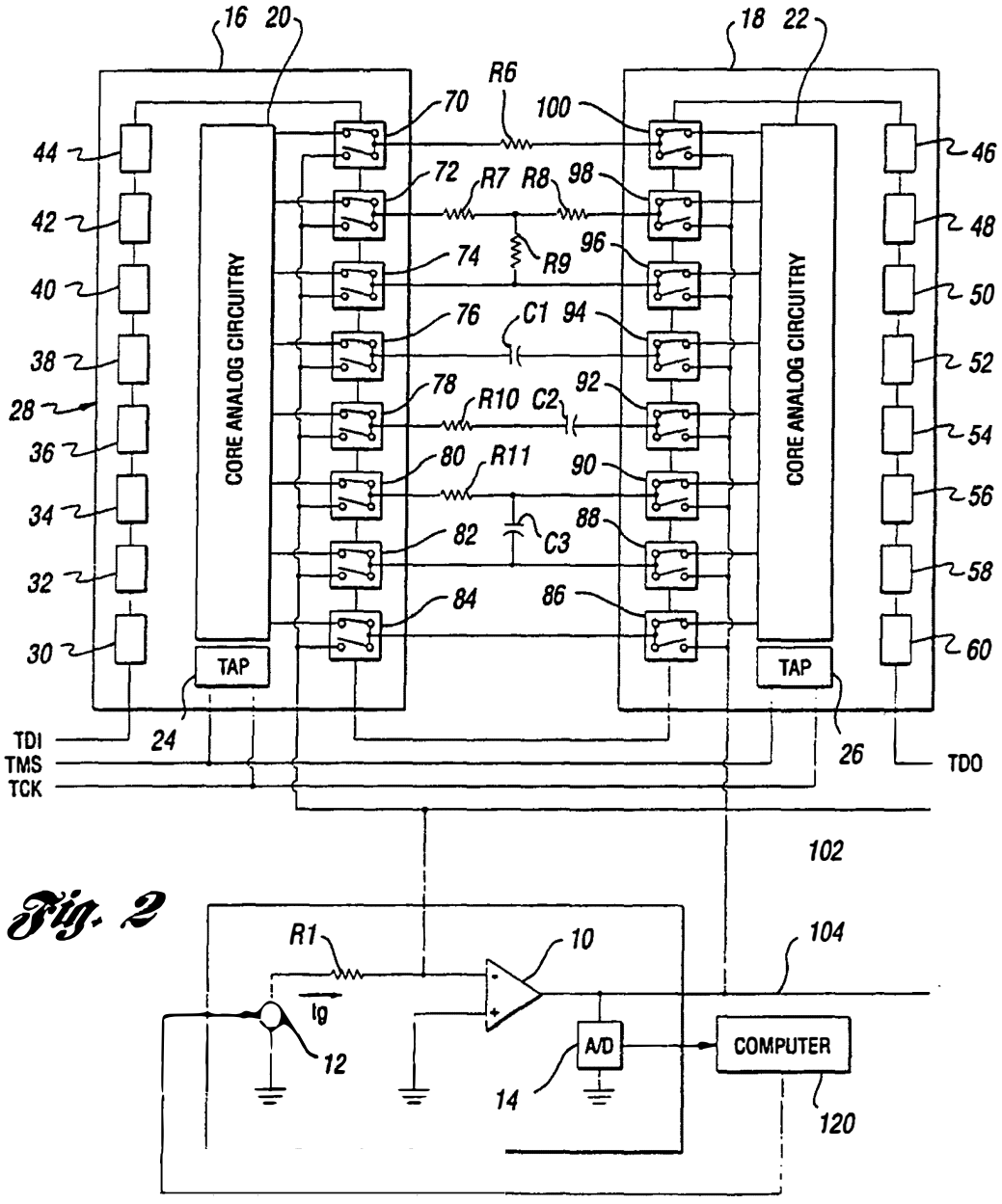



Fig. 2

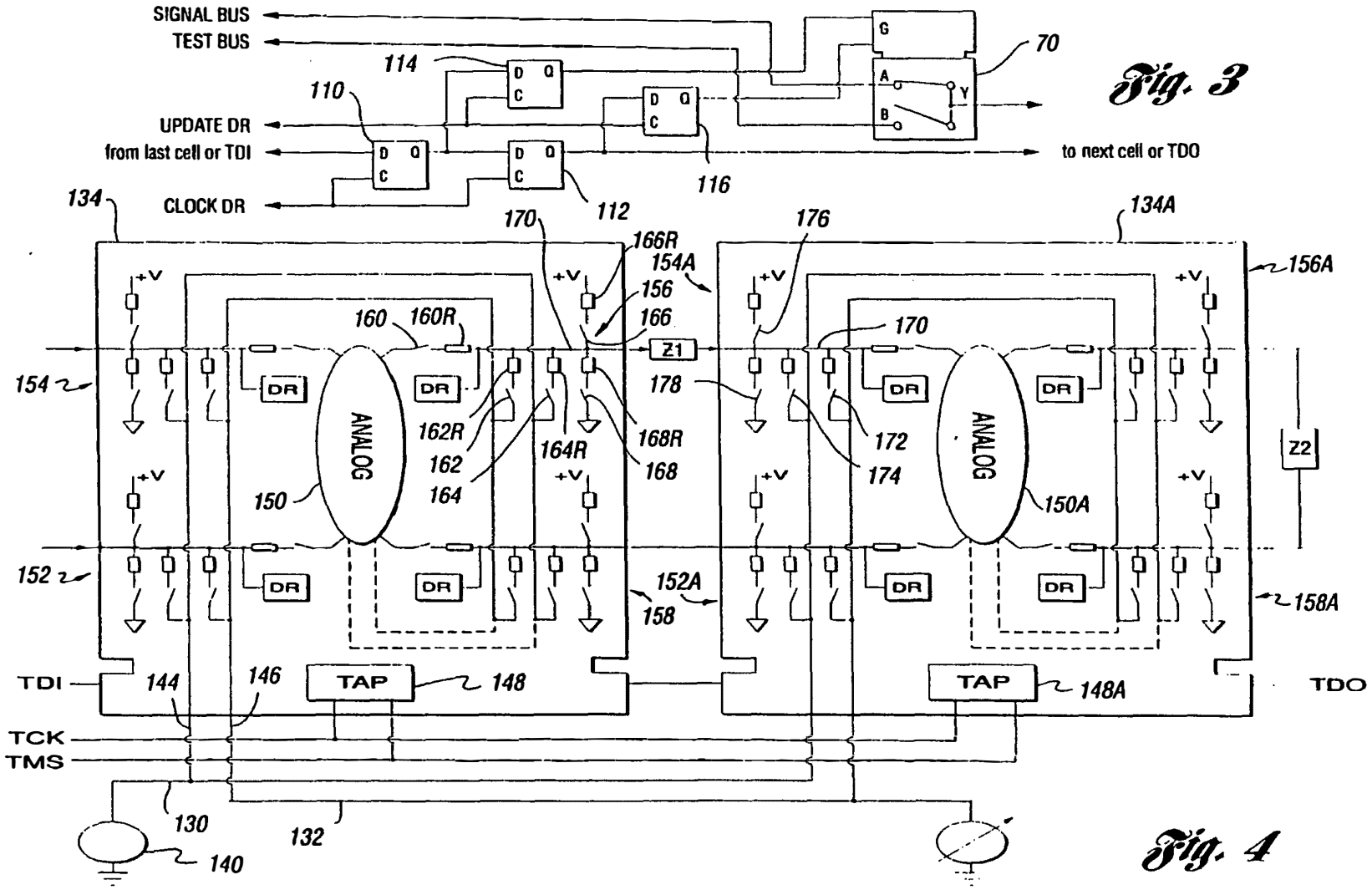



Fig. 3

Fig. 4

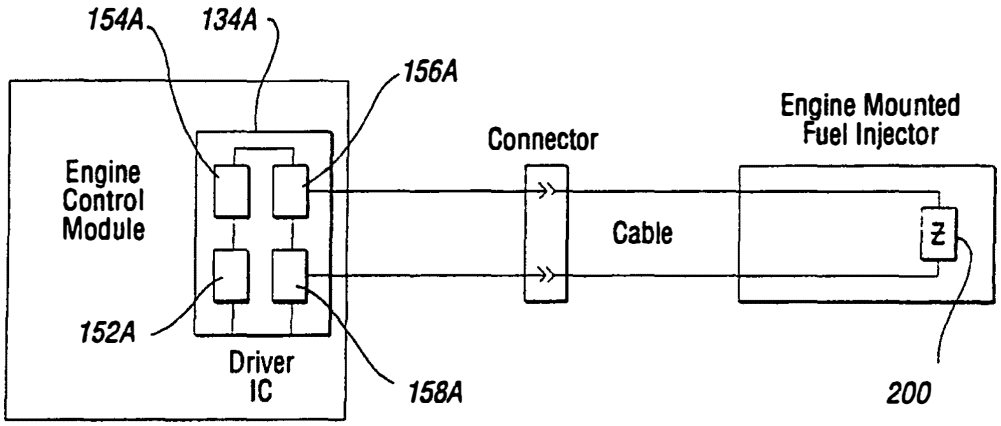

154A
134A
156A
Engine Mounted Fuel Injector
Connector
Engine Control Module
Cable
Z
152A
Driver IC
158A
200

Fig. 5

# METHOD AND APPARATUS FOR TESTING INTEGRATED CIRCUITS

This invention relates to a method and apparatus for testing integrated circuits in a mixed signal environment and more particularly to testing interconnects between integrated circuits mounted on printed circuit boards and for measuring the value of electrical components interconnecting the integrated circuits.

A printed circuit board and system level interconnect test is a high priority need in industry. This is particularly so in the automotive industry where many different phases of electronic activity, from IC design to vehicle warranty and customer service, are present and thus involve several areas of testing and diagnostics. At the IC level a significant amount of testing of mixed-signal devices is required. In order to meet the electronic test and diagnostic needs of the automotive industry, the Design-for-Testability (DFT) real estate (both pin count and silicon) must be kept to a minimum in order for the cost to justify the benefits.

The extended period of vehicle warranty requires significant field test and diagnostic capability, and hierarchial testing concepts are required, beginning at the integrated circuit (IC) level and extending to the discrete components on mixed-signal boards and peripheral analog elements in control systems. The increasing trend to integrate greater capability into IC's, resulting in embedded complexities, has significantly reduced the effectiveness of the present in-circuit testing methods at the board level via a "bed of nails" interface. There is therefore a need to provide a "virtual in-circuit" testing at all levels over an analog test bus.

IC, subsystem and system level DFT approaches should entail structures that provide a means for testing for analog drift trends at critical locations within the IC's, PC boards and systems. Data paths to failure under harsh operating conditions are required to establish appropriate

warranty data. Pertinent data feedback over the life of the product to all levels of the process would enhance continuous improvement and project future requirements amidst increasing complexities.

With the foregoing in mind, it is an object of the present invention to provide a method and apparatus for testing interconnects between integrated circuits which exist in a mixed signal environment.

It is a another object of the invention to provide for the measurement of passive components on printed circuit boards which components interconnect analog circuitry on separate IC's mounted on the board, wherein the measurement approach is compatible with boundary scan techniques used in prior art tests of digital integrated circuits.

In accordance with the present invention each IC is provided with multiplex switches for selectively connecting one or more electrical components, such as resistors, capacitors or conductors, either to core analog circuitry in two separate IC's or to a test bus on the IC's. The selection is accomplished by providing a digital test signal which connects the appropriate components to the test bus. In one embodiment each IC includes a single bus. When connected with the test bus, a programmable constant current is supplied to the component and the resulting voltage developed across the bus is used for identifying the value of the component. In a second embodiment each IC includes a pair of buses which permits measurement of the impedance of the multiplex switches providing a more accurate measurement of the component values. Other switches and storage elements are provided on each IC for providing a digital test of the integrity of connections between pins on or between the IC's and for storing the result of the test.

The invention will now be described further, by way of example, with reference to the accompanying drawings, in which:

Figure 1 is a diagram of a conventional in-circuit tester;

Figure 2 is a schematic diagram of the present invention applied to a printed circuit board environment;

Figure 3 is a schematic diagram showing greater detail of the switch control circuitry in Figure 2;

Figure 4 is a schematic diagram of a second embodiment of the invention;

Figure 5 is a block diagram showing application of the invention to the automotive system environment.

Referring now to the drawings and initially to Figure 1, a conventional in-circuit tester employed in many manufacturing plants where printed circuit boards are tested, is shown. An operational amplifier 10 having positive and negative inputs amplifies the difference between the two inputs by the gain of the circuit. Both inputs are extremely high impedance, and for most applications, they can be considered infinite in value. The op-amp is used to determine the value of analog components on the printed circuit board.

In the standard in-circuit tester, electro-mechanical switches make up a front-end matrix to interface the amplifier 10 to a probe assembly designed to match the printed circuit nodal pattern. The switches S1 and S2 (in the matrix) are closed as required to sequence each analog component to be tested into the feedback path of the amplifier 10. S3 and S4 (in the matrix) are closed to ground resistors R2 and R3. A constant voltage source 12 is connected with Node 1 through resistor R1. An unknown resistor Rx in the feedback path forms a voltage divider with R1 at Node 1. An analog-to-digital converter 14 measures the output voltage (Vo) of the amplifier 10. With the positive input tied to a reference voltage (ground), the negative input (Node 1) becomes a virtual ground due to the amplifier forcing current through Rx until the voltage

difference across the two inputs is essentially zero. For instance, if the negative input tends to move positive, the output will be amplified in the opposite direction until the potential between the two inputs is essentially zero. If indeed Node 1 is virtual ground, and resistors R2 and R3 have zero potential across them, then all of the current from source 12 (Ig) must go through Rx. The amplifier 10, voltage source 12 and resistore R1 form a constant current source. Since Ig is known and Vo is measured, Rx can be calculated. Excess current from the amplifier 10 (Ia and Ib) go through resistors R4 and R5, but have no effect on the calculation.

Referring now to Figure 2, a portion of the in-circuit tester of Figure 1 is used in accordance with the present invention to test the integrity of the interconnections between a pair of mixed-signal integrated circuits 16 and 18 and to measure passive components such as resistors R6-R11 and capacitors C1-C3, or a conductor 19 between the IC's. These components are mounted on a printed circuit board, which also supports the IC's 16 and 18. The IC's 16 and 18 include core or "mission" analog circuitry 20 and 22 as well as digital circuitry, not shown. A Test Access Port (TAP) control circuitry, generally designated 24 and 26, is provided on each IC 16 and 18 respectively. The TAP's 24 and 26 receive a Test Clock (TCK) and Test Mode Select (TMS) inputs and provide timing outputs, designated UPDATE DR and CLOCK DR in Figure 3, which control a data register generally designated 28.

The register 28 includes eight stages 30-44 contained in IC 16 and eight stages 46-60 contained in IC 18. The data shifted through the register 28 controls multiplex devices 70-100 each of which includes a pair of switches. The devices 70-84 selectively connect the aforementioned passive board mounted components either to the input/output conductors of the analog circuitry 20, or to a test bus 102, a portion of which is contained within the IC 16 but accessible through a pin of the IC 16. Similarly, the devices 86-100 selectively connect the components either to

the input/output conductors of the circuitry 22 or to a test bus 104. The position of the switches in the devices 70-100 is determined by a test vector or data word that is shifted in the register 28 via a Test Data In (TDI) line and shifted out via a Test Data Out (TDO) line all under the control of the TAP control circuitry 24 and 26. Node 1 at the negative input of the operational amplifier 10 is connected with the test bus 102 and the output of the amplifier 10 is connected with the test bus 104. When at least one of the devices 70-84 and one of the devices 86-100 is placed in a test mode position, a constant current from the generator 12 is fed through the closed switches to one or more of the passive components on the circuit board. The analog voltage developed at the output of the amplifier 10 is converted by the A/D converter 14 and fed to a computer 120 for determining the value of the component(s). The computer 120 also controls the programmable generator 12 to set the desired current level.

With reference to Figure 3, each of the multiplex devices 70-100 may contain D-type flip-flops 110-116. The test vector is shifted through the register 28 and the flip-flop 110 and 112 in each multiplex devices. At any particular point in time one of four binary data pairs, 00,01,10, and 11 appear at the Q outputs of the flip-flops 110 and 112. When the desired test vector has been serially loaded, the UPDATE DR signal shifts the data at the Q outputs of the F/F's 110, 112 to the F/F's 114 and 116 respectively. The latched outputs of the F/F's control the gates of two FET switches respectively, to thereby select either the signal bus to the circuits 20 and 22 or the test buses 102 and 104.

There are significant differences between the on-board test IC of Figure 2 and the external in-circuit tester shown on Figure 1. Some of these differences are as follows: 1) The on-board test op-amp will not be powered by two power supplies, one for the positive voltage, and the other for the negative voltage. Instead, a protected voltage source derived from the vehicle battery (+V) would provide for

both. 2) The positive input to the op-amp, stimuli and voltage measuring circuit could be referenced to a voltage equal to +V/2. 3) The switching matrix, probe assembly, interconnect wiring and associated control software in the in-circuit tester are no longer needed for the simpler IC integrated approach. This will reduce the cost of future testers.

Referring now to Figure 4, a second embodiment of the invention is shown. In this embodiment an analog bus having input and output lines 130 and 132 respectively extend within each of the plurality of IC's 134, and 134A mounted on the printed circuit board. The additional bus on each IC adds an additional pin over the embodiment of Figure 2, but provides offsetting advantages in accuracy of measurement of components, where the impedance of the multiplex switches is large. In order to conserve silicon real estate, the multiplex switches may be located on the IC so that relatively small amounts of silicon are used which will necessarily result in higher switch impedance values.

A current source generally designated 140 is connected with the bus 130 and a voltage detector generally designated 142 is connected with the bus 132. Alternatively, the source 140 could be a constant voltage source and the detector 142 would then be a current detector. The IC 134 includes conductors 144 and 146 which connect with the buses 130 and 132 respectively and to a plurality of switches. These switches are actuable to either an open or closed position under the control of test circuitry in a Test Access Port (TAP) 148 as previously discussed. The control circuitry includes a boundary-scan register (not shown) as is well known in the art and includes a standard interface providing instructions for control of the switches. In Figure 4, for purposes of illustration, each IC includes four groups of switches generally designated 152-158, and 152A-158A respectively. In the interest of brevity only group 156 will be discussed in detail. The switch group 156 includes switches 160-168. Associated with each switch is an internal impedance designated by the suffix "R". The

switch 160 is actuable to connect or disconnect the analog circuit 150 with a conductor 170 connected with an input pin of the IC 134. When a test mode is selected the switch 160 is opened. The switch may be contained within the analog circuit 150. For example, the function performed by the switch 160 may be performed by turning off the output driver of an operational amplifier forming a part of the circuit 150. In that case, it would be the responsibility of the IC designer to fabricate the appropriate level of control from the boundary scan test word. The switches 164 and 166 connect the conductor 170 to the bus 130 and 132 through the conductors 144 and 146 respectively. The switches 166 and 168 are connected with an IC operating voltage and ground respectively, and are provided to simulate the IEEE Standard 1149.1 EXTEST in a mixed-signal environment. EXTEST is a connectivity test procedure for testing digital integrated circuits. Further details regarding EXTEST as well as background information may be had from the IEEE Standard Test Access Port and Boundary-Scan Architecture published by the IEEE, May 21, 1990. While not shown in Figure 4, it will be understood that the IC's contain digital as well as analog circuits. Control of the switches 166 and 168 will for example permit the detection of a cross family short between an IC pin connected with analog circuitry and an IC pin connected with digital circuitry. By selective closure of the switches to +V or to ground a digital "1" or "0" can be generated and then detected by a data register which includes a stage DR, associated with each switch group.

By selective closure of the appropriate switches in the switch groups in IC's 134, and 134A, the component Z1 can be connected with the constant current source 140 and appropriate measurements can be made by the detector 142 in order to determine the impedance of the component(s). Considering, for example, the component Z1 and the switch group 156 in IC 134 and switch group 154A in IC 134A, the switch 164 is closed to connect one side of Z1 to the current source 140 and switch 178A is closed to connect the other side of Z1 to ground. The value of Z1 is determined

by connecting the voltage detector 142 to the left side of Z1, by closure of switch 162, and measuring a voltage $V_3$, then opening the switch 162 and closing the switch 172A, connecting the voltage detector 142 to the right side of Z1 and measuring a voltage $V_4$. The value of Z1 is then the difference between the voltage measurements $V_3$ and $V_4$ divided by the constant current. Any switch impedance in series with Z1 will change $V_3$ or $V_4$ but not the difference $V_3-V_4$.

The dotted line extensions of the conductors 144 and 146 in IC 134, as well as the corresponding conductors in the IC 134A, are intended to indicate that, if desired, measurement can be made within the analog circuit 150.

Figure 5 shows the test bus extending beyond the control module board level into a typical sub-system such as an engine control module and to sensors or actuators connected with the module and existing in a harsh environments. In the automotive electronic industry, a control module interfaces with many peripheral sensors for monitoring the many variations of conditions through which the system must operate. For example, in the engine control system the air-fuel ratio must be at the right mixture under all atmospheric conditions, whether it be for temperature, moisture, altitude, etc. Many actuators are involved to meter the fuel, adjust the spark timing, re-circulate crankcase fumes, etc. to assure quality operating vehicles. Drift in impedance through the interconnecting circuitry cannot be ignored. The harsh operating environments of temperature extremes, temperature cycles, anti-freeze spills, road salts, etc., all effect the aging process. The many interconnections making up the system must be measured for analog changes. The common trial and error practices of replacing a sensor or actuator, disconnecting cables for test, etc., masks many real conditions producing failures, and destroy any hope of identifying the failure mechanisms in the natural setting. In Figure 5, the value of an electrical component forming an actuator 200 driven by IC 134A, can be measured using the approach shown in Figure 4.

The switch groups 156A and 158A can be selectively closed in order to connect the sensor 200 with the constant current source such as 140 of Figure 4 and then voltage measurements on either side of the sensor are made using a voltage detector such as 142 of Figure 4.

**CLAIMS**

1. Apparatus for measuring electrical component means interconnecting first and second integrated circuit devices which devices include first and second analog circuits respectively, said apparatus comprising a first and a second analog test bus means included in said first and second devices respectively, multiplex means included in each of said devices for selectively connecting said component means either to said analog circuit means or to said analog test bus means, test circuit means connected with said first and second test bus means and including a source for supplying a current to said component means when said component means is connected with said test bus means and detector means for determining the value of said component means.

2. Apparatus as claimed in Claim 1, wherein each of said devices further including switch means for selectively connecting a pin of the device with a voltage source or a reference voltage, each of said devices including storage means for storing a digital 1 or 0 for indicating the integrity of the interconnection between said pin and one or more other pins on said devices.

3. Apparatus as claimed in Claim 1, wherein said constant current is supplied by a programmable constant current generator and said voltage is measured by an analog to digital converter.

4. Apparatus as claimed in Claim 3, wherein said constant current source includes an operational amplifier, means connecting one input of the amplifier to a reference voltage, resistor means connecting a second input of said amplifier to a constant voltage source, means connecting a node between said resistor means and said second input of said amplifier to said first test bus, means connecting the output of said amplifier to said second test bus, said converter means converting the analog voltage developed

across said first and second test buses to a digital value, and computer means for determining said selected component value based on said digital value.

5. Apparatus as claimed in Claim 1, wherein said electrical component means includes a plurality of passive components, said first and second analog circuits each including a plurality of input/output conductors, said first and second switch means each including a plurality of pairs of switches, one of each pair of said pairs of switches adapted to connect said components with said input/output conductors to establish a predetermined circuit configuration between said first and second analog circuits, the other of each pair of said pairs of switches adapted to connect one or more of said components across said first and second test buses.

6. Apparatus as claimed in Claim 5, wherein said multiplex means includes switch control means, said switch control means including a plurality of storage elements for selectively activating said pairs of semiconductor switches in accordance with a digital test vector.

7. Apparatus as claimed in Claim 6, wherein each of said storage elements includes at least a first and second flip flops for controlling respective switches in said pairs of switches.

8. A method of measuring the value of an electrical component interconnecting analog circuitry located on first and second integrated circuit devices and comprising the steps of:

a. selecting the component for measurement by disconnecting the component from said analog circuitry and connecting the component to a test bus and loading an appropriate digital test vector in memory means located on each of said devices,

b. passing a constant current through the selected component, over an analog bus including at least one conductor and a switch located on each device and measuring the voltage developed across said conductors on said devices,

c. determining the component value between said devices using the voltage measured in step b.

9. A method as claimed in Claim 8, wherein each analog bus includes a pair of conductors and a pair of switches located on each device and wherein said step b. includes passing the current over one of the pair of conductors and one of the pair of switches on each device in one direction through said component, passing the current over the other of the pair of conductors and the other of the pair of switches in the opposite direction through said component, and passing the current through the pair of switches on one device and then the other device.

10. Apparatus as claimed in Claim 1, wherein each of said first and second analog test bus means includes a single conductor on each of said devices, the conductor on said first device connected with said source and the conductor on said second device connected with said detector means.

11. Apparatus as claimed in Claim 1, wherein each of said first and second analog test bus means includes a pair of conductor on each of said devices, one of each of said pair of conductors connected with said source and the other of each of said pair of conductors connected with said detector means.

12. Apparatus as claimed in Claim 11, wherein each of said devices includes at least first and second switches adapted to be concurrently closed and placed in series across said pair of conductors whereby the impedance of said first and second switches can be measured.

13. Apparatus as claimed in Claim 12, wherein each of said devices includes an internal conductor connected to one side of each of said first and second switches, the other side of one of said switches connected with said source, the other side of the other of said switches connected with said detector.

14. Apparatus as claimed in Claim 13, wherein each of said devices includes a third switch connected between said internal conductor and a voltage source for the device and a fourth switch connected between said internal conductor and ground, said internal conductor being connected with a pin of said device, a storage element connected with said internal conductor for storing the logic level on said internal conductor when said third or fourth switch is closed.

15. A method of measuring the value of one of a plurality of electrical components interconnecting analog circuitry located on first and second integrated circuit devices and for testing the integrity of the interconnection between said devices, comprising the steps of:

a. selecting a component by loading an appropriate digital test vector in memory means located on each of said devices,

b. passing a constant current through the selected component and measuring the voltage developed across said selected component,

c. determining the component value or the integrity of interconnection between said devices using the voltage measured in step b.

16. Apparatus for testing integrated circuits substantially as herein before described with reference to figures 2 to 5 of the accompanying drawings.

17. A method for testing integrated circuits substantially as herein before described with reference to figures 2 to 5 of the accompanying drawings.

| Patents Act 1977<br>Examiner's report to the Comptroller under Section 17<br>(The Search report) | 15 | Application number<br>GB 9409164.2 |
|---|---|---|
| **Relevant Technical Fields**<br><br>(i) UK Cl (Ed.M) G1U (VR3128 AND VR3130)<br><br>(ii) Int Cl (Ed.5) G01R (31/28, 31/30 AND 31/302) | | Search Examiner<br>KEN LONG<br><br>Date of completion of Search<br>4 AUGUST 1994 |
| **Databases** (see below)<br>(i) UK Patent Office collections of GB, EP, WO and US patent specifications.<br><br>(ii) NONE | | Documents considered relevant following a search in respect of Claims :-<br>1 TO 17 |

**Categories of documents**

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|---|---|---|---|
| **X:** | Document indicating lack of novelty or of inventive step. | **P:** | Document published on or after the declared priority date but before the filing date of the present application. |
| **Y:** | Document indicating lack of inventive step if combined with one or more other documents of the same category. | **E:** | Patent document published on or after, but with priority date earlier than, the filing date of the present application. |
| **A:** | Document indicating technological background and/or state of the art. | **&:** | Member of the same patent family; corresponding document. |

| Category | Identity of document and relevant passages | | Relevant to claim(s) |
|---|---|---|---|
| A | GB 2180355 A | (N V PHILIPS) see particularly page 1 lines 69 to 72 and 81 to 108 | |
| A | GB 2157837 A | (MARS) see particularly page 1 lines 5 to 12 and 69 to 101 | |
| A | US 5070296 | (HONEYWELL) see particularly column 2 lines 28 to 49 | |

**Databases:**The UK Patent Office database comprises classified collections of GB, EP, WO and US patent specifications as outlined periodically in the Official Journal (Patents). The on-line databases considered for search are also listed periodically in the Official Journal (Patents).

**Amendments to the Claims:**

A clean version of the entire set of pending claims (including amendments to the claims, if any) is submitted herewith per 37 CFR 1.121(c)(3). This listing of claims will replace all prior versions, and listings, of claims in the application.

**Listing of Claims:**

1. (Canceled)

2. (Currently amended) An electronic circuit ~~(100)~~ as ~~claimed in Claim 1~~ recited in claim 1~~0~~, wherein the test unit ~~(120)~~ comprises a Read Only Memory (ROM).

3. (Currently amended) An electronic circuit ~~(100)~~ as ~~claimed in Claim 1~~ recited in claim 1~~0~~, wherein the test unit ~~(120)~~ comprises a read/write register.

4. (Currently amended) An electronic circuit ~~(402)~~ as ~~claimed in Claim 1~~ recited in claim 1~~0~~, wherein the test unit ~~(406)~~ comprises a combinatorial circuit ~~(502)~~ implementing an XNOR function and being connected to the I/O nodes.

5. (Currently amended) An electronic circuit ~~(402)~~ as ~~claimed in Claim~~ recited in claim 4, wherein a first selection ~~(410)~~ of the I/O nodes are arranged to carry respective input signals and a second selection ~~(412)~~ of the I/O nodes are arranged to carry respective output signals and wherein the test unit ~~(406)~~ is arranged according to the following rules:

each output signal results from an XNOR function having at least two input signals,

each output signal is dependent on a unique subset of the input signals,

each input signal contributes to at least one output signal via a particular XNOR function.

6. (Currently amended) An electronic circuit ~~(402)~~ as ~~claimed in Claim 1~~ recited in claim 10, wherein the test unit ~~(406)~~ comprises a combinatorial circuit ~~(602)~~ implementing an XOR function and connected to the I/O nodes.

7. (Currently amended) An electronic circuit ~~(100)~~ as ~~claimed in Claim 1~~ recited in claim 10, wherein the main unit ~~(110)~~ is arranged to bring the electronic circuit ~~(100)~~ into the test mode on receipt via a subset of the I/O nodes ~~(130)~~ of a predefined pattern or sequence of patterns.

8. (Currently amended) An electronic circuit ~~(100)~~ as ~~claimed in Claim 1~~ recited in claim 10, wherein the electronic circuit is provided with a test control node and wherein the electronic circuit is arranged to switch into the test mode on the basis of a signal value on the test control node.

9. (Currently amended) An electronic circuit as ~~claimed in Claim 1~~ recited in claim 10, wherein the main unit is a Synchronous Dynamic Random Access Memory

(SDRAM) and the test mode is activatable by a read action following power up of the electronic circuit.

10. (Currently amended) An electronic circuit ~~(100)~~ comprising:

a plurality of input/output (I/O) nodes ~~(130)~~ for connecting the electronic circuit to a further electronic circuit via interconnects,

a main unit ~~(110)~~ for implementing a normal mode function of the electronic circuit,

and a test unit ~~(120)~~ for testing the interconnects,

the electronic circuit having a normal mode in which the I/O nodes ~~(130)~~ are logically connected to the main unit ~~(110)~~ and a test mode in which the I/O nodes ~~(130)~~ are logically connected to the test unit ~~(120)~~,

~~characterised in that~~ wherein the test unit comprises at least one combinatorial circuit ~~(502)~~ implementing at least one of an XNOR function and an XOR function with at least two function inputs and a function output, the function inputs being connected to particular I/O nodes arranged to operate as input nodes of the test circuit and the function output being connected to a particular I/O node arranged to operate as output node of the test circuit.

11-13 (Canceled)

| Issue Classification | Application No. | Applicant(s) | |
|---|---|---|---|
| | 10/621,002 | DE JONG ET AL. | |
| | Examiner | Art Unit | |
| | Craig Miller | 2857 | |

# ISSUE CLASSIFICATION

| ORIGINAL CLASS | ORIGINAL SUBCLASS | CROSS REFERENCE(S) CLASS | CROSS REFERENCE(S) SUBCLASS (ONE SUBCLASS PER BLOCK) |
|---|---|---|---|
| 702 | 118 | 324 | 500 |

| INTERNATIONAL CLASSIFICATION |
|---|
| G 01 R 31/28 |
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| / |
| / |

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TECHNOLOGY CENTER 2800
(Primary Examiner) 4/29/04 (Date)

**Total Claims Allowed: 9**

| O.G. Print Claim(s) | O.G. Print Fig. |
|---|---|
| 1 | 1 |

☐ Claims renumbered in the same order as presented by applicant ☐ CPA ☐ T.D. ☐ R.1.47

| Final | Original | Final | Original | Final | Original | Final | Original | Final | Original | Final | Original | Final | Original |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | 1 | | 31 | | 61 | | 91 | | 121 | | 151 | | 181 |
| 2 | 2 | | 32 | | 62 | | 92 | | 122 | | 152 | | 182 |
| 3 | 3 | | 33 | | 63 | | 93 | | 123 | | 153 | | 183 |
| 4 | 4 | | 34 | | 64 | | 94 | | 124 | | 154 | | 184 |
| 5 | 5 | | 35 | | 65 | | 95 | | 125 | | 155 | | 185 |
| 6 | 6 | | 36 | | 66 | | 96 | | 126 | | 156 | | 186 |
| 7 | 7 | | 37 | | 67 | | 97 | | 127 | | 157 | | 187 |
| 8 | 8 | | 38 | | 68 | | 98 | | 128 | | 158 | | 188 |
| 9 | 9 | | 39 | | 69 | | 99 | | 129 | | 159 | | 189 |
| 1 | 10 | | 40 | | 70 | | 100 | | 130 | | 160 | | 190 |
| | 11 | | 41 | | 71 | | 101 | | 131 | | 161 | | 191 |
| | 12 | | 42 | | 72 | | 102 | | 132 | | 162 | | 192 |
| | 13 | | 43 | | 73 | | 103 | | 133 | | 163 | | 193 |
| | 14 | | 44 | | 74 | | 104 | | 134 | | 164 | | 194 |
| | 15 | | 45 | | 75 | | 105 | | 135 | | 165 | | 195 |
| | 16 | | 46 | | 76 | | 106 | | 136 | | 166 | | 196 |
| | 17 | | 47 | | 77 | | 107 | | 137 | | 167 | | 197 |
| | 18 | | 48 | | 78 | | 108 | | 138 | | 168 | | 198 |
| | 19 | | 49 | | 79 | | 109 | | 139 | | 169 | | 199 |
| | 20 | | 50 | | 80 | | 110 | | 140 | | 170 | | 200 |
| | 21 | | 51 | | 81 | | 111 | | 141 | | 171 | | 201 |
| | 22 | | 52 | | 82 | | 112 | | 142 | | 172 | | 202 |
| | 23 | | 53 | | 83 | | 113 | | 143 | | 173 | | 203 |
| | 24 | | 54 | | 84 | | 114 | | 144 | | 174 | | 204 |
| | 25 | | 55 | | 85 | | 115 | | 145 | | 175 | | 205 |
| | 26 | | 56 | | 86 | | 116 | | 146 | | 176 | | 206 |
| | 27 | | 57 | | 87 | | 117 | | 147 | | 177 | | 207 |
| | 28 | | 58 | | 88 | | 118 | | 148 | | 178 | | 208 |
| | 29 | | 59 | | 89 | | 119 | | 149 | | 179 | | 209 |
| | 30 | | 60 | | 90 | | 120 | | 150 | | 180 | | 210 |

## Search Notes

| Application No. | Applicant(s) | |
|---|---|---|
| 10/621,002 | DE JONG ET AL. | |
| **Examiner** | **Art Unit** | |
| Craig Miller | 2857 | |

| SEARCHED | | | |
|---|---|---|---|
| Class | Subclass | Date | Examiner |
| 702 | 57-59 | | |
| | 108 | | |
| | 117, 118 | | |
| 324 | 500, 512 | | |
| | 527 | | |
| 326 | 16, 106 | | |
| 714 | 25, 27 | | |
| | 30, 718 | | |
| | 719, 726 | | |
| | 727, 733 | 4/7/2004 | CSM |
| | | | |
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| INTERFERENCE SEARCHED | | | |
|---|---|---|---|
| Class | Subclass | Date | Examiner |
| **702** | **118** | | |
| 324 | 500 | 4/7/2004 | CSM |
| | | | |
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| SEARCH NOTES (INCLUDING SEARCH STRATEGY) | | |
|---|---|---|
| | DATE | EXMR |
| EAST, see enclosed | 4/7/2004 | CSM |
| Conferred, P. Assouad, RE Search | 4/7/2004 | CSM |
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PA-IDC

| QUERY CONTROL FORM | | | | RTIS USE ONLY | |
|---|---|---|---|---|---|
| Application No. | 10/621,002 | Prepared by | BSH | Tracking Number | 059529926 |
| Examiner-GAU | Hoff-2857 | Date | 06-17-04 | Week Date | 05-17-2004 |
| | | No. of queries | 1 | IFW-RU4 | |

| JACKET | | | |
|---|---|---|---|
| a. Serial No. | f. Foreign Priority | k. Print Claim(s) | p. PTO-1449 |
| b. Applicant(s) | g. Disclaimer | l. Print Fig. | q. PTOL-85b |
| c. Continuing Data | h. Microfiche Appendix | m. Searched Column | r. Abstract |
| d. PCT | i. Title | n. PTO-270/328 | s. Sheets/Figs |
| e. Domestic Priority | j. Claims Allowed | o. PTO-892 | t. Other |

**SPECIFICATION**

a. Page Missing
b. Text Continuity
c. Holes through Data
d. Other Missing Text
e. Illegible Text
f. Duplicate Text
g. Brief Description
h. Sequence Listing
i. Appendix
j. Amendments
k. Other

**CLAIMS**

a. Claim(s) Missing
b. Improper Dependency
c. Duplicate Numbers
d. Incorrect Numbering
e. Index Disagrees
f. Punctuation
g. Amendments
h. Bracketing
i. Missing Text
j. Duplicate Text
k. Other

**MESSAGE**

Specification ends on pg 17-but ends incompletly without period. Last line of text references "Example 3" which is not to be found on pg 17. Should there be a pg 18? Please advise.

WO99/39718

Thank you

initials BSH

**RESPONSE** Yes, CLM begins with p. 19, supplied p. 18

initials dlf

E-5 (Rev. 10/01/02)

Figure 6 schematically shows an alternative for the test unit for five inputs and two outputs. This figure corresponds with the Example 3 above. The test unit 406 has a three-input XOR gate 602 which implements the required exclusive-or function between o1 and i1, i2 and i3. The test unit further has a three-input XOR gate 604 which implements the exclusive-or function between the input pins i3, i4 and i5 and the output pin o2.

The following table gives the patterns for Example 3 together with the required outputs.

| pattern number | iiiii 12345 | oo 12 |
|---|---|---|
| 1 | 00000 | 00 |
| 2 | 10000 | 10 |
| 3 | 01000 | 10 |
| 4 | 00100 | 11 |
| 5 | 00010 | 01 |
| 6 | 00001 | 01 |
| 7 | 11111 | 11 |
| 8 | 01111 | 01 |
| 9 | 10111 | 01 |
| 10 | 11011 | 00 |
| 11 | 11101 | 10 |
| 12 | 11110 | 10 |

It is to be noted that the above-mentioned embodiments illustrate rather than limit the invention and that those skilled in the art will be able to design many alternative embodiments without departing from the scope of the appended claims. In the claims, any reference signs placed between parentheses shall not be construed as limiting the claim.

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24737 7590 05/04/2004

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DANIEL G. MICHALCHIK (Depositor's name)
(Signature)
04-AUG-04. (Date)

| APPLICATION NO. | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. | CONFIRMATION NO. |
|---|---|---|---|---|
| 10/621,002 | 07/16/2003 | Franciscus G.M. De Jong | PHN 17203A | 9122 |

TITLE OF INVENTION: CIRCUIT WITH INTERCONNECT TEST UNIT

| APPLN. TYPE | SMALL ENTITY | ISSUE FEE | PUBLICATION FEE | TOTAL FEE(S) DUE | DATE DUE |
|---|---|---|---|---|---|
| nonprovisional | NO | $1330 | $300 | $1630 | 08/04/2004 |

| EXAMINER | ART UNIT | CLASS-SUBCLASS |
|---|---|---|
| MILLER, CRAIG S | 2857 | 702-117000 |

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(B) RESIDENCE: (CITY and STATE OR COUNTRY): Eindhoven, The Netherlands

Please check the appropriate assignee category or categories (will not be printed on the patent); ☐ individual ☒ corporation or other private group entity ☐ government

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