UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

APPLE INC.
Petitioner

v.

FUTURE LINK SYSTEMS, LLC
Patent Owner

Inter Partes Review Case No. IPR2021-01488
U.S. Patent No. 6,807,505

DECLARATION OF DR. DAVID KUAN-YU LIU

I, David Kuan-Yu Liu, hereby declare the following:

I. BACKGROUND AND QUALIFICATIONS

1. My name is David Kuan-Yu Liu, Ph.D and I am over 21 years of age and otherwise competent to make this Declaration. I make this Declaration based on facts and matters within my own knowledge and on information provided to me by others.

2. I have been retained by counsel for Petitioner as a technical expert in the above-captioned case. Specifically, I have been asked to render certain opinions in regard to the IPR petition with respect to U.S. Patent No. 6,807,505 (the "'505 Patent"). I understand that the Challenged Claims are claims 1, 6, and 8. My opinions are limited to those Challenged Claims.

3. My compensation in this matter is not based on the substance of my opinions or the outcome of this matter. I have no financial interest in Petitioner.

4. In writing this declaration, I have considered my own knowledge and experience, including my work experience in the field of electrical and computer engineering and my experience working with others involved in this field, including in the design and analysis of integrated circuit systems and subsystems. In reaching my opinions in this matter, I have also reviewed the following references and materials:

- The '505 Patent (Ex. 1001)
- Article on JTAG Boundary Scan IEEE Standard (Ex. 1002)

- Inventor Article on Boundary Scan Testing Standard (Ex. 1003)
- Prosecution History for the '505 Patent (Ex. 1005)
- U.S. Patent No. 4,241,307 ("Hong") (Ex. 1006)
- Any additional background materials cited below

A. Educational Background

5. I received a Bachelor of Science degree in Electrical Engineering from the University of California, Berkeley, in 1983. I received a Master of Science and Ph.D. degrees in Electrical Engineering from Stanford University in 1985 and 1989, respectively.

B. Professional Experience

6. From 1989 to 1992, I was a member of technical staff at Texas Instruments, Inc. At Texas Instruments, my job responsibilities included process integration, device modeling, high-voltage CMOS process integration, and investigating novel source-side injection mechanisms for Flash EPROM channel hot-electron programming.

7. From 1992 to 1995, I was a member of the technical staff at Advanced Micro Devices, Inc. (AMD) where I was a key contributor in optimizing Flash cell and periphery devices in AMD's CMOS-based 0.5um and 0.35um Flash EPROM technology. My job responsibilities at AMD also included process integration, device modeling, and development of triple-well process technology for accommodate x-decoder transistors and high voltage transistors for negative gate

erase operation. While at AMD, I was awarded a Spotlight Award for developing a method of manufacturing a self-aligned source (SAS) etch for a NOR flash memory.

8. I spent the next five years of my career in managerial and director roles at several California-based semiconductor companies. I was responsible for increasing yield and for leading teams of engineers working to develop next-generation memory devices.

9. In 2000, I co-founded Progressant Technologies in Fremont, California. Progressant Technologies developed IP for negative differential resistance transistor technology and was eventually acquired by Synopsys, Inc.

10. From 2000 to 2004, I was a Senior Manager at Xilinx, Incorporated, where I was responsible for developing nonvolatile memory process technology for flash and CPLD product applications, as well as advanced CMOS process technology (specifically 75nm CMOS technology node, a half node version between 90nm and 65nm). The flash memory products I developed at Xilinx are used as the configuration memory for the FPGA, with the configuration interface between them being the JTAG interface.

11. From 2004 to 2007, I was a Senior Scientist at Maxim Integrated Products where I was responsible for developing Embedded Non-volatile Memory process technology for Power Management product applications.

12. Since 2007, I have served as a technical consultant where I have provided expert advice regarding Flash memory technology, CMOS process technology, and semiconductor device physics.

13. I have 20 years of experience as an engineer and engineering manager/director of Complementary Metal Oxide Semiconductor (CMOS) technology development. During my career, I have worked at some of the leading technology companies in the world, such as Texas Instruments, Advanced Micro Devices, Altera Corporation (now a subsidiary of Intel Corp.), and Xilinx. At these companies, my work focused on various aspects of CMOS and semiconductor technology.

14. I hold over 95 U.S. patents, a large number of which are directed to logic CMOS processes technology and high voltage CMOS process technology. The vast majority of my patents are in the area of CMOS process technology and memory architecture. As such, I am intimately familiar with the implementation of integrated process flows that essentially are repetitive sequences of modules, each composed of a layer patterning step followed by selective deposition and etching of various semiconductor materials, with the area of selectivity dictated by the layer patterning.

15. I have also authored several technical papers that have been published in well-respected, peer-reviewed journals, such as the IEEE Electron Device Letters, the IEEE Journal of Solid-State Circuits, and the IEEE Transactions on Electron

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