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De Jong et al.

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(54) **CIRCUIT WITH INTERCONNECT TEST UNIT**

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Related U.S. Application Data

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(30) **Foreign Application Priority Data**

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May 6, 1998 (EP) 98201482
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(51) **Int. Cl.**[7] **G01R 31/28**

(52) **U.S. Cl.** **702/118**; 324/500

(58) **Field of Search** 702/57–59, 108, 702/117, 118; 324/500, 512, 527; 326/16, 106; 714/25, 27, 30, 718, 719, 726, 727, 733

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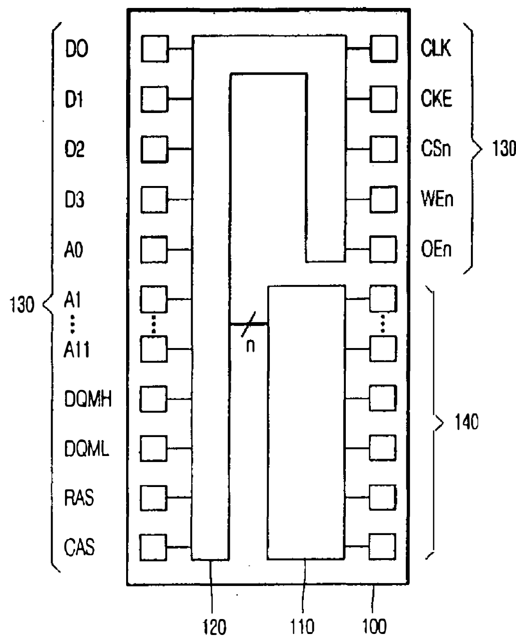
(57) **ABSTRACT**

An electronic circuit comprises a plurality of input/output (I/O) nodes for connecting the electronic circuit to a further electronic circuit via interconnects. A main unit implements a normal mode function of the electronic circuit. A test unit tests the interconnects. The electronic circuit has a normal mode in which the I/O nodes are logically connected to the main unit and a test mode in which the I/O nodes are logically connected to the test unit. In the test mode the test unit is operable as a low complexity memory via the I/O nodes.

9 Claims, 3 Drawing Sheets



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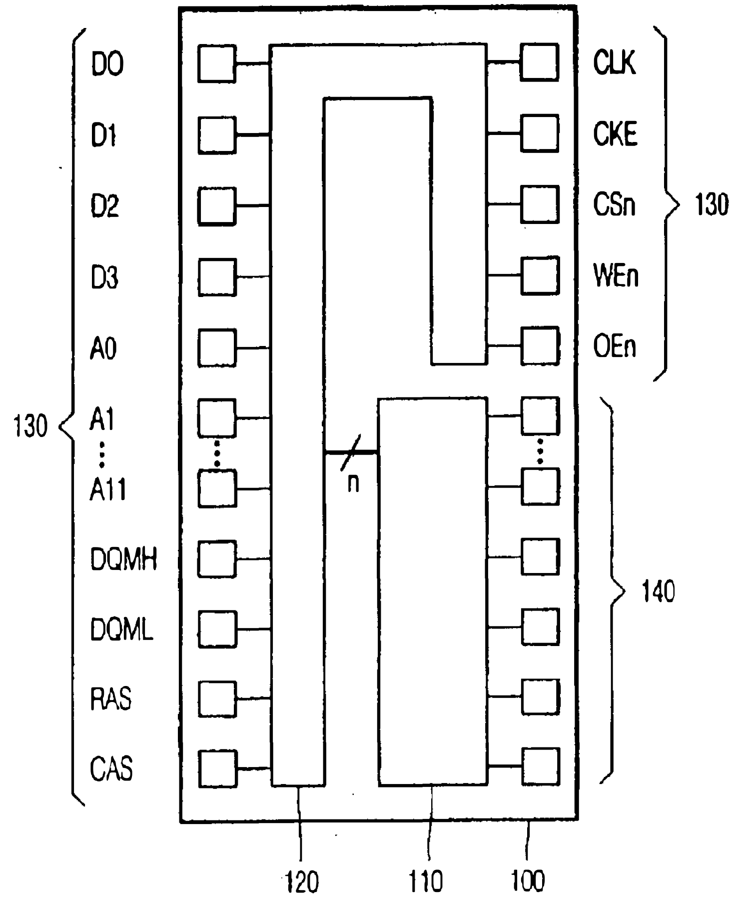

FIG. 1

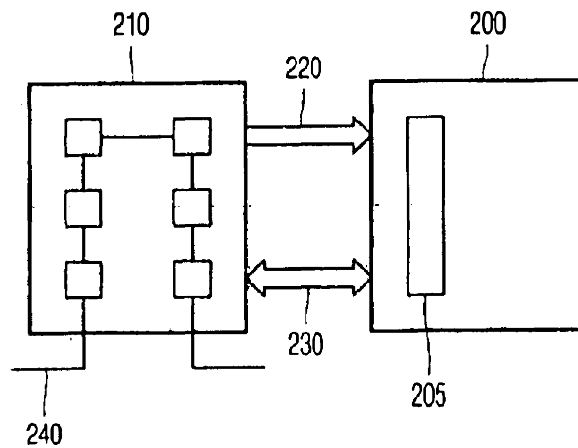

FIG. 2

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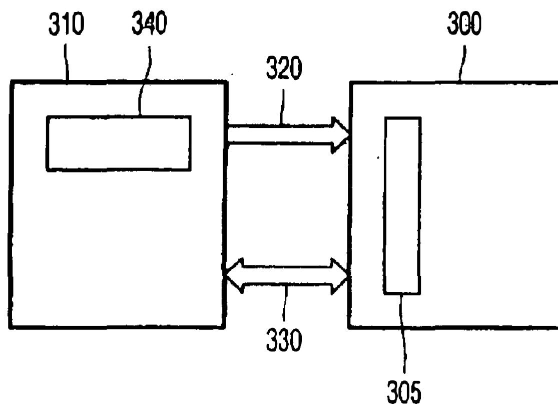

FIG. 3

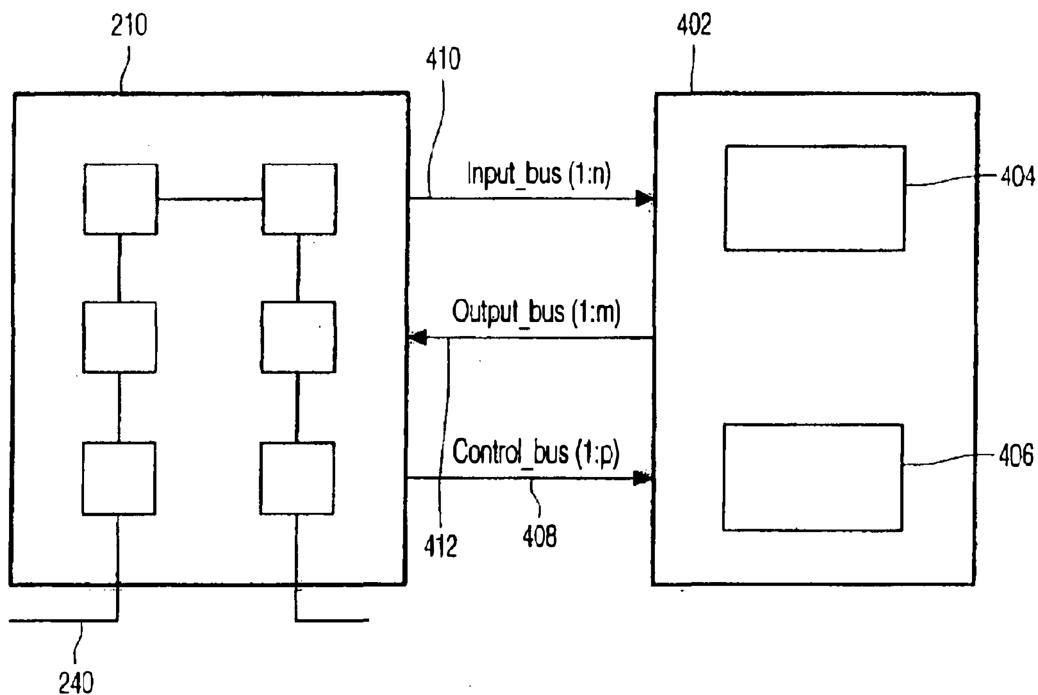

FIG. 4

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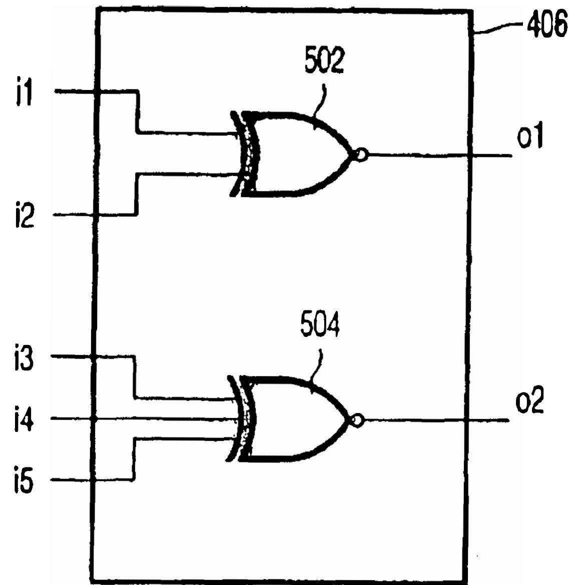

FIG. 5

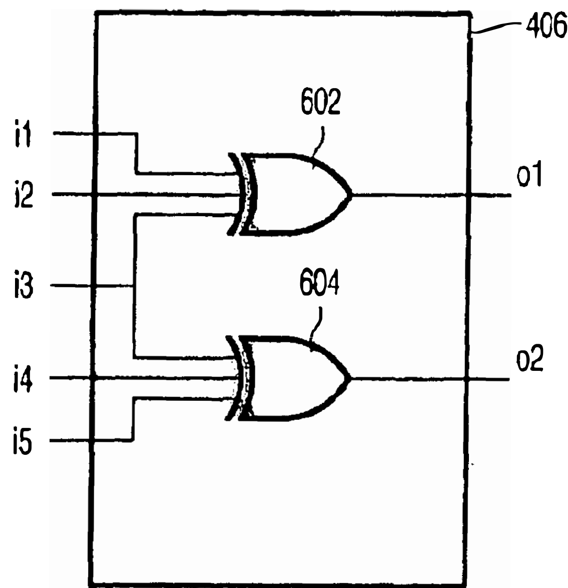

FIG. 6

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CIRCUIT WITH INTERCONNECT TEST UNIT

This application is a divisional of Ser. No. 09/402,154 filed Sep. 29, 1999 now U.S. Pat. No. 6,622,108 which is a 371 of PCT/IB99/00172 filed Jan. 29, 1999.

The invention relates to an electronic circuit comprising: a plurality of input/output (I/O) nodes for connecting the electronic circuit to a further electronic circuit via interconnects, a main unit for implementing a normal mode function of the electronic circuit, and a test unit for testing the interconnects, the electronic circuit having a normal mode in which the I/O nodes are logically connected to the main unit and a test mode in which the I/O nodes are logically connected to the test unit.

The invention further relates to a method of testing interconnects between a first electronic circuit and a second electronic circuit, the first electronic circuit comprising a main unit implementing a normal mode function of the first electronic circuit, and a test unit for testing the interconnects, the method comprising the steps of logically connecting the test unit to the interconnects, and putting test data on the interconnects by the second electronic circuit.

Such a circuit is known from "Boundary-scan test, a practical approach", H. Bleeker, P. van den Eijnden and F. de Jong, Kluwer, Boston, 1993, ISBN 0-7923-9296-5, FIGS. 1–19, which shows an integrated (IC) in accordance with the boundary-scan test standard IEEE Std. 1149.1. The known circuit has a main unit or core logic that is responsible for providing some arbitrary specified function in a normal mode of the circuit. The known circuit further has a test unit for in a test mode performing an interconnect test, i.e. a test whether the circuit is properly connected to a further circuit via its I/O nodes or IC pins. Efficient interconnect test of miniaturised and/or complex circuit assemblies is a necessary part of the production process of such assemblies. The boundary-scan test technique is accepted as standardised solution for interconnect test. It is available in most of the leading microprocessor families and is supported for in-house developed application specific ICs through automated tools in the IC design process.

The test unit of the known boundary-scan circuit includes a test control unit or Test Access Port controller and a shift register or boundary-scan register along the circuit boundary, cells of the shift register being connected to I/O nodes corresponding to the interconnects to be tested. The test control unit has a state machine controlling states of the shift register, examples of such states being a shift state for shifting in/out data into the shift register and a capture state for capturing data originating from the interconnects into the shift register. The shift register is accessible from outside the circuit via a Test Data In (TDI) node and a Test Data Out (TDO) node. A Test Clock signal (TCK) and a Test Mode Select signal (TMS) are provided from outside the circuit to the test control unit for stepping through the various states. In the normal mode of the known circuit, the I/O nodes are logically connected to the main unit, thereby allowing the circuit to perform its normal mode function. In the test mode of the known circuit, the I/O nodes are logically connected to the test unit, thereby giving the test unit access to the interconnects.

Provided that also the further circuit is equipped with a test unit in accordance with the boundary-scan test standard, the interconnects between the two circuits can be tested according to the standard boundary-scan test method.

the interconnects. Then, response data originating from the interconnects is captured into the shift registers and subsequently shifted out of the shift registers for observation. From the response data it can be determined whether the circuits are properly interconnected. For a single interconnect this means that to one of its ends a signal is applied and at the other end it is observed whether that signal is transmitted. In this way, an open circuit in an interconnect can be found. Additionally, a number of test patterns will be applied to the interconnects in order to check for short-circuits between neighbouring interconnects, or between an interconnect and a power supply line. Essentially, interconnect testing comes down to applying test data to one end of an interconnect and observing response data at another end, in such a way that open circuits and short circuits are detected.

A problem with the boundary-scan approach is that for some circuits pin count and pin compatibility considerations inhibit the addition of extra pins to a circuit design for the TCK, TMS, TDI, TDO and the optional TRSTN signals. Moreover, the price-pressure in some semiconductor fields is such that it is considered to be too expensive to reserve area for interconnect test of the size as required by boundary-scan circuitry.

It is an object of the invention to provide a circuit as specified in the preamble, that allows interconnect testing with reduced overhead in terms of required I/O nodes and/or area. This object is achieved according to the invention in an electronic circuit, which is characterised in that in the test mode the test unit is operable as a low complexity memory via the I/O nodes. Low complexity memories are those memories that do not have to be put through a complex initialisation process before they can be accessed, and that have simple access protocols without dynamic restrictions. Such a test unit enables an alternative procedure for applying test data to one end of an interconnect and observing response data at the other end. If the low complexity memory has a read-only character and holds pre-stored test data at a number of addresses, the test unit produces this pre-stored test data at its side of the interconnects when address data and appropriate control data are applied to it by the further circuit via the interconnects. The further circuit then receives response data, which should be identical to the pre-stored test data. In this way, both the interconnects that are used to carry the address and control data and the interconnects that are used to carry the pre-stored data itself are tested. It is important that particular input data for the test unit, i.e. the address, result in output data from the test unit that are known a priori, i.e. the stored data. If the low complexity memory allows both read and write access, the further circuit can apply test data to its side of the interconnects in a write mode of the test unit, thereby storing the test data in the test unit. In a subsequent read mode of the test unit, the further circuit can read back response data.

Whether the test unit has a read-only or a read/write behaviour, it does not need a state machine like the boundary-scan state machine and can therefore be implemented consuming less area. Moreover, the simple operation of the test unit allows less pins or even no pins at all to be reserved for controlling the test unit in the test mode. For both a read-only and a read/write test unit, a subset of the interconnects is used as a data bus for exchanging the storage data. At least in the case that the test unit has a read/write behaviour, a further subset of the interconnects is used as a control bus, including, for example, control lines

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