JTAG BOUNDARY-SCAN, FIRMLY BASED ON IEEE STANDARDS - JTAG

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JTAG boundary-scan, firmly based on IEEE standards

The serial interface and logic were originally developed by a group of test professionals from Philips, BT, GEC, TI and others known as JTAG (the Joint Test Action Group) throughout the late 1980s. The group continued as an IEEE working group to complete the final standard which then got the official name IEEE Std 1149.1 (https://standards.ieee.org/standard/1149 1-1990.html), the IEEE Standard Test Access Port (JTAG interface) and Boundary-Scan Architecture. The standard was first released in 1990. Since then enhancements have been made and the latest update was done in 2013, see IEEE 1149.1-2013.

The IEEE Std 1149.1 is often referred to by other names such as JTAG, JTAG boundary-scan, or Dot1. JTAG devices are officially referred to as IEEE 1149.1 compliant devices.

The standard defines the serial (JTAG) interface, called the Test Access Port (TAP), and the test logic architecture built into chips. One specific example of test logic is defined in the standard, the so called boundary-scan register, for testing connections between devices on a PCBA.

The TAP features four (or sometimes five) signals:

- TCK (Test clock)
- TMS (Test Mode Select)
- TDI (Test Data In)
- TDO (Test Data Out)
- TRST (Test logic Reset) (optional)

To simplify the test infrastructure within a PCBA it is common to connect the devices in serial (da

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The test logic architecture comprises of one Instruction Register (IR) and multiple Data Registers (DR). By loading an opcode in the IR with an IR-scan a specific DR is selected which is then accessed with consecutive DR-scans.

When the boundary-scan register is selected as DR, this register will control the device's pins while isolating the primary core functions of the device.

The test logic architecture from Dot1 is defined such that other data registers (DRs) can easily be added in a chip design. For example the debug logic of microprocessors and microcontrollers or the programming logic in modern CPLDs and FPGAs. These DRs are defined in additional standards building upon and enhancing the original Dot1 (https://www.jtag.com/other-standards-since-the-release-of-dot-1/).

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