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Paper 8
Entered: April 11, 2022

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

APPLE INC.,
Petitioner,

v.

FUTURE LINK SYSTEMS, LLC,
Patent Owner.

IPR2021-01488
Patent 6,807,505 B2

Before KARL D. EASTHOM, KEVIN C. TROCK, and JOHN A. HUDALLA, *Administrative Patent Judges.*

TROCK, *Administrative Patent Judge*.

DECISION
Granting Institution of *Inter Partes* Review
35 U.S.C. § 314

I. INTRODUCTION

A. Background

Apple Inc. ("Petitioner") filed a Petition, Paper 1 ("Pet." or "Petition"), to institute an *inter partes* review of claims 1, 6, and 8 (the "challenged claims") of U.S. Patent No. 6,807,505 B2 (Ex. 1001, "the '505 patent"). Future Link Systems, LLC ("Patent Owner") timely filed a Preliminary Response, Paper 7 ("Prelim. Resp.").

The Director has discretion to institute an *inter partes* review under 35 U.S.C. § 314(a) and has delegated that authority to the Board under 37 C.F.R. § 42.4(a). *See* 35 U.S.C. § 314(a) (stating "[t]he Director may not authorize an inter partes review to be instituted unless the Director determines that the information presented in the petition . . . shows that there is a reasonable likelihood that the petitioner would prevail with respect to at least 1 of the claims challenged in the petition)."

Upon consideration of the Petition, the Preliminary Response, and the evidence of record, we determine that Petitioner has shown a reasonable likelihood that it would prevail in showing the unpatentability of at least one of the challenged claims. Accordingly, we institute an *inter partes* review.

B. Real Party in Interest

Petitioner identifies itself as the only real party in interest. Pet. 55. Patent Owner also identifies itself as the only real party in interest. Paper 4, 1.

C. Related Proceedings

According to the parties, the '505 patent is the subject of the following action: *Future Link Systems, LLC v. Apple Inc.*, No. 6:21-cv-00263 (W.D. Tex.) (the "parallel proceeding"). Pet. 55; Paper 4, 1.

D. The '505 Patent (Ex. 1001)

The '505 patent relates to an electronic circuit comprising a plurality of input/output ("I/O") nodes for connecting the electronic circuit to a further electronic circuit via interconnects, a main unit for implementing a normal mode function of the electronic circuit, and a test unit for testing the interconnects. Ex. 1001, 1:7–12. The electronic circuit has a normal mode in which the I/O nodes are logically connected to the main unit and a test mode in which the I/O nodes are logically connected to the test unit. *Id.* at 12–15.

Figure 1 of the '505 patent is shown below.

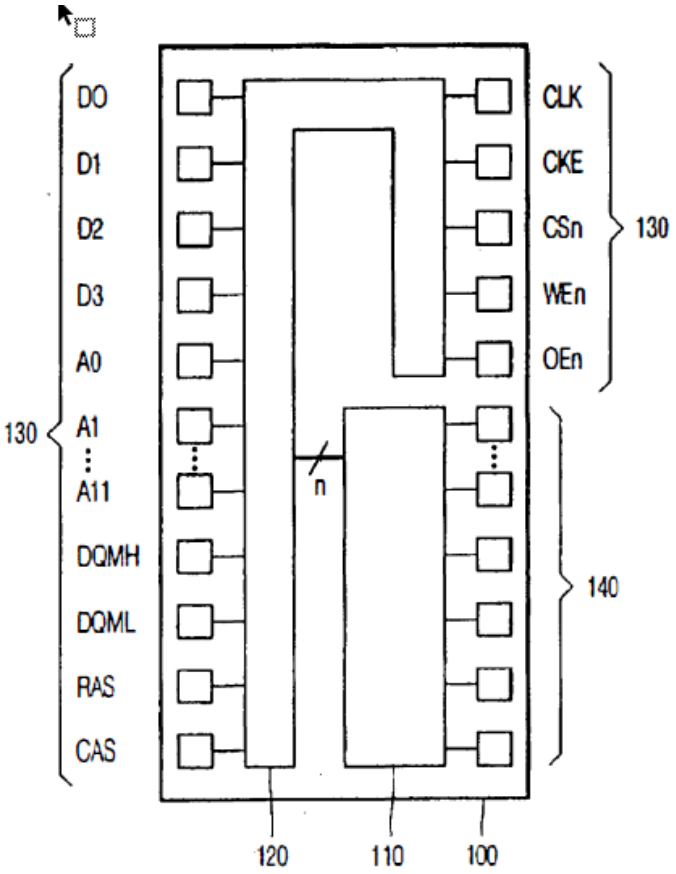

FIG. 1

Figure 1, above, illustrates electronic circuit 100. *Id.* at 5:31–32. Circuit 100 has I/O nodes 130, 140, through which circuit 100 is connectable to external circuits. *Id.* at 5:32–34. Circuit 100 is part of an assembly, whereas interconnects between circuit 100 and further parts of the assembly are testable. *Id.* at 5:41–43. Circuit 100 further has test unit 120, which is connected to main unit 110 via n parallel connections and to I/O nodes 130. *Id.* at 5:43–46. In a normal mode of circuit 100, test unit 120 is transparent, and signals can pass freely between I/O nodes 130 and main unit 110. *Id.* at 5:46–48. In a test mode of circuit 100, main unit 110 is logically disconnected from I/O nodes 130 and test unit 120 is in control. *Id.* at 5:48–50.

Figure 2 of the ’505 patent is shown below.

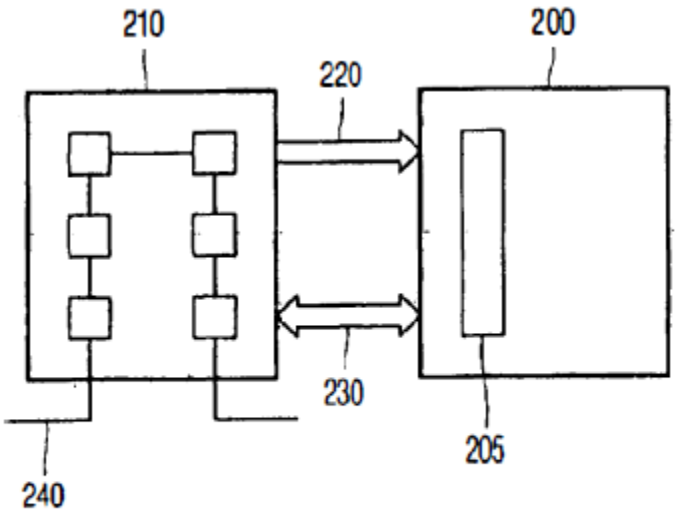

FIG. 2

Figure 2, above, illustrates a way to provide access during interconnect test to circuit 200 that is testable. *Id.* at 8:21–23. Circuit 200 includes test unit 205 that is operable as a low complexity memory. *Id.* at 8:23–24. Neighboring circuit 210, which has boundary-scan circuitry, provides data

to, and receives data from, circuit 200 via control and address bus 220 and bi-directional data bus 230. *Id.* at 8:24–27. Via boundary-scan chain 240, data is shifted to circuit 210, where the data makes up read and/or write commands to be supplied to circuit 200. *Id.* at 8:39–41. After a read command, boundary-scan chain 240 captures data supplied to data bus 230 by circuit 200. *Id.* at 8:41–43. Subsequently, the data is shifted out to be analyzed externally. *Id.* at 8:43–44.

Figure 6 of the '505 patent is shown below.

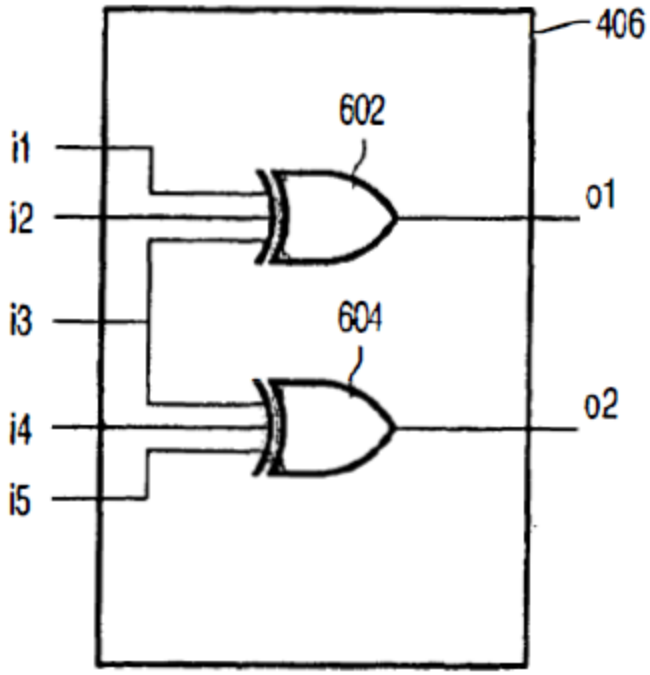

FIG. 6

Figure 6, above, schematically shows a test unit for five inputs and two outputs. *Id.* at 11:62–63. Test unit 406 has three-input XOR gate 602, which implements an exclusive-or function between output pin o1 and input pins i1, i2, and i3. *Id.* at 11:64–66. Test unit 406 further has three-input

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