

UNITED STATES PATENT AND TRADEMARK OFFICE

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BEFORE THE PATENT TRIAL AND APPEAL BOARD

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APPLE, INC.,

Petitioner,

v.

FUTURE LINK SYSTEMS, LLC,

Patent Owner.

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Case No.: IPR2021-01488

U.S. Patent No. 6,807,505

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**PATENT OWNER FUTURE LINK SYSTEMS, LLC'S  
PRELIMINARY RESPONSE**

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## EXHIBITS

Exhibit No.	Description
2001	Joint Agreed Scheduling Order, dated October 7, 2021 (Dkt. 29)
2002	Defendant's Preliminary Invalidity Contentions, dated September 16, 2021

## I. INTRODUCTION

The Petition seeks review of claims 1, 6, and 8 of U.S. Patent No. 6,807,505 (the “505 patent”) on a single asserted ground of single reference obviousness under 35 U.S.C. § 103. Claim 1 is the only challenged independent claim. The challenged claims relate to testing electronic circuits and the use of a test unit to test interconnects between the electronic circuit and other electronic circuits using a combinatorial circuit. The claims contemplate an electronic circuit comprising various elements, including interconnects – input/output nodes, a main unit, and a test unit. The Petition, however, contains significant inconsistencies in its attempt to identify the claim elements in the prior art. These inconsistencies constitute a failure of the Petition to meet the basic standard for institution.

Additionally, the Board should exercise its discretion and decline to institute the Petition under the *Fintiv* criteria. Petitioner conceded that the trial date proposed for the parallel District Court action is approximately two months before the final decision date for this matter. Since the filing of the Petition, the District Court entered the schedule proposed by the parties. Petitioner offers little more than speculation to suggest that this date will change based on unproduced and unverifiable data. But even if Petitioner’s “evidence” in Exhibit 1010 were to be accepted, it shows that even if the average amount of “slippage” of the trial date occurred, trial would still occur well before the final decision date for this

proceeding. Thus, Patent Owner respectfully submits that the Board should apply its discretion to deny institution of the Petition for this additional reason.

## II. OVERVIEW OF '505 PATENT AND CHALLENGED CLAIMS

The '505 patent (Ex. 1001) issued October 19, 2004 from a U.S. Application filed July 16, 2003. It claims priority to several foreign applications, the earliest of which was filed February 22, 1998. The '505 patent discloses improved electronic circuits containing test units for testing interconnects of the electronic circuits. In particular, the patent teaches the use of test units comprising a combinatorial circuit implementing at least one of an XNOR and an XOR function.

The '505 patent explains that the invention provides for efficient testing of interconnects without the need for compliance with a particular protocol. Ex. 1001 at col. 2:25-54. It further relates to an electronic circuit that includes a test unit for testing interconnects as part of the circuit itself. *Id.* at col. 1:7-15. The patent goes on to provide various examples of test units implemented using combinatorial circuits. *See generally*, Ex. 1001 at col. 9:57-12:20.

The Petition challenges claims 1, 6, and 8. Only claim 1 is independent. It recites:

1. An electronic circuit comprising:  
  
a plurality of input/output (I/O) nodes for connecting the electronic circuit to a further electronic circuit via interconnects,

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