UNITED STATES PATENT AND TRADEMARK OFFICE

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BEFORE THE PATENT TRIAL AND APPEAL BOARD

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MICROCHIP TECHNOLOGY, INC.,
Petitioner

v.

HD SILICON SOLUTIONS LLC,
Patent Owner

Case Nos. IPR2021-01420 and IPR2021-01421
U.S. Patent No. 7,260,731

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DECLARATION OF SYLVIA HALL-ELLIS, PH.D. IN SUPPORT OF PETITIONER'S PETITION FOR *INTER PARTES* REVIEW

I, Sylvia D. Hall-Ellis, Ph.D., declare as follows:

I. INTRODUCTION

1. My name is Sylvia D. Hall-Ellis. I have been retained as an expert by Microchip Technology Inc. ("the Petitioner"), who I am informed is the Petitioner seeking for the Patent Trial and Appeal Board to institute *inter partes* review (IPR) proceeding.

2. I have written this declaration at the request of the Petitioner to provide my expert opinion regarding the public availability of several publications, identified below. My Declaration sets forth my opinions in detail and provides the basis for my opinions regarding the public availability of these publications.

3. I reserve the right to supplement or amend my opinions, and bases for them, in response to any additional evidence, testimony, discovery, argument, and/or other additional information that may be provided to me after the date of this Declaration.

4. As of the preparation and signing of this declaration, many libraries across the nation are closed or permit only limited access due to the COVID-19 virus. However, were the libraries open, I would expect to be able to obtain paper copies of at least some of the documents in this declaration. I reserve the right to supplement my declaration when the libraries reopen to provide such information.

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5. I am being compensated for my time spent working on this matter at my normal consulting rate of $325 per hour, plus reimbursement for any additional reasonable expenses. My compensation is not in any way tied to the content of this report, the substance of my opinions, or the outcome of this litigation. I have no other interests in this proceeding or with any of the parties.

6. All of the materials that I considered and relied upon are discussed explicitly in this declaration.

II. QUALIFICATIONS

7. I am currently an Adjunct Professor in the School of Information at San José State University in San José, California. I obtained a Master of Library Science from the University of North Texas in 1972 and a Ph.D. in Library Science from the University of Pittsburgh in 1985. Over the last fifty years, I have held various positions in the field of library and information resources. I was first employed as a librarian in 1966 and have been involved in the field of library sciences since, holding numerous positions.

8. I am a member of the American Library Association (ALA) and its Association for Library Collections & Technical Services (ALCTS) Division, and I served on the Committee on Cataloging: Resource and Description (which wrote the new cataloging rules) and as the chair of the Committee for Education and Training of Catalogers and the Competencies and Education for a Career in

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Cataloging Interest Group. I also served as the Chair of the ALCTS Division's Task Force on Competencies and Education for a Career in Cataloging. Additionally, I have served as the Chair for the ALA Office of Diversity's Committee on Diversity, as a member of the REFORMA National Board of Directors, and as a member of the Editorial Board for the ALCTS premier cataloging journal, *Library Resources and Technical Services*. Currently I serve as a Co-Chair for the Library Research Round Table of the American Library Association.

9. I have also given over one hundred presentations in the field, including several on library cataloging systems and Machine-Readable Cataloging ("MARC") standards. My current research interests include library cataloging systems, metadata, and organization of electronic resources.

10. My full curriculum vitae is attached hereto as **Exhibit A**.

III.   PRELIMINARIES

A.   Scope of Declaration and Legal Standards

11. I am not an attorney and will not offer opinions on the law. I am, however, rendering my expert opinion on the authenticity of the documents referenced herein and on when and how each of these documents was disseminated or otherwise made available to the extent that persons interested and ordinarily skilled in the subject matter or art, exercising reasonable diligence,

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could have located the documents before the dates discussed below with respect to the specific documents.

12. I am informed by counsel that a printed publication qualifies as publicly accessible as of the date it was disseminated or otherwise made available such that a person interested in and ordinarily skilled in the relevant subject matter could locate it through the exercise of ordinary diligence.

13. While I understand that the determination of public accessibility under the foregoing standard rests on a case-by-case analysis of the facts particular to an individual publication, I also understand that a printed publication is rendered "publicly accessible" if it is cataloged and indexed by a library such that a person interested in the relevant subject matter could locate it (*i.e.*, I understand that cataloging and indexing by a library is sufficient, though there are other ways that a printed publication may qualify as publicly accessible). One manner of sufficient indexing is indexing according to subject matter category. I understand that the cataloging and indexing by a single library of a single instance of a particular printed publication is sufficient, even if the single library is in a foreign country. I understand that, even if access to a library is restricted, a printed publication that has been cataloged and indexed therein is publicly accessible so long as a presumption is raised that the portion of the public concerned with the relevant subject matter would know of the printed publication. I also understand

that the cataloging and indexing of information that would guide a person interested in the relevant subject matter to the printed publication, such as the cataloging and indexing of an abstract for the printed publication, is sufficient to render the printed publication publicly accessible.

14. I understand that routine business practices, such as general library cataloging and indexing practices, can be used to establish an approximate date on which a printed publication became publicly accessible.

B.   Persons of Ordinary Skill in the Art

15. I am told by counsel that the subject matter of this proceeding generally relates to reducing the power consumed by processors and voltage regulators in a computer system.

16. I have been informed by counsel that a "person of ordinary skill in the art at the time of the invention" (POSITA) is a hypothetical person who is presumed to be familiar with the relevant field and its literature at the time of the inventions. This hypothetical person is also a person of ordinary creativity, capable of understanding the scientific principles applicable to the pertinent field.

17. I am told by counsel that a POSITA as of October 23, 2000, would have possessed a bachelor's degree in electrical engineering, computer engineering, or computer science, with two years of experience in computer system development, including experience in developing power/voltage regulation systems for

portable devices. A person could also have qualified as a POSITA with some combination of (1) more formal education (such as a master's of science degree) and less technical experience or (2) less formal education and more technical or professional experience in the fields listed above. I have been further informed by counsel that a POSITA would have been familiar with and able to understand the information known in the art relating to these fields, including the publications discussed in this declaration. I have been further informed by counsel that a POSITA would have been familiar with and able to understand the information known in the art relating to these fields, including the publication discussed in this declaration.

C.   Use of Authoritative Databases

18. In preparing this report, I used authoritative databases, such as the OCLC bibliographic database and the Library of Congress Online Catalog, to confirm citation details of the publication discussed.

19. A researcher may discover material relevant to his or her topic in a variety of ways. One common means of discovery is to search for relevant information in an index of periodical and other publications. Having found relevant material, the researcher will then normally obtain it online, look for it in libraries, or purchase it from the publisher, a bookstore, a document delivery service, or other provider. Sometimes, the date of a document's public

accessibility will involve both indexing and library date information.

20. Indexing services use a wide variety of controlled vocabularies to provide subject access and other means of discovering the content of documents. The formats in which these access terms are presented vary from service to service.

21. Online indexing services and digital repositories commonly provide bibliographic information, abstracts, and full-text copies of the indexed publications, along with a list of the documents cited in the indexed publication. These services also often provide lists of publications that cite a given document. A citation of a document is evidence that the document was publicly available and in use by researchers no later than the publication date of the citing document.

D. Summary of Opinions

22. I am informed by counsel that the priority date for the patent at issue is October 23, 2000. As I will explain below, it is my opinion that the printed publication discussed in my Declaration was publicly accessible more than one year before the October 23, 2000, priority date.

IV. LIBRARY CATALOGING PRACTICES

A. MARC Records and OCLC

23. I am fully familiar with the library cataloging standard known as the MARC standard, which is an industry-wide standard method of storing and organizing library catalog information. MARC was first developed in the 1960's

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by the Library of Congress. A MARC-compatible library is one that has a catalog consisting of individual MARC records for works made available at that library.

24. Since at least the early 1970s and continuing to the present day, MARC has been the primary communications protocol for the transfer and storage of bibliographic metadata in libraries.[1] As explained by the Library of Congress:

You could devise your own method of organizing the bibliographic information, but you would be isolating your library, limiting its options, and creating much more work for yourself. Using the MARC standard prevents duplication of work and allows libraries to better share bibliographic resources. Choosing to use MARC enables libraries to acquire cataloging data that is predictable and reliable. If a library were to develop a "home-grown" system that did not use MARC records, it would not be taking advantage of an industry-wide standard whose primary purpose is to foster communication of information.

Using the MARC standard also enables libraries to make use of commercially

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[1] A complete history of the development of MARC can be found in *MARC: Its History and Implications* by Henrietta D. Avram (Washington, DC: Library of Congress, 1975) and available online from the Hathi Trust (https://babel.hathitrust.org/cgi/pt?id=mdp.39015034388556;view=1up;seq=1; last visited July 15, 2021).

available library automation systems to manage library operations. Many systems are available for libraries of all sizes and are designed to work with the MARC format. Systems are maintained and improved by the vendor so that libraries can benefit from the latest advances in computer technology. The MARC standard also allows libraries to replace one system with another with the assurance that their data will still be compatible.

Why Is a MARC Record Necessary? LIBRARY OF CONGRESS, http://www.loc.gov/marc/umb/um01to06.html#part2 (last visited July 15, 2021).

25. Thus, almost every major library in the world is MARC-compatible. *See, e.g.*, *MARC Frequently Asked Questions (FAQ)*, LIBRARY OF CONGRESS, https://www.loc.gov/marc/faq.html (last visited July 15, 2021) ("MARC is the acronym for MAchine-Readable Cataloging. It defines a data format that emerged from a Library of Congress-led initiative that began nearly fifty years ago. It provides the mechanism by which computers exchange, use, and interpret bibliographic information, and its data elements make up the foundation of most library catalogs used today."). MARC is the ANSI/NISO Z39.2-1994 standard (reaffirmed in 2016) for Information Interchange Format. The full text of the standard is available from the Library of Congress at http://www.loc.gov/marc/bibliographic/ (last visited July 15, 2021).

26. A MARC record comprises several fields, each of which contains

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specific data about the work. Each field is identified by a standardized, unique, three-digit code corresponding to the type of data that follow. *See, e.g.,* http://www.loc.gov/marc/umb/um07to10.html (last visited July 15, 2021); http://www.loc.gov/marc/bibliographic/ (last visited July 15, 2021). For example, a work's title is recorded in field 245, the primary author of the work is recorded in field 100, a work's International Standard Book Number ("ISBN") is recorded in field 020, a work's International Standard Serial Number ("ISSN") is recorded in field 022, and the publication date is recorded in field 260 under the subfield "c." *Id.*[2] If a work is a periodical, then its publication frequency is recorded in field 310, and the publication dates (e.g., the first and last publication) are recorded in field 362, which is also referred to as the enumeration/chronology field. *See* http://www.loc.gov/marc/bibliographic/bd3xx.html (last visited July 15, 2021).[3]

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[2] In some MARC records, field 264 is used rather than field 260 to record publication information. *See* http://www.loc.gov/marc/bibliographic/bd264.html (last visited July 15, 2021) ("Information in field 264 is similar to information in field 260 (Publication, Distribution, etc. (Imprint)). Field 264 is useful for cases where the content standard or institutional policies make a distinction between functions").

[3] Upwards of two-thirds to three-quarters of book sales to libraries come from a jobber or wholesaler for online and print resources. These resellers make it their

27. The library that initially created the MARC record is reflected in field 040 in subfield "a" with that library's unique library code. *See, e.g.*, http://www.loc.gov/marc/umb/um07to10.html (last visited July 15, 2021); http://www.loc.gov/marc/bibliographic/ (last visited July 15, 2021). Once a MARC record for a particular work is originally created by one library, other libraries can use that original MARC record to then create their own MARC records for their own copies of the same work. These other libraries may modify or add to the original MARC record as necessary to reflect data specific to their own copies of the work. However, the library that created the original MARC record would still be reflected in these modified MARC records (corresponding to other copies of the same work at other libraries) in field 040, subfield "a". The modifying library (or libraries) is reflected in field 040, subfield "d". *See* http://www.loc.gov/marc/bibliographic/bd040.html (last visited July 15, 2021).

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business to provide books to their customers as fast as possible, often providing turnaround times of only a single day after publication. Libraries purchase a significant portion of the balance of their books directly from publishers themselves, which provide delivery on a similarly expedited schedule. In general, libraries make these purchases throughout the year as the books are published and shelve the books as soon thereafter as possible in order to make the books available to their patrons. Thus, books are generally available at libraries across the country within just a few days of publication.

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28. I consulted the Directory of OCLC Libraries (http://www.oclc.org/contacts/libraries.en.html; last visited July 15, 2021) in order to identify the institution that created or modified the MARC record. Moreover, when viewing the MARC record online via Online Computer Library Center's ("OCLC") bibliographic database, which I discuss further below, hovering over a library code in field 040 with the mouse reveals the full name of the library. I also used this method of "mousing over" the library codes in the OCLC database to identify the originating and modifying libraries for the MARC records discussed in this report.

29. MARC records also include one or more fields that show information regarding subject matter classification. For example, 6XX fields are termed "Subject Access Fields." *See* http://www.loc.gov/marc/bibliographic/bd6xx.html (last visited July 15, 2021). Among these, for example, is the 650 field; this is the "Subject Added Entry – Topical Term" field. *See* http://www.loc.gov/marc/bibliographic/bd650.html (last visited July 15, 2021). The 650 field is a "[s]ubject added entry in which the entry element is a topical term." *Id.* These entries "are assigned to a bibliographic record to provide access according to generally accepted thesaurus-building rules (e.g., *Library of Congress Subject Headings* (LCSH), *Medical Subject Headings* (MeSH))." *Id.*

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30. Further, MARC records can include call numbers, which themselves contain a classification number. For example, a MARC record may identify a 050 field, which is the "Library of Congress Call Number." *See* http://www.loc.gov/marc/bibliographic/bd050.html (last visited July 15, 2021). A defined portion of the Library of Congress Call Number is the classification number, and "source of the classification number is *Library of Congress Classification* and the *LC Classification-Additions and Changes*." *Id.* Thus, the 050 field may be used to show information regarding subject matter classification.

31. Each item in a library has a single classification number. A library selects a classification scheme (*e.g.*, the Library of Congress Classification scheme just described or a similar scheme such as the Dewey Decimal Classification scheme) and uses it consistently. When the Library of Congress assigns the classification number, it appears as part of the 050 field, as discussed above. For MARC records created by libraries other than the Library of Congress (e.g., a university library or a local public library), the classification number may appear in a 09X (e.g., 090) field. *See* http://www.loc.gov/marc/bibliographic/bd09x.html (last visited July 15, 2021).

32. When a MARC-compatible library acquires a work, it creates a MARC record for its copy of the work in its computer catalog system in the ordinary

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course of its business. This MARC record (for the copy of a work available at the particular library) may be later accessed by researchers in a number of ways. For example, many libraries, including the Library of Congress, make their MARC records available through their website. As an example, the MARC record for the copy of *The Unlikely Spy*, by Daniel Silva,[4] available at the Library of Congress can be viewed through the Library of Congress website, at https://catalog.loc.gov/vwebv/staffView?searchId=20265&recPointer=1&recCount=25&bibId=2579985 (last visited July 15, 2021). One could, of course, always physically visit the library at which the work is available, and request to see that library's MARC record for the work. Moreover, members of the Online Computer Library Center ("OCLC") can access the MARC records of other member institutions through OCLC's online bibliographic database, as I explain further below.

33. The OCLC was created "to establish, maintain and operate a computerized library network and to promote the evolution of library use, of libraries themselves, and of librarianship, and to provide processes and products for the benefit of library users and libraries, including such objectives as increasing availability of library resources to individual library patrons and

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[4] *The Unlikely Spy* is a 1996 novel written by Daniel Silva, who happens to be one of my favorite authors.

reducing the rate of rise of library per-unit costs, all for the fundamental public purpose of furthering ease of access to and use of the ever-expanding body of worldwide scientific, literary and educational knowledge and information."[5] Among other services, OCLC and its members are responsible for maintaining the WorldCat database (http://www.worldcat.org/; last visited July 15, 2021), used by independent and institutional libraries throughout the world. All libraries that are members of OCLC are MARC-compatible. *See, e.g.*, https://help.oclc.org/Metadata_Services/OCLC-MARC_records/About_OCLC-MARC_records (last visited July 15, 2021) ("OCLC-MARC records describes records produced since November 1993."); https://www.oclc.org/support/services/worldcat/documentation/cataloging/electronicresources.en.html (last visited July 15, 2021) ("Like the two superseded OCLC documents, this revised set of guidelines is intended to assist catalogers in creating records for electronic resources in WorldCat, the OCLC Online Union Catalog. These guidelines pertain to OCLC-MARC tagging (that is, content designation). Cataloging rules and manuals (such as AACR2) govern the content

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[5] Third Article, Amended Articles of Incorporation of OCLC Online Computer Library Center, Incorporated (available at https://www.oclc.org/content/dam/oclc/membership/articles-of-incorporation.pdf; last visited July 15, 2021).

of records. You should implement these guidelines immediately.").

34. When an OCLC member institution acquires a publication, like the other MARC-compatible libraries discussed above, it creates a MARC record for this publication in its computer catalog system in the ordinary course of its business. MARC records created at the Library of Congress are tape-loaded into the OCLC database through a subscription to MARC Distribution Services daily or weekly. Once the MARC record is created by a cataloger at an OCLC member library or is tape-loaded from the Library of Congress, the MARC record is then made available to any other OCLC members online, and thereby made available to the public. Accordingly, once the MARC record is created by a cataloger at an OCLC member library or is tape-loaded from the Library of Congress, any publication corresponding to the MARC record has been cataloged and indexed according to its subject matter such that a person interested in that subject matter could, with reasonable diligence, locate and access the publication through any library with access to the OCLC bibliographic database or through the Library of Congress.

35. *Fields 008, 005, and 955 in MARC Records as Indicators of Public Accessibility.* When a MARC-compatible library creates an original MARC record for a work, the library records the date of creation of that MARC record in **field 008**, characters 00 through 05, in the ordinary course of its business. *See*

http://www.loc.gov/marc/bibliographic/bd008a.html (last visited July 15, 2021).

For OCLC member institutions that use OCLC software to create original MARC records, the date of creation in field 008 is automatically supplied by the OCLC software. The MARC record creation date in field 008 thus reflects the date on which, or shortly after which, a work was first acquired and cataloged by the library that created the original MARC record.

36. When other MARC-compatible libraries subsequently acquire their own copies of the same work, as mentioned, they create MARC records in their own computer catalog systems for their copies in the ordinary course of business.[6] They may use a MARC record previously created for that work (by another MARC-compatible library) to create their own MARC records for their own copies of that same work.[7] The previously created MARC record used by subsequently-acquiring libraries to create MARC records for their own copies may be obtained through the OCLC bibliographic database, as described above. If, when creating a MARC record to represent its own copy of the work, the

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[6] Initial contributions to the bibliographic database for a work are called "master records."

[7] When a local library uses a master record in OCLC and produces (or downloads) it to the in-house system, the three-character symbol for the subsequent library is added to the holdings for the work.

subsequently-acquiring library uses the master MARC record in its original form, the subsequently-acquiring library cannot reenter data into the 008 field; therefore, the date in the 008 field will continue to reflect the date the MARC record was initially created by the originating library. On the other hand, if the subsequently-acquiring library modifies the previously created MARC record when creating its own MARC record for its own copy of the work, the subsequently-acquiring library may enter into the 008 field of its own MARC record the date its own MARC record was created.[8] But the library that created the original MARC record used by the subsequently-acquiring library would still be reflected in the MARC record of the subsequently-acquiring library in field 040, subfield "a". Thus, the work identified by any MARC record possessed by any MARC-compatible library would have been accessible to the public <u>at least</u> as of the date shown in the 008 field, or shortly thereafter, either from the library that possesses the MARC record itself, or from the originating library indicated in field 040, subfield "a". As discussed, a MARC-compatible library in the

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[8] This practice is not required by, but is nevertheless consistent with, the MARC standard. Many MARC records exist today whose 008 fields indicate when the first original MARC record for a work was created, rather than when a derivative record was created based on the original MARC record by a subsequently-acquiring library for its own computer catalog system.

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ordinary course of its business creates a MARC record in its own catalog system for a work when it acquires a copy of that work.

37. Moreover, when a MARC record is created by a library for its own copy of a work, **field 005** is automatically populated with the date that MARC record was created in year, month, day format (YYYYMMDD). *See* http://www.loc.gov/marc/bibliographic/bd005.html (last visited July 15, 2021).[9] Thereafter, the library's computer system may automatically update the date in field 005 every time the library updates the MARC record (*e.g.*, to reflect that an item has been moved to a different shelving location within the library). *Id.*[10] Thus, the work identified by any MARC record possessed by any MARC-compatible library would have been accessible to the public <u>at least</u> as of the date shown in the 005 field, or shortly thereafter, from the library that possesses the MARC record itself. As noted, because the 005 field may be updated each time the library updates its MARC record, the work identified by the MARC record may, in fact, have been accessible to the public from that library much earlier

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[9] Some of the newer library catalog systems also include hour, minute, second (HHMMSS).

[10] Field 005 is visible when viewing a MARC record via an appropriate computerized interface. But when a MARC record is printed directly to hardcopy from the OCLC database, the "005" label is not shown. The date in the 005 field instead appears next to the label "Replaced."

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than the date indicated in the 005 field.

38.Moreover, MARC records for copies of works available at the Library of Congress can have a **955 field**. *See* http://www.loc.gov/cds/PDFdownloads/dcm/DCM_2007-03.pdf (last visited July 15, 2021). The 955 field in MARC records obtained from the Library of Congress provides Local Tracking Information, which is a record of internal steps in the cataloging process followed by the Library of Congress. *Id.* Entries in the 955 field for a particular work are generated by Library of Congress staff as the work progresses through the cataloging process. *Id.* One of the mandatory fields that library staff must enter for each step is the date (in the form of "yyyy-mm-dd" or "yy-mm-dd") the step was taken. *Id.* Thus, the work identified by a MARC record possessed by the Library of Congress would have been accessible to the public <u>at least</u> as of the earliest date shown in the 955 field, or shortly thereafter, from the Library of Congress.

39.Based on my personal experience as a professional librarian using the MARC and OCLC resources, it has been my experience that both of these resources were continuously operational and available since at least 1992. Indeed, in the course of my work, I have extensively used both of these resources over the past 30+ years, and I have consistently found the information contained within these resources to be complete and reliable. I have never found the date

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of accessibility as indicated in fields 008, 005, or 955 to be incorrect. And in only a minute number of cases have I found any errors at all in these records – none of which affected my ability to render an accurate opinion as to accessibility, indexing, or subject headings.

V. PUBLICATIONS IN THIS PROCEEDING

A. *1990 Single-Chip Microcontroller Data Book* [Exhibit 1005]

40. Exhibit 1005 attached to my Declaration is a copy of a book titled *1990 Single-Chip Microcontroller Data Book* prepared and issued by NEC Electronics, Inc. in 1990. Exhibit 1005 is a true and correct copy of the entire book as held by the University of Alberta Libraries (Edmonton, Alberta, Canada). The entire book can be downloaded from the Internet.[11] The text in Exhibit 1005 is complete; no pages are missing, and the text on each page appears to flow seamlessly from one page to the next; further, there are no visible alterations to the document. Exhibit 1005 is a true and correct copy in a condition that creates no suspicion about its authenticity.

41. Attached hereto as Attachment 1a is a true and correct copy of the MARC record for this monograph from the University of Alberta Libraries online

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https://archive.org/details/bitsavers_necdatabooMicrocontrollerDataBook_571183 08/page/n285/mode/2up

catalog. The library ownership is indicated by the presence of the library's code (AEU) in the 049 field. The library continues to update this MARC record and enhanced the MARC record to meet current cataloging rules. I personally identified and retrieved the library catalog record which is Attachment 1a.

42. Based on finding a print copy of the *1990 Single-Chip Microcontroller Data Book* in the University of Alberta Libraries and MARC record in its online library catalog attached as Attachment 1a, it is my opinion that the book was publicly available on or shortly after October 29, 1992, as shown in field 008 ("921029").

43. Attached hereto as Attachment 1b is a true and correct copy of the MARC record for the *1990 Single-Chip Microcontroller Data Book* obtained from the OCLC bibliographic database. I personally identified and retrieved the MARC record that is Attachment 1b. As previously noted, the library that created the record is recorded in field 040 with a unique library code. For Attachment 1b, that library code is "PNX," which means that the MARC record for this book was created at the Phoenix Public Library (Phoenix, Arizona). As can be seen in the "Entered" field in the MARC record for this exhibit, a cataloger at the Phoenix Public Library created OCLC record number 32402931 on May 1, 1995, as shown in the "Entered" field ("19950501"). The library continues to update and enhance this MARC record to meet current cataloging rules. The most recent

enhancement to Attachment 1b occurred on June 1, 2018, as shown in the "Replaced" field ("20180601"). I personally identified and retrieved the MARC record that is Attachment 1b.

44. Attachment 1b further includes an entry in field 050 ("TK7874.5 $b .N42 1990")—as described above, this includes a subject matter classification number consistent with the Library of Congress classification system (analogous to the Dewey Decimal classification system). Attachment 1b further includes an entry in field 082 ("621.3916 $b N364n"), a subject matter consistent with the Dewey Decimal classification system. Attachment 1b further includes three descriptor terms reading "Microcomputers $v Catalogs" (see Attachment 1c, Library of Congress subject heading sh2010101665), "Integrated circuits $v Catalogs" (see Attachment 1d, Library of Congress subject heading sh2008123900), and "Microprocessors $v Catalogs" (see Attachment 1e, Library of Congress subject heading sh85084898 and Attachment 1f, Library of Congress subject heading sh85020898) in the 650 fields. Thus, as of its cataloging, the publication corresponding to the MARC record attached hereto as Attachment 1b was indexed according to its subject matter by virtue of at least three independently sufficient classifications: the field 050 entry, the field 082 entry, and the field 650 entries. Further, as of May 1, 1995, the MARC record attached hereto as Attachment 1b was accessible through any library with access to the

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OCLC bibliographic database or the online catalog at a library that added this book to its collection, which means that the corresponding publication was publicly available on or before that same date through any library with access to the OCLC bibliographic database or through an individual library.

45.Attachment 1b indicates that the *1990 Single-Chip Microcontroller Data Book* as cataloged at the Phoenix Public Library is currently available from 2 libraries. In view of above, the *1990 Single-Chip Microcontroller Data Book* was publicly available on or shortly after October 24, 1992, because by that date it had been received, cataloged, and indexed at the University of Alberta Libraries. For these reasons, it is my opinion that Exhibit 1005 was published and accessible to the public on or shortly after October 24, 1992.

B.   Burd conference paper (Exhibit 1006)

46.Attached hereto as Exhibit 1006 is a true and correct copy of the conference paper titled "A Dynamic Voltage Scaled Microprocessor System" by Thomas D. Burd, Trevor A. Pering, Anthony J. Stratakos, and Robert W. Brodersen (hereafter "Burd"). The Burd conference paper was published in the *Digest of Technical Papers: 2000 IEEE International Solid-State Circuits Conference* with a 2000 copyright date that can be found in the Linda Hall Library (Kansas City, Missouri). The 2000 IEEE International Solid-State Circuits Conference as held February 7-9, 2000, in San Francisco, California.

The Burd conference paper is also available from the *IEEE Xplore* database.[12] I obtained this conference paper from the *IEEE Xplore* database through the King Library at San Jose State University and Exhibit 1006 is a copy. Specifically, the text is complete; no pages are missing, and the text on each page appears to flow seamlessly from one page to the next; further, there are no visible alterations to the document. Exhibit 1006 can be found within the custody of a library – a place where, if authentic, a copy of this conference paper would likely be. Exhibit 1006 is a true and correct copy in a condition that creates no suspicion about its authenticity.

47. Attached hereto as Attachment 2a is a true and correct copy of the MARC record for the *Digest of Technical Papers: 2000 IEEE International Solid-State Circuits Conference* in the Linda Hall Library. The library ownership is indicated by the presence of the library's code (LHL) in the 049 field. I personally identified and retrieved the MARC record that is Attachment 2a.

48. The MARC record for the *Digest of Technical Papers: 2000 IEEE International Solid-State Circuits Conference* shows that it was cataloged in the Linda Hall Library on April 24, 2000, as shown in field 008 ("000424") and contributed to the OCLC bibliographic database. The most recent enhancement

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[12] https://ieeexplore-ieee-org.libaccess.sjlibrary.org/document/839787

to Attachment 2a occurred on January 17, 2002, as shown in field 005 ("200020117"). Therefore, this volume would have been available to users in the Linda Hall Library on or shortly after April 24, 2000.

49. Attached hereto as Attachment 2b is a true and correct copy of the MARC record for the *Digest of Technical Papers: 2000 IEEE International Solid-State Circuits Conference* obtained from the OCLC bibliographic database. I personally identified and retrieved the MARC record that is Attachment 2b. As previously noted, the library that created the record is recorded in field 040 with a unique library code. For Attachment 2b, that library code is "LHL," which means that the MARC record for this volume was created at the Linda Hall Library. As can be seen in the "Entered" field in the MARC record for this exhibit, a cataloger at the Linda Hall Library created OCLC record number 43917176 on April 24, 2000 and contributed it to the OCLC bibliographic database.

50. Attachment 2b further includes an entry in field 050 ("TK7870 $b .I64 2000")—as described above, this includes a subject matter classification number consistent with the Library of Congress classification system. Attachment 2b further includes three descriptor terms reading "Electronic circuits systems $v Congresses" (see Attachment 2c, Library of Congress subject heading sh2008102920), "Solid state electronics $v Congresses" (see Attachment 2d,

Library of Congress subject heading sh2008111513), and "Semiconductors $v Congresses" (see Attachment 2e, Library of Congress subject heading sh2008111509) in the 650 fields. Thus, as of its cataloging, the publication corresponding to the MARC record attached hereto as Attachment 2b was indexed according to its subject matter by virtue of at least three independently sufficient classifications: the field 050 field entry, the field 082 entry, and the field 650 entries. Further, as of April 24, 2000, the MARC record attached hereto as Attachment 2b was accessible through any library with access to the OCLC bibliographic database or the online catalog at a library that added this conference proceedings volume to its collection, which means that the corresponding publication was publicly available on or before that same date through any library with access to the OCLC bibliographic database or through an individual library.

51. Attachment 2b indicates that the conference proceedings volume *Digest of Technical Papers: 2000 IEEE International Solid-State Circuits Conference* as cataloged at the Linda Hall Library is currently available from 35 libraries. In view of above, the conference proceedings volume *Digest of Technical Papers: 2000 IEEE International Solid-State Circuits Conference* was publicly available on or shortly after April 24, 2000, because by that date it had been received, cataloged, and available at the Linda Hall Library and made part of the OCLC bibliographic database. For these reasons, it is my opinion that Exhibit 1006 was

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published and accessible to the public on or shortly after April 24, 2000.

C. ***High-Efficiency, PWM, Step-Down DC-DC Controllers in 16-Pin QSOP (Exhibit 1011)***

52. Exhibit 1011 attached to my Declaration is a copy of a document titled *High-Efficiency, PWM, Step-Down DC-DC Controllers in 16-Pin QSOP* (hereafter "Maxim High efficiency") prepared and issued by Maxim Integrated Products in July 1998. Exhibit 101 is a true and correct copy of the entire document that can be downloaded from the Internet.[13] The text in Exhibit 1011 is complete; no pages are missing, and the text on each page appears to flow seamlessly from one page to the next; further, there are no visible alterations to the document. Exhibit 1011 is a true and correct copy in a condition that creates no suspicion about its authenticity.

53. The *High-Efficiency, PWM, Step-Down DC-DC Controllers in 16-Pin QSOP* is identified as Revision 1 of document 19-1357 and has a July 1998 date. I obtained the document filed as Exhibit 1011 from the Internet.[14]

54. Exhibit 1011 is a true and correct copy in a condition that creates no suspicion about its authenticity. Based on the date recorded in the document, it is my opinion that the *High-Efficiency, PWM, Step-Down DC-DC Controllers in 16-Pin QSOP* document was available to the public on July 31, 1998, or shortly

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[13] https://datasheets.maximintegrated.com/en/ds/MAX1652-MAX1655.pdf

[14] *Ibid.*

thereafter.

D. *MAX1711 Voltage Positioning Evaluation Kit* **(Exhibit 1012)**

55.Exhibit 1012 attached to my Declaration is a copy of a document titled *MAX1711 Voltage Positioning Evaluation Kit* (hereafter "MAX1711") prepared and issued by Maxim Integrated Products in November 1999. Exhibit 1012 is a true and correct copy of the entire document that can be downloaded from the Internet.[15] The text in Exhibit 1012 is complete; no pages are missing, and the text on each page appears to flow seamlessly from one page to the next; further, there are no visible alterations to the document. Exhibit 1012 is a true and correct copy in a condition that creates no suspicion about its authenticity.

56.The *MAX1711 Voltage Positioning Evaluation Kit* is identified as Revision 0 of document 19-1647 and has a November 1999 date. I obtained the document filed as Exhibit 1012 from the Internet.[16]

57.Exhibit 1012 is a true and correct copy in a condition that creates no suspicion about its authenticity. Based on the date recorded in the document, it is my opinion that the *MAX1711 Voltage Positioning Evaluation Kit* document was available to the public on November 30, 1999, or shortly thereafter.

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[15] https://pdfserv.maximintegrated.com/en/ds/2191.pdf

[16] *Ibid.*

ACTIVE/111989782.1

E.   *Electric Circuits,* 4th edition (Exhibit 1013)

58.Exhibit 1013 attached to my Declaration is a copy of a book titled *Electric Circuits*, 4th edition, by James W. Nilsson issued by Addison-Wesley in 1993.   Exhibit 1013 is a true and correct copy of the entire book as held by the University of Wisconsin Libraries (Madison, Wisconsin).   The text in Exhibit 1013 is complete; no pages are missing, and the text on each page appears to flow seamlessly from one page to the next; further, there are no visible alterations to the document.   Exhibit 1013 is a true and correct copy in a condition that creates no suspicion about its authenticity.

59.Attached hereto as Attachment 3a is a true and correct copy of the MARC record for this monograph from the University of Wisconsin Libraries online catalog. The library ownership is indicated by the presence of the library's code (GZZ) in the 049 field. The library continues to update this MARC record and enhanced the MARC record to meet current cataloging rules. I personally identified and retrieved the library catalog record which is Attachment 3a.

60.Based on finding a print copy of the book titled *Electric Circuits*, 4th edition, in the University of Wisconsin Libraries and MARC record in its online library catalog attached as Attachment 3a, it is my opinion that the book was publicly available on or shortly after July 20, 1992, as shown in field 008 ("920720").

61. Attached hereto as Attachment 3b is a true and correct copy of the MARC record for the book titled *Electric Circuits*, 4th edition, obtained from the OCLC bibliographic database. I personally identified and retrieved the MARC record that is Attachment 3b. As previously noted, the library that created the record is recorded in field 040 with a unique library code. For Attachment 3b, that library code is "DLC," which means that the MARC record for this book was created at the Library of Congress. As can be seen in the "Entered" field in the MARC record for this exhibit, a cataloger at the Library of Congress created OCLC record number 26361995 on July 20, 1992, as shown in the "Entered" field ("19920720"). The library continues to update and enhance this MARC record to meet current cataloging rules. The most recent enhancement to Attachment 3b occurred on June 13, 2020, as shown in the "Replaced" field ("20200613"). I personally identified and retrieved the MARC record that is Attachment 3b.

62. Attachment 3b further includes an entry in field 050 ("TK454 $b .N54 1993")—as described above, this includes a subject matter classification number consistent with the Library of Congress classification system (analogous to the Dewey Decimal classification system). Attachment 3b further includes an entry in field 082 ("621.391/2"), a subject matter consistent with the Dewey Decimal classification system. Attachment 3b further includes a descriptor term reading

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"Electric circuits" (see Attachment 3c, Library of Congress subject heading sh85042279) in the 650 field. Thus, as of its cataloging, the publication corresponding to the MARC record attached hereto as Attachment 3b was indexed according to its subject matter by virtue of at least three independently sufficient classifications: the field 050 entry, the field 082 entry, and the field 650 entry. Further, as of July 20, 1992, the MARC record attached hereto as Attachment 3b was accessible through any library with access to the OCLC bibliographic database or the online catalog at a library that added this book to its collection, which means that the corresponding publication was publicly available on or before that same date through any library with access to the OCLC bibliographic database or through an individual library.

63. Attachment 3b indicates that the book titled *Electric Circuits*, 4th edition, as cataloged at the Library of Congress is currently available from 209 libraries. In view of above, the book titles *Electric Circuits*, 4th edition, was publicly available on or shortly after July 20, 1992, because by that date it had been received, cataloged, and indexed at the University of Wisconsin Libraries. For these reasons, it is my opinion that Exhibit 1013 was published and accessible to the public on or shortly after July 20, 1992.

VI. CONCLUSION

64. In signing this Declaration, I recognize that the Declaration will be filed

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as evidence in a case before the Patent Trial and Appeal Board of the United States Patent and Trademark Office. I also recognize that I may be subject to cross-examination in the case and that cross-examination will take place within the United States. If cross-examination is required of me, I will appear for cross-examination within the United States during the time allotted for cross-examination.

65. I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true, and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code.

Dated: September ___14___, 2021

Respectfully submitted,

Sylvia D. Hall-Ellis

Sylvia D. Hall-Ellis, Ph.D.

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EXHIBIT A

CURRICULUM VITAE
SYLVIA D. HALL-ELLIS

EDUCATION

Ph.D., University of Pittsburgh, Pittsburgh, Pennsylvania, 1985
M.P.S., University of Denver, Denver, Colorado, 2014
Post Graduate Studies, University of Texas – San Antonio, Texas, 1975-1976
M.L.S., University of North Texas, Denton, Texas, 1972
B.A., Rockford University, Rockford, Illinois, 1971

PROFESSIONAL EXPERIENCE

1981-	**Consultant for higher education, non-profit organizations, and corporations.**
2002-	**Adjunct Professor, School of Information, San José State University, San José, California.** Serve as part-time faculty member teaching graduate students in technical services (cataloging, bibliographic control, classification), "core courses," and special topics.
2014-2016	**Director, Grants and Resource Development, Colorado Community College System.** Provided leadership and vision to foster the continued growth of rigorous scholarship, innovative projects, and creative work for statewide system, 13 campuses, and 50 teaching sites serving 155,000 students. Responsible for leadership and ensured efficient functioning of contract and grants in compliance with state & federal requirements and successful implementation and management. Served as a subject matter expert and liaison for college Grant Directors for all issues relating to grants and subcontracts.
2010-2014	**Senior Grant Administrator, Morgridge College of Education, University of Denver (Colorado).** Provided leadership and vision to foster continued growth of rigorous scholarship, innovative research, and creative work in the Morgridge College of Education. Ensure that contract and grants processes function effectively and efficiently for 60 faculty and researchers with a focus on the successful progression and efficient management of grants totaling $13M. Worked effectively and collegially with Department Chairs and Program Coordinators on operational grant-related management activities and with a broad range of internal and external constituencies. Supported the dissemination and promotion of faculty research and scholarship to outside constituents at conferences and through publications. Assisted Principal Investigators and grant project teams by coaching, mentoring, and financial management.
2011-2013	**Interim Director & Assistant Dean, Westminster Law Library, Sturm College of Law, University of Denver.** Planned, organized, and directed all administrative activities for the library serving students, faculty, and alumni; oversaw the employment, retention, promotion, transfer and termination of library personnel; represented the library at professional conferences and public meetings; created and promoted a climate and culture of acceptance for new programs and services, a positive high-quality image of the law library, and that reflect the organization's values, encourage excellent performance, and reward high productivity and innovation; provided leadership and set strategic direction of the organization; ensured that the library provided excellent customer service through solution-oriented staff response to patron needs and by responsiveness and continuous improvement of the organization; promoted, developed, and maintained positive working relationships with colleagues and customers including key stakeholders and groups, higher education institutions, the legal community, other regional libraries and districts statewide, and national library organizations.
2007-2014	**Associate Professor, Library & Information Science, Morgridge College of Education, University of Denver (Colorado).** Served in leadership role and worked collaboratively in program, college, campus and community environments. Advised and supervised students, taught core and specialized courses at the graduate level in an integrative, student-centered learning environment. Served on LIS, College, and University committees, and maintained

working relationships with colleagues in other academic units and information professionals in the Rocky Mountain region and beyond. Served on and chair doctoral student dissertation committees. Oversaw and facilitated the College and LIS graduate student association.

2002-2007   **Assistant Professor, Library & Information Science, College of Education, University of Denver (Colorado).** Served as tenure-track faculty member teaching graduate students in "core courses," resource description and access, service learning, and independent studies. Advised graduate students, participate on LIS and College committees, and serve on doctoral student dissertation committees. Oversaw and facilitated the LIS graduate student association and alumni association.

2000-2002   **Affiliate Faculty, Library & Information Science, College of Education, University of Denver (Colorado).** Served as part-time faculty member teaching graduate students in technical services (cataloging, bibliographic control, classification), "core courses," and special topics. Oversaw and facilitated the LIS graduate student association and alumni association.

2000-2001   **Special Assistant to the Secretary's Regional Representative, U.S. Department of Education, Region VIII, Denver, Colorado.** Served as the principal advisor and representative of the U. S. Secretary of Education's Regional Representative (SRR). Ensured the implementation of major goals of the SRR and the Secretary. Provided leadership on behalf of the SRR in contacts with high-level officials in Region VIII requiring sensitive policy interpretation in communication with senior Department officials to solve problems and resolve issues raised by State and local education officials. Served as the primary contact for School-to-Work/Career, Children's Health Insurance Program, and Safe and Drug-Free Schools. Delivered technical assistance to local education agencies and institutions of higher education in technology, professional development, and school construction.

1999-2000   **Catalog Librarian, Jefferson County Public Library, Lakewood, Colorado.** Performed original, copy cataloging and classification of library materials (English and Spanish) using standard library protocols; completed original descriptive cataloging and subject analysis; enhanced brief catalog and authority records in III.

1997-1999   **Development Officer, McREL International, Aurora, Colorado.** Served as senior member of corporate management team in strategic planning, development of proposals and contracts, implementation, and evaluation of new services, products, and programs for educational agencies. Provided creative leadership to corporate committees to solicit ideas, identify goals and objectives, plan, develop, present, and evaluate professional development opportunities.

1995-1997   **Education Specialist, Education Service Center, Region One, Edinburg, Texas.** Served as member of Administrative Cabinet team in strategic planning, development of proposals and contracts, implementation, and evaluation of telecommunications capabilities, services, products, and programs for 40 school districts serving 283,000 students in 7 counties. Provided creative leadership to regional and state committees to solicit ideas, identify strategic goals and objectives, plan, develop, present, and evaluate funding opportunities and professional development for 400 librarians.

1993-1996   **Assistant Professor of Library Science, Sam Houston State University, Huntsville, Texas.** Served a faculty member teaching 400 graduate students in technical services (cataloging, bibliographic control, classification), automation, and networking. Participated in distance education program and coordinated annual conference. Conducted university and Texas Library Association-funded field research focused on library collection development and academic achievement.

1992-1993 **Head Librarian, Rocky Mountain College of Art & Design, Denver, Colorado.** Responsible for the daily operation, selection and acquisition of materials, formulation of policies for library operations, media center, and photography/slides archives. Designed and implemented library automation and delivery of electronic resources to college community.

1981-1985 **Development Officer, PRLC, Inc., Pittsburgh, Pennsylvania.** Served as senior member of corporate management team in strategic planning, development of proposals and contracts, implementation, and evaluation of new services, products, and programs for 100 institutional member organizations. Coordinated the development of proposals and contracts totaling $4,000,000 annually. Provided creative leadership to corporate committees to solicit ideas, identify goals and objectives, plan, develop, present, and evaluate professional development opportunities.

1981 **Director of Library Development, Pennsylvania Department of Education, Harrisburg, Pennsylvania.** Responsible for statewide development, technical assistance, professional development, resource sharing, children's services, institutional library services, networking, and state aid program for all libraries throughout the Commonwealth. Functioned as liaison to Governor's Advisory Council, LSCA Advisory Council, District Administrators, private colleges, universities, consortia managers, and network directors. Supervised $14,000,000 formula-based state aid program and $3,000,000 grant awards to individual libraries, consortia, and networks.

1978-1981 **Assistant Director, Southern Tier Library System, Corning, New York.** Coordinated operation of system-wide programs (technical assistance, professional development, resource sharing, technical services, outreach) to 40 public libraries in 5 counties serving 500,000 residents. Solicited ideas, identified goals, sponsored, and evaluated professional development opportunities and technical assistance sessions.

1976-1978 **Division Librarian for Technical Services, Corpus Christi Public Libraries, Corpus Christi, Texas.** Provided leadership in acquisitions, cataloging, serials control, and processing for main library and 4 branches serving 250,000 residents. Participated as senior member of library management team. Compiled and prepared technical evaluations, reports, and statistical analyses of Division operations to measure the achievement and cost of annual goals, objectives, and staff performance.

1975-1976 **System Coordinator, San Antonio Major Resource Center, San Antonio, Texas.** Served as senior member of the management team for District X Office, charged to provide technical assistance, resource sharing, media services, and professional development to librarians and staff representing 30 public library jurisdictions in 21 counties serving 1,500,000 residents. Functioned as liaison to System Director, staff, and members of governing bodies with the System Board of Directors and the Texas State Library and Historical Commission. Prepared LSCA grant applications and monitored awards totaling $1,100,000 annually.

1973-1975 **Bilingual Branch Librarian, San Antonio Public Library, San Antonio, Texas.** Worked as librarian providing reference, information, and readers' advisory services in branch serving 50,000 Spanish-speaking residents in southwest San Antonio. Participated in collection development and resource acquisition activities, specializing in children's work, Spanish language resources, and multicultural studies.

1972-1973 **Librarian, Holding Institute, Laredo, Texas.** Worked as high school librarian serving 500 boarding students in Spanish-speaking environment of private school. Provided reference, research assistance, and library instruction to students and 35 faculty members.

1966-1971 **Rockford Public Library, Rockford, Illinois.** Worked in branches as part-time as a Library Assistant, Clerk, and Page in city library serving 150,000 residents.

PUBLICATIONS

Editor-reviewed Monographs (Completed and in Progress)

Hall-Ellis, Sylvia D., and Mary Beth Weber. *Contemporary Cataloging in an RDA Environment: A Handbook for Students and Practitioners.* Chicago, IL: American Library Association. Under contract & In development.

RDA Testing: Lessons Learned and Challenges Revealed. Sylvia D. Hall-Ellis and Robert O. Ellett, Jr., eds. Binghamton, N.Y.: Haworth, 2012. 128 p.

Hall-Ellis, Sylvia D., Stacey L. Bowers, Christopher D. Hudson, and M. Claire Williamson. *Librarian's Handbook for Seeking, Writing, and Managing Grants.* Santa Barbara, Calif.: Libraries Unlimited, 2011. 315 p.

Hall-Ellis, Sylvia D., with Ann Jerabek, and Merrie W. Valliant. *Contemporary Cataloging: A Handbook for Practitioners and Students.* Open access text. Athens, GA: University of Georgia System Regents, 2011. 767 p.

Grealy, Deborah S. and Sylvia D. Hall-Ellis. *From Research to Practice: The Scholarship of Teaching and Learning in LIS Education.* Westport, Conn.: Libraries Unlimited, 2009. 175 p.

Hall-Ellis, Sylvia D. with J. Ann Jerabek. *Grants for School Libraries.* Westport, Conn.: Libraries Unlimited, 2003. 197 p.

Hall-Ellis, Sylvia D., Doris Meyer, Frank W. Hoffmann, with J. Ann Jerabek. *Grant Writing for Small Libraries and School Library Media Centers.* Boulder, Colo.: NetLibrary, 2001. 173 p.

Hall-Ellis, Sylvia D., Doris Meyer, Frank W. Hoffmann, with J. Ann Jerabek. *Grant Writing for Small Libraries and School Library Media Centers.* Englewood, Colo: Libraries Unlimited, 2000. 173 p.

Editor-reviewed Chapters (Completed and In Progress)

Hall-Ellis, Sylvia D. "Prepared to Lead: Talent, Skills, and Competencies." In *Telling the Technical Services Story*. Chicago, IL: American Library Association, 2020. In development and review.

Hall-Ellis, Sylvia D. "Grant Writing and Sponsored Research Funding for Academic Librarians." In *The New Librarianship.* Vol. 4. Bradford Lee Eden, ed. New York: Scarecrow Press, 2015. (pp. 163-174)

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Hall-Ellis, Sylvia D. "Applying for Grants from Foundations, Corporations, or Government." In *The Volunteers' Guide to Fundraising: Raise Money for Your School Team, Library or Community Group.* 1st ed. Ilona M. Bray, ed. Berkeley, Calif.: Nolo, 2011. (pp. 1-38 on accompanying disc)

Hall-Ellis, Sylvia D., ed. "Standard III: The Faculty." In the *Library and Information Science Program Self-Study Document for Accreditation by the American Library Association.* Denver, Colo.: University of Denver, Morgridge College of Education, 2010. 22 p.

Hall-Ellis, Sylvia D. "Library and Information Science Programs and Education for Catalogers and Metadata Specialists: Challenges for the Twenty-first Century." In *Conversations with Catalogers in the Twenty-First Century.* Elaine R. Sanchez, ed. Santa Barbara, Calif.: ABC-Clio, 2010. (pp. 226-254)

Hall-Ellis, Sylvia D., ed. "Standard III: The Faculty." In the *Library and Information Science Program Self-Study Document for Accreditation by the American Library Association.* Denver, Colo.: University of Denver, College of Education, 2003. 15 p.

Lesesne, Teri S. and Sylvia D. Hall-Ellis. "The Selection, Evaluation, and Integration of Culturally Authentic Texts: A Case for Making the Online Catalog Reflect Parallel Cultures." In *Literacy: Traditional, Cultural, Technological.* Pittsburgh, Pa.: International Association of School Librarianship, 1995. (pp. 110-113)

Lesesne, Teri S. and Sylvia D. Hall-Ellis. *The Selection, Evaluation, and Integration of Culturally Authentic Texts: A Case for Making the Online Catalog Reflect Parallel Cultures.* In *Conference Proceedings* of the 23rd Annual International Association of School Librarianship, Pittsburgh, Pennsylvania, July 17-22, 1994. ERIC Document ED374816. 17 p.

Hall-Ellis, Sylvia D. "Curriculum Folio for School Library Media Specialist Programs." In the *National Council for Accreditation of Teacher Education Self-Study for Sam Houston State University.* Huntsville, Tex.: Sam Houston State University, College of Education and Applied Science, 1994. 25 p.

Bruntjen, Scott and Sylvia D. Hall. "Attempting to Automate: Lessons Learned Over Five Years." In *Advances in Library Administration*. Volume 4. Weston, Conn.: JAI Press, 1985. (pp. 177-192)

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Hall-Ellis-Sylvia D. "Job Design for Cataloging and Metadata Librarians." Submitted to *Journal of Library Administration.* In progress.

Hall-Ellis, Sylvia D. "The Relationship of Situational Leadership and the Dreyfus Model of Skill Acquisition for Supervisors in Cataloging and Metadata Services." To be submitted to *Library Resources and Technical Services.* In progress.

Hall-Ellis, Sylvia D. *The Relationship of Core Competencies on Learning Outcomes and Employers' Expectations for Catalog Librarians and Metadata Specialists.* To be submitted to the *Journal of Education for Library and Information Science.* In progress.

Hall-Ellis, Sylvia D. "Building Cataloger Competencies: The Dreyfus Model as a Prototype for the Education and Professional Development of Catalog Librarians and Metadata Specialists in Bibliographic Control." To be submitted to the *Cataloging & Classification Quarterly.* In progress.

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Hall-Ellis, Sylvia D. "Succession Planning and Staff Development – A Winning Combination." *The Bottom Line 28*, no. 3 (May 2015): 95-98.

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Hall-Ellis, Sylvia D. "Onboarding to Improve Library Retention and Productivity." *The Bottom Line 27*, no. 4 (October 2014).

Hall-Ellis, Sylvia D. "Accept, Coach, and Inspire: A Formula for Success." *The Bottom Line 27*, no. 3 (July 2014): 103-106.

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Hall-Ellis, Sylvia D. "Investment in Staff Development for Seeking External Grant Funds." *The Bottom Line 27*, no. 1 (January 2014): 22-25.

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Hall-Ellis, Sylvia D. "Language Proficiencies among Catalogers and Technical Services Librarians." *Technical Services Quarterly* 25, no. 2 (2007) 31-47. http://tsq.haworthpress.com/doi:10.1300/J124v25n02_03

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Hall-Ellis, Sylvia D. *Grant Writing Tips and Resources.* Denver, Colo.: University of Denver, 2008-2014. http://portfolio.du.edu/grants

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Hall-Ellis, Sylvia D. *Strategic Plan for Denver Medical Library System: Final Report.* Denver, Colo.: HealthONE and Denver Medical Library, 2008.

Hall-Ellis, Sylvia D. and Duan Zhang. *Project Homeless Connect 5 Event Evaluation.* Denver, Colo.: Center for Community Engagement and Service Learning, 2008.

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Hall-Ellis, Sylvia D. and Duan Zhang. *Project Homeless Connect 4 Event Evaluation.* Denver, Colo.: Center for Community Engagement and Service Learning, 2007.

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Hall-Ellis, Sylvia D. *Planning for Educational Technology: the Distance Education Implementation Phase: An Investigation of Technology and Telecommunication Needs for Region One Education Service Center, South Texas Community College, TCI Cablevision of South Texas, Inc., Tech Prep of the Rio Grande Valley, Inc., Texas State Technical College, Centro Cultural en el Valle de Texas, McAllen Independent School District, Harlingen Consolidated Independent School District, Donna Independent School District, Edinburg Consolidated Independent School District, La Joya Independent School District, Mercedes Independent School District, Pharr-San Juan-Alamo Independent School District, Sharyland Independent School District, Easter Seal Society of the Rio Grande Valley, Inc., and McAllen Memorial Library.* Harlingen, Tex.: Tech Prep of the Rio Grande Valley, 1996.

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Hall-Ellis, Sylvia D. *[et. al.] Planning for Educational Technology: A Study of Future Technology Needs for the Donna Independent School District, Region One Education Region Service Center, Tech Prep of the Rio Grande Valley, Inc. South Texas Community College, and the Department of Library Science, Sam Houston State University.* Research team: Sylvia D. Hall-Ellis, Ruth Ann Riggins, Noe Torres, Patricia G. Bubb, and Michael D. Bell. Harlingen, Tex.: Tech Prep of the Rio Grande Valley, 1994. Funded through a grant award from the Texas Education Agency.

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Hall-Ellis, Sylvia D. and Clarence L. Coffindaffer. *Montana Federation Study Identification Paper*. Denver, Colo.: The Blue Bear Group, Inc., 1992.

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Hall, Sylvia D. *Iowa Computer-Assisted Network (ICAN Users' Manual. IBM Compatible Edition: Version 7.0.* Des Moines, Ia.: State Library of Iowa, 1988.

Hall, Sylvia D. *Iowa Computer-Assisted Network (ICAN Users' Manual. IBM Compatible Edition: Version 5.0.* Des Moines, Ia.: State Library of Iowa, 1986.

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Bruntjen, Scott and Sylvia D. Hall. *The Iowa Locator: Final Report.* Central City, Colo.: The Blue Bear Group, Inc., 1986.

Bruntjen, Scott and Sylvia D. Hall. *Discovering Resource Sharing Treasures: Accessing Pennsylvania's High School Library Collections*. Harrisburg, Pa.: State Library of Pennsylvania, Bureau of School Library Media Resources, 1985.

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Frugal Librarian. Carol Smallwood, ed. Chicago, IL: American Library Association, 2011. 978-0-83891-075-7, $42.00 [*Colorado Libraries,* February 2012]

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Keret, Etgar. Traducción de Ana María Bejarano. *Pizzería Kamikaze y Otras Relatos.* México, D.F.: Editorial Sexto Piso, 2008. 968-5679-29-0, no price given [*Críticas*, September 2008]

Littauer, Marita, and Florence Littauer. *Enriquece tu Comunicación. Miami, Fla.: Editorial Unilit, 2008.* 978-0-7899-1521-4, $11.99 [*Críticas*, August 2008]

Martínez, Guillermo. *La Muerte Lenta de Luciana B.* New York: Rayo Planeta, 2008. 978-0-06-156551-9, $14.95 [*Críticas*, May 2008]

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Matthews, Joseph R. *Library Assessment in Higher Education.* Westport, Conn.: Libraries Unlimited, 2007. 978-1-59158-531-2, $45.00 [*Colorado Libraries,* February 2008]

Chacón, Inma. *La Princesa India: Cuando el Viento Azul.* México: Alfaguara, 2006. 970-770398-9, $19.95 [*Críticas*, June 2006]

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Alponte, Juan María. *Colón: el Hombre, el Navegante, la Leyenda.* México, D.F.: Aguilar, 2003. 968-19-1260-8, $16.95 [*Críticas*, 2004]

Olcese Salvatecci, Alfieri. *Cómo Estudiar con Éxito: Téchnicas yHhábitos Para Aprender Major.* México, D.F.: Alfaomega Grupo Editor, 2002. 970-15-0764-9 [*Críticas*, 2003]

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Tibol, Raquel. *Los Murales de Diego Rivera: Universidad Autónoma Chapingo.* México, D.F.: Editorial RM, Universidad Autónoma Chapingo, 2002. 968-5208-08-5 [*Críticas*, 2003]

Lindsay-Poland, John. *Emperors in the Jungle: the Hidden History of the U.S. in Panama.* Durham, N.C.: Duke University Press, 2003. 0-8223-3098-9, $18.95 [*Críticas*, 2003]

Kaplan, Allison G. and Ann Marlowe Riedling. *Catalog It! A Guide to Cataloging School Library Materials.* Worthington, Ohio: Linworth Pub., 2002. 1-58683-014-7, $44.95 [*Colorado Libraries,* 2002]

Bardach, Ann Louise. *Cuba Confidential: Love and Vengeance in Miami and Havana.* New York: Random, 2002. 0-375-50489-3, $25.95 [*Library Journal*, 2002]

Swan, James. *Fundraising for Libraries: 25 Proven Ways to Get More Money for Your Library.* New York: Neal Schuman, 2002. 1-55570-433-6, $69.95 [*Colorado Libraries,* 2002]

Puíg de Lange, Victoria. *Sol Con Agua.* Nashville, Tenn.: Editorial Vistazo/Ediciones Reio Negro, 2002. 0-9724506-0-2, $17.75 [*Críticas*, 2002]

The Encyclopedia of Latin American Politics. Edited by Diana Kapiszewski; assistant editor, Alexander Kazan. Westport, Conn.: Oryx Press, 2002. 1-57356-306-4, $74.95 [*Library Journal*, 2002]

Vargas Lizano, Isabel. *Y Si Quieres Saber de Mi Pasado.* Con la colaboración de J.C. Vales. Madrid: Santillana Ediciones Generales, S.L., 2002. 84-03-09278-4, $18.95 [*Críticas*, 2002]

Ruy Sánchez, Alberto. *Los Jardines Secretos de Mogador: Voces de Tierra.* México, D.F.: Alfaguara, S.A., 2001. 968-19-0879-1, $16.95 [*Críticas*, 2002]

Chávez, Ricardo and Celso Santajuliana. *El Final de las Nubes.* Barcelona: RBA Libros, S.A., 2001. 84-7901-760-0, $11.95 [*Críticas*, 2002]

The Power of Language / El Poder de la Palabra: Selected Papers from the Second REFORMA National Conference. Edited by Lillian Castillo-Speed and the REFORMA National Conference Publications Committee. Englewood, Colo.: Libraries Unlimited, 2001. 1-563089459, $35.00 [*Colorado Libraries,* 2001]

Martínez, Rubén. *Crossing Over: A Mexican Family on the Migrant Trail.* Metropolitan: Holt, 2001. 0-8050-4908-8, $26.00 [*Library Journal*, 2001]

Guevara, Ernesto "Che." *The African Dream: the Diaries of the Revolutionary War in the Congo.* Translated from the Spanish by Patrick Camiller. With an introduction by Richard Gott and a foreword by Aleida Guevara March. New York: Grove Press, 2001. 0-8021-3834-9, $13.00 [*Library Journal*, 2001]

Cooper, Gail and Garry Cooper. *New Virtual Field Trips.* Englewood, Colo.: Libraries Unlimited, 2001. 1-56308-887-8, $27.50 [*Colorado Libraries,* 2001]

NATIONAL SERVICE & PROFESSIONAL AFFILIATIONS

American Library Association, Life Member
Association for Library Collections & Technical Services
Cataloging, Classification, and Metadata Section
ALCTS Editorial Board, Member, 2015-2019
Committee on Cataloging: Description and Access, Member, 2008-2012
Test Site for RDA, Manager, 2009-2011
Nominating Committee, Member, 2007-2008
Committee for Education and Training of Catalogers, Chair, 2006-2007, Member, 2003-2007
Competencies & Education for a Career in Cataloging Interest Group, Chair, 2010-2012; Member, 2010-
President's Program Committee, 2015-2016
Education Committee, Member, 2005-2007
Task Force on Competencies and Education for a Career in Cataloging, Chair, 2007-2009
2007 Annual Meeting Pre-conference, "What They Don't Teach in Library School: Competencies, Education and Employer Expectations for a Career in Cataloging," Steering Committee Chair
Fundraising Committee, Member, 2004-2006
Office of Diversity
Committee on Diversity, Chair, 2010-2011
Diversity Research Advisory Committee, Member, 2009-2010
Spectrum Scholar Mentor, 2009
Diversity Grants Review Committee, Member, 2007, 2010, 2012
Office of Statistics and Research
Research and Statistics Committee, Member, 2005-2007; Intern, 2003-2005
Library Research Round Table
Membership Committee, 2019-2021
Board of Directors, Member At-Large, 2009-2012
Member, 2003-
Office of Accreditation
Accreditation Panel Member (training completed 2004)
Accreditation Review Panel Member (training completed 2004)

REFORMA, Life Member
National Board of Directors, 2005-2013
National Fundraising Chair, 2005-2013
National Recruiting and Mentoring Committee, 2008-2010
Colorado Chapter, Secretary, 2004-2005
Colorado Chapter Liaison to National Board of Directors, 2004-2013

American Association of Law Libraries (AALL), Life Member
Online Audiovisual Catalogers Association (OLAC)
Colorado Association of Law Librarians (CoALL)

American Association of University Women
Association for Library and Information Science Education (ALISE)
University of Denver ALISE Representative, 2003-2008; 2010-2011
Membership Advisory Committee, 2007-2010
Technical Services Education Special Interest Group, 2003-
Garfield Doctoral Dissertation Award Reviewer, 2012
Garfield Doctoral Dissertation Scholarship Reviewer, 2014
American Association of University Professors (AAUP), 2006-

American Grant Writers Association, 2014-
Grant Professionals Institute, 2016-
National Grants Management Association, 2014-
Grant Reviewer (National and Regional Team Leader), U.S. Department of Education, 1998-
Grant Reviewer, Broadband Technologies Opportunity Program, U.S. Department of Commerce, 2009
Grant Reviewer, Institute of Museum and Library Services, 1998-2000
Grant Reviewer, Colorado Department of Education, 2014-
Grant Reviewer, Colorado State Library, 1998-
Grant Reviewer, American Association of Community Colleges *Working Connections* program, 1999
Peer Reviewer, *Journal for Library and Information Science Education,* 2005-
Peer Reviewer, *Journal of Library Metadata,* 2009
Peer Reviewer, *International Journal of Library and Information Science,* 2011
Regular Columnist, *The Bottom Line*, 2013-2016
Book Reviewer, *Library Journal*, 2001
Book Reviewer, *Críticas*, 2002-2009
Book Reviewer, *Colorado Libraries,* 2000-2012

REGIONAL SERVICE & PROFESSIONAL AFFILIATIONS

Mountain Plains Library Association
    Professional Development Grants Committee, Member, 2005-2006
    Professional Development Policy and Guidelines Sub-committee Chair, 2006

Colorado Association of Libraries
    "Student Voices" Column Editor, *Colorado Libraries,* 2005-2006
    Conference Planning Committee, Member, 2002
    Technical Services and Automation Division, Chair, 2002-2003; Member, 2000-
    Academic Libraries Division, Peer Review Conference Papers Committee, Member, 2007-2009
    Education Committee, Member, 1988-1993
    Diverse Populations Committee, Member, 2009-2013

SERVICE TO THE UNIVERSITY OF DENVER
Center for Teaching and Learning Faculty Advisory Board, 2007-2008; 2010-2012
Center for Community Engagement and Service Learning Advisory Board, 2007-2012
Faculty Senate
    Executive Committee, 2008-2013
    Nominations, Rules & Credentials Committee, Chair, 2008-2013; Member 2007-2013
    Appointment, Promotion, and Tenure Revision Committee, 2010-2012
    Grievance Policy Committee Member, 2007-2010
Law Library Director Search Committee Chair, 2012-2013
PROF Grant Review, College Representative to the University Review Team, 2006, 2008
Project Homeless Connect Evaluations, Principal Investigator, 2006-2009
University Technology Council, 2007-2009
University of Denver Hyde Interviews for Incoming Freshmen, 2003-2012

SERVICE TO THE MORGRIDGE COLLEGE OF EDUCATION
Appointment, Tenure & Review Committee
    Member, voting, 2003-2005; 2007- 2009
    Chair, Clinical Faculty Promotion & Tenure Policy Subcommittee, 2008-2009
    Member, Community Engagement Subcommittee, 2007-2009
    Member, Tenure Review Panel, 2003
Advancement and Alumni Relations Committee, Chair, 2003-2007; Member, 2002-2007
College Building Committee Member, 2004-2010
College of Education Student Association, Faculty Advisor, 2004-2007; 2009-2010
Faculty Senator, 2007-2013
Research and Scholarship Committee, Chair, 2008-2009; Member, 2002-2003, 2008-2009

Research and Grant Mentoring Committee, Chair, 2009-2010
Research Task Force Member, 2010-2012
Search Committee Member, Assistant Professor for Curriculum & Instruction, 2010-2011
Workload Task Force Member, 2010-2011

SERVICE TO THE LIBRARY & INFORMATION SCIENCE PROGRAM
Library and Information Science Student and Alumni Association, Faculty Advisor, 2002-2008
ALA Student Chapter, Faculty Advisor, 2005-2008
Beta Phi Mu Phi Chapter, Faculty Advisor, 2004-2014
Steering Committee Member, Accreditation by the American Library Association, 2001-2004
Search Committee Member, Associate Professor for LIS, 2006
Search Committee Chair, Assistant Professors for LIS, 2003, 2005, 2006, 2007
Search Committee Ex-Officio Member, Director for LIS, 2004

SERVICE TO SAM HOUSTON STATE UNIVERSITY
Rio Roundup: South Texas Literature Conference, Conference Coordinator, 1993
External Relations, Fund Raising, Grants Committee, Chair, 1993-1995
Advisory Council Committee, Chair, 1993-1995
Students, Admissions, and Advisement Committee, Chair, 1994
Institutional Effectiveness Committee, Member, 1993-1995

SERVICE TO THE COLLEGE OF EDUCATION AND APPLIED SCIENCE
Faculty Affairs Committee, Member, 1993-1995
Curriculum Committee, Member, 1993-1995
Continuing Education Committee, Member, 1993-1995

SERVICE TO THE COMMUNITY
French Teacher & Student Exchange with Laon, France, Monarch High School, Boulder Valley School District
     (Boulder, Colorado), 2017-
Denver/Boulder Games 2022, Board of Directors, Secretary-Treasurer, 2015-2018
United Way Campaign Committee, College of Education, 2006
Arapahoe County, Election Judge for the County Clerk and Recorder, 2000-2005
Arthritis Foundation, Rocky Mountain Chapter, Certified Educator & Trainer, 1999-2008
Bonfils Blood Center, Silver Level Donor, 2000-2016
Denver Museum of Natural History, Docent, 1992
Tech Prep of the Lower Rio Grande Valley, Inc. (Harlingen, Texas) Board of Directors, 1995-1997
     Executive Committee, 1996-1997; Chair, Development Committee, 1995-1997; Chair, Fiscal Agency
     Committee, 1995-1996; Chair, Colleges and Universities Committee, 1996-1997
Gilpin County (Colorado) Public Library Board of Trustees, 1986-1989; Vice President, 1987-1989
City of Central (Colorado) Economic Development Committee, 1987-1989
Columbine Family Health Centers, Inc. (Nederland and Black Hawk, Colorado) Board of Directors, 1988-1989

CERTIFICATION
     Permanent Public Librarian Certificate - Pennsylvania, New York, Texas
     Westlaw Expert Witness, 2008-
     Certified Grant Writer®, 2016-

AWARDS AND HONORS
Advanced Practitioner for Service Learning and Community Engagement, University of Denver, 2011
Platinum Star Alumnae, College of Information, Library Science & Technologies, University of North Texas, 2009
Commendation for Integration of Technologies in Teaching & Learning Environment, University of Denver, 2006
Outstanding Adjunct Faculty Member Award, College of Education, University of Denver, 2002
Beta Phi Mu, Pi, University of Pittsburgh, 1985
Alpha Lambda Sigma, University of North Texas, 1972

Albert Nelson Marquis Lifetime Achievement Award, Who's Who in America
Who's Who in American Women
Who's Who of Women Executives
Dictionary of International Biography
Who's Who in the East
Who's Who in the South and Southwest
Who's Who in the World
Who's Who of Online Professionals
Who's Who in Library and Information Science
2,000 Notable Women
Who's Who of Emerging Leaders
Who's Who in Professional and Executive Women
Who's Who in American Education
International Who's Who of Professional and Business Women
International Leaders in Achievement
International Educator of the Year
Who's Who in Finance and Industry
Who's Who in Finance and Business

Invited International and National Conference Presentations

Driscoll, Margaret, Christy Confetti Higgins, Scott Brown, and Sylvia D. Hall-Ellis. *A View from Within: Open House Tour of Three Canvas Core Courses*. Presentation to be delivered at the School of Information, San José State University Professional Development Seminar, San José, California, October 17, 2019.

Hall-Ellis, Sylvia D. *Invest in Me -- I'm Your Future: Succession Planning for Libraries.* Keynote presentation delivered at the ALCTS President's Symposium, Boston, Mass., January 8, 2016.

Seidel, Kent E. and Sylvia D. Hall-Ellis. *Making Grants Work for You: Strategies for Doctoral Students and Early Career Scholars.* Presentation delivered at the University Council for Educational Administration, Early Career Scholars Session, Indianapolis, Ind., November 9, 2013.

Hall-Ellis, Sylvia D. *So You Want to be a Manager; Leadership Skills and Competencies for Technical Services Managers and Administrators.* Presentation delivered at the 138th Annual Conference, American Library Association, Chicago, Ill., June 29, 2013.

Seidel, Kent E., Karen S. Riley, Lyndsay Agans, Susan Korach, and Sylvia D. Hall-Ellis. *Making Grants Work for You (Instead of Just Working for Grants).* A panel discussion delivered at the University Council for Educational Administration, Early Career Scholars Session, Denver, Colo., November 17, 2012.

Hall-Ellis, Sylvia D. *After the Great TS Reorganization: The Westminster Law Library.* Presentation delivered at the 137th Annual Conference, American Library Association, Anaheim, Calif., June 23, 2012.

Hall-Ellis, Sylvia D. *Conversations with Catalogers in the 21st Century.* A panel discussion sponsored by the ALCTS Competencies for a Career in Cataloging Interest Group, delivered at the 137th Annual Conference, American Library Association, Anaheim, Calif., June 22, 2012.

Hall-Ellis, Sylvia D., moderator. *Mid-Career Leaders Program.* A panel discussion sponsored by the ALA Committee on Diversity delivered at the 136th Annual Conference, American Library Association, New Orleans, La., June 26, 2011.

Hall-Ellis, Sylvia D., moderator. *Diversity Town Hall.* A community conversation sponsored by the ALA Committee on Diversity delivered at the 136th Annual Conference, American Library Association, New Orleans, La., June 24, 2011.

LaBarre, Kathryn, Sylvia D. Hall-Ellis, Karen Anderson, Rick Hasenyager, Christopher Cronin, and Penny Baker. *Briefings from RDA Test Participants.* A panel discussion delivered at the Midwinter Conference, American Library Association, San Diego, Calif., January 7, 2011.

Miksa, Shawne, Marjorie Bloss, and Sylvia D. Hall-Ellis. *Educating the Next Generation of Catalogers: Teaching RDA.* A panel discussion delivered at the 97th Annual Conference, Association for Library and Information Science Education, San Diego, Calif., January 7, 2011.

Hall-Ellis, Sylvia D., Robert Maxwell, John Hostage, and George Prager. *RDA Panel: What Cataloging Managers Need to Know.* Presentation delivered at the 103rd Annual Conference, American Association of Law Librarians, Denver, Colo., July 12, 2010.

Hall-Ellis, Sylvia D. and Stacey L. Bowers. *Catalogers in the RDA Environment: Skill Sets, Expectations and Challenges.* Presentation delivered at the 103rd Annual Conference, American Association of Law Librarians, Denver, Colo., July 11, 2010.

Hall-Ellis, Sylvia D. *Comfortable in Your Cataloging and Metadata Specialist Skin? Or, So You Want to Hire a Cataloger.* Presentation delivered to the ALCTS Research Group at the 134th Annual Conference, American Library Association, Chicago, Ill., July 11, 2009.

Perez, Megan, Sylvia D. Hall-Ellis, and Denise Anthony. *From Novice to Expert: Collaboration for Succession Planning.* A "hot topic" presentation delivered at the 14th ACRL Conference, Seattle, Wash., March 13, 2009.

Hall-Ellis, Sylvia D. *Cataloging in the RDA Environment: Skill Sets, Expectations and Challenges.* Presentation delivered to the ALCTS Research and Publications Committee at the Midwinter Conference, American Library Association, Denver, Colo., January 24, 2009.

Hall-Ellis, Sylvia D. *LIS Cataloging Education for the 21st Century: Expectations and Challenges.* A panel discussion held at the 95th Annual Conference, Association for Library and Information Science Education, Denver, Colo., January 23, 2009.

Chu, Clara, Sylvia D. Hall-Ellis, and Mark Winston. *The Doctoral Degree & Building a Career.* A panel discussion delivered at the ALA Office of Diversity Spectrum Doctoral Fellows E.J. Josey Leadership Institute, Midwinter Conference, American Library Association, Denver, Colo., January 20, 2009.

Hall-Ellis, Sylvia D. and Robert O. Ellett, Jr. *Fundamentals of Cataloging Course: An Overview of the ALCTS Online Course.* Presentation delivered to the ALCTS Big Heads Group, 133rd Annual Conference, American Library Association, Anaheim, Calif., June 30, 2008.

Hall-Ellis, Sylvia D. *Employers' Expectations for Technical Services Librarians: What We Don't Know.* Presentation delivered to the ALCTS Research and Publications Committee Program, 133rd Annual Conference, American Library Association, Anaheim, Calif., June 28, 2008.

Hall-Ellis, Sylvia D., Virginia R. Maloney, and Mary Stansbury. *Institutional Responses to Engaged Scholarship: The Carnegie Foundation Engaged University Classification at Two Universities.* Presentation delivered to the 94th Annual Conference, Association for Library and Information Science Education, Philadelphia, Pa., January 11, 2008.

Hall-Ellis, Sylvia D. *Puzzles, Problems, and Predicaments.* Presentation delivered to the ALCTS Research Discussion Group, 132nd Annual Conference, American Library Association, Washington, D.C., June 23, 2007.

Hall-Ellis, Sylvia D. *Cataloging Education: A New Emphasis for the Library and Information Science Curriculum.* Presentation delivered to the ALCTS Pre-conference, 132nd Annual Conference, American Library Association, Washington, D.C., June 22, 2007. http://www.loc.gov/catdir/cpso/careercat.html

Ellett, Jr., Robert O. and Sylvia D. Hall-Ellis. *Copy Cataloging Done Smarter.* Presentation delivered to the International Conference on Interdisciplinary Information Sciences and Technologies (InSciT2006), October 25-28, 2006.

Hall-Ellis, Sylvia D. and Robert O. Ellett, Jr. *Cooperative Cataloging: Challenges and Opportunities for Defense Libraries.* Presentation delivered to the 1st Annual Conference of Defense Libraries, Spanish Ministry of Defense, Madrid, Spain, July 7, 2006.

Hall-Ellis, Sylvia D. *Cataloger Competencies: Do the Employers Require What the Professors Teach?* Presentation delivered to the ALCTS CCS Heads of Cataloging Discussion Group, 131st Annual Conference, American Library Association, New Orleans, La., June 26, 2006.

Grealy, Deborah S. and Sylvia D. Hall-Ellis. *From Research to Practice: The Scholarship of Teaching and Learning in LIS Education.* Presentation delivered to the at the 92nd Annual Conference, Association for Library and Information Science Education, San Antonio, Tex., January 18, 2006.

Hall-Ellis, Sylvia D. *Employers' Expectations for Entry-Level Catalogers: What Position Announcement Data Indicate.* Research paper delivered to the Technical Services Special Interests Group, 91st Annual Conference, Association for Library and Information Science Education, Boston, Mass., January 12, 2005. http://dlist.sir.arizona.edu/

Hall-Ellis, Sylvia D. *Common Errors in MARC Records Prepared by LIS Students: What Does It Mean?* Research paper delivered to the ALCTS CCS Cataloging Norms Discussion Group, Mid-Winter Conference, 90th American Library Association, San Diego, Calif., January 10, 2004.

Hall-Ellis, Sylvia D. *Visual Arts as Foundation for Successful Library Automation: The Rocky Mountain College of Art & Design Experience.* Paper delivered at the 6th Annual Conference of Higher Education, Charleston, S. C., 1993.

Hall, Sylvia D. *Design Elements for Bibliographic Databases: An Overview.* Paper delivered at the 14th Online National Conference, New York, 1983.

Invited Regional Conference Presentations

Hall-Ellis, Sylvia D., Hudson, Christopher D., Brittany Cronin, and Kathryn Michaels. "The Colorado Law Project: Meeting the Public's Need for Legal Information." Panel discussion delivered at the Mountain Plains Library Association Conference, Billings, Mont., April 9, 2011.

Grealy, Deborah S. and Sylvia D. Hall-Ellis. *Education for Information Professionals in New Mexico: Library & Information Science Graduate Education at the University of Denver.* Presentation delivered at the New Mexico Library Education Summit, Las Vegas, N.M., September 26, 2005.

Hall-Ellis, Sylvia D. *Public Library-School Library Partnerships.* Presentation delivered at the 3rd Annual Colorado Association of Libraries Conference with the Mountain Plains Library Association, Denver, Colo., October 22, 2004.

Hall-Ellis, Sylvia D. *Learn All You Can – Educational Partnership Opportunities for the Lewis and Clark Bicentennial Commemoration.* Paper delivered at the 3rd Annual Lewis and Clark Bicentennial Council National Planning Conference, Bismarck, N.D., April 26, 1998.

Invited State Conference Presentations

Grealy, Deborah S. and Sylvia D. Hall-Ellis. *Academic Library Leadership Changes: Using Succession Planning and Mentoring.* Presentation delivered at the Minnesota Library Education Conference, St. Cloud, Minn., October 10, 2013.

Hall-Ellis, Sylvia D., Merrie Valliant, and Melissa Powell. *RDA: What Is It and What Do You Need To Do With It At Your Library?* Presentation delivered at the Colorado Library Consortium Spring Conference, Ft. Morgan, Colo., April 26, 2013.

Hall-Ellis, Sylvia D. *Service Learning and the Library & Information Science Graduate Education at the University of Denver.* Presentation delivered at the 4th LEADS Scholars Orientation, Denver, Colo., August 5, 2009.

Hall-Ellis, Sylvia D. *Service Learning: Enhancement to Library & Information Science Graduate Education at the University of Denver.* Presentation delivered at the 3rd LEADS Scholars Orientation, Denver, Colo., June 2008.

Hall-Ellis, Sylvia D. *Law Librarianship: A Community Conversation.* Sponsored by the Colorado Association of Law Libraries. Paper delivered at the Colorado Supreme Court Library, Denver, Colo., May 14, 2008.

Hall-Ellis, Sylvia D. *Opportunities and Challenges in Law Librarianship: A Community Conversation.* Presentation delivered at the Sturm College of Law, Denver, Colo., November 7, 2007.

Hall-Ellis, Sylvia D. *Grant Writing Resources for Nursing Professionals.* Presentation delivered at the Presbyterian / St. Luke's Health One Medical Center 1st Annual Research Symposium, Denver, Colo., October 17, 2007.

Hall-Ellis, Sylvia D. *Project Homeless Connect 4 Event Evaluation – Insights and Lessons Learned.* Presentation delivered at the Homelessness Research Symposium: What is DU Doing about Homelessness in Denver, Denver, Colo., September 14, 2007.

Hall-Ellis, Sylvia D. *Service Learning and the Library & Information Science Graduate Education at the University of Denver.* Presentation delivered at the 2nd LEADS Scholars Orientation, Denver, Colo., August 10, 2007.

Hall-Ellis, Sylvia D. *Education for Information Professionals in a Digital Environment: Library & Information Science Graduate Education at the University of Denver.* Presentation delivered at the 15th Spring Mountains and Plains Parapros Conference, Denver, Colo., February 24, 2007.

Hall-Ellis, Sylvia D. *Public Library Service to Spanish-Speaking and Latino Residents in Denver: A Case Study.* Presentation delivered at the 4th Annual Colorado Association of Libraries Conference, Denver, Colo., November 10, 2005.

Hall-Ellis, Sylvia D. *Education for Information Professionals in a Digital Environment: Library & Information Science Graduate Education at the University of Denver.* Presentation delivered at the 14th Annual Mountains and Plains Parapros Conference, Aurora, Colo., July 29, 2005.

Hall-Ellis, Sylvia D. *Educational Opportunities: Library & Information Science Graduate Education at the University of Denver.* Presentation delivered at the 13th Annual Mountains and Plains Parapros Conference, Centennial, Colo., August 6, 2004.

Hall-Ellis, Sylvia D. *Library Education & Training: Focus on the West: An LIS Faculty Member's Personal Response*. Presentation delivered at the 1st Annual Colorado Association of Libraries Conference, Keystone, Colo., October 18, 2002.

Hall-Ellis, Sylvia D. *Grant Writing for School Librarians.* Presentation delivered at the 2002 Annual Colorado Education Media Association Conference, Colorado Springs, Colo., February 15, 2002.

Hall-Ellis, Sylvia D. *Grants – Opportunities for the Future.* Paper delivered at the Southeast Regional Accountability Annual Conference, Lamar, Colo., November 12, 1998.

Hall-Ellis, Sylvia D. *The Texas Library Connection and Interlibrary Loan: An Experiment in Resource Sharing.* Paper delivered at the Texas Computer Educators' Association Annual Conference, Austin, Tex., February 6, 1997.

Hall-Ellis, Sylvia D. *Finding Grant Sources on the Internet: A Guide for Librarians.* Paper delivered at the 2nd Annual Institute for School Library Personnel, Pharr-San Juan-Alamo North High School, Pharr, Tex., July 29, 1996**.**

Hall-Ellis, Sylvia D. *Mathematical and Logical Thinking: A Critical Intelligence.* Paper delivered at the 3rd Annual Paraprofessional Conference at the University of Texas - Pan American, Edinburg, Tex., March 8, 1996.

Hall-Ellis, Sylvia D. *Cataloging Trends and Issues: Update Session.* Paper delivered at the 1st Annual Institute for School Library Personnel, South Texas Community College, McAllen, Tex., July 19, 1995.

Hall-Ellis, Sylvia D. *Grant Writing: Tips and Encouragement for School Librarians.* Paper delivered at the 1st Annual Institute for School Library Personnel, South Texas Community College, McAllen, Tex., July 18 and 19, 1995.

Hall-Ellis, Sylvia D. *How to Become an Expert Grant Writer.* Paper delivered at the 3rd Annual High School Principals' Academy, South Padre Island, Port Isabel, Tex., June 19, 1995.

Hall-Ellis, Sylvia D. *Texas Library Study: Results from Regions I and II.* Paper delivered at the 3rd Annual Technology Conference, Texas A&M University, College Station, Tex., November 18, 1994.

Hall-Ellis, Sylvia D. *Academic Achievement and Middle School Students.* Paper delivered at the 8th Annual Young Adult Conference, Sam Houston State University, Huntsville, Tex., November 5, 1994.

Hall-Ellis, Sylvia D. *Multimedia Resources for Library Leaders.* Paper delivered at the Institute for Librarians in A Multicultural Environment, Sam Houston State University, Huntsville, Tex., June 10, 1994.

Hall-Ellis, Sylvia D. *Finding the Resource: Empowering the User, or, the Case for Curriculum Based Subject Access to Learning Resource Center Collections.* Paper delivered at the 81st Annual Texas Library Association Conference, Corpus Christi, Tex., April 12-16, 1994.

Hall-Ellis, Sylvia D. and William H. Pichette. *Sam Houston State University Makes Use of OCLC/AMIGOS Collection Analysis CD.* Paper delivered at the 81st Annual Texas Library Association Conference, Corpus Christi, Tex., April 12-16, 1994.

Hall, Sylvia D. *Funding and Library Development in Pennsylvania: A Symbiotic Relationship.* Paper delivered at the Annual Graduate Student Colloquia, University of Pittsburgh, School of Library and Information Science, 1982.

Hall, Sylvia D. *Leadership for Public Library Trustees.* Paper delivered for the Trustees Division, Pennsylvania Library Association Annual Conference, Lancaster, Penn., 1981.

Seminar and Professional Development Presentations

Taylor, Meredith, and Sylvia D. Hall-Ellis. *Talent Management and Succession Planning.* ALCTS eForum, held March 22, 2017.

Hirsh, Sandra, Heather O'Brien, Michelle Holschuh Simmons, Michael Krasulski, and Sylvia D. Hall-Ellis. *Information Services Today: An Introduction. Part 3: Information Services: Roles in the Digital Age.* Rowan and Littlefield in partnership with Library Journal webinar, recorded February 5, 2015.

Hall-Ellis, Sylvia D. and Jennifer Sweda. *Copy Cataloging in an RDA Environment.* ALCTS eForum, held May 14 and 15, 2013.

Hall-Ellis, Sylvia D. *Law Librarianship: A Community Conversation.* Sponsored by the Colorado Association of Law Libraries, presented at the Colorado Supreme Court Library, Denver, Colo., May 14, 2008.

Hall-Ellis, Sylvia D. and Beatrice Z. Gerrish. *Reading and Libraries: Recent Research in Reading.* Presentation at the Ricks Center for Gifted Education, Denver, Colo., March 4, 2008.

Hall-Ellis, Sylvia D. *Cataloger Competencies: Do the Employers Require What the Professors Teach?* Presentation for the School of Library and Information Science, San José State University, February 12, 2008.

Hall-Ellis, Sylvia D. and Robert O. Ellett, Jr. *Cooperative Cataloging: Rules, Tools, and Conventions for Building a Multi-institutional Catalog.* Sponsored for the Spanish Ministry of Defense, Madrid, Spain, July 10, 2006.

Hall-Ellis, Sylvia D. *Cash for Kids: Grant Writing Opportunities for Youth Services Librarians.* Sponsored by the Colorado Young Adult Librarians; presented at Bemis Memorial Library, Littleton, Colo., November 13, 2002.

Hall-Ellis, Sylvia D. *MARC Records and Authority Control: Planning for Bibliographic Database Migration.* Sponsored and held at the Douglas County Public Library, Castle Rock, Colo., May 28, 2002.

Hall-Ellis, Sylvia D. *Grant Writing: A Refresher for Librarians.* Sponsored by Library and Information Science Program, College of Education, University of Denver; presented at University Center at Chaparral, August 12, 2000.

Hall-Ellis, Sylvia D. *Shaking the Money Tree – Basic Grant Writing for Colorado Educators.* Sponsored by the Office of Educational Telecommunications of the Colorado Department of Education.
      Pikes Peak Community College, Colorado Springs, Colo., November 16, 1998.
      Pueblo School District 60, Pueblo, Colo., November 12, 1998.
      University of Northern Colorado, Greeley, Colo., November 10, 1998.
      United Technology Educational Partnership, Grand Junction, Colo., November 9, 1998.

Hall-Ellis, Sylvia D. *Cataloging Multimedia, Kits, Globes and Map Materials in USMARC.* Sponsored and hosted by Region One Education Service Center, Edinburg, Tex., April 24, 1997 and December 12, 1996.

Hall-Ellis, Sylvia D. *New Standards for School Library Media Centers.* Sponsored and hosted by Region One Education Service Center, Edinburg, Tex., April 15, 1997.

Hall-Ellis, Sylvia D. *The School Library Media Specialist in the 21st Century: Visions for the Future.* Sponsored and hosted by Pharr-San Juan-Alamo Independent School District, Pharr, Tex., April 4, 1997.

Hall-Ellis, Sylvia D. *Cataloging Sound Recordings and Audio Materials in USMARC.* Sponsored and hosted by Region One Education Service Center, Edinburg, Tex., March 20, 1997 and November 21, 1996.

Hall-Ellis, Sylvia D. *Evaluating and Selecting CD-ROMS for School Library Media Collections.* Sponsored and hosted by Region One Education Service Center, Edinburg, Tex., March 18, 1997.

Hall-Ellis, Sylvia D. *Cataloging Audiovisual Materials in USMARC.* Sponsored and hosted by Region One Education Service Center, Edinburg, Tex., February 27, 1997, November 7, 1996 and October 24, 1996.

Hall-Ellis, Sylvia D. *Introduction to Dialog: Basic Searching Strategies.* Sponsored and hosted by Region One Education Service Center, Edinburg, Tex., February 14, 1997.

Hall-Ellis, Sylvia D. *Cataloging Books in USMARC.* Sponsored and hosted by Region One Education Service Center, Edinburg, Tex., January 30, 1997, October 10, 1996, September 26, 1996 and August 8, 1996.

Hall-Ellis, Sylvia D. *Advanced Internet Searching Techniques for Librarians.* Sponsored and hosted by Region One Education Service Center, Edinburg, Tex., January 21, 1997.

Hall-Ellis, Sylvia D. *Texas Library Connection Full-Text Searching.* Sponsored and hosted by Region One Education Service Center, Edinburg, Tex., December 13, 1996 and October 25, 1996.

Hall-Ellis, Sylvia D. *Developing Evaluation Strategies for Grants and Proposals.* Sponsored and hosted by Region One Education Service Center, Edinburg, Tex., December 10, 1996.

Hall-Ellis, Sylvia D. *Developing Needs Assessment for Grants and Proposals.* Sponsored and hosted by Region One Education Service Center, Edinburg, Tex., November 12, 1996.

Hall-Ellis, Sylvia D. *Texas Library Connection Union Catalog Searching.* Sponsored and hosted by Region One Education Service Center, Edinburg, Tex., November 8, 1996 and September 6, 1996.

Hall-Ellis, Sylvia D. *Grant Resources on the Internet.* Sponsored and hosted by Region One Education Service Center, Edinburg, Tex., October 23, 1996.

Hall-Ellis, Sylvia D. *Preparing a Response to the Telecommunications Infrastructure Fund Board: Needs Assessment, Professional Development Framework, and Evaluation Strategies.* Sponsored and hosted by Region One Education Service Center, Edinburg, Tex., October 16, 1996.

Hall-Ellis, Sylvia D. *Texas Library Connection: Building the Districtwide Bibliographic Database.* Sponsored and hosted by Mercedes Independent School District, Mercedes, Tex., September 13, 1996 and August 8, 1996. Sponsored and hosted by Los Fresnos Consolidated Independent School District, Los Fresnos, Tex., August 12, 1996.

Hall-Ellis, Sylvia D. *School-to-Work and Special Education: An Inclusive Partnership for Success.* Sponsored and hosted by the Office of Special Education, Region One Education Service Center, Edinburg, Tex., September 11, 1996.

Hall-Ellis, Sylvia D. *Telecommunications Infrastructure Fund Board: An Overview of Funding for Secondary Schools.* Sponsored and hosted by Region One Education Service Center, Edinburg, Tex., August 31, 1996.

Hall-Ellis, Sylvia D. *Cataloging Books, Multimedia, and Realia in USMARC.* Sponsored and hosted by Edinburg Consolidated Independent School District, Edinburg, Tex., August 6, 1996.

Hall-Ellis, Sylvia D. *Internet Resources for Grant Writers.* Sponsored and hosted by Region One Education Service Center, Edinburg, Tex., April 20, 1996.

Hall-Ellis, Sylvia D. *Enhanced Grant Writing Skills for Mathematics Educators: Writing Skills for Campus Teams.* Sponsored and hosted by the Office of General Education, Region One Education Service Center, Edinburg, Tex., March 22, 1996.

Hall-Ellis, Sylvia D. *Internet Resources for Grant Writers.* Sponsored and hosted by the College of Education and Applied Science, Sam Houston State University, Huntsville, Tex., March 9, 1996.

Hall-Ellis, Sylvia D. *Grant Writing for Mathematics Educators: A Development Process for Campus Teams.* Sponsored and hosted by the Office of General Education, Region One Education Service Center, Edinburg, Tex., March 4, 1996.

Hall-Ellis, Sylvia D. *Shaking the Money Tree: Preparing Successful Technology Grant Applications.* Sponsored and hosted by the Office of Technology and Media Services, Region One Education Service Center, Edinburg, Tex., February 29, 1996 and April 29, 1996.

Hall-Ellis, Sylvia D. *District-wide Technology Planning: Technical Assistance for the Texas Education Agency Initiative.* Sponsored and hosted by the Office of Technology and Media, Region One Education Service Center, Edinburg, Tex., February 2, 1996.

Hall-Ellis, Sylvia D. *Enhanced Grant Writing Skills.* Sponsored and hosted by Pharr-San Juan-Alamo Independent School District, Pharr, Tex., January 27, 1996.

Hall-Ellis, Sylvia D. *United States Copyright Act of 1976, Video Transmissions, Computer Software and the Internet.* Sponsored and hosted by the Office of Technology and Media, Region One Education Service Center, Edinburg, Tex., January 24, 1996.

Hall-Ellis, Sylvia D. *The Grant Writing Development Process.* Sponsored and hosted by Pharr-San Juan-Alamo Independent School District, Pharr, Tex., January 20, 1996.

Hall-Ellis, Sylvia D. *MARC Cataloging of Materials for Library Media Centers.* Sponsored and hosted by the Office of Media Services, Region One Education Service Center for the Donna Independent School District, Donna, Tex., August 17, 1995.

Hall-Ellis, Sylvia D. *Classification.* Sponsored by AJ Seminars, Rockville, Maryland; presented at University Hilton Hotel, Houston, Tex., May 10, 1995.

Hall-Ellis, Sylvia D. *Library Technical Services.* Sponsored by AJ Seminars, Rockville, Maryland; presented at University Hilton Hotel, Houston, Tex., April 26, 1995.

Hall-Ellis, Sylvia D. *Grant Writing: An Introduction for Public School Administrators.* Sponsored and hosted by the Office of Administrative Services, Region One Education Service Center, Edinburg, Tex., April 19, 1995.

Hall-Ellis, Sylvia D. *The School Library Media Specialist in the 21ˢᵗ Century: Visions for the Future.* Sponsored and hosted by the United Independent School District, Laredo, Tex., March 31, 1995.

Hall-Ellis, Sylvia D. *Using USMARC.* Sponsored by AJ Seminars, Rockville, Maryland; presented at University Hilton Hotel, Houston, Tex., March 29, 1995.

Hall-Ellis, Sylvia D. *Library Media Center Policies and Guidelines: How to Prepare for School Board Adoption.* Sponsored and hosted by the Office of Technology and Media Services, La Joya Independent School District, La Joya, Tex., March 10, 1995.

Hall-Ellis, Sylvia D. *Developing District-wide Policies and Guidelines for Library Media Centers.* Sponsored and hosted by the Office of Technology and Media Services, La Joya Independent School District, La Joya, Tex., January 10, 1995.

Hall-Ellis, Sylvia D. *MARC Cataloging of Audiovisual Materials for Library Media Centers.* Sponsored and hosted by the Office of Library Media and Technology Services, Cypress-Fairbanks Independent School District, Houston, Tex., December 1, 1994.

Hall-Ellis, Sylvia D. *The School Library Media Specialist in the 21ˢᵗ Century: Visions for the Future.* Sponsored and hosted by United Independent School District, Laredo, Tex., October 14, 1994.

Hall-Ellis, Sylvia D. *The School Library Media Specialist in the 21ˢᵗ Century: Visions for the Future.* Sponsored and hosted by the Laredo Independent School District, Laredo, Tex., October 7, 1994.

Hall-Ellis, Sylvia D. *MARC Cataloging for Library Media Centers.* Sponsored by the Office of Library Media and Technology Services, Cypress-Fairbanks Independent School District, Houston, Tex., October 5, 1994.

Hall-Ellis, Sylvia D. *Jump to the Head of the Class: Undergraduate Library Resources Available at Sam Houston State University.* Sponsored by the Office of the Associate Vice President for Student Services, Sam Houston State University, Huntsville, Tex., October 4, 1994.

Hall-Ellis, Sylvia D. *CD-ROMs - 1994's Newest and the Best for Secondary Level Media Centers.* Sponsored and hosted by Clear Lake Independent School District, Houston, Tex., June 3, 1994.

Hall-Ellis, Sylvia D. *Introduction to Classification.* Sponsored by AJ Seminars, Rockville, Maryland; presented at Holiday Inn, Market Center, Dallas, Tex., May 18, 1994.

Hall-Ellis, Sylvia D. *Basic Descriptive Cataloging.* Sponsored by AJ Seminars, Rockville, Maryland; presented at University Hilton Hotel, Houston, Tex., May 4, 1994.

Hall-Ellis, Sylvia D. *Shaking the Money Tree - Part II: Writing Successful Grant Applications.* Sponsored by Donna Independent School District, Donna, Texas, and Region One Education Service Center Edinburg, Texas; presented at South Texas Community College Library, McAllen, Tex., April 29, 1994.

Hall-Ellis, Sylvia D. *Using MARC.* Sponsored by AJ Seminars, Rockville, Maryland; presented at Holiday Inn, Market Center, Dallas, Tex., April 6, 1994.

Hall-Ellis, Sylvia D. *Automated Authority Control.* Sponsored by AJ Seminars, Rockville, Maryland; presented at University Hilton Hotel, Houston, Tex., March 23, 1994.

Hall-Ellis, Sylvia D. *Automating the District School Library Media Centers: Choices and Opportunities.* Sponsored and hosted by the Office of Technology and Library Media Services, Fort Bend Independent School District, Sugar Land, Tex., March 4, 1994.

Hall-Ellis, Sylvia D. *Shaking the Money Tree - Part I: Preparing Successful Grant Applications.* Sponsored and hosted by the Office of Library Media Services, Donna Independent School District, Donna, Tex., February 4, 1994.

GRADUATE COURSES TAUGHT

San José State University, School of Library and Information Science
    INFO 249 – Advanced Cataloging and Classification (Fall 2015, 2016; Summer 2016)
    INFO 287 – Special Topics in Cataloging and Classification (Spring 2017, 2018, 2019, 2020, 2021; Fall 2020, 2021)
    LIBR 248 – Beginning Cataloging and Classification (Summer 2002, 2003, 2004, 2005, 2006)
    LIBR 249 – Advanced Cataloging and Classification (Summer 2003; Fall 2014; Summer 2015)

University of Denver, University College
    Grant Writing Certificate Seminar for Non-Profit Organizations (Fall 2020, 2021; Spring 2021)

University of Denver, Morgridge College of Education
    HED 5991 – Grant Writing in Higher Education (Spring 2011)
    LIS 4010 – Organization of Information (Fall 2002, 2003, 2004, 2005, 2006, 2009; Winter 2005; Spring 2004, 2005, 2006)
    LIS 4020 – Professional Principles and Ethics (Summer 2000)
    LIS 4040 – Management of Libraries and Information Centers (Fall 2010; Spring 2003, 2009 (DS); Winter 2005)
    LIS 4070 – Cataloging and Classification (Winter 2008, 2009, 2010, 2011, 2012; Fall 2009 (DS))
    LIS 4321 – Collection Management (Spring 2005)
    LIS 4326 – LIS Research (Winter 2009 (DS); Spring 2009 (DS))
    LIS 4350 – Adult Materials and Services (Summer 2006, 2009)
    LIS 4379 – Social Sciences Resources (Spring 2009)
    LIS 4400 – Cataloging and Classification (Spring 2000, 2001; Winter 2002, 2003, 2004, 2005, 2006, 2007, 2008, 2009; Summer 2005, 2006 – course renumbered LIS 4070, September 2007)
    LIS 4401 – Descriptive Cataloging (Winter 2001; Spring 2002, 2003, 2006, 2007, 2008, 2009; Summer 2005)
    LIS 4402 – Subject Cataloging (Spring 2001, 2009; Summer 2005, 2006, 2007, 2008)
    LIS 4403 – Classification Schemes (Fall 2007, 2008, 2009 (DS))
    LIS 4405 – Authority Control (Winter 2009)
    LIS 4510 – Materials and Services for Children (Winter 2004; Summer 2005)
    LIS 4620 – Grant Writing and Fundraising (Summer 2000, 2002, 2004, 2010; Winter 2006; Fall 2006, 2007, 2008, 2009)
    LIS 4700 – Seminar in Technical Services (Fall 2001)
    LIS 4700 – Seminar in Public Libraries (Summer 2002)
    LIS 4804 – Management of Electronic Records (Spring 2004; Fall 2005)
    LIS 4902 – Capstone Projects (Winter 2003, Spring 2008, 2009, 2011)
    LIS 4910 – Independent Study (every quarter Winter 2000 through Spring 2011)
    LIS 4920 – Service Learning (every quarter Summer 2004 through Spring 2011)
    RMS 4954 – Grant Writing (Summer 2013, 2014)
    RMS 4959 – Content Analysis Methodology (Spring 2015)
    QRM 4978 – Grant Writing (Summer 2011, 2012)

Rutgers University, School of Communication and Information
    SC&I 522 – Cataloging and Classification (Summer 2013)

University of Arizona, College of Behavioral and Social Sciences
    LIS 602 – Cataloging and Classification (Summer 1995)
    LIS 612 – Advanced Online Search and Retrieval (Summer 1995)

Sam Houston State University, College of Education & Applied Science
    LIS 532 - Cataloging and Classification (Fall 1993, 1994, 1995)
    LIS 563 - Advanced Cataloging and Classification (Summer 1994)
    LIS 567 - Research Methods (Spring 1994, Spring 1995)
    LIS 591 - Educational Technology (Spring 1994, 1995)
    LIS 596 - Networking and Computer Technologies in Education (Fall 1993, Summer 1994, Fall 1995)

Dissertations at the University of Denver

Bowers, Stacey L. *Library Anxiety of Law School Students: A Study Utilizing the Multidimensional Library Anxiety Scale.* Chair, May 5, 2010.

Fattor, Melissa M. *Student Engagement Differences by Ethnicity and Scale for Ninth Grade Students.* Chair, November 1, 2010.

Fulton, Roseanne. *A Case Study of Culturally Responsive Teaching in Middle School Mathematics.* Kent Seidel, Chair, June 18, 2009, Outside Chair.

Grealy, Deborah S. *Tribes and Territories in Library and Information Studies Education.* Bruce Uhrmacher, Chair, June 10, 2008, Committee Member.

McCord, J. Michael. *Developing a Standard of Care for Educational Malpractice.* Chair, April 15, 2011.

Priebe, Sarah J. *Distinguishing Effects of Domain and General Knowledge on Passage Fluency and Comprehension.* Jan Keenan, Chair. July 21, 2011, Outside Chair.

Snyder-Mondragon, Sandra M. *Institutional Factors that Impact the Retention of Graduate Students of Color in Schools of Library and Information Science: A Metaregression of Accredited Library School Statistics on Student Retention and Graduation Rates.* Kathy Green, Chair, July 24, 2009, Committee Member.

Taylor, Karen Pickles. *Effective Teaching.* Elinor Katz, Chair, July 15, 2009, Outside Chair.

Thompson, Jennifer. *Distinguishing a Western Women's College: A History of the Curriculum and Student Experience at Colorado Women's College.* Edith W. King, Chair, July 16, 2010, Committee Member.

Walker, Emelda. *Influence of Organizational Factors on Job Satisfaction of Disability Service Providers at Postsecondary Institutions.* Chair, April 29, 2010.

Dissertation Proposals at the University of Denver

Bowers, Stacey L. *Library Anxiety of Law School Students: A Study Utilizing the Multidimensional Library Anxiety Scale.* Chair, November 5, 2009.

McCord, J. Michael. *Developing a Standard of Care for Educational Malpractice.* Edith W. King, Chair. April 23, 2010.

Thompson, Jennifer. *History of Colorado Women's College.* Edith W. King, Chair, October 30, 2008. Committee Member.

Walker, Emelda. *Influence of Organizational Factors on Job Satisfaction of Disability Service Providers at Postsecondary Institutions.* Chair, July 21, 2009.

Dissertations at Other Institutions

Rodríguez-Mori, Howard. *The Information Behavior of Puerto Rican Immigrants to Central Florida, 2003-2009: Grounded Analysis of Six Case Studies Use of Social Networks during the Migration Process.* Kathleen Burnett, Chair, April 10, 2009, Florida State University, Committee Member.

Schwartz, Brian *More than a Look-up Skill: Medical Information Literacy Education in Osteopathic Medical Schools.* D. Mirah Dow, Chair, July 18, 2017. Emporia State University, Committee Member.

Snow, Karen. *A Study of the Perception of Cataloging Quality among Catalogers.* Shawne D. Miksa, Chair, August 1, 2011. University of North Texas, Committee Member.

Dissertation Proposals at Other Institutions

Schwartz, Brian *More than a Look-up Skill: Medical Information Literacy Education in Osteopathic Medical Schools.* D. Mirah Dow, Chair, December 4, 2015. Emporia State University, Committee Member.

Snow, Karen. *A Study of the Perception of Cataloging Quality among Catalogers.* Shawne D. Miksa, Chair, May 11, 2010. University of North Texas, Committee Member.

Master's Thesis at the University of Denver

Hemingson, Jeff. *Recital Paper.* Lamont School of Music, February 2010, Outside Chair.

Capstones at the University of Denver

Anthony, Alisa. *Correlation of Library and Information Science Program outcomes and Vacant Position Qualifications Listed on the Colorado State Library Jobline by Employers During the Period September 1, 2000 through August 31, 2002.* Chair, Winter Quarter, 2003.

Borden, Donna M. *Improving Emergency Communications Systems: Is a Radio Communications Network the Answer?* Fall Quarter, 2014.

Bowden, Heather L.M. *Exploring Biological Models for Long-term Data Preservation.* Chair, Spring Quarter, 2008.

Casenada, Cassandra Y. *Challenges to the Recruitment, Education, and Retention of Librarians of Color.* Chair, Spring Quarter, 2008.

Chang, Jennifer C. *Legal Research Practice and Preference: A Law Firm Perspective.* Chair, Spring Quarter 2011.

Ellis, Megan S. Fitzgerald. *Design of a Public Library Adult Volunteer Recruitment Program and Training Curriculum.* Chair, Winter Quarter, 2003.

Kircher, Kathy. *Development of a Library Pathfinder for Exobiology and Posting it on the Internet.* Chair, Winter Quarter, 2003.

Melhado, Loretta. *Design of St. John's Episcopal Church Library.* Chair, Spring Quarter, 2008.

Radcliff, Kathy. *Original Cataloging of Archival materials in the HERS Collection in Penrose Library.* Chair, Winter Quarter, 2003.

Sass, Carol Ann. *ACT Periodical Index: Access to Catholic Thinking Periodical Index: Web Index to Select Catholic Periodicals.* Spring Quarter 2000.

Stone, Sergio D. *Conducting Community Analysis for the Bemis Public Library (Littleton, Colorado) Using 2002 U.S. Census Data and the Online Outcome-Based Evaluation Toolkit.* Chair, Winter Quarter, 2003.

Tureson, Tamara. *Design and Use of an Information Audit Tool for Use in a Law Library.* Chair, Winter Quarter, 2003.

Tweed, Beth. *Evaluation of Email Reference Service in a Consumer Health Library Environment.* Chair, Winter Quarter, 2003.

GRANTS AND CONTRACTS

Student Learning in Agriculture STEM through Teacher Professional Development. Research team: Stanton Gartin (PI) and Cyndi Hofmeister, Northeast Junior College; Jeff Cash, Cheryl Sánchez, Anne-Marie Crampton, Lamar Community College; Suzanna Spears, Morgan Community College; Jack Wiley, Kerry Gabrielson, Trinidad State Junior College; Michael J. Miller, Colorado State University; Michael Womochil (Co-PI), Casey Sacks, and Sylvia D. Hall-Ellis, Colorado Community College System. U.S. Department of Agriculture, Agriculture and Food Research Initiative, Food, Agriculture, Natural Resources and Human Sciences Education and Literacy Initiative, $404,460 (2017-2020)

Leading and Achieving: the Colorado Agriculture Regional Consortium. Research team: Jack Wiley (PI), Kerry Gabrielson, Trinidad State Junior College; Jeff Cash (PI), Cheryl Sánchez, Anne-Marie Crampton, Lamar Community College; Suzanna Spears, Morgan Community College; Cyndi Hofmeister, Northeast Junior College; Michael Womochil (Co-PI), Casey Sacks, and Sylvia D. Hall-Ellis, Colorado Community College System. U.S. Department of Agriculture, Hispanic Serving Institutions Education Grants Program, $504,414 (2017-2020)

Cyber Prep Program Planning Grant. Research team: Debbie Sagen (PI), Brenda Lauer, Pikes Peak Community College; Gretchen Martin, Koiosa Insights; and, Sylvia D. Hall-Ellis, Colorado Community College System. U.S. Department of Commerce, Regional Alliances and Multi-stakeholder Partnerships to Stimulate (RAMPS) Cybersecurity Education and Workforce Development, $199,681 (2016-2018)

Career and Technical Education in Colorado: Pathways to Education and Employment. Research team: Heather McKay (PI), Rutgers University; Sarah Heath, Casey Sacks, Sylvia D. Hall-Ellis, Colorado Community College System. U.S. Department of Education, Institute of Education Sciences, $1,400,000 (2017-2021)

Pre-Alliance Planning Grant Colorado Community College Alliance. Research team: Victor Vialpondo (PI) and Janel Highfill, Community College of Aurora; Heidi Loshbaugh (Co-PI), Community College of Denver; Rick Reeves, Bill McGreevy, Liz Cox, and Kristin Aslin, Red Rocks Community College; Cathy Pellish, Front Range Community College; Samuel DeVries, Arapahoe Community College; Sylvia D. Hall-Ellis, Colorado Community College System. National Science Foundation, Louis Stokes Alliance for Minority Participation (LSAMP), $86,817 (2016-2017)

Towards Scalable Differentiated Instruction Using Technology-enabled, Competency-based, Dynamic Scaffolding. Research team: Karen Wilcox (PI) and Vijay Kumar, Center for Computational Engineering, Massachusetts Institute of Technology; Flora McMartin, Broad-based Knowledge; Quinsigamond Community College; and, Casey Sacks, and Sylvia D. Hall-Ellis, Colorado Community College System. U.S. Department of Education, First in the World Developmental Grant, $2,891,882 (2015-2019)

Colorado Strategic Partnerships Emergency Grant. Research team: Elise Lowe-Vaughn (PI), Amy Hodson, Celia Hardin, Barbara McBride, James Newby, Christopher Dewhurst, Nina Holland, Kate Anderson, MaryAnn Roe, Chrystalynn Chrystalynn, Elaine Edon, Mona Barnes, Tom Morgan, Rob Hanni, and Marie Valenzuela, Colorado Department of Labor and Employment; Steve Anton, Joelle Brouner, and, Katie Griego, Colorado Department of Human Services; Rebecca Holmes, Judith Martinez, and Jennifer Jirous, Colorado Department of Education; Emily Templin Lesh, Colorado Workforce Development Council; Cory Everett, Colorado Department of Regulatory Agencies; and, Casey Sacks and Sylvia D. Hall-Ellis, Colorado Community College System. U.S. Department of Labor, Strategic Partnerships Emergency Grant, $5,000,000 (2015-2017)

CAEL Jump Start Program: Competency-Based Education. Research team: Jerry Migler (PI), Casey Sacks, Debra Cohn, Thomas Hartman, and Sylvia D. Hall-Ellis, Colorado Community College System; Matt Jamison, Front Range Community College; Mike Coste, Red Rocks Community College; Amanda Corum, Pueblo Community College; Janet Colvin, Pikes Peak Community College; and, MaryAnn Matheny, Community College of Denver. Council for Adult and Experiential Learning, $15,000 (2015)

Summit on the Redesign of Developmental Education. Research team: Jerry Migler (PI), Casey Sacks, and Sylvia D. Hall-Ellis, Colorado Community College System; Chip Nava, Pueblo Community College; Kim Moultney,

Arapahoe Community College; Debbie Ulibarri, Trinidad State Junior College; and, Kris Bernard, Front Range Community College. American Association of Community Colleges, $15,000 (2015-2016)

Equity in Excellence at Colorado Community Colleges. Research team: Keith Howard (PI) and Sylvia D. Hall-Ellis, Colorado Community College System; Estela Mata Bensimon, Center for Urban Education, University of Southern California; and Kerry Gabrielson, Trinidad State Junior College. Colorado Department of Higher Education, Colorado Opportunity Scholarship Program, $150,000 (2015-2016)

MBA High School of Business in Colorado. Research team: Laurie Urich (PI) and Sylvia D. Hall-Ellis, Colorado Community College System; Rudolph Sumpter and Beatrice Gerrish, Boulder Valley Schools; Keith Curry Lance, RSL Research Group. Colorado Department of Higher Education, Colorado Opportunity Scholarship Program, $501,295 (2015-2016)

Fullbridge Program in Colorado. Research team: Keith Howard (PI) and Sylvia D. Hall-Ellis, Colorado Community College System; Suzanna Spears, Fort Morgan Community College; and, Cheryl Sánchez and Anne-Marie Compton, Lamar Community College. Colorado Department of Higher Education, Colorado Opportunity Scholarship Program, $300,000 (2015-2017)

Colorado Community College System Alternative Credit Program. Research team: Jerry Migler (PI), Keith Howard, and Sylvia D. Hall-Ellis, Colorado Community College System. American Council on Education, $13,000 (2015)

Internationalization in Higher Education. Researcher: Samuel D. Museus. Technical reviewer for MCE: Sylvia D. Hall-Ellis. University of Denver, Office of Internationalization, $8,000 (2014-2015)

International Perspectives on Bilingual Education. Researcher: Sharolyn Pollard-Durodola. Technical reviewer for MCE: Sylvia D. Hall-Ellis. University of Denver, Office of Internationalization, $3,700 (2014-2015)

Cultivating Culturally Relevant and Responsive Curriculum and Pedagogy in College. Researcher: Samuel Museus. Technical reviewer for MCE: Sylvia D. Hall-Ellis. University of Denver, iRise Grant, $5,000 (2014-2015)

Project EMERGE (Educational Model for Evaluation and Replicability in Gifted Environments). Research team: Norma Hafenstein (PI) and Bruce Uhrmacher. Technical reviewer for MCE: Sylvia D. Hall-Ellis. Lynde and Harry Bradley Foundation, $235,000 (2014-2015)

Collecting Asian American Refugee Stories. Researcher: Samuel Museus. Technical reviewer for MCE: Sylvia D. Hall-Ellis. American Educational Research Association, Research Grant, $5,000 (2014-2015)

Developing Expertise in Teaching K-5 Mathematics. Research team: Julie Sarama (PI) and Douglas H. Clements (Co-PI), in partnership with the School of Education at the University of Michigan. Technical reviewer for MCE: Sylvia D. Hall-Ellis. National Science Foundation, $130,344 (2013-2015)

Investigation of the Long-Term Outcomes for Special Education Students. Researcher: Antonio Olmos-Gallos. Technical reviewer for MCE: Sylvia D. Hall-Ellis. Jefferson County School District, Office of Assessment, $40,000 (2014)

Refugee Community Collaboration. Researcher: Vicki Tomlin (PI) in partnership with the African Community Center and Jewish Family Service. Technical reviewer for MCE: Sylvia D. Hall-Ellis. University of Denver, Center for Community Engagement and Service Learning, $14,854 (2014-2015)

Access to Mathematics for All. Research team: Richard S. Kitchen (PI), Nicole M. Russell (Co-PI), and Terrence Blackman (Co-PI), Curriculum Studies and Teaching Program, Morgridge College of Education; Álvaro Árias (Co-PI, Department of Mathematics); and, James Gray (Co-PI), Department of Mathematics, Community

College of Aurora. Technical reviewer for MCE: Sylvia D. Hall-Ellis. National Science Foundation, The Robert Noyce Scholarship Program, Capacity Building Project, $349,926 (2014-2016)

Cognitive Test Battery for Intellectual Disabilities. Research team: Karen Riley (PI), Lyndsay Agans, Jessica Lerner, and Karin Dittrick-Nathan in partnership with David Hessl (PI), The MIND Institute at the University of California – Davis, and Elizabeth Berry-Kravis, Rush University Medical Center. Technical reviewer for MCE: Sylvia D. Hall-Ellis. National Institutes of Health, Outcome Measures for Use in Treatment Trials for Individuals with Intellectual and Developmental Disabilities (R01), $2,499,996 ($588,672 at DU) (2014-2019)

Broadening Participation in Engineering among Women and Latino/as: A Longitudinal, Multi-Site Study. Researcher: Patton Garriott (PI) in partnership with the University of North Dakota and the University of Missouri. Technical reviewer for MCE: Sylvia D. Hall-Ellis. National Science Foundation, HER Core Research, $677,390 ($69,992 at DU) (2014-2019)

Designing a Teacher Evaluation System to Improve Teacher Effectiveness for Culturally and Linguistically Diverse Learners. Research team: María del Carmen Sálazar (PI), Jessica Lerner, and Kathy Green. Technical reviewer for MCE: Sylvia D. Hall-Ellis. University of Denver, Professional Research Opportunities for Faculty, $29,988 (2014-2016)

Developing a College-Going Culture in Latina/O Families: Exploring the Influence of Funds of Knowledge on Family Outreach Programs. Researcher: Judy Marquez Kiyama. Technical reviewer for MCE: Sylvia D. Hall-Ellis. University of Denver, Professional Research Opportunities for Faculty, $18,720 (2014-2016)

Assessment of Quality of Life in Neutral Implantation Surgery for the Treatment of Parkinson's Disease. Researcher: Cynthia McRae. Technical reviewer for MCE: Sylvia D. Hall-Ellis. University of Denver, Office of Internationalization, $3,967 (2014-2015)

Pura Vida: Cloud Forest, Curriculum and Cross-Cultural Study. Research team: Norma Hafenstein (PI) and Bruce Uhrmacher (Co-PI). Technical reviewer for MCE: Sylvia D. Hall-Ellis. University of Denver, Office of Internationalization, $8,000 (2014-2015)

Online Course Development for Curriculum and Instruction. Researcher: Ruth Chao. Technical reviewer for MCE: Sylvia D. Hall-Ellis. University of Denver, Office of Teaching and Learning, $3,000 (2014)

Online Course Development for Curriculum and Instruction. Researcher: María del Carmen Sálazar. Technical reviewer for MCE: Sylvia D. Hall-Ellis. University of Denver, Office of Teaching and Learning, $3,000 (2014)

Online Course Development for Curriculum and Instruction. Researcher: Jessica Lerner. Technical reviewer for MCE: Sylvia D. Hall-Ellis. University of Denver, Office of Teaching and Learning, $3,000 (2014)

Online Course Development for Curriculum and Instruction. Researcher: Duan Zhang. Technical reviewer for MCE: Sylvia D. Hall-Ellis. University of Denver, Office of Teaching and Learning, $3,000 (2014)

The Mathematics Education of African Americans, 1866 – 1954. Researcher: Nicole M. Russell. Technical reviewer for MCE: Sylvia D. Hall-Ellis. National Academy of Education, Spencer Foundation Postdoctoral Fellowship, $55,000 (2014-2016)

Early Childhood Care and Education Study. Research team: Carrie Germeroth (PI), Melissa Mincic, and Douglas H. Clements. Technical reviewer for MCE: Sylvia D. Hall-Ellis. State of North Dakota, Department of Public Instruction, $73,500 (2013-2014)

Graduate Level Specialty in Addiction Counselor Training with Emphasis on Integration of Native American Specific Content. Research team: Ruth Chao (PI) and Michael J. Faragher (Co-PI). Technical reviewer for MCE: Sylvia D. Hall-Ellis. The Galena Foundation, $289,732 (2013-2016)

The Collecting Asian American and Pacific Islander Refugee Stories (CARS) Project. Researcher: Samuel Museus. Technical reviewer for MCE: Sylvia D. Hall-Ellis. University of Denver, Center for Community Engagement and Service Learning, $15,000 (2014)

Parents in Transition: A Multiple Case Study of Parent and Family Orientation Programs. Researcher: Judy Marquéz Kiyama. Technical reviewer for MCE: Sylvia D. Hall-Ellis. University of Denver, Faculty Research Fund, $1,500 (2014-2015)

The Sistah Network: Black Women Graduate Students Supporting and Retaining Each Other. Researcher; Nicole M. Russell. Technical reviewer for MCE: Sylvia D. Hall-Ellis. University of Denver, Faculty Research Fund, $2,708 (2014-2015)

Evaluation of the Northeast Denver Babies Ready for College Program. Research team: Carrie Germeroth (PI), Melissa Mincic, and Douglas H. Clements. Technical reviewer for MCE: Sylvia D. Hall-Ellis. Mile High Montessori, $9,922 (2013-2014)

Developing Teaching Expertise in K-5 Mathematics. Research team: Julie Sarama (PI) and Douglas Clements (University of Denver), in partnership with Timothy Boerst (PI), Meghan Shaughnessy, Deborah Ball, Hyman Bass (School of Education at the University of Michigan). Technical reviewer for MCE: Sylvia D. Hall-Ellis. National Science Foundation, $449,827 ($130,344 at the University of Denver (2013-2015)

Early Learning Care and Education Study Program Grant for the State of North Dakota. Research team: Carrie Germeroth (PI), Melissa Mincic, and Sheridan Green. Technical reviewer for MCE: Sylvia D. Hall-Ellis. State of North Dakota Department of Public Instruction, $73,500 (2013-2014)

Local Professional Learning Community for School Leaders. Research team: Susan Korach (PI), Kristina Hesbol, and Rebecca McClure. Technical reviewer for MCE: Sylvia D. Hall-Ellis. Education Development Center, $10,950 (2013)

Healthy Eaters, Lifelong Movers 2: Implementing Evidence-Based School Environment, Policy, and Curricular Changes to Increase Opportunities for Healthy Eating and Physical Activity in Low Income, Rural Colorado. Research team: Elaine Berlansky, University of Colorado at Denver (PI), Nicholas Cutforth, University of Denver (Co-PI), and Allison Reeds. Technical reviewer for MCE: Sylvia D. Hall-Ellis. Colorado Health Foundation, $3,103,108 (2013-2017)

Hughes Rare Books Library Room Renovation in the Sturm College of Law. Project team: Patti H. Marks, Sylvia D. Hall-Ellis, and Leigh Elliott. Mabel T. Hughes Charitable Trust, $34,000 (2013-2014)

The Promise Center Partnership with the Marsico Institute for Early Learning and Literacy and the City and County of Denver. Research team: Karen Riley (PI), Douglas H. Clements (Co-PI), and Sheridan Green. Technical reviewer for MCE: Sylvia D. Hall-Ellis. The Piton Foundation, $223,468 (2013-2014)

Center of Excellence for Problem Gambling. Research team: Ruth Chao (PI) and J. Mike Faragher. Technical reviewer for MCE: Sylvia D. Hall-Ellis. Colorado Department of Behavioral Health, $68,021 (2012-2013)

United Way Implementation and Validation Review. Research team: Douglas H. Clements (PI), Amanda Moreno, and Sheridan Green. Technical reviewer for MCE: Sylvia D. Hall-Ellis. Mile High United Way, $19,737 (2013)

Math/Science Partnership in Rural Districts. Research team: Kristen Bunn (PI, Eagle County Schools), Paul Michalec (Co-PI), and Alegra Reiber. Technical reviewer for MCE: Sylvia D. Hall-Ellis. Colorado Department of Education, Colorado's Mathematics and Science Partnership Program, $750,000 (2013-2014)

Mathematics and Science Education of African Americans. Research team: Nicole Russell (PI), Sylvia D. Hall-Ellis, Steve Fisher (Penrose Library). Technical reviewer for MCE: Sylvia D. Hall-Ellis. University of Denver, Professional Research Opportunities for Faculty, $29,994 (2013-2015)

Online Course Development for Curriculum and Instruction. Researcher: Nicole Russell. Technical reviewer for MCE: Sylvia D. Hall-Ellis. University of Denver, Office of Teaching and Learning, $3,000 (2013)

Discourse and Opportunity: Undocumented Students and Higher Education Policy. Researcher: Ryan Gildersleeve. Technical reviewer for MCE: Sylvia D. Hall-Ellis. National Academy of Education, Spencer Foundation Postdoctoral Fellowship, $55,000 (2012-2014)

An Anthropological Study of the Latino Graduation Ceremony. Researcher: Ryan Gildersleeve. Technical reviewer for MCE: Sylvia D. Hall-Ellis. Spencer Foundation, $39,900 (2012-2013)

Fragile-X and Pharmaceutical Company: Clinical Trial of AFQ056. University of California – Davis Children's Hospital MIND Institute (Sacramento), Children's Hospital Denver, and Rush Children's Hospital at Rush University Medical Center (Chicago). Karen Riley, PI. Technical reviewer for MCE: Sylvia D. Hall-Ellis. Novartis Pharmaceuticals Corporation, $394,206 (2012-2014)

Project Engage, Phase 2, a DAPRA Grant in partnership with Total Immersion Systems, Inc., and Texas A&M University. Research team: Karen Riley (PI) and Lyndsay Agans (Co-PI). Technical reviewer for MCE: Sylvia D. Hall-Ellis. U.S. Department of Defense, $60,000 (2011-2013)

International School Psychology Practicum Exchange. Researcher: Gloria L. Miller. Technical reviewer for MCE: Sylvia D. Hall-Ellis. University of Denver, Center for Community Engagement and Service Learning, $14,951 (2012-2013)

Online Course Development for Curriculum and Instruction. Research team: Bruce Uhrmacher (PI) and Norma Hafenstein (Co-PI). Technical reviewer for MCE: Sylvia D. Hall-Ellis. University of Denver, Office of Teaching and Learning, $18,193 (2012-2014)

Writers in the Schools. Research team: Karen Riley (PI) and Amanda Moreno (Co-PI).Technical reviewer for MCE: Sylvia D. Hall-Ellis. Colorado Humanities, $4,965 (2012-2013)

Learning Ecosystem Validation Grant. Research team: Karen Riley (PI), Lyndsay Agans, Kent Seidel, and Shimelis Assefa. Technical reviewer for MCE: Sylvia D. Hall-Ellis. Bill & Melinda Gates Foundation, $315,000 (2012-2013)

Project Words of Oral Reading and Language Development (WORLD). Research team: Jorge E. Gonzalez (PI), Texas A&M University; Laura Saenz (Co-PI), University of Texas – Pan American; and, Sharolyn Pollard-Durodola (Co-PI), University of Denver. Technical reviewer for MCE: Sylvia D. Hall-Ellis. U.S. Department of Education, Institute of Education Sciences, $53,354 (2012-2015); award $640,718, transfer from Texas A&M University

Increasing the Efficacy of an Early Mathematics Curriculum with Scaffolding Designed to Promote Self-Regulation. Research team: Douglas H. Clements (PI) and Julie Sarama (Co-PI). Technical reviewer for MCE: Sylvia D. Hall-Ellis. U.S. Department of Education, Institute of Education Sciences, $1,445,315 (2008-2014); award $4,541,975, transfer from University at Buffalo, The State University of New York

Using Rule Space and Poset-based Adaptive Testing Methodologies to Identify Ability Patterns in Early Mathematics and Create a Comprehensive Mathematics Ability Test. Research team: Douglas H. Clements (PI) and Julie Sarama (Co-PI). Technical reviewer for MCE: Sylvia D. Hall-Ellis. National Science Foundation, $323,791 (2010-2014); award $1,194,944, transfer from University at Buffalo, The State University of New York

Comprehensive Postdoctoral Training in Scientific Education Research. Researcher: Julie Sarama (PI). Technical reviewer for MCE: Sylvia D. Hall-Ellis. U.S. Department of Education, Institute of Education Sciences, $133,458 (2010-2014); award $613,353, transfer from University at Buffalo, The State University of New York

Longitudinal Study of a Successful Scaling Up Project: Extending TRIAD. Research team: Douglas H. Clements (PI), Julie Sarama (Co-PI), and Abt Associates (Carolyn Layzer, Fatih Unlu, Laurie Bozzi, Lily Fesler, Alina Martinez, Cristofer Price, James van Orden). Technical reviewer for MCE: Sylvia D. Hall-Ellis. Institute of Education Sciences, $384,940 (2011-2015; award $1,250,286, transfer from University at Buffalo, The State University of New York

Early Childhood Education in the Context of Mathematics, Science, and Literacy. Research team: Julie Sarama (PI), Douglas H. Clements (Co-PI). Technical reviewer for MCE: Sylvia D. Hall-Ellis. National Science Foundation, $990,020 (2010-2014; award $2,285,228, transfer from University at Buffalo, The State University of New York

Early Childhood Clearinghouse Information Center Redesign. Research team: Karen Riley (PI) and Amanda Moreno (Co-PI).Technical reviewer for MCE: Sylvia D. Hall-Ellis. Office of the Lt. Governor of Colorado, $12,000 (2012-2013)

Morgridge Rural Educational Leadership Initiative. Research team: Lyndsay Agans (PI), Linda Brookhart (Co-PI), Susan Korach, and Rebecca McClure. Technical reviewer for MCE: Sylvia D. Hall-Ellis. Morgridge Family Foundation, $100,000 (2012-2014)

Center of Excellence for Problem Gambling. Research team: Patrick Sherry (PI) and J. Mike Faragher. Technical reviewer for MCE: Sylvia D. Hall-Ellis. Colorado Department of Behavioral Health, $55,000 (2012-2013)

Intermodal Transportation Institute Research Initiatives. Researcher: Patrick Sherry. Technical reviewer for MCE: Sylvia D. Hall-Ellis. University Transportation Centers Program, Research and Innovative Technology Administration, U.S. Department of Transportation. $600,000 (2012-2014)

Mile High United Way Social Innovation Fund Early Literacy Initiative. Gloria L. Miller, PI, Amanda Moreano, Kim Hartnett-Edwards, and Sheridan Green. Technical reviewer for MCE: Sylvia D. Hall-Ellis. Mile High United Way, $89,992 (2012-2013)

International School Psychology Practicum Exchange. Researcher: Gloria L. Miller. Technical reviewer for MCE: Sylvia D. Hall-Ellis. University of Denver, Center for Community Engagement and Service Learning, $1,000 (2012-2013)

Refugee Student Art Outreach. Researcher: Karin Dittrick-Nathan. Technical reviewer for MCE: Sylvia D. Hall-Ellis. University of Denver, Faculty Research Fund, $3,000 (2012-2013)

Resistance, Resilience, and Reciprocity: Centering the Voices of Black Doctoral Women with Faculty Aspirations. Researcher: Nicole M. Russell. Technical reviewer for MCE: Sylvia D. Hall-Ellis. University of Denver, Faculty Research Fund, $2,965 (2012-2013)

Assessing Learning through Student Notebooks. Research team: Keith Miller, Nancy Sasaki, and Kathy Green. Technical reviewer for MCE: Sylvia D. Hall-Ellis. University of Denver, Professional Research Opportunities for Faculty, $30,000 (2012-2014)

International School Psychology Practicum Exchange. Researcher: Gloria L. Miller. Technical reviewer for MCE: Sylvia D. Hall-Ellis. University of Denver, Office of Internationalization, $2,000 (2012-2013)

ELO in Colorado. Research team: Cynthia Hazel and Duan Zhang. Technical reviewer for MCE: Sylvia D. Hall-Ellis. Colorado Legacy Foundation, $150,000 (2012-2013)

Creating Online LIS Courses. Research team: Mary C. Stansbury (PI), Shimelis Assefa, Denise Anthony, Xiao Hu, and Krystyna Matusiak. Technical reviewer for MCE: Sylvia D. Hall-Ellis. University of Denver, Center for Teaching and Learning, $15,000 (2011-2013)

Maritime Piracy Seminar. Researcher: Ved Nanda, The Nanda Center, Sturm College of Law. Technical reviewer for Sturm College of Law: Sylvia D. Hall-Ellis. Arsenault Family Foundation, $15,000 (2012-2013).

Early Childhood Librarianship: An Interdisciplinary, Experiential Learning MLIS. Researcher: Mary C. Stansbury (PI). Technical reviewer for MCE: Sylvia D. Hall-Ellis. Laura Bush's 21st Century Librarians Program, Institute for Museums and Library Services, $249,066 (2012-2014)

Learning Ecosystem Planning Grant. Research team: Karen Riley (PI), Lyndsay Agans, Kent Seidel, and Shimelis Assefa. Technical reviewer for MCE: Sylvia D. Hall-Ellis. Bill & Melinda Gates Foundation, $281,217 (2011-2012)

Advanced Service Learning Practitioner Faculty Grant, Sylvia D. Hall-Ellis, University of Denver, Center for Community Engagement and Service Learning, $400 (2011)

Evaluating and Enhancing the EspeciallyMe Program. Research team: Lori D. Patton and Nicole Russell. Technical reviewer for MCE: Sylvia D. Hall-Ellis. University of Denver, Center for Community Engagement and Service Learning, Public Good Fellowship Grant, $24,780 (2012)

Choosing Excellence: Let Every Child Bloom. Research team: Shimelis Assefa (PI) and Mary C. Stansbury (Co-PI). Technical reviewer for MCE: Sylvia D. Hall-Ellis. University of Denver, Center for Community Engagement and Service Learning, Public Good Grant, $7,657 (2012)

K-8 STEM Content Specific Professional Development to Improve Elementary Student Achievement. Research team: Kent Seidel (PI), Nicole Russell (Co-PI), Kimberly Hartnett-Edwards, Paul Michalec, Jeff Farmer, Keith Miller, Alegra Reiber, and Nancy Sasaki. Technical reviewer for MCE: Sylvia D. Hall-Ellis. Colorado Department of Education, Improving Teacher Quality Grant, (Title II ESEA), $307,299 (2011-2012)

Building a Better Principal Pipeline to Boost Student Achievement. Researcher: Susan Korach. Technical reviewer for MCE: Sylvia D. Hall-Ellis. Denver Public Schools; a subcontract from the Wallace Foundation Grant, $170,000 (2011-2017)

Center of Excellence for Problem Gambling. Research team: J. Mike Faragher (Co-PI) and Bobbie Vollmer (PI). Technical reviewer for MCE: Sylvia D. Hall-Ellis. Colorado Department of Behavioral Health, $79,999 (2011-2012)

An Exploration of Novice Teachers' Core Competencies: Impacts on Student Achievement, and Effectiveness of Preparation. Research team: Kent Seidel (PI), Kathy Green (Co-PI), Kimberly Hartnett-Edwards, and Duan Zhang. Technical reviewer for MCE: Sylvia D. Hall-Ellis. Institute of Education Sciences, Effective Teachers and Effective Teaching, $990,987 (2012-2015)

Project Engage, a DAPRA Grant in partnership with Total Immersion Systems, Inc., and Texas A&M University. Research team: Karen Riley (PI) and Lyndsay Agans (Co-PI). Technical reviewer for MCE: Sylvia D. Hall-Ellis. U.S. Department of Defense, $49,964 (2011-2014)

User-centered Evaluation of Music Search Engines. Researcher: Xiao Hu. Technical reviewer for MCE: Sylvia D. Hall-Ellis. University of Denver, Faculty Research Fund, $2,931 (2011-2012)

Educational Practicum in Vietnam and China to Promote the Inclusion of Young Children with Disabilities. Researcher: Gloria L. Miller. Technical reviewer for MCE: Sylvia D. Hall-Ellis. University of Denver, Office of Internationalization, $5,000 (2011-2012)

Evaluation of Colorado's Enhancing Quality in Infant-Toddler (EQIT) Initiative. Research team: Virginia R. Maloney and Amanda Moreno. Technical reviewer for MCE: Sylvia D. Hall-Ellis. Buell Foundation, $395,884 (2011-2013)

Creating Engaging Environments to Teach Pre-Algebra Mathematics to Elementary Students. Research team: Álvaro Arias, Mario López, María del Carmen Salazar, and Lyndsay Agans. Technical reviewer for MCE: Sylvia D. Hall-Ellis. University of Denver Interdisciplinary Grant, $60,000 (2011-2012)

Morgridge Education Technology Accessible (META) Resource Project. Research team: Lyndsay Agans (PI) and Shimelis Assefa (Co-PI). Technical reviewer for MCE: Sylvia D. Hall-Ellis. Morgridge Family Foundation, $36,000 (2011)

MCE Connect: A 21st Century Framework for Faculty Development. Research team: Bruce Uhrmacher (PI), Shimelis Assefa (Co-PI), Lyndsay Agans (Co-PI), Kimberly Hartnett-Edwards, Norma Hafenstein, Xiao Hu, Paul Michalec (Co-PI), María del Carmen Salazar (Co-PI), and Sandra Snyder-Mondragon. Technical reviewer for MCE: Sylvia D. Hall-Ellis. University of Denver, Center for Teaching and Learning, $22,355 (2011-2012)

Parent Education and Parent Leadership and Advocacy. Research team: Virginia Maloney (PI) and Amanda Moreno, Marsico Institute for Early Learning and Literacy. Technical reviewer for MCE: Sylvia D. Hall-Ellis. Colorado Health Foundation, $27,358 (2010-2011)

Intentional School Culture. Researcher: Cynthia Hazel. Technical reviewer for MCE: Sylvia D. Hall-Ellis. Denver Public Schools, $38,040 (2010-2011)

Healthy Eaters, Lifelong Movers: Implementing Evidence-Based School Environment, Policy, and Curricular Changes to Increase Opportunities for Healthy Eating and Physical Activity in Low Income, Rural Colorado. Research team: Elaine Berlansky, University of Colorado at Denver (PI), Nicholas Cutforth, University of Denver (Co-PI), and Allison Reeds. Technical reviewer for MCE: Sylvia D. Hall-Ellis. Colorado Health Foundation, $1,683,277 (2011-2014)

Second Life Learning Community. Research team: Don McCubbrey (PI), Sylvia D. Hall-Ellis (Co-PI), Walter LaMendola, and Paul Novak. University of Denver, Center for Teaching and Learning, $13,000 (2010-2011)

Reintroducing the Value of Law Librarians to Academic and Public Librarians in Colorado through the Identification and Use of Emerging Technologies. Research team: Sylvia D. Hall-Ellis (Co-PI), Stacey L. Bowers (PI), and Christopher Hudson, in partnership with Denver Public Library, Arapahoe Library District, and the Colorado State Supreme Court Library. University of Denver, Center for Community Engagement and Service Learning, $5,773 (2010-11)

Reintroducing the Value of Law Librarians to Public Librarians through the Identification and Use of Emerging Technologies and Resources. Research team: Stacey Bowers (PI) and Sylvia D. Hall-Ellis (Co-PI). American Association of Libraries, Wolters Kluwer Law & Business Grant Program, $2,725 (2010-2011)

Faculty Service Learning Pod. Research team: María del Carmen Salazar and Nicholas Cutforth (Curriculum and Instruction Program), Frank Tuitt (Higher Education Program), Cynthia Hazel and Gloria Miller (Child, Family, and School Psychology Program), and Sylvia D. Hall-Ellis (Library and Information Science Program). University of Denver, Center for Community Engagement and Service Learning, $8,000 (2010-2011)

Lincoln Collaborative. Research team: Antonio Esquibel (Principal, Lincoln High School), María del Carmen Salazar (Curriculum and Instruction Program), and. Sylvia D. Hall-Ellis. School Improvement Grant, Denver Public Schools, $375,000 (2010-2012)

Future LEADers of America: Leaders III. Research team: Denver Public Library (Kristen Svendson, PI), the University of Denver (Sylvia D. Hall-Ellis), the Colorado Chapter of REFORMA (Orlando Archibeque), and the Colorado Association of Libraries (Martin Garnar). Laura Bush's Recruiting Librarians for the 21st Century Program, Institute for Museums and Library Services, $988,366 (2009-2012)

Teaching for Success in the Library Environment: LIS 4030 in Library 2.0. Research team: Deborah S. Grealy (PI) and Sylvia D. Hall-Ellis (Co-PI). University of Denver, Center for Teaching and Learning, $ 9,350 (2009-10)

Writing Group Faculty Grant, Sylvia D. Hall-Ellis, University of Denver, Center for Community Engagement and Service Learning, $750 (2008-2009)

Collaborative Learning Faculty Grant, Sylvia D. Hall-Ellis, University of Denver, Center for Teaching and Learning, $1,500 (2008)

Connecting Information Literacy to Learning. Research team: Lori Micho, Merrie Valliant, Amanda Samland, and Sylvia D. Hall-Ellis. Colorado State Library, LSTA Discretionary Grant Program, $19,548 (2008-2009)

Law Librarianship Fellows Program. Research team: Sylvia D. Hall-Ellis (PI), Stacey Bowers (Co-PI), and Christopher Hudson, Westminster Law Library. Laura Bush's 21st Century Librarians Program, Institute for Museums and Library Services, $999,370 (2008-2012)

Grant Writing in a Cooperative Learning Environment. Sylvia D. Hall-Ellis. University of Denver, Center for Teaching and Learning, $2,000 (2008-2009)

Project Homeless Connect 6 Event Evaluation. Research team: Sylvia D. Hall-Ellis and Duan Zhang. University of Denver Center for Community Engagement and Service Learning, $9,785 (2008)

Project Ecuador: International Learning Service Libraries – A Faculty Development Experience in Ecuador. Sylvia D. Hall-Ellis, Office of Internationalization, University of Denver, $600 (2007)

Project Ecuador: International Learning Service Libraries – A Faculty Development Experience in Ecuador. Sylvia D. Hall-Ellis, International Service Learning Office, University of Denver, $400 (2007)

Project Homeless Connect 5 Event Evaluation. Research team: Sylvia D. Hall-Ellis and Duan Zhang. University of Denver Center for Community Engagement and Service Learning, $1,000 (2007)

Project Homeless Connect 4 Event Evaluation. Research team: Sylvia D. Hall-Ellis and Duan Zhang. University of Denver Center for Community Engagement and Service Learning, $4,595 (2007)

Future LEADers of America: Leaders II. Research team: Denver Public Library (Kristen Svendson, PI), the University of Denver (Sylvia D. Hall-Ellis), and the Colorado Chapter of REFORMA (Orlando Archibeque). Laura Bush's Recruiting Librarians for the 21st Century Program, Institute for Museums and Library Services, $988,518 (2007-2010)

Strategic Planning Assistance for the Denver Medical Library. Sylvia D. Hall-Ellis. Denver Medical Library, Inc., $30,000 (2006-2007)

Destiny Software for JMAC Student Lab. Sylvia D. Hall-Ellis, gift from the Sagebrush Corporation, Minneapolis, Minnesota, $10,000 (2006)

Libraries: Tools for Education and Development Worldwide: A Faculty Development Experience in France. Sylvia D. Hall-Ellis, Office of Internationalization, University of Denver, $800 (2005)

Denver Public Library: Opportunities for Change. Sylvia D. Hall-Ellis, Colorado Community Based Research Network, $2,000 (2005)

Future LEADers of America. Research team: Denver Public Library (Letty Icolari and Steve Taylor, PIs), Emporia State University (Jim Agee), and the University of Denver (Sylvia D. Hall-Ellis). Recruiting Librarians for the 21st Century Program, Institute for Museums and Library Services, $670,315 (2005-2008)

American Association of University Professors Summer Institute Professional Development Grant. Sylvia D. Hall-Ellis, American Association of University Professors, $300 (2005)

Beta Phi Mu Alumni Tea. Sylvia D. Hall-Ellis, gift from the Office of Alumni and Parent and Relations, University of Denver, $2,000 (2005)

Spectrum Software for LIS Student Lab. Sylvia D. Hall-Ellis, gift from the Sagebrush Corporation, Minneapolis, Minnesota, $5,000 (2005)

Developing Research Capacity in Community Organizations and Residents through Training and Technical Assistance. Nicholas J. Cutforth (PI) and Sylvia D. Hall-Ellis. Piton Foundation, $25,000 (2005-2006)

Libraries: Tools for Education and Development Worldwide: A Faculty Development Experience in Argentina. Sylvia D. Hall-Ellis, Office of Internationalization, University of Denver, $500 (2004)

Developing Research Capacity in Community Organizations and Residents through Training and Technical Assistance. Research team: Nicholas J. Cutforth (PI), Gary Lichtenstein and Sylvia D. Hall-Ellis, Piton Foundation, $25,000 (2003-2004)

Increasing Spanish-Speaking and Hispanic Diversity among Library and Information Science Students at the University of Denver: Development of a Student Recruitment Model. Researcher: Sylvia D. Hall-Ellis (PI), Office of Multicultural Excellence, University of Denver, $2,750 (2003-2004)

Collection Development Enrichment to Support the Cataloging & Classification Specialization and School Librarianship within the Library & Information Science Program at the University of Denver. Research team: Sylvia D. Hall-Ellis (PI) and Deborah S. Grealy. Women's Library Association, University of Denver, $4,000 (2003)

Collection Development Enrichment to Support the Library & Information Science Program at the University of Denver. Research team: Deborah S. Grealy (PI) and Sylvia D. Hall-Ellis. Women's Library Association, University of Denver, $4,000 (2001)

Wireless LAN for Library Education. Research team: Deborah S. Grealy (PI) and Sylvia Hall-Ellis. University of Denver, Center for Teaching and Learning, $24,000 (2001-2002)

Upward Bound – A Program for South Texas Youth. Research team: Monte Churchill, Executive Director of Community Relations; Gary R. Sauceda, Outreach Coordinator; Raymond Hernandez, (PI) Associate Dean for Student Success; and Sylvia D. Hall-Ellis, South Texas Community College (McAllen, Texas). U.S. Department of Education, Office of Postsecondary Education, $2,672,003 (1999-2003)

Write Now! Improving Elementary Students' Writing Skills. Research team: Caryl G. Thomason, Assistant Superintendent (PI); Karen Tankersley, Principal; and, Hal Anderson, Director of Technology, Cheyenne Mountain School District 12 (Colorado Springs, Colorado); and Sylvia D. Hall-Ellis. Colorado Department of Education, Educational Telecommunications Unit, $189,453 (1999-2001)

Operation Quick Start -- Distance Learning in Rural Colorado. Research team: Randal Weigum, Technology Coordinator (PI); Bonnie Barns, Director of Federal Programs and Staff Development; and, Adam "Joe" Raskop, Executive Director, Southeastern Board of Cooperative Educational Services (Lamar, Colorado); and Sylvia D. Hall-Ellis. Colorado Department of Education, Educational Telecommunications Unit, $400,000 (1999-2001)

Advanced Technological Training for Information Professionals for the 21st Century. Research team: Mario Reyna, Division of Business Director (PI) and Sylvia D. Hall-Ellis, South Texas Community College (McAllen, Texas). Phi Delta Kappa and the National Science Foundation, $250,000 (1999-2001)

Working Connections – Training Information Technologies Professionals for the 21st Century. Research team: Mario Reyna, Division of Business Director (PI) and Sylvia D. Hall-Ellis, South Texas Community College

(McAllen, Texas). Microsoft Corporation and the American Association of Community Colleges, $1,147,775 (1999-2001)

The ROAD (Research Oriented Amplification of Development to Literacy) Program. Research team: Deborah J. Leong (PI), Metropolitan State University; Elena Bodrova, Metropolitan State University; Dmitri Semenov, Robert J. Marzano, and Sylvia D. Hall-Ellis, Mid-continent Regional Educational Laboratory (Aurora, Colorado). Hewlett-Packard Foundation, $25,000 (1998-1999)

Press to Literacy. Research team: Deborah J. Leong (PI), Metropolitan State University; Elena Bodrova, Metropolitan State University; Dmitri Semenov, Robert J. Marzano, and Sylvia D. Hall-Ellis, Mid-continent Regional Educational Laboratory (Aurora, Colorado). The Denver Post and the Robert S. McCormick Foundation, $49,818 (1998-1999)

International Telementor Center. Research team: David Neils, David B. Frost (PI), and Sylvia D. Hall-Ellis, Mid-continent Regional Educational Laboratory (Aurora, Colorado). Hewlett-Packard Philanthropy, $100,000 (1998-1999)

America Reads: Providing Tutor Training for the America Reads Challenge. Research team: Louis F. Cicchinelli (PI) and Sylvia D. Hall-Ellis, Mid-continent Regional Educational Laboratory (Aurora, Colorado). U.S. Department of Education, Office of Educational Research and Improvement, $306,000 (1998-1999)

Comprehensive School Reform. Research team: Louis F. Cicchinelli (PI), J. Timothy Waters, and Sylvia D. Hall-Ellis, Mid-continent Regional Educational Laboratory (Aurora, Colorado). U.S. Department of Education, Office of Educational Research and Improvement, $285,000 (1998-1999)

Sustainable Energy Education (SEE) Program for Grades 4-8: Preparing Today's Youth for Lifelong Learning and Responsible Actions in Energy Conservation. Research team: Mary Gromko, Colorado Department of Education; Gene McCarthy, Rocky Flats Field Office, U.S. Department of Energy; Gina Kissell, National Renewable Energy Laboratory; and Barbara L. McCombs (PI), Janet L. Bishop, and Sylvia D. Hall-Ellis, Mid-continent Regional Educational Laboratory (Aurora, Colorado). State of Colorado Governor's Office for Energy Conservation, $499,936 (1997-1999)

Review of Kansas Curriculum Standards in Mathematics and Language Arts. Research team: Robert J. Marzano (PI), John S. Kendall, David B. Frost, and Sylvia D. Hall-Ellis, Mid-continent Regional Educational Laboratory (Aurora, Colorado). Submitted to the Kansas State Department of Education, $25,903 (1998)

International Telementor Center. Research team: David Neils, John Kuglin, Chris Rapp, David B. Frost (PI), and Sylvia D. Hall-Ellis, Mid-continent Regional Educational Laboratory (Aurora, Colorado). Hewlett-Packard Company, $54,752 (1998)

Genesis Mission: Education Public Outreach. Developed in partnership by the Jet Propulsion Laboratory, California Institute of Technology, Los Alamos National Laboratory, Lockheed Martin Astronautics, and the Mid-continent Regional Educational Laboratory (Aurora, Colorado). Research team: John T. Sutton (PI), Alice Krueger, Martha Henry, Greg Rawls, Shae Isaacs, Jeff Johnson, Deb Jordan, Arlene Mitchell, David B. Frost, Jana Caldwell, J. Timothy Waters, and Sylvia D. Hall-Ellis. National Aeronautics and Space Administration, $139,700,000; subcontract award, $4,750,000 (1997-2007)

North Dakota Mathematics Assessment Project. Developed in partnership by the North Dakota Department of Education and Mid-continent Regional Educational Laboratory (Mid-continent Regional Educational Laboratory). Research team: Ann Clapper, Clarence Bina, Greg Gallagher, North Dakota Department of Education; Don Burger (PI), Hillary Michaels, and Sylvia D. Hall-Ellis, Mid-continent Regional Educational Laboratory (Aurora, Colorado). U.S. Office of Education, $1,618,214; subcontract award, $389,076 (1997-2001)

Pacific Resources for Education and Learning Distance Education: Project Evaluation. Developed in partnership by the Pacific Educational Community, the Pacific Resources for Education and Learning (PREL), and Mid-continent Regional Educational Laboratory (McREL). Research team: John W. Kofel (PI), Executive Director, PREL; J. Timothy Waters, Executive Director; Joan Buttram, Robert Keller, and Sylvia D. Hall-Ellis, Mid-continent Regional Educational Laboratory (Aurora, Colorado). U.S. Office of Education, Star Schools Program, $10,000,000; subcontract award, $500,000 (1997-2002)

Identification of Bilingual Gifted and Talented Children: A Comprehensive School Grants for Bilingual Education. Developed in partnership by Hidalgo (Texas) ISD, Los Fresnos (Texas) CISD, Progreso (Texas) ISD, University of Texas – Pan American (Edinburg, Texas), and Education Service Center, Region One (Edinburg, Texas). Research team: Hilda Medrano, Dean, College of Education, University of Texas – Pan American; Linda Phemister (PI), Janie Navarro, and Sylvia D. Hall-Ellis, Education Service Center, Region One. U.S. Department of Education, Office of Bilingual Education and Minority Languages Affairs, $1,670,633 (1997-2002)

Academics 2000: First Things First -- The Texas Goals 2000. Developed for Jim Hogg (Hebbronville, Texas) County ISD, Mirando City (Texas) ISD, and San Isidro (Texas) ISD. Research team: Hilda Medrano, Dean, College of Education, University of Texas - Pan American (Edinburg, Texas); Angie Lehmann, Amy Mares, Ellen Gonzalez (PI), and Sylvia D. Hall-Ellis, Education Service Center, Region One (Edinburg, Texas). Texas Education Agency, $339,987 (1997-2000)

Southwestern Bell's Learning Communities Initiative. Developed for Tech Prep of the Rio Grande Valley, Inc. (Harlingen, Texas); the Center for Professional Teacher Development, University of Texas – Brownsville; Teach for America – Rio Grande Valley (McAllen, Texas); and Education Service Center, Region One (Edinburg, Texas). Research team: Patricia G. Bubb, Executive Director (PI), Tech Prep of the Rio Grande Valley; Martin Winchester, Executive Director, Teach for America – Rio Grande Valley; Aileen Johnson, Director, School of Education, University of Texas – Brownsville; and Sylvia D. Hall-Ellis. Southwestern Bell Foundation, $100,000 (1997-1998)

Texas School to Work: Regional Implementation. Developed for Tech Prep of the Rio Grande Valley, Inc. (Harlingen), South Texas Community College (McAllen), Texas State Technical College (Harlingen), Texas Southmost College (Brownsville), Empowerment Zone of the Rio Grande Valley (Mercedes), Project VIDA (Weslaco), Youth Fair Chance (McAllen), and Education Service Center, Region One (Edinburg). Research team: Patricia G. Bubb (PI), Tech Prep of the Rio Grande Valley; Stephen Vassberg, Texas State Technical College; Ellen Trevino, Youth Fair Chance; Wanda Garza, Project VIDA; Leonardo Olivares, University of Texas – Pan American; Michael Bell, South Texas Community College; and Sylvia D. Hall-Ellis. Texas Workforce Commission, $4,250,000 (1997-2002).

Comprehensive Bilingual Education Grant for Hidalgo ISD and Roma ISD. Developed for Hidalgo (Texas) ISD, Roma (Texas) ISD, College of Education, University of Texas – Pan American (Edinburg, Texas), and Education Service Center, Region One (Edinburg, Texas). Research team: Tomas Thomas (PI), Director, Office of Bilingual Education and Sylvia D. Hall-Ellis. U.S. Department of Education, Office of Bilingual Education and Minority Languages Affairs, $1,531,361 (1997-2002)

Lopez High School, Porter High School, Rivera High School, Central Middle School, and Perkins Middle School, Brownsville (Texas) Independent School District. Telecommunications Infrastructure Fund Board, $1,473,611 (1997-1998)

Donna High School, Todd Middle School, and Solis Middle School, Donna (Texas) Independent School District. Telecommunications Infrastructure Fund Board, $704,052 (1997-1998)

Memorial Middle School and Nellie Schunior Middle School, La Joya Independent School District (Texas). Telecommunications Infrastructure Fund Board, $293,641 (1997-1998)

Martin High School, Christen Middle School, Cigarroa Middle School, Lamar Middle School, Laredo (Texas) Independent School District. Telecommunications Infrastructure Fund Board, $1,200,000 (1997-1998).

Lasara Middle School, Lasara (Texas) Independent School District. Telecommunications Infrastructure Fund Board, $246,210 (1997-1998)

Los Fresnos High School and Resaca Middle School, Los Fresnos (Texas) Consolidated Independent School District. Telecommunications Infrastructure Fund Board, $500,000 (1997-1998)

Lyford Junior High School, Lyford (Texas) Independent School District. Telecommunications Infrastructure Fund Board, $354,997 (1997-1998)

Travis Middle School, McAllen (Texas) Independent School District. Telecommunications Infrastructure Fund Board, $269,139 (1997-1998)

Mission High School, Mission (Texas) Independent School District. Telecommunications Infrastructure Fund Board, $297,010 (1997-1998)

Progreso High School, Progreso (Texas) Independent School District. Telecommunications Infrastructure Fund Board, $300,000 (1997-1998)

San Perlita High School, San Perlita (Texas) Independent School District. Telecommunications Infrastructure Fund Board, $293,490 (1997-1998)

Myra Green Junior High School, Raymondville (Texas) Independent School District. Telecommunications Infrastructure Fund Board, $225,000 (1997-1998)

Rio Grande City High School, Ringgold Middle School, Gruella Middle School, Rio Grande City (Texas) Independent School District. Telecommunications Infrastructure Fund Board, $809,934 (1997-1998)

Rio Hondo Junior High School, Rio Hondo (Texas) Independent School District. Telecommunications Infrastructure Fund Board, $297,024 (1997-1998)

Roma High School, Roma (Texas) Independent School District. Telecommunications Infrastructure Fund Board, $333,178 (1997-1998)

San Benito High School, Miller Jordan Junior High School, San Benito (Texas) Consolidated Independent School District. Telecommunications Infrastructure Fund Board, $547,000 (1997-1998)

Santa Maria High School and Santa Maria Middle School, Santa Maria (Texas) Independent School District. Telecommunications Infrastructure Fund Board, $400,000 (1997-1998)

Salvador High School, United Independent School District (Laredo, Texas). Telecommunications Infrastructure Fund Board, $250,879 (1997-1998)

Weslaco High School, Cabaza Middle School, Cuellar Middle School, Weslaco (Texas) Independent School District. Telecommunications Infrastructure Fund Board, $874,242 (1997-1998)

Principals' Assessment and Training Center. Developed for Education Service Center, Region One (Edinburg, Texas). Research team: Roberto Zamora, Leonel Barrera, William H. Parry, and Sylvia D. Hall-Ellis. Texas Principals' Leadership Initiative, Texas Association of Secondary School Principals, Texas Association of Elementary School Principals, and the Sid Richardson Foundation. $461,439 (1996-1998)

The Texas Library Connection -- Integrating and Sharing Resources. Developed for Hidalgo County Library System (McAllen), Cameron County Library System (Brownsville), South Texas Community College (McAllen), the

University of Texas - Pan American (Edinburg), University of Texas – Brownsville, and Education Service Center, Region One (Edinburg). Research team: William R. McGee, Coordinator, Hidalgo County Library System; Joe Garcia, Director, Cameron County Library System; Michael D. Bell, Library Director, South Texas Community College; Eleanor Folger Foster, University Library, University of Texas - Pan American; Jaime Vela (PI), Director of Instructional Technology and Media Services, Ron Pontius, Instructional Technology, and Fabiola Fuentes, Media Services, Education Service Center, Region One; and Sylvia D. Hall-Ellis. Office of Library Media Services, Technology Services, Texas Education Agency. $8,000 (1996-1997)

Developing Leadership Communities for Improving Algebra I for All Students. Developed for a partnership of the Region One Statewide Systemic Initiative Team. Research team: Noel Villarreal (PI), Eduardo Cancino, and Sylvia D. Hall-Ellis, Education Service Center, Region One (Edinburg). Texas Statewide Systemic Initiative for Reform in Mathematics, Science and Technology Education to The Charles A. Dana Center for Mathematics and Science Education, The University of Texas at Austin. $25,000 (1996-1997)

Academics 2000: First Things First -- The Texas Goals 2000. Developed for Edinburg (Texas) CISD. Research team: Hilda Medrano, Dean, College of Education, University of Texas - Pan American (Edinburg); Helen Jones, Director (PI), Gifted and Talented Education, Edinburg CISD; and Sylvia D. Hall-Ellis, Education Service Center, Region One (Edinburg). Texas Education Agency, $750,000 (1996-2001)

Texas Teachers Empowered for Achievement in Mathematics (TEXTEAM) Institute for Algebra I. Developed for Hidalgo ISD, Jim Hogg (Hebbronville) County ISD, La Joya ISD, La Villa ISD, Lyford ISD, Mission CISD, Pharr-San Juan-Alamo ISD, Rio Hondo ISD, San Isidro ISD, San Perlita ISD, Santa Maria ISD, Santa Rosa, Sharyland ISD, Valley View ISD, Webb (Laredo) CISD, Weslaco ISD, and Zapata County (Zapata) ISD. Research team: Noel Villarreal (PI), Chuck McInteer, Ellen M. Gonzalez, Education Service Center, Region One (Edinburg); and Sylvia D. Hall-Ellis. Charles A. Dana Center for Mathematics and Science Education, University of Texas - Austin, $15,975 (1996)

Community Learning Center for La Villa, Texas. Developed for Edcouch-Elsa Independent School District. Research team: Noe Gonzalez (PI), Assistant Superintendent, Edcouch-Elsa Independent School District, and Sylvia D. Hall-Ellis. Delta Region Subzone, Rio Grande Valley (Texas) Rural Empowerment Zone, $325,000 (1996-1997)

Monte Alto (Texas) Community Learning Center. Developed for Monte Alto Independent School District. Research team: Homero A. Diaz (PI), Superintendent, Monte Alto Independent School District, and Sylvia D. Hall-Ellis. Delta Region Subzone, Rio Grande Valley (Texas) Rural Empowerment Zone, $300,000 (1996-1997)

Community Learning Center for La Villa, Texas. Developed for La Villa Independent School District. Research team: Sam Gonzalez (PI), Assistant Superintendent, La Villa Independent School District; and Sylvia D. Hall-Ellis. Delta Region Subzone, Rio Grande Valley (Texas) Rural Empowerment Zone, $325,000 (1996-1997)

Building Project for Taylor Elementary. Developed for Mercedes (Texas) Independent School District. Research team: Mrs. Denise Rivera, Librarian, and Eduardo Infante, Principal, Taylor Elementary School; Ismael S. Cantu (PI), Federal Programs Director, Mercedes Independent School District; and Sylvia D. Hall-Ellis. Delta Region Subzone, Rio Grande Valley (Texas) Rural Empowerment Zone, $375,000 (1996-1997)

Border Education Network (BEN) - Distance Education through Cable Television. Developed for Edinburg (Texas) Consolidated Independent School District. Research team: Noe Torres (PI), Library Media Specialist, Magdalena Rosas, Library Media and Technology Coordinator, Edinburg Consolidated Independent School District; and Sylvia D. Hall-Ellis, Education Service Center, Region One (Edinburg). Edinburg (Texas) Consolidated School District, $250,000 (1996-1997)

Multiservice One-Stop Open Enrollment Charter School. Developed for the Information Referral Resource Assistance, Inc. (McAllen, Texas). Research team: Pablo Perez and Aguie Pena (PI), Executive Director, Information Referral Resource Assistance, Inc.; Roberto Zamora and Sylvia D. Hall-Ellis, Education Service Center, Region One (Edinburg). Texas Education Agency, $3,066,000 (1996-2001)

Project OK: A Community Youth Opportunities Grant for Summer, 1996. Developed for McAllen (Texas) Independent School District, St. Joseph the Worker Catholic Church, and the Office of Adult Education, Education Service Center, Region One. Research team: Father Bart Flatt, St. Joseph the Worker Catholic Church; Noe Calvillo (PI), Office of Adult Education; Maria Louisa Garcia, McAllen Independent School District; and Sylvia D. Hall-Ellis, Education Service Center, Region One (Edinburg). Texas Protective and Regulatory Agency through the Office of the Mayor, City of McAllen, $350,000 (1996-2001).

Early Childhood: a Time of Discovery. Developed for a partnership of Lasara ISD, Rio Hondo ISD, San Perlita ISD, the School of Education, University of Texas - Brownsville, and Education Service Center, Region One (Edinburg). Research team: Hugo Rodriguez, Dean, School of Education, University of Texas - Pan American; Leonel Barrera and Jack Damron, Field Service Agents, Ellen M. Gonzalez (PI), Administrator for Student Instructional Services, Ruth Solis, Education Specialist in Special Education, and Sylvia D. Hall-Ellis, Education Service Center, Region One (Edinburg). Texas Education Agency, $722,090 (1996-2001)

Innovative Gifted and Talented Programs for Early Childhood and Elementary Education Students. Developed for a partnership of Edinburg (Texas) CISD, the School of Education, University of Texas - Pan American (Edinburg), and Education Service Center, Region One (Edinburg). Research team: Hilda Medrano, Dean, School of Education, University of Texas - Pan American; Helen de la Garza (PI), Director of Elementary Curriculum and Instruction, Edinburg CISD; and Sylvia D. Hall-Ellis. Texas Education Agency, $750,000 (1996-2001)

Reading Recovery in Early Elementary Grades. Developed for a partnership of La Villa (Texas) ISD the School of Education, University of Texas - Pan American (Edinburg), and Education Service Center, Region One (Edinburg). Research team: Hilda Medrano, Dean, School of Education, University of Texas - Pan American; Marcario Salinas (PI), Supervisor of Elementary Curriculum and Instruction, La Villa ISD; and Sylvia D. Hall-Ellis, Education Service Center, Region One. Texas Education Agency, $750,000 (1996-2001)

Connected Mathematics Project for Middle and Junior High Students. Developed for a partnership of Michigan State University, The Charles A. Dana Center for Mathematics and Science Education, The University of Texas at Austin and Region One Statewide Systemic Initiative Team. Research team: Jack Damron, Chuck McInteer, Noel Villarreal (PI), and Sylvia D. Hall-Ellis, Education Service Center, Region One (Edinburg). National Science Foundation through Michigan State University to the Charles A. Dana Center at the University of Texas - Austin, $539,610 (1996-1999)

Sharing Resources: Testing the Interlibrary Loan Potential of the Texas Library Connection -- Integrating Media Resources. Developed under the sponsorship of the Hidalgo County Library System (McAllen) and Education Service Center, Region One (Edinburg). Research team: William H. McGee, Hidalgo County System Coordinator; Fabiola Fuentes, Library Media; Ronald Pontius (PI), Instructional Technology, Education Service Center, Region One; and Sylvia D. Hall-Ellis. Library Media Services Program, Office of Technology Services, Texas Education Agency, $25,000 (1996-1997)

State and Federal Adult Education JOBS Program. Developed for Education Service Center, Region One (Edinburg). Research team: Noe Calvillo (PI), Director, Adult Education Program, and Sylvia D. Hall-Ellis. Adult Education Program, Texas Education Agency, $532,846 (1995-1996)

Creating Safe and Drug-Free Schools and Communities. Developed for a partnership of the Region One Consortium for Safe and Drug-Free Education Environments. Research team: Clara Contreras (PI), Health Specialist, and Sylvia D. Hall-Ellis, Education Service Center, Region One (Edinburg). Texas Education Agency, $150,000 (1995-1996)

Developing Leadership Communities for Improving Mathematics Performance for All Students on Title I Campuses. Developed for a partnership of the Region One Statewide Systemic Initiative Team. Research team: Jack Damron, Chuck McInteer, Noel Villarreal (PI), and Sylvia D. Hall-Ellis, Education Service Center, Region One (Edinburg). Texas Statewide Systemic Initiative for Reform in Mathematics, Science and Technology Education to The Charles A. Dana Center for Mathematics and Science Education, The University of Texas at Austin, $50,669 (1995-1996)

The Impact of Library Resource Centers on Academic Achievement in Selected Public Schools in South Texas.
Sylvia D. Hall-Ellis (PI). Developed under the sponsorship of the Department of Library Science, College of
Education and Applied Science, Sam Houston State University (Huntsville). Texas Association of School
Librarians, Children's Services Round Table, and Young Adults Round Table (Austin, Texas), $2,500 (1995)

School Library Media Specialists Fellowship Program. Sylvia D. Hall-Ellis (PI). Developed under the sponsorship
of the Department of Library Science, College of Education and Applied Science, Sam Houston State University
(Huntsville, Texas). U.S. Department of Education, HEA Title II-B, Library Education and Human Resource
Development Program, $44,000 (1995-1996)

Planning for Educational Technology. Research team: Ruth Ann Riggins (PI), Director of Library Media and
Technology Services, Donna (Texas) Independent School District; Noe Torres, Education Service Center,
Region One; Patricia G. Bubb, Tech Prep of the Rio Grande Calley, Inc; Michael D. Bell, South Texas
Community College; and Sylvia D. Hall-Ellis, Sam Houston State University. Developed under the sponsorship
of Donna (Texas) Independent School District, Education Service Center, Region One (Edinburg), Tech Prep of
the Rio Grande Valley, Inc. (Harlingen), South Texas Community College (McAllen), and the Department of
Library Science, Sam Houston State University (Huntsville). Funded through Infusion of Educational
Technology Planning Grant Program (H.B. 18: Models). Texas Education Agency, $18,000 (1993-1994)

The Impact of Library Resource Centers on Academic Achievement in Selected Public Schools in South Texas.
Sylvia D. Hall-Ellis (PI) and Mary Ann Berry. Developed under the sponsorship of the Department of Library
Science, College of Education and Applied Science, Sam Houston State University (Huntsville). Sam Houston
State University Research Enhancement Fund, $7,500 (1993-1994)

Electronic Mail Resource Sharing System: Management and Operation of the Iowa Computer-Assisted Network.
State Library of Iowa, $294,000 (1986-1993)

The Iowa Locator: A CD-ROM Resource Sharing Tool. State Library of Iowa, $567,000 (1986-1992)

Statewide Database Development: An OCLC Tape Analysis To Determine Feasibility. State Library of South
Dakota, $15,000 (1987)

The Iowa Locator: A Feasibility Study. State Library of Iowa, $50,000 (1986)

Electronic Mail Resource Sharing System: A Feasibility Study for Libraries in the State of Iowa. State Library of
Iowa, $5,000 (1985)

Access Pennsylvania: A Feasibility Study. State Library of Pennsylvania, $50,000 (1984)

*Automating Library Administrative and Management Tasks: Procurement and Distribution of Microcomputer
Systems for District Library Centers in the Commonwealth of Pennsylvania.* State Library of Pennsylvania,
$495,000 (1982)

*Sharing Serial Titles Resources: Procurement and Distribution of Microfiche Readers for 550 Libraries in the
Commonwealth of Pennsylvania.* State Library of Pennsylvania, $500,000 (1982)

Electronic Mail System: A Pilot Project for Libraries throughout the Commonwealth of Pennsylvania. State Library
of Pennsylvania, $125,000 (1982)

Literacy Program for Adults in Rural Upstate New York State: Program Outreach and Evaluation - Phase 3.
Appalachian Regional Commission, $50,000 (1981)

*Database Building: A Cooperative Project of the Finger Lakes Library System (Ithaca), Four County Library
System (Binghamton), and the Southern Tier Library System (Corning).* New York State Library, $450,000
(1980-1985)

Faces of the Southern Tier: A Professional Photographer-in-Residence. New York State National Endowment for the Humanities, $25,000 (1980)

Literacy Program for Adults in Rural Upstate New York State: Program Implementation - Phase 2. Appalachian Regional Commission, $50,000 (1980)

Small Business Resources Center: A Pilot Project for Rural Public Libraries. New York State Library, $50,000 (1980)

Media Programming: A Professional Development Program for Public Librarians in Upstate New York: A Program in Allegheny, Chemung, Schuyler, Steuben, and Yates Counties. New York State Library, $35,000 (1979)

Information and Library Resources for Inmates and Prisoners in Selected Upstate New York Facilities: A Cooperative Program in Allegheny, Chemung, Schuyler, Steuben, and Yates Counties. New York State Library, $25,000 (1979)

Library Resources for Homebound Adults in Upstate New York: An Outreach Program in Allegheny, Chemung, Schuyler, Steuben, and Yates Counties. New York State Library, $40,000 (1979)

Literacy Program for Adults in Rural Upstate New York State: Program Initiation and Establishment - Phase 1. Funded by the Appalachian Regional Commission. Awarded to the Corning (New York) Public Library, $50,000 (1979)

Information Reference Services to Homebound Adults. New York State Library, $31,000 (1978)

Books-By-Mail Services to Homebound Adults. New York State Library, $31,000 (1978)

System Headquarters Services and Programs for Public Libraries in District 10. Funded through Library Services and Construction Act Title I. Texas State Library and Historical Commission, $880,000 (1976)

County Library Development Grant for Atascosita County. Funded through Library Services and Construction Act Title I. Texas State Library and Historical Commission, $15,000 (1976)

Spanish Language Materials Collection Development Program. Texas State Library and Historical Commission, $40,000 (1975)

Establishment of System Headquarters for Alamo Regional Library System (District 10) Headquartered at the San Antonio (Texas) Public Library. Texas State Library and Historical Commission, $800,000 (1975)

SELECTED CONSULTANTSHIPS

Project Strategic Planning & Funding Proposal Development

Walden University, 2015.

Pikes Peak Library District, 2014.

Douglas County Public Libraries, 2011-2012.

Denver School for Science and Technology, 2008-2011.

Johnson & Wales University, Denver Campus, 2007-2009.

Challenges, Choices, and Images K-12 Charter School, Denver Public Schools, 2007.

Denver Medical Library, Inc., 2006-2010.

Bemis Public Library (Littleton), Ergonomic Design and Facilities Enhancement Consultant, 2003.

Curtis Park Community Center (Denver), Community Technology Center Evaluation and Proposal Development Consultant, 2003.

Colorado Community Based Research Network (Denver), Funding Research Associate, 2002-

Our Lady of the Rosary Academy (Edgewater), Learning Resource Center Development Project Consultant, 2001-

University of Southern Colorado (Pueblo). Technology Integration and Curriculum Enhancement into Higher Education Learning Environment. Proposal Development Consultant, 2000.

Jefferson County Library System (Lakewood), 1999-2000.

Southeastern BOCES (Lamar, CO). Distance Learning Curriculum Content Development Project. Proposal Development Consultant, 1998-2004.

Cheyenne Mountain School District 12 (Colorado Springs, CO). Technology Integration into Elementary Writing Curriculum Project. Proposal Development Consultant, 1998.

Telecommunications Infrastructure Fund Board Round #2 Application, 1997. Technical assistance to the following: La Villa (Texas) Independent School District; Mirando City (Texas) Independent School District; Monte Alto (Texas) Independent School District; San Isidro (Texas) Independent School District.

Telecommunications Infrastructure Fund Board Round #1, 1996. Technical assistance to the following: Brownsville (Texas) Independent School District; Donna (Texas) Independent School District; Edinburg (Texas) Consolidated Independent School District; Harlingen (Texas) Consolidated Independent School District; Jim Hogg County Independent School District (Hebbronville, Texas); La Feria (Texas) Independent School District; La Joya (Texas) Independent School District; La Villa (Texas) Independent School District; Los Fresnos (Texas) Consolidated Independent School District; Progreso (Texas) Independent School District; Raymondville (Texas) Independent School District; Rio Hondo (Texas) Independent School District; San Benito (Texas) Independent School District; Sharyland Independent School District (Mission, Texas); Weslaco (Texas) Independent School District; Zapata (Texas) County Independent School District.

South Texas Community College (McAllen). Strategy Development to Meet the Technology Instructional Needs for Vocational, School-To-Work and Academic Programs, 1994-2000. Development Consultant.

Donna (Texas) Independent School District. Planning for the Infusion of Technology in Middle Schools Serving High At-Risk Students, 1994-1995. Research Associate.

Pettus (Texas) Independent School District. Planning for District-wide Automation in School Library Media Centers: Preparation of Data, and CD-ROM Hardware/Software Configuration Evaluation, 1994. Principal Investigator.

Fort Bend Independent School District (Sugar Land, TX). Planning for District-wide Automation in School Library Media Centers, Preparation of Data, and CD-ROM Hardware/Software Configuration Evaluation, 1994-1995. Principal Investigator.

Northern Waters Library Services (Ashland, WI). Professional Consulting Services to Make Recommendations on the Development of System-Wide Efforts of the Northern Waters Library Service, 1988-1989. Research Associate.

State Library of Iowa (Des Moines). The Iowa Locator Compact Disc to Support Multi-Type Libraries Resource Sharing including Database Design, Building, Production, and Distribution, 1986-1991. Project Director.

State Library of Iowa (Des Moines). Iowa Computer-Assisted Network Development, Enhancement, and Operation, 1985-1992. Technical Director.

State Library of South Dakota (Pierre). Statistical Sampling and Analysis of Multi-Institutional OCLC Archive Tape for Statewide Online Database Building, 1985-1986. Research Associate.

District of Columbia Public Library (Washington, DC). Planning Document for the Retrospective Conversion of Bibliographic Records and Automation Issues in the 1990's, 1984-1985. Research Associate.

State Library of Pennsylvania (Harrisburg). Database Development for High School Libraries, 1984-1985. Research Associate.

MINITEX (Minneapolis, MN). Workshops for Retrospective Conversion, Bar Coding, Library Statistics, and OCLC Serials Format, 1985. Presenter and Research Associate.

ABC Film Consortium (Altoona, Bellefonte, Johnstown, PA). Database Building, System Design, and Implementation of Online Film Booking System, 1983-1985. Database Manager.

Library Automation -- System Design & Implementation

Douglas County Library District (Castle Rock, CO). Library Automation Technical and System Performance Specifications, 2001.

Pharr-San Juan-Alamo Independent School District (Pharr, TX). Library Automation Technical and System Performance Specifications, 1997. Project Development Consultant.

Harlingen (Texas) Independent School District. Planning for District-wide Automation in Junior High School Library Media Centers: Preparation of Data, and CD-ROM Hardware/Software Configuration Evaluation, 1996. Principal Investigator.

Sharyland (Texas) Independent School District. Design and Construction of New Elementary School Library and Technology Resources Center, 1995-1996. Principal Investigator.

South Texas Independent School District (Mercedes, TX). Design and Construction of a New High School Library and Technology Resources Center, 1995-1996. Principal Investigator.

Citizens' Library (Washington, PA). Online Community Resources Files: Design and Implementation, 1984. Research Associate.

Altoona (Pennsylvania) Hospital. Integrated Online System Upgrade Study, 1984. Research Associate.

State Library of South Dakota (Pierre). Automation Plan and State Database Development, 1982-1983. Principal Investigator.

State Library of Pennsylvania (Harrisburg). COM Production and Preparation of the Technical Specifications Document, Procurement, and Distribution of Microcomputers in the Commonwealth of Pennsylvania, 1983-1984. Research Associate.

Altoona (Pennsylvania) Area Public Library. Integrated System (Circulation/Online Catalog) Study, 1982-1983. Principal Investigator.

COPSCAULD (Council of Pennsylvania State College and University Library Directors, Edinboro, PA). Design of Online Media Catalog, 1982. Principal Investigator.

Erie (Pennsylvania) County Library System. Operations Research and Design for Automated Circulation, Hardware Upgrade and Re-Retrospective Conversion, 1982. Research Associate.

Michigan Library Consortium (Lansing, MI). Tape Management System Design and Implementation, 1982-1984. Research Associate.

State Library of Pennsylvania (Harrisburg). Preparation of the Technical Specifications Document, Procurement and Distribution of Microfiche Readers in the Commonwealth of Pennsylvania, 1982. Research Associate.

Community College of Allegheny County, Allegheny Campus (Pittsburgh, PA). Integrated Systems Study, 1981. Principal Investigator.

Community College of Allegheny County, South Campus (West Mifflin, PA). Retrospective Conversion Training Program for Handicapped Students, 1981. Technical Director.

Southern Tier Library System (Corning, NY). OCLC Acquisitions Subsystem Evaluation, 1981. Principal Investigator.

South Central Reference and Research Council (Ithaca, NY). South Central Regional Delivery System, 1980. Principal Investigator.

Southern Tier Library System (Corning, NY). Newspapers on Microfilm in the Chemung-Southern Tier Library System, 1979-1981. Principal Investigator.

Cataloging & Bibliographic Database Building

Challenges, Choices, and Images K-12 Charter School, Denver Public Schools, 2007.

Denver Medical Library, Inc., 2006-2010.

Ricks Gifted and Talented School Library, 2005-

American Humane Society (Englewood), 2004-2006.

Fisher Early Learning Center Library, 2004-

Colorado Community Based Research Network (Denver), 2004-

Boulder Valley School District (Boulder), 2002-2003.

Douglas Public Library District (Castle Rock), 2001-2002.

Bibliographic Center for Research, Inc. (Denver). Original Cataloging, 2001-2003 & 1992-1993. Professional Cataloger. Libraries include Arapahoe Library District (Centennial); Clarke College (Clarke, IA); Kaiser Permanente Center for Health Research (Portland, KS); Douglas County Library System (Carson City, NV); Grinnell College (Grinnell, IA); Kansas State University (Manhattan, KS); Kansas State Library (Topeka, KS); McPherson College (McPherson, KS); Newman University (Wichita, KS); Montana Technical University (Helena, MT); Montana State Library (Helena, MT); University of Texas Southwest Medical Center Library (Dallas, TX); Community College of Southern Nevada (Las Vegas, NV); Pikes Peak Library District (Colorado Springs); Mesa Community College (Grand Junction); Coe College (Cedar Rapids, IA); Briar Cliff College (Sioux City, IA); Tri-Care Health Systems (Aurora); The Penrose-St. Francis Healthcare System (Colorado Springs); Westminster Public Library (Westminster); Lutheran Medical Center Medical Library (Wheat Ridge); American Heritage Center, University of Wyoming (Laramie, WY); National Wildlife Research Center Library (Lakewood); University of Colorado Health Sciences Center, Denison Memorial Library (Denver); Water Resources Library, Denver District Office, Bureau of Land Management (Lakewood); Mesa State Community College Learning Resources Center (Pueblo); Front Range Community College Learning Resources Center (Westminster).

Colorado Historical Society Library (Denver). Original Cataloging of Serials for Multi-Institutional Union Listing Project, 1993. Technical Services Associate. Institutional partners: Denver Art Museum, Denver Museum of Natural History Library, and Denver Botanical Gardens Library.

Arapahoe Library District (Centennial). Original Cataloging of Major Media, 1991.

Original Cataloging Projects: Davis and Elkins College (Elkins, WV), 1989-1990; Waldorf College (Forest City, IA), 1989-1990; Kennametal Corporation (Latrobe, PA), 1984-1985; Pennsylvania Public Libraries Film Center (Harrisburg), 1982-1985.

Retrospective Conversion Projects: North Central Regional Library Service (Mason City, IA), 1987-1988; Southeastern Library Services (Davenport, IA), 1986-1987; Virginia Theological Seminary (Alexandria), 1984-1985; California University of Pennsylvania (California, PA), 1984-1985; Kennametal Corporation (Latrobe, PA), 1984-1985;West Virginia University (Morgantown), 1983-1985; Altoona Area Public Library (Altoona, PA), 1983-1984; George Washington University (Washington, DC), 1983-1984; Indiana University of Pennsylvania (Indiana, PA), 1983-1985; Health Education Center (Pittsburgh), 1983-1984; Central Pennsylvania District Library Center (Bellefonte, PA), 1982-1985; Duquesne University Law School Library (Pittsburgh), 1982-1983; Allegheny County Law Library (Pittsburgh), 1982-1984;Calgon Technical Information Center (Pittsburgh), 1982; Dow Corning Corporation, Technical Information Center (Midland, MI), 1982-1983; Tri-System Public Library Retrospective Conversion Project (Binghamton, Corning, and Ithaca, NY), 1978-1981, Technical Project Director.

Updated May 2021

ATTACHMENT 1a

NEOS
Library Consortium
Catalogue

new search   **advanced search**   **reserve desk**   **my account**

Go Back   **New Search**   **Kept**   **Logout**

record 1 of 1 for search **"1990 single-chip microcontroller data book."**
us

| Item Information | **Catalogue Record** |

1990 single-chip microcontroller data book
NEC Electronics.

000:   : am a0c a

001:   : 837047

003:   : CaAEU

008:   : 921029s1990 cau 0 eng c

035:   : ocm32402931

040:   : |beng

049:   : AEU|beng

055:   3   : TJ 223 P76|bN7145 1990

090:   0   : TJ 223 P76 N7145 1990

245:   00   : 1990 single-chip microcontroller data book.

260:   : Mountain View, Calif. :|bNEC Electronics Inc.,|c1990.

300:   : 1 v. (various pagings) :|bill. ;|c23 cm.

336:   : text|btxt|2rdacontent

337:   : unmediated|bn|2rdamedia

338:   : volume|bnc|2rdacarrier

596:   : 38

650:   0   : Programmable controllers|vCatalogs.

710:   2   : NEC Electronics.

image not available

Google Preview

☐ **Mark**

Change Display

.: Brief Display

.: Full Display

.: MARC Display

.: Create Permanent Link

.: Send Correction

.: del.icio.us

.: Digg

.: Google Bookmarks

.: Reddit

Search Also

.: Edmonton Public

.: TAL Online

.: CISTI

.: Library of Congress

.: University of Toronto

.: Abebooks.com

.: Amazon.ca

.: Amazon.com

.: Chapters.Indigo

.: WorldCat

.: LibraryThing

.: goodreads

.: Google

NEOS Library Consortium Catalogue
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Top

ATTACHMENT 1b

						Rec Stat	En tere d	199 505 01	Re place d	2018060 1222829 .1

Books

Type	a	**ELvl**	l	**Srce**	d	**Audn**		**Ctrl**		**Lang**	eng
BLvl	m	**Form**		**Conf**	0	**Biog**		**MRec**		**Ctry**	cau
		Cont	c	**GPub**		**LitF**	0	**Indx**	0		cau
Desc	a	**Ills**	a	**Fest**	0	**DtSt**	s	**Dates**	1990	,	

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040    PNX $b eng $c PNX $d SYB $d OCLCF $d OCLCQ $d OCLCO $d UAB
050  4 TK7874.5 $b .N42 1990
055  3 TJ 223 P76 $b N7145 1990
082  4 621.3916 $b N364n
090    $b
110 2  NEC Electronics.
245 10 1990 single-chip microcontroller data book / $c NEC Electronics Inc.
246 30 Single-chip microcontroller data book
260    Mountain View, CA : $b NEC, $c 1990.
300    1 volume (unpaged) : $b illustrations ; $c 23 cm
336    text $b txt $2 rdacontent
337    unmediated $b n $2 rdamedia
338    volume $b nc $2 rdacarrier
500    "May 1990."
500    "Document no. 50053."
650  0 Microcomputers $v Catalogs.
650  0 Integrated circuits $v Catalogs.
650  0 Microprocessors $v Catalogs.
650  7 Integrated circuits. $2 fast $0 (OCoLC)fst00975535
650  7 Microcomputers. $2 fast $0 (OCoLC)fst01019642
650  7 Microprocessors. $2 fast $0 (OCoLC)fst01020008
655  7 Catalogs. $2 fast $0 (OCoLC)fst01423692
```

ATTACHMENT 1c

LIBRARY OF CONGRESS AUTHORITIES

The Library has opened access to some reading rooms by appointment only. More. Library buildings otherwise remain closed to the public. More.

| Help ⓘ | New Search | Search History | Headings List | Start Over |

◀ Previous   Next ▶

MARC Display | Labelled Display

LC control no.: sh2010101665

LCCN Permalink: https://lccn.loc.gov/sh2010101665

HEADING: Microcomputers Catalogs

000 00510cz a2200169n 450

001 8157155

005 20110729163602.0

008 100126|| anannbabn |n ana

010 __ |a sh2010101665

035 __ |a (DLC)452648

035 __ |a (DLC)sh2010101665

040 __ |a DLC |b eng |c DLC

150 __ |a Microcomputers |v Catalogs

667 __ |a Record generated for validation purposes.

670 __ |a Work cat.: A directory of library and information retrieval software for microcomputers, c1990

906 __ |t 8888 |u tc00 |v 0

953 __ |a tc00

◀ Previous   Next ▶

| **Save, Print or Email Records (View Help)** |
| Select Download Format: Text (Labelled Display) ⌄   Press to SAVE or PRINT |
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Library of Congress
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ATTACHMENT 1d

The Library of Congress

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◀ Previous   Next ▶

MARC Display | Labelled Display

LC control no.: sh2008123900

LCCN Permalink: https://lccn.loc.gov/sh2008123900

HEADING: Integrated circuits Catalogs

000 00468cz a2200169n 450

001 7526973

005 20110729161547.0

008 080425|| anannbabn |n ana

010 __ |a sh2008123900

035 __ |a (DLC)402379

035 __ |a (DLC)sh2008123900

040 __ |a DLC |b eng |c DLC

150 __ |a Integrated circuits |v Catalogs

667 __ |a Record generated for validation purposes.

670 __ |a Work cat.: IC cross reference book, c1994, 1998

906 __ |t 8888 |u te00 |v 0

953 __ |a te00

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ATTACHMENT 1e

The Library of Congress

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| Help ⓘ | New Search | Search History | Headings List | Start Over |

◄ Previous   Next ►

MARC Display | **Labelled Display**

LC control no.: sh 85084898

LCCN Permalink: https://lccn.loc.gov/sh85084898

HEADING: Microprocessors

000 00358cz a2200157n 450

001 4735345

005 20120327093821.0

008 860211i| anannbabn |b ana

010 __ |a sh 85084898

035 __ |a (DLC)sh 85084898

035 __ |a (DLC)82030

040 __ |a DLC |c DLC

150 __ |a Microprocessors

550 __ |w g |a Minicomputers

906 __ |t 8528 |u fk03 |v 0

953 __ |a xx00

◄ Previous   Next ►

| **Save, Print or Email Records (View Help)** |
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ATTACHMENT 1f

LIBRARY OF CONGRESS AUTHORITIES

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| Help 🛈 | New Search | Search History | Headings List | Start Over |

◀ Previous   Next ▶

MARC Display | **Labelled Display**

LC control no.: sh 85020898

LCCN Permalink: https://lccn.loc.gov/sh85020898

HEADING: Catalogs

000 01003cz a2200217n 450

001 4673448

005 20120322080455.0

008 860211i| anannbabn |b ana

010 __ |a sh 85020898

035 __ |a (DLC)sh 85020898

035 __ |a (DLC)20133

035 __ |a (DLC)6971473

035 __ |a (DLC)sp 85020898

035 __ |a (DLC)349216

040 __ |a DLC |c DLC |d DLC |d NNFr |d DLC

150 __ |a Catalogs

360 __ |i subdivision |a Catalogs |i under names of individual artists, craftspersons, families of artists and craftspersons, persons or families doing business as sellers under their personal names, and corporate bodies, and under individual objects, e.g. |a Automobiles--Catalogs; Painting--Catalogs; |i and subdivision |a Catalogs and collections |i under natural objects and individual musical instruments and families of instruments, e.g. |a Fishes--Catalogs and collections; Piano--Catalogs and collections

450 __ |a Catalogs and collections

450 __ |a Catalogues

906 __ |t 0646 |u te04 |v 0

953 __ |a xx00 |b ta25

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ATTACHMENT 2a

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035    ##$9458580
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040    ##$aLHL $cLHL
049    ##$aLHLA
090    ##$aTK7870 $b.I64 2000
111    2#$aIEEE International Solid-State Circuits Conference
$d(2000 : $cSan Francisco, Calif.)
245    10$aDigest of technical papers : $b2000 IEEE International
Solid-State Circuits Conference.
246    30$a2000 IEEE International Solid-State Circuits Conference
246    30$aISSCC 2000
250    ##$a1st ed.
260    ##$aCastine, ME : $bJohn H. Wuorinen ; $a[New York, N.Y.] :
$bInstitute of Electrical and Electronics Engineers, $cc2000.
300    ##$a496 p. : $bill. ; $c28 cm.
500    ##$a"February, 2000."
500    ##$aHeld at the San Francisco Marriott Hotel, February 7-9,
2000.
500    ##$a"IEEE catalog number 00CH37056."
500    ##$a"Volume 43"--T.p. verso.
500    ##$a"ISSN 0193-6530"--T.p. verso.
504    ##$aIncludes bibliographical references and index.
650    #0$aElectronic circuits $vCongresses
650    #0$aSolid state electronics $vCongresses
650    #0$aSemiconductors $vCongresses
710    2#$aInstitute of Electrical and Electronics Engineers
948    ##$aLTI 09/01/2008
994    ##$aE0 $bLHL
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ATTACHMENT 2b

OCLC	43917176	No holdings in XXX - 35 other holdings							

						Rec Stat	c	**Entered**	20000424	**Replaced**	20190312001925.6

Books

Type	a	**ELvl**	I	**Srce**	d	**Audn**		**Ctrl**		**Lang**	eng
BLvl	m	**Form**		**Conf**	1	**Biog**		**MRec**		**Ctry**	meu
		Cont	b	**GPub**		**LitF**	0	**Indx**	1		
Desc	a	**Ills**	a	**Fest**	0	**DtSt**	s	**Dates**	2000	,	

040 LHL $b eng $c LHL $d OCL $d E9X $d OCLCQ $d BAKER $d ZWZ $d CEF $d OCLCQ $d YDXCP $d OCLCO $d OCLCF $d OCLCQ $d OCLCO $d UKMGB $d OCL $d OCLCO $d OCLCA $d OCLCQ

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020   9780780358546 $q (casebound)

020   0780358554 $q (microfiche)

020   9780780358553 $q (microfiche)

020   0780358562 $q (CD-ROM)

020   9780780358560 $q (CD-ROM)

050 4 TK7870 $b .I64 2000

090    $b

111 2 IEEE International Solid-State Circuits Conference $d (2000 : $c San Francisco, Calif.)

245 10 Digest of technical papers : $b 2000 IEEE International Solid-State Circuits Conference.

246 30 2000 IEEE International Solid-State Circuits Conference

246 30 ISSCC 2000

250   1st ed.

260   Castine, ME : $b John H. Wuorinen ; $a [New York, N.Y.] : $b Institute of Electrical and Electronics Engineers, $c ©2000.

300   496 pages : $b illustrations ; $c 28 cm

336   text $b txt $2 rdacontent

337   unmediated $b n $2 rdamedia

338   volume $b nc $2 rdacarrier

500   "February, 2000."

500   Held at the San Francisco Marriott Hotel, February 7-9, 2000.

500   "IEEE catalog number 00CH37056."

500   "Volume 43"--Title page verso.

500   "ISSN 0193-6530"--Title page verso.

504   Includes bibliographical references and index.

530   Also available via the World Wide Web with additional title: Solid-State Circuits Conference, 2000, digest of technical papers, ISSCC, 2000 IEEE International.

650 0 Electronic circuits $v Congresses.

650 0 Solid state electronics $v Congresses.

650 0 Semiconductors $v Congresses.

650 7 Electronic circuits. $2 fast $0 (OCoLC)fst00906874

650 7 Semiconductors. $2 fast $0 (OCoLC)fst01112198

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650 7 Électronique de l'état solide $x Congrès. $2 ram

650 7 Circuits électroniques. $2 ram

650 7 Microprocesseurs $x Congrès. $2 ram

655 7 Conference papers and proceedings. $2 fast $0 (OCoLC)fst01423772

710 2 Institute of Electrical and Electronics Engineers.

740 0 Solid-State Circuits Conference, 2000, digest of technical papers, ISSCC, 2000 IEEE International.

856 41 $3 IEEE Xplore $u http://ieeexplore.ieee.org/lpdocs/epic03/RecentCon.htm?punumber=6780

856 41 $3 IEEE Xplore $u http://ieeexplore.ieee.org/servlet/opac?punumber=6780

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LC control no.: sh2008102920

LCCN Permalink: https://lccn.loc.gov/sh2008102920

HEADING: Electronic circuits Congresses

000 00463cz a2200169n 450

001 7440866

005 20110729160214.0

008 080208|| anannbabn |n ana

010 __ |a sh2008102920

035 __ |a (DLC)378486

035 __ |a (DLC)sh2008102920

040 __ |a DLC |b eng |c DLC

150 __ |a Electronic circuits |v Congresses

667 __ |a Record generated for validation purposes.

670 __ |a Work cat.: Conference proceedings, c2001

906 __ |t 8888 |u te00 |v 0

953 __ |a te00

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LC control no.: sh2008111513

LCCN Permalink: https://lccn.loc.gov/sh2008111513

HEADING: Solid state electronics Congresses

000 00510cz a2200169n 450

001 7469750

005 20110729160803.0

008 080311|| anannbabn |n ana

010 __ |a sh2008111513

035 __ |a (DLC)388016

035 __ |a (DLC)sh2008111513

040 __ |a DLC |b eng |c DLC

150 __ |a Solid state electronics |v Congresses

667 __ |a Record generated for validation purposes.

670 __ |a Work cat.: 2003 IEEE Conference on Electron Devices and Solid-State Circuits, c2003

906 __ |t 8888 |u te00 |v 0

953 __ |a te00

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MARC Display | **Labelled Display**

LC control no.: sh2008111509
LCCN Permalink: https://lccn.loc.gov/sh2008111509
HEADING: Semiconductors Congresses

000 00474cz a2200169n 450
001 7469746
005 20110729160803.0
008 080311|| anannbabn |n ana
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035 __ |a (DLC)388012
035 __ |a (DLC)sh2008111509
040 __ |a DLC |b eng |c DLC
150 __ |a Semiconductors |v Congresses
667 __ |a Record generated for validation purposes.
670 __ |a Work cat.: Passivity of metals and semiconductors, c2001
906 __ |t 8888 |u te00 |v 0
953 __ |a te00

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MARC Bibliographic Record

LEADER		00974mam a22003258a 4500
001		9925616003602122
005		19990604113142.0
008		920720t19931993maua 001 0 eng
010		$a 92023491
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040		$aDLC$beng$cDLC
049		$aGZZK
050	00	$aTK454$b.N54 1993
082	00	$a621.319/2$220
100	1_	$aNilsson, James William.
245	10	$aElectric circuits /$cJames W. Nilsson with contributions by Susan A. Riedel ... [and others]
250		$aFourth edition.
264	_1	$aReading, Mass. :$bAddison-Wesley Pub. Co.,$c[1993]

264	_4	$c©1993
300		$axxiv, 923 pages :$billustrations ;$c24 cm
336		$atext$btxt$2rdacontent
337		$aunmediated$bn$2rdamedia
338		$avolume$bnc$2rdacarrier
500		$aIncludes index.
650	_0	$aElectric circuits.
700	1_	$aRiedel, Susan A.
997		$aMARCIVE

MMS IDs

Document ID:
999697278902121
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999697278902121
mms_mad_ids:
9925616003602122
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BLvl	m	**Form**		**Conf**	0	**Biog**		**MRec**		**Ctry**	mau
		Cont	b	**GPub**		**LitF**	0	**Indx**	1		
Desc	a	**Ills**	a	**Fest**	0	**DtSt**	s	**Dates**	1993	,	

010   92023491

040   DLC $b eng $c DLC $d BTCTA $d LVB $d YDXCP $d DEBBG $d BDX $d GBVCP $d OCLCF $d I8M $d OCLCO $d OCLCQ $d LEATE $d OKS $d OCLCO $d CSA $d OCLCO $d UKUOY $d OCLCA $d UKMGB

016 7 009788678 $2 Uk

019   775917060

020   0201549875

020   9780201549874

020   0201581795

020   9780201581799

050 00 TK454 $b .N54 1993

082 00 621.319/2 $2 20

084   ZN 5300 $2 rvk

090    $b

100 1 Nilsson, James William.

245 10 Electric circuits / $c James W. Nilsson with contributions by Susan A. Riedel [and others].

250   4th ed.

260   Reading, Mass. : $b Addison-Wesley Pub. Co., $c 1993.

300   xxiv, 923 pages : $b illustrations (some color) ; $c 25 cm.

336   text $b txt $2 rdacontent

337   unmediated $b n $2 rdamedia

338   volume $b nc $2 rdacarrier

490 1 Addison-Wesley series in electrical and computer engineering

520 3 -- Introduction to Pspice (3C.) -- Solution manual 2V (V.1 ch.1-10; V.2 ch. 11-20.) -- Instructor's road map.

505 00 $t 2. Introduction to PSpice: a supplement.

650 0 Electric circuits.

650 6 Circuits électriques.

650 7 Electric circuits. $2 fast $0 (OCoLC)fst00904545

650 7 Einführung $2 gnd $0 (DE-588)4151278-9

650 7 Elektrisches Netzwerk $2 gnd $0 (DE-588)4014214-0

650 07 Einführung. $2 swd

650 07 Elektrisches Netzwerk. $2 swd

653 0 Electric circuits

700 1 Riedel, Susan A.

830 0 Addison-Wesley series in electrical and computer engineering.

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000 00467cz a2200193n 450

001 4694179

005 20120323072907.0

008 860211|| anannbabn |b ana

010 __ |a sh 85042279

035 __ |a (DLC)sh 85042279

035 __ |a (DLC)40864

040 __ |a DLC |c DLC

150 __ |a Electronic circuits

450 __ |a Electron-tube circuits

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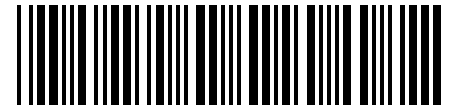
Rush

Request Date:	06/16/2021 09:41am
Requester:	Sylvia Hall-Ellis - San Jose State University
Phone:	3037566860
Reference:	JoaquinGP
Delivery email:	**sophia06219@msn.com**

Maxcost: 75.00

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Citation:

 1990 Single-Chip Microcontroller Data Book. Mountain View, CA : NEC, 1990.

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Selection Guides `1`

Reliability and Quality Control `2`

μ**PD7500 Series: 4-Bit Microcomputers** `3`

μ**PD75000 Series: 4-Bit Microcomputers** `4`

μ**PD7800 Series: 8-Bit Microcomputers** `5`

μ**PD78K2 Series: 8-Bit Microcomputers** `6`

μ**PD78K3 Series: 16-Bit Microcomputers** `7`

μ**PD722x Series: LCD Controller/Drivers** `8`

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Section 1
Selection Guides

Part Numbering System

µPD72001L	Typical microdevice part number
µP	NEC monolithic silicon integrated circuit
D	Device type (D = digital MOS)
72001	Device identifier (alphanumeric)
L	Package type (L = PLCC)

A part number may include an alphanumeric suffix that identifies special device characteristics; for example, µPD72001L-11 has an 11-MHz data clock rating.

4-Bit, Single-Chip CMOS Microcomputers

Device, μPD	Features	Clock (MHz)	Supply Voltage (V)	ROM (X8)	RAM (X4)	I/O	# Package	Pins
7502	LCD controller/driver	0.41	2.5 to 6.0	2K	128	23	QFP	64
7503	LCD controller/driver	0.41	2.5 to 6.0	4K	224	23	QFP	64
7507	General-purpose	0.41	2.5 to 6.0	2K	128	32	DIP SDIP QFP	40 40 52
7507H	General-purpose	4.19	2.7 to 6.0	2K	128	32	DIP SDIP QFP	40 40 52
7508	General-purpose	0.41	2.5 to 6.0	4K	224	32	DIP SDIP QFP	40 40 52
7508H	General-purpose	4.19	2.7 to 6.0	4K	224	32	DIP SDIP QFP	40 40 52
75CG08	Piggyback EPROM	0.41	4.5 to 5.5	2K or 4K	224	32	Ceramic DIP	40
75CG08H	Piggyback EPROM	4.19	4.5 to 5.5	2K or 4K	224	32	Ceramic DIP	40
7527A	FIP controller/driver	0.61	2.7 to 6.0	2K	128	35	DIP SDIP	42 42
7528A	FIP controller/driver	0.61	2.7 to 6.0	4K	160	35	DIP SDIP	42 42
75CG28	Piggyback EPROM; FIP controller/driver	0.5	4.5 to 5.5	4K	160	35	Ceramic DIP	42
7533	A/D converter	0.5	2.7 to 6.0	4K	160	30	DIP SDIP QFP	42 42 44
75CG33	Piggyback EPROM; A/D converter	0.5	4.5 to 5.5	4K	160	30	Ceramic DIP	42
7537A	FIP controller/driver	0.61	2.7 to 6.0	2K	128	35	DIP SDIP	42 42
7538A	FIP controller/driver	0.61	2.7 to 6.0	4K	160	35	DIP SDIP	42 42
75CG38	Piggyback EPROM; FIP controller/driver	0.61	4.5 to 5.5	4K	160	35	Ceramic DIP	42
7554	Serial I/O; external clock or RC oscillator	0.71	2.5 to 6.0	1K	64	16	SDIP SOP	20 20
7554A	Serial I/O; external clock or RC oscillator	0.71	2.0 to 6.0	1K	64	16	SDIP SOP	20 20
75P54	Serial I/O; external clock or RC oscillator	0.71	4.5 to 6.0	1K OTPROM	64	16	SDIP SOP	20 20
7564/7564A	Serial I/O; ceramic oscillator	0.71	2.7 to 6.0	1K	64	15	SDIP SOP	20 20
75P64	Serial I/O; ceramic oscillator	0.71	4.5 to 6.0	1K OTPROM	64	15	SDIP SOP	20 20
7556	Comparator; external clock or RC oscillator	0.71	2.5 to 6.0	1K	64	20	SDIP SOP	24 24
7556A	Comparator; external clock or RC oscillator	0.71	2.0 to 6.0	1K	64	20	SDIP SOP	24 24
75P56	Comparator; external clock or RC oscillator	0.71	4.5 to 6.0	1K OTPROM	64	20	SDIP SOP	24 24
7566/7566A	Comparator; ceramic oscillator	0.71	2.7 to 6.0	1K	64	19	SDIP SOP	24 24
75P66	Comparator; ceramic oscillator	0.71	4.5 to 6.0	1K OTPROM	64	19	SDIP SOP	24 24
75004	General-purpose	4.19	2.7 to 6.0	4K	512	34	SDIP QFP	42 44

\# Plastic unless ceramic (or cerdip) is specified.
* Under development; consult Microcontroller Marketing for availability.

4-Bit, Single-Chip CMOS Microcomputers (cont)

Device, μPD	Features	Clock (MHz)	Supply Voltage (V)	ROM (X8)	RAM (X4)	I/O	# Package	Pins
75006	General-purpose	4.19	2.7 to 6.0	6K	512	34	SDIP	42
							QFP	44
75008	General-purpose	4.19	2.7 to 6.0	8K	512	34	SDIP	42
							QFP	44
75P008	General-purpose	4.19	4.5 to 5.5	8K OTPROM	512	34	SDIP	42
							QFP	44
75028 *	A/D converter	4.19	2.7 to 6.0	8K	512	48	SDIP	64
							QFP	64
75P036 *	A/D converter	4.19	2.7 to 6.0	16K	1024	48	SDIP	64
							QFP	64
75048 *	A/D converter; 1K x 4 EEPROM	4.19	2.7 to 6.0	8K	512	48	SDIP	64
							QFP	64
75P056 *	A/D converter; 1K x 4 EEPROM	4.19	2.7 to 6.0	16K	512	48	SDIP	64
							QFP	64
75104	High-end with 8-bit instruction	4.19	2.7 to 6.0	4K	320	58	SDIP	64
							QFP	64
75104A	High-end with 8-bit instruction	4.19	2.7 to 6.0	4K	320	58	QFP	64
75106	High-end with 8-bit instruction	4.19	2.7 to 6.0	6K	320	58	SDIP	64
							QFP	64
75108	High-end with 8-bit instruction	4.19	2.7 to 6.0	8K	512	58	SDIP	64
							QFP	64
75108A	High-end with 8-bit instruction	4.19	2.7 to 6.0	8K	512	58	QFP	64
75P108	High-end with 8-bit instruction; on-chip OTPROM or UVEPROM	4.19	4.5 to 5.5	8K	512	58	QFP	64
							SDIP	64
							QFP	64
							Shrink cerdip	64
75P108B	High-end with 8-bit instruction; on-chip OTPROM	4.19	2.7 to 6.0	8K	512	58	SDIP	64
							QFP	64
75112	High-end with 8-bit instruction	4.19	2.7 to 6.0	12K	512	58	SDIP	64
							QFP	64
75116	High-end with 8-bit instruction	4.19	2.7 to 6.0	16K	512	58	SDIP	64
							QFP	64
75P116	High-end with 8-bit instruction on-chip OTPROM	4.19	4.5 to 5.5	16K OTPROM	512	58	SDIP	64
							QFP	64
75206	FIP controller/driver	4.19	2.7 to 6.0	6K	369	33	SDIP	64
							QFP	64
75208	FIP controller/driver	4.19	2.7 to 6.0	8K	497	33	SDIP	64
							QFP	64
75CG208	FIP controller/driver; piggyback EPROM	4.19	4.5 to 5.5	8K	512	33	Ceramic SDIP	64
							Ceramic QFP	64
75212A	FIP controller/driver	4.19	2.7 to 6.0	12K	512	33	SDIP	64
							QFP	64
75216A	FIP controller/driver	4.19	2.7 to 6.0	16K	512	33	SDIP	64
							QFP	64
75CG216A	FIP controller/driver; piggyback EPROM	4.19	4.5 to 5.5	16K	512	33	Ceramic SDIP	64
							Ceramic QFP	64
75P216A	FIP controller/driver	4.19	4.5 to 5.5	16K OTPROM	512	33	SDIP	64
75268	FIP controller/driver	4.19	2.7 to 6.0	8K	512	32	SDIP	64
							QFP	64
75304	LCD controller/driver	4.19	2.7 to 6.0	4K	512	40	QFP	80
75306	LCD controller/driver	4.19	2.7 to 6.0	6K	512	40	QFP	80
75308	LCD controller/driver	4.19	2.7 to 6.0	8K	512	40	QFP	80
75P308	LCD controller/driver; on-chip OTPROM or UVEPROM	4.19	4.75 to 5.25	8K	512	40	QFP	80
							Ceramic LCC	80

1-4

4-Bit, Single-Chip CMOS Microcomputers (cont)

Device, µPD	Features	Clock (MHz)	Supply Voltage (V)	ROM (X8)	RAM (X4)	I/O	# Package	Pins
75312	LCD controller/driver	4.19	2.7 to 6.0	12K	512	40	QFP	80
75316	LCD controller/driver	4.19	2.7 to 6.0	16K	512	40	QFP	80
75P316	LCD controller/driver; on-chip OTPROM	4.19	4.75 to 5.25	16K OTPROM	512	40	QFP	80
75P316A *	LCD controller/driver; on-chip OTPROM or UVEPROM	4.19	2.7 to 6.0	16K OTPROM	512	40	QFP Ceramic LCC	80 80
75328	LCD controller/driver; A/D converter	4.19	2.7 to 6.0	8K	512	44	QFP	80
75P328	LCD controller/driver; A/D converter	4.19	4.5 to 5.5	8K OTPROM	512	44	QFP	80
75402A	Low-end	4.19	2.7 to 6.0	2K	64	22	DIP SDIP QFP	28 28 44
75P402	Low-end	4.19	4.5 to 5.5	2K OTPROM	64	22	DIP SDIP QFP	28 28 44
75512	High-end; A/D converter	4.19	2.7 to 6.0	12K	512	64	QFP	80
75516	High-end; A/D converter	4.19	2.7 to 6.0	16K	512	64	QFP	80
75P516	High-end; A/D converter	4.19	4.75 to 5.5	16K OTPROM	512	64	QFP Ceramic LCC	80 80

8-Bit, Single-Chip CMOS Microcomputers

Device, µPD	Features	Clock (MHz)	Supply Voltage (V)	ROM (X8)	RAM (X8)	I/O	# Package	Pins
78C10/78C10A	CMOS; A/D converter	15	4.5 to 5.5	External	256	32	QUIP SDIP QFP PLCC	64 64 64 68
78C11/78C11A	CMOS; A/D converter	15	4.5 to 5.5	4K	256	44	QUIP SDIP QFP PLCC	64 64 64 68
78C12A	CMOS; A/D converter	15	4.5 to 5.5	8K	256	44	QUIP SDIP QFP PLCC	64 64 64 68
78C14/78C14A	CMOS; A/D converter	15	4.5 to 5.5	16K	256	44	QUIP SDIP QFP PLCC	64 64 64 68
78CP14	CMOS; A/D converter	15	4.75 to 5.25	16K OTPROM	256	44	QUIP SDIP QFP PLCC	64 64 64 68
				16K UVEPROM	256	44	Ceramic QUIP Shrink cerdip	64 64
78CG14	CMOS; A/D converter; piggyback EPROM	15	4.5 to 5.5	4K, 8K or 16K	256	44	Ceramic QUIP	64
78213	CMOS; A/D converter; advanced peripherals	12	4.5 to 5.5	External	512	54	SDIP QUIP QFP PLCC	64 64 74 68
78214	CMOS; A/D converter; advanced peripherals	12	4.5 to 5.5	16K	512	54	SDIP QUIP QFP PLCC	64 64 74 68

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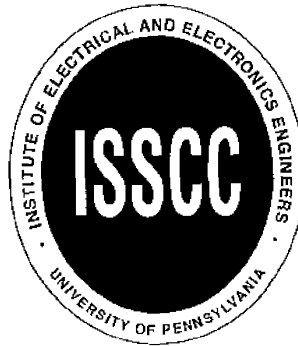
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Low-Temperature Circuits and
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Session 14
Signal Processing for Multimedia

WA 17.4 A Dynamic Voltage Scaled Microprocessor System

Thomas Burd, Trevor Pering[1], Anthony Stratakos[2], Robert Brodersen

Berkeley Wireless Research Center, Univ. of California, Berkeley, CA
[1]Intel, Hillsboro, OR
[2]Volterra, Fremont, CA

The microprocessor system in portable electronic devices often has a time-varying computational load which is comprised of: 1) compute-intensive and low-latency processes, 2) background and high-latency processes, and 3) system idle. The key design objectives for the processor systems in these applications are providing the highest possible peak performance for the compute-intensive code (e.g., handwriting recognition, image decompression) while maximizing the battery life for the remaining low performance periods.

A common power-saving technique is to reduce clock frequency during non-compute intensive activity. This reduces power, but does not affect the total energy consumed per process. On the other hand, reducing the voltage of the processor improves its energy efficiency, but compromises its peak performance. If, however, clock frequency (f_{CLK}) and supply voltage (V_{DD}) are dynamically varied in response to computational load demands, then energy consumed per process can be reduced for the low computational periods, while retaining peak performance when required. This strategy, which achieves the highest possible energy efficiency for time-varying computational loads, is called dynamic voltage scaling (DVS).

A prototype DVS-enabled chip-set in 0.6µm 3-metal $V_T \approx 1V$, CMOS contains a battery-powered (3.3-6.0V) switching regulator, a microprocessor, SRAM memory chips, and an interface chip for connecting to commercial I/O peripherals. The microprocessor operates from 1.2-3.8V and 5-80MHz with 0.54mW/MIP minimum energy consumption. This is an improvement of 4x in both frequency range and minimum energy consumption over previous work which optimized energy for a fixed frequency at power-on, and demonstrates DVS on a microprocessor, under direct operating system control, and over a complete chip-set [1].

A voltage scheduler is required in the operating system of a DVS system. It controls f_{CLK} (and V_{DD}) by writing a desired frequency (in MHz) to a coprocessor register. Individual applications supply a completion deadline, and the voltage scheduler uses the applications' previous execution history to determine the number of processor cycles required and sets f_{CLK} accordingly. By optimally adjusting f_{CLK}, the CPU system always operates at the minimum performance level required by the current active processes and thereby consumes the minimal amount of energy [2].

Figure 17.4.1 shows two seconds of a user-interface process, which is generally bursty and high-latency. The top trace demonstrates typical microprocessor operation, running at full-speed or idling. The lower trace shows the voltage scheduler operating, demonstrating that much of the computation can be done at low V_{DD}, dramatically improving energy efficiency.

A regulation feedback loop for setting the variable V_{DD} and f_{CLK} is shown in Figure 17.4.2. The ring oscillator, which tracks the critical paths of the microprocessor over voltage, outputs f_{CLK} as a function of V_{DD}. The f_{CLK} signal is digitally quantized in 1MHz steps, and used to generate a frequency error, F_{ERR}. The loop filter implements a hybrid pulse-width/pulse-frequency modulation algorithm that generates an M_P or M_N enable. The regulated V_{DD}, which is fed back to the CPU chip to close the loop, is generated across the capacitor.

The converter operates in either tracking or regulation mode, as indicated by the track status signal. A new frequency request initiates tracking mode in which the converter either delivers or removes charge from the capacitor, depending upon the sign of F_{ERR}. When the error magnitude is less than 4MHz, the converter switches to the regulation mode in which M_N is disabled and only the processor circuits can remove charge.

The efficiency of the dc-dc converter ranges from 90% at high V_{DD}, to 80% at the lowest V_{DD}. The transition time is at most 70µs, shown by the maximum 5-80MHz transition in Figure 17.4.3. Conversion losses create an energy penalty when changing voltage on the external capacitance. This penalty is at most 4µJ, which is equivalent to 712 full-load cycles at 80MHz.

The complete microprocessor system is shown in Figure 17.4.4. The CPU chip contains a custom-implementation ARM8 processor core[3]; a 16kB, 32-way set-associative unified cache; a 12-element write buffer; a bus interface with a simple memory controller; and a system coprocessor which contains the desired frequency register, the regulator interface, real-time counter, performance counters, and other system control state. The SRAM chip contains 64kB of memory and supports burst-mode accesses. The I/O chip level-converts to 3.3V and performs flow control. Connecting these three chips is a custom system bus which is powered by the variable V_{DD}.

There are constraints on the digital circuits to ensure they operate properly with a varying V_{DD}. Capacitance cannot hold state for more than 1/2 of a clock cycle, such as in DRAMs and tri-state busses; otherwise, false logic lows can be induced when V_{DD} increases. To prevent this, all tri-state busses have weak pMOS feedback to maintain the V_{DD} voltage level on high signals. Sense-amp circuits are restricted to being precharged all the way to V_{DD}. Also, nMOS pass gates are not allowed because they fail for $V_{DD} < V_{tP} + V_{tN}$. Figure 17.4.5 shows the cache-tag CAM cell which is modified for DVS. The match devices (M1, M2) are typically nMOS pass gates. However, rather than switch to CMOS pass gates, pMOS match devices are used in conjunction with pre-discharge devices (M3, M4) so that the bitlines are precharged high between match operations, which is the same polarity for reads and writes to the cell.

As shown in Figure 17.4.6, system performance ranges from 6-85 Dhrystone 2.1MIPs, and the total system energy consumption ranges from 0.54-5.6mW/MIP. In the optimum case when only a small fraction of the computation requires peak performance, the microprocessor system can effectively deliver 85MIPs while consuming on average 0.54mW/MIP. A halt command can put the processor into a sleep mode in which the system will dissipate only 800µW, with a one cycle start-up.

To evaluate DVS, three benchmarks are executed on the system: video decompression (mpeg), audio processing (audio), and a PDA-like application (ui). They are first run at constant maximum performance to measure baseline energy consumption. They are then run with the voltage scheduler (shown in Figure 17.4.1 for the ui benchmark) and their energy consumption is measured again. The highly compute-intensive mpeg benchmark has only a 11% energy reduction from DVS, while the audio and ui benchmarks have a 4.5x and 3.5x energy reduction, respectively.

References:
[1] Kuroda, T, et al., "Variable Supply-Voltage Scheme for Low-Power High-Speed CMOS Digital Design", IEEE J. Solid-State Circuits, vol. 33, no. 3, pp. 454-462, Mar. 1998.
[2] Pering, T., et al., "The Simulation and Evaluation of Dynamic Voltage Scaling Algorithms", Proc. of ISLPED, pp. 76-81, Aug. 1998
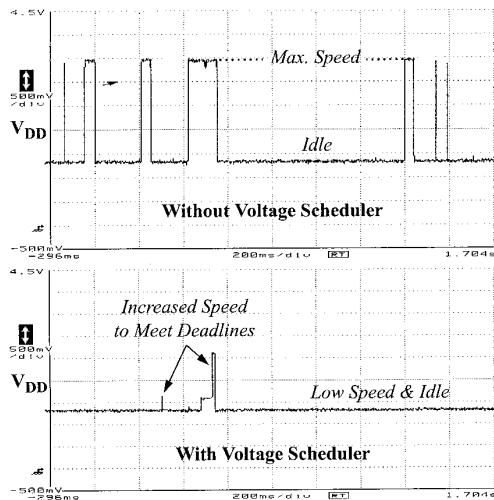[3] ARM 8 Data-Sheet, Document Number ARM-DDI-0080C, ARM Ltd., July 1996.
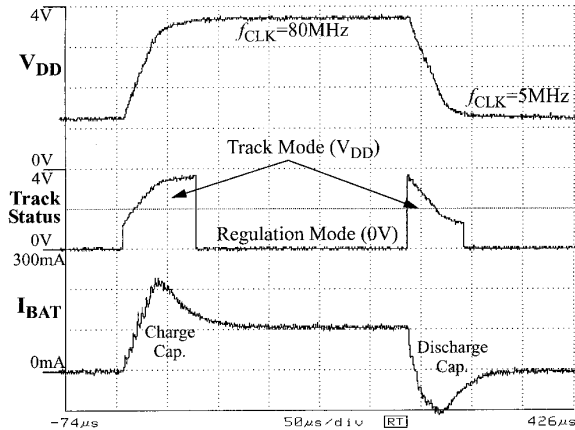
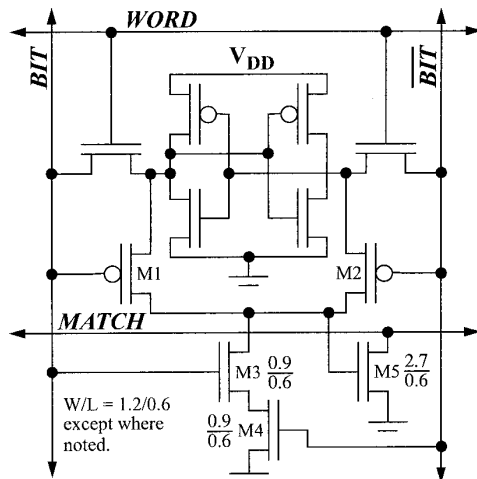Figure 17.4.1: DVS improvement for UI process.

Figure 17.4.2: Frequency to voltage feedback loop.

Figure 17.4.3: Transient response of regulation loop.
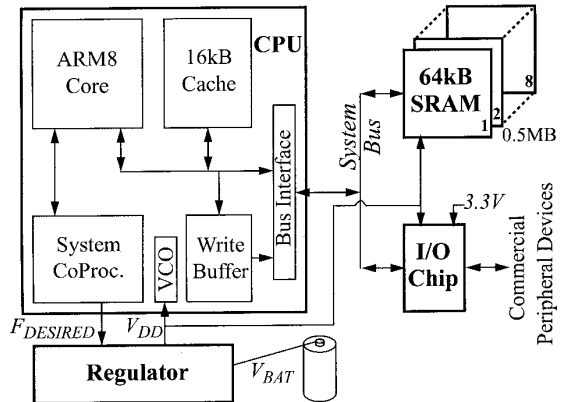
Figure 17.4.4: System architecture - 4 custom chips.

Figure 17.4.5: DVS-compatible CAM cell.
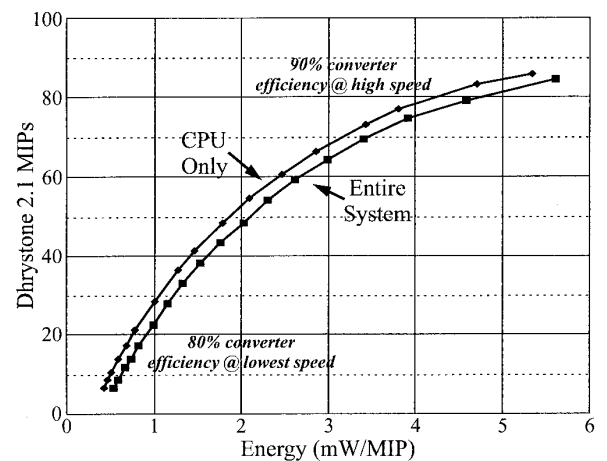
Figure 17.4.6: Measured performance vs. energy.

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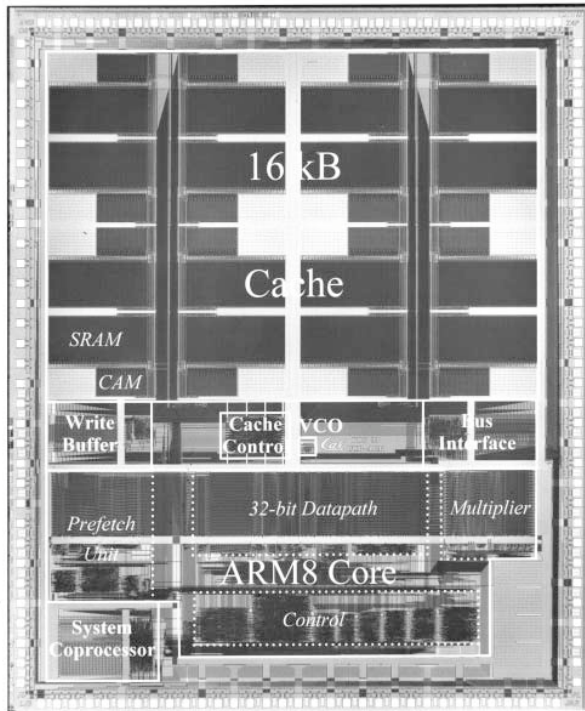
Figure 17.4.7: CPU micrograph
(7.5x9.0mm², 1.3M transistors).
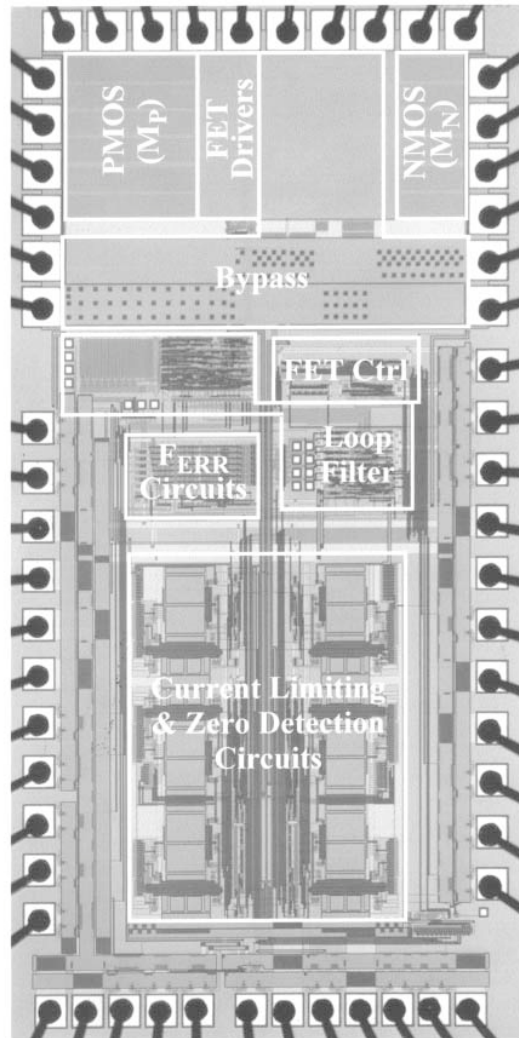
Figure 17.4.8: Regulator micrograph (1.7x3.4mm²).

EXHIBIT 3

EVALUATION KIT AVAILABLE

MAXIM

High-Efficiency, PWM, Step-Down DC-DC Controllers in 16-Pin QSOP

MAX1652–MAX1655

General Description

The MAX1652–MAX1655 are high-efficiency, pulse-width-modulated (PWM), step-down DC-DC controllers in small QSOP packages. The MAX1653/MAX1655 also come in 16-pin narrow SO packages that are pin-compatible upgrades to the popular MAX797. Improvements include higher duty-cycle operation for better dropout, lower quiescent supply currents for better light-load efficiency, and an output voltage down to 1V (MAX1655).

The MAX1652–MAX1655 achieve up to 96% efficiency and deliver up to 10A using a unique Idle Mode™ synchronous-rectified PWM control scheme. These devices automatically switch between PWM operation at heavy loads and pulse-frequency-modulated (PFM) operation at light loads to optimize efficiency over the entire output current range. The MAX1653/MAX1655 also feature logic-controlled, forced PWM operation for noise-sensitive applications.

All devices operate with a selectable 150kHz/300kHz switching frequency, which can also be synchronized to an external clock signal. Both external power switches are inexpensive N-channel MOSFETs, which provide low resistance while saving space and reducing cost.

The MAX1652 and MAX1654 have an additional feedback pin that permits regulation of a low-cost second output tapped from a transformer winding. The MAX1652 provides an additional positive output. The MAX1654 provides an additional negative output.

The MAX1652–MAX1655 have a 4.5V to 30V input voltage range. The MAX1652/MAX1653/MAX1654's output range is 2.5V to 5.5V while the MAX1655's output range extends down to 1V. An evaluation kit (MAX1653EVKIT) is available to speed designs.

Applications

Notebook Computers

PDAs

Cellular Phones

Hand-Held Computers

Handy-Terminals

Mobile Communicators

Distributed Power

Pin Configurations appear at end of data sheet.

Idle Mode is a trademark of Maxim Integrated Products.

Features

♦ **96% Efficiency**
♦ **Small, 16-Pin QSOP Package (half the size of a 16-pin narrow SO)**
♦ **Pin-Compatible with MAX797 (MAX1653/MAX1655)**
♦ **Output Voltage Down to 1V (MAX1655)**
♦ **4.5V to 30V Input Range**
♦ **99% Duty Cycle for Lower Dropout**
♦ **170µA Quiescent Supply Current**
♦ **3µA Logic-Controlled Shutdown**
♦ **Dual, N-Channel, Synchronous-Rectified Control**
♦ **Fixed 150kHz/300kHz PWM Switching, or Synchronized from 190kHz to 340kHz**
♦ **Programmable Soft Start**
♦ **Low-Cost Secondary Outputs (MAX1652/MAX1654)**

Ordering Information

PART	TEMP. RANGE	PIN-PACKAGE
MAX1652EEE	-40°C to +85°C	16 QSOP
MAX1653ESE	-40°C to +85°C	16 Narrow SO
MAX1653EEE	-40°C to +85°C	16 QSOP
MAX1654EEE	-40°C to +85°C	16 QSOP
MAX1655ESE	-40°C to +85°C	16 Narrow SO
MAX1655EEE	-40°C to +85°C	16 QSOP

Selection Guide

PART	FEEDBACK VOLTAGE (V)	SPECIAL FEATURE	COMPATIBILITY
MAX1652	2.5	Regulates positive secondary voltage (such as +12V)	Same pin order as MAX796, but smaller package
MAX1653	2.5	Logic-controlled, low-noise mode	Pin-compatible with MAX797
MAX1654	2.5	Regulates negative secondary voltage (such as -5V)	Same pin order as MAX799, but smaller package
MAX1655	1	Low output voltages (1V to 5.5V); logic-controlled, low-noise mode	Pin compatible with MAX797 (except for feedback voltage)

MAXIM _____ **Maxim Integrated Products   1**

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For small orders, phone 408-737-7600 ext. 3468.

High-Efficiency, PWM, Step-Down DC-DC Controllers in 16-Pin QSOP

ABSOLUTE MAXIMUM RATINGS

V+ to GND ....-0.3V to +36V
GND to PGND ....-0.3V to +0.3V
VL to GND ....-0.3V to +6V
BST to GND ....-0.3V to +36V
DH to LX ....-0.3V to (BST + 0.3V)
LX to BST ....-6V to +0.3V
$\overline{\text{SHDN}}$ to GND..-0.3V to (V+ + 0.3V)
SYNC, SS, REF, SECFB, $\overline{\text{SKIP}}$, FB to GND...-0.3V to (VL + 0.3V)
DL to PGND ....-0.3V to (VL + 0.3V)
CSH, CSL to GND ....-0.3V to +6V
VL Short Circuit to GND..Momentary

REF Short Circuit to GND ....Continuous
VL Output Current ....+50mA to -1mA
REF Output Current..+5mA to -1mA
Continuous Power Dissipation (T_A = +70°C)
    SO (derate 8.70mW/°C above +70°C) 696mW
    QSOP (derate 8.3mW/°C above +70°C) 667mW
Operating Temperature Range
    MAX165_E_E ....-40°C to +85°C
Storage Temperature Range ....-65°C to +160°C
Lead Temperature (soldering, 10sec) ....+300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V+ = +15V, GND = PGND = 0V, SYNC = REF, I_{VL} = I_{REF} = 0A, **T_A = 0°C to +85°C**, unless otherwise noted.)

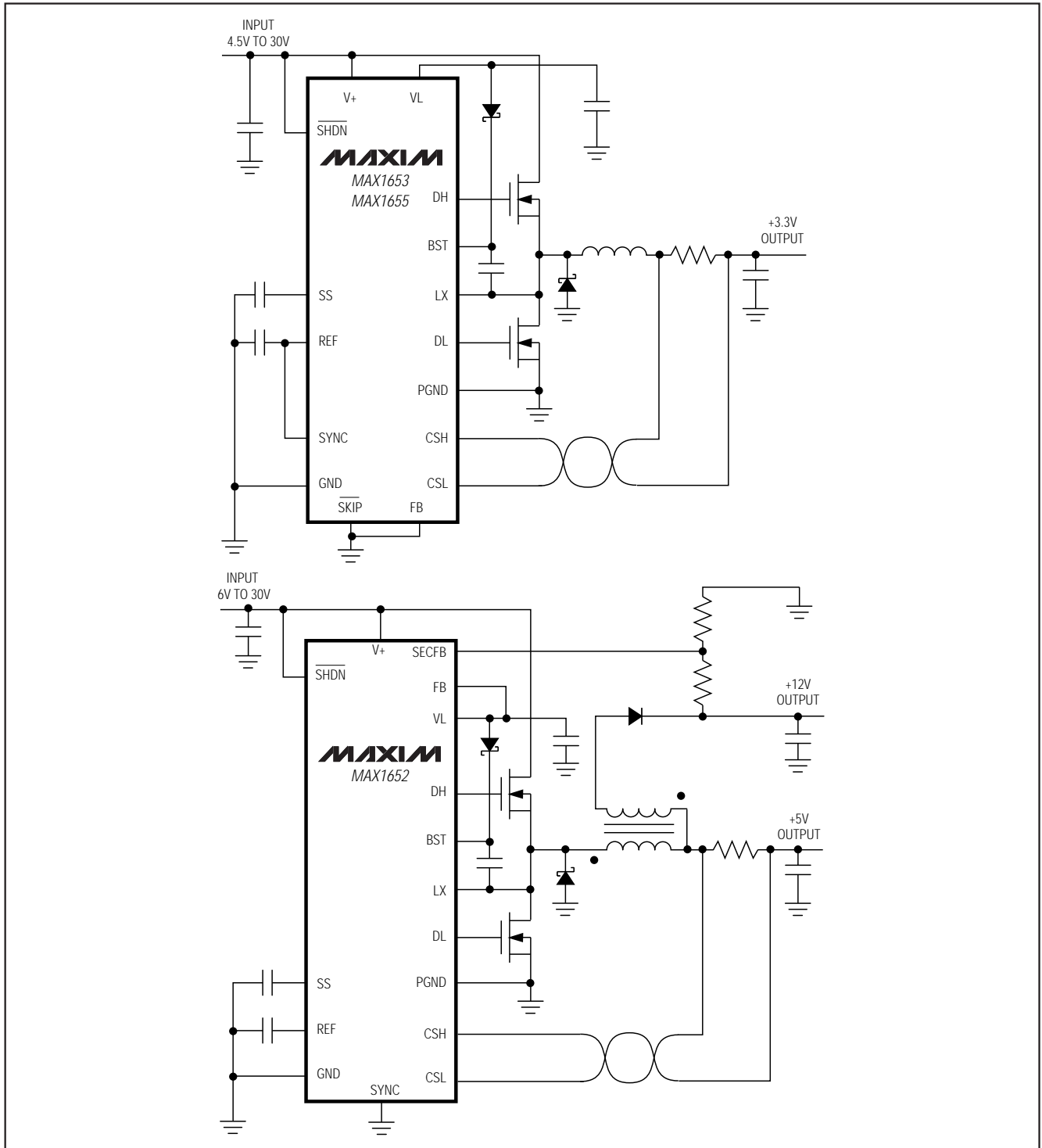| PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
3.3V AND 5V STEP-DOWN CONTROLLERS						
Input Supply Range			4.5		30	V
5V Output Voltage (CSL)	0 < (CSH - CSL) < 80mV, FB = VL, 6V < V+ < 30V, includes line and load regulation		4.85	5.06	5.25	V
3.3V Output Voltage (CSL)	0 < (CSH - CSL) < 80mV, FB = 0V, 4.5V < V+ < 30V, includes line and load regulation		3.20	3.34	3.46	V
Nominal Adjustable Output Voltage Range	External resistor divider	MAX1655	1		5.5	V
		MAX1652/MAX1653/ MAX1654	2.5		5.5	
Feedback Voltage	CSH - CSL = 0V, CSL = FB, $\overline{\text{SKIP}}$ = 0V, 4.5V < V+ < 30V	MAX1655	0.97	1.00	1.03	V
		MAX1652/MAX1653/ MAX1654	2.43	2.50	2.57	
Load Regulation	0 < (CSH - CSL) < 80mV			2		%
	25mV < (CSH - CSL) < 80mV			1.2		
Line Regulation	6V < V+ < 30V			0.03	0.06	%/V
Current-Limit Voltage	CSH - CSL, positive		80	100	120	mV
	CSH - CSL, negative		-50	-100	-160	
SS Source Current	V_{SS} = 0V		2.5	4.0	6.5	µA
SS Fault Sink Current	V_{SS} = 4V		2.0			mA
FLYBACK/PWM CONTROLLER						
SECFB Regulation Setpoint	Falling edge, rising edge, hysteresis = 22mV (MAX1652)		2.45	2.50	2.55	V
	Rising edge, falling edge, hysteresis = 22mV (MAX1654)		-0.05	0	0.05	
INTERNAL REGULATOR AND REFERENCE						
VL Output Voltage	$\overline{\text{SHDN}}$ = 2V, 0 < I_{VL} < 25mA, 5.5V < V+ < 30V		4.7	5.0	5.3	V
VL Fault Lockout Voltage	Rising edge, falling edge hysteresis = 50mV		3.8	3.9	4.0	V
VL/CSL Switchover Voltage	Rising edge, falling edge hysteresis = 60mV		4.2	4.5	4.7	V

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MAXIM

ELECTRICAL CHARACTERISTICS (continued)

(V+ = +15V, GND = PGND = 0V, SYNC = REF, I_{VL} = I_{REF} = 0A, **T_A = 0°C to +85°C,** unless otherwise noted.)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Reference Output Voltage	No external load (Note 1)	2.46	2.50	2.54	V
Reference Fault Lockout Voltage	Falling edge	2.0		2.4	V
Reference Load Regulation	0 < I_{REF} < 100µA			15	mV
CSL, CSH Shutdown Leakage Current	$\overline{SHDN}$ = 0V, CSL = 5.5V, CSH = 5.5V, V+ = 0 or 30V, VL = 0V		0.1	1	µA
V+ Shutdown Current	$\overline{SHDN}$ = 0V, V+ = 30V, CSL = 0 or 5.5V		3	7	µA
V+ Off-State Leakage Current	FB = CSH = CSL = 5.5V, VL switched over to CSL		5	15	µA
Dropout Power Consumption	V+ = 4.5V, CSH = CSL = 4.0V (Note 2)		1	8	mW
Quiescent Power Consumption	CSH = CSL = 5.5V		1	2	mW
OSCILLATOR AND INPUTS/OUTPUTS					
Oscillator Frequency	SYNC = REF	270	300	330	kHz
	SYNC = 0 or 5V	125	150	175	
SYNC High Pulse Width		200			ns
SYNC Low Pulse Width		200			ns
SYNC Rise/Fall Time	Guaranteed by design, not tested			200	ns
Oscillator Sync Range		190		340	kHz
Dropout-Mode Maximum Duty Cycle	SYNC = REF	97	98		%
	SYNC = 0 or 5V	98	99		
Input High Voltage	SYNC	VL - 0.5			V
	$\overline{SHDN}$, $\overline{SKIP}$	2.0			
Input Low Voltage	SYNC			0.8	V
	$\overline{SHDN}$, $\overline{SKIP}$			0.5	
Input Current	$\overline{SHDN}$, 0 or 30V			3.0	µA
	SECFB, 0 or 4V			0.1	
	SYNC, $\overline{SKIP}$			1.0	
	CSH, CSL, CSH = CSL ≤ 4V			70	
	FB, FB = REF			±0.1	
DL Sink/Source Current	DL forced to 2V		1		A
DH Sink/Source Current	DH forced to 2V, BST - LX = 4.5V		1		A
DL On-Resistance	High or low		1.5	5	Ω
DH On-Resistance	High or low, BST - LX = 4.5V		1.5	5	Ω

Note 1: Since the reference uses VL as its supply, V+ line-regulation error is insignificant.
Note 2: At very low input voltages, quiescent supply current may increase due to excessive PNP base current in the VL linear regulator. This occurs if V+ falls below the preset VL regulation point (5V nominal).

MAXIM _____ **3**

MAX1652–MAX1655

ELECTRICAL CHARACTERISTICS (continued)

(V+ = +15V, GND = PGND = 0V, SYNC = REF, I$_{VL}$ = I$_{REF}$ = 0A, **T$_A$ = -40°C to +85°C,** unless otherwise noted.) (Note 3)

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
3.3V and 5V STEP-DOWN CONTROLLERS						
Input Supply Range			4.5		30	V
5V Output Voltage (CSL)	0 < (CSH - CSL) < 70mV, FB = VL, 6V < V+ < 30V, includes line and load regulation		4.80		5.30	V
3.3V Output Voltage (CSL)	0 < (CSH - CSL) < 70mV, FB = VL, 4.5V < V+ < 30V, includes line and load regulation		3.16		3.50	V
Feedback Voltage	CSH - CSL = 0V, 5V < V+ < 30V, CSL = FB, $\overline{SKIP}$ = 0V	MAX1655	0.96		1.04	V
		MAX1652/MAX1653/MAX1654	2.40		2.60	
Line Regulation	6V < V+ < 30V				0.06	%/V
Current-Limit Voltage	CSH - CSL, positive		70		130	mV
	CSH - CSL, negative		-40		-160	
FLYBACK/PWM CONTROLLER						
SECFB Regulation Setpoint	Falling edge, hysteresis = 22mV (MAX1652)		2.40		2.60	V
	Falling edge, hysteresis = 22mV (MAX1654)		-0.08		0.08	
INTERNAL REGULATOR AND REFERENCE						
VL Output Voltage	$\overline{SHDN}$ = 2V, 0 < I$_{VL}$ < 25mA, 5.5V < V+ < 30V		4.7		5.3	V
VL Fault Lockout Voltage	Rising edge, hysteresis = 50mV		3.75		4.05	V
VL/CSL Switchover Voltage	Rising edge, hysteresis = 60mV		4.2		4.7	V
Reference Output Voltage	No external load (Note 1)		2.43		2.57	V
Reference Load Regulation	0 < I$_{REF}$ < 100µA				15	mV
V+ Shutdown Current	$\overline{SHDN}$ = 0V, V+ = 30V, CSL = 0 or 5.5V				10	µA
V+ Off-State Leakage Current	FB = CSH = CSL = 5.5V, VL switched over to CSL				15	µA
Quiescent Power Consumption					2	mW
OSCILLATOR AND INPUTS/OUTPUTS						
Oscillator Frequency	SYNC = REF		250		350	kHz
	SYNC = 0 or 5V		120		180	
SYNC High Pulse Width			250			ns
SYNC Low Pulse Width			250			ns
Oscillator Sync Range			210		320	kHz
Maximum Duty Cycle	SYNC = REF		97			%
	SYNC = 0 or 5V		98			
DL On-Resistance	High or low				5	Ω
DH On-Resistance	High or low, BST - LX = 4.5V				5	Ω

Note 3: Specifications from 0°C to -40°C are guaranteed by design, not production tested.

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MAX1652–MAX1655

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MAX1652–MAX1655

Typical Operating Circuits (continued)
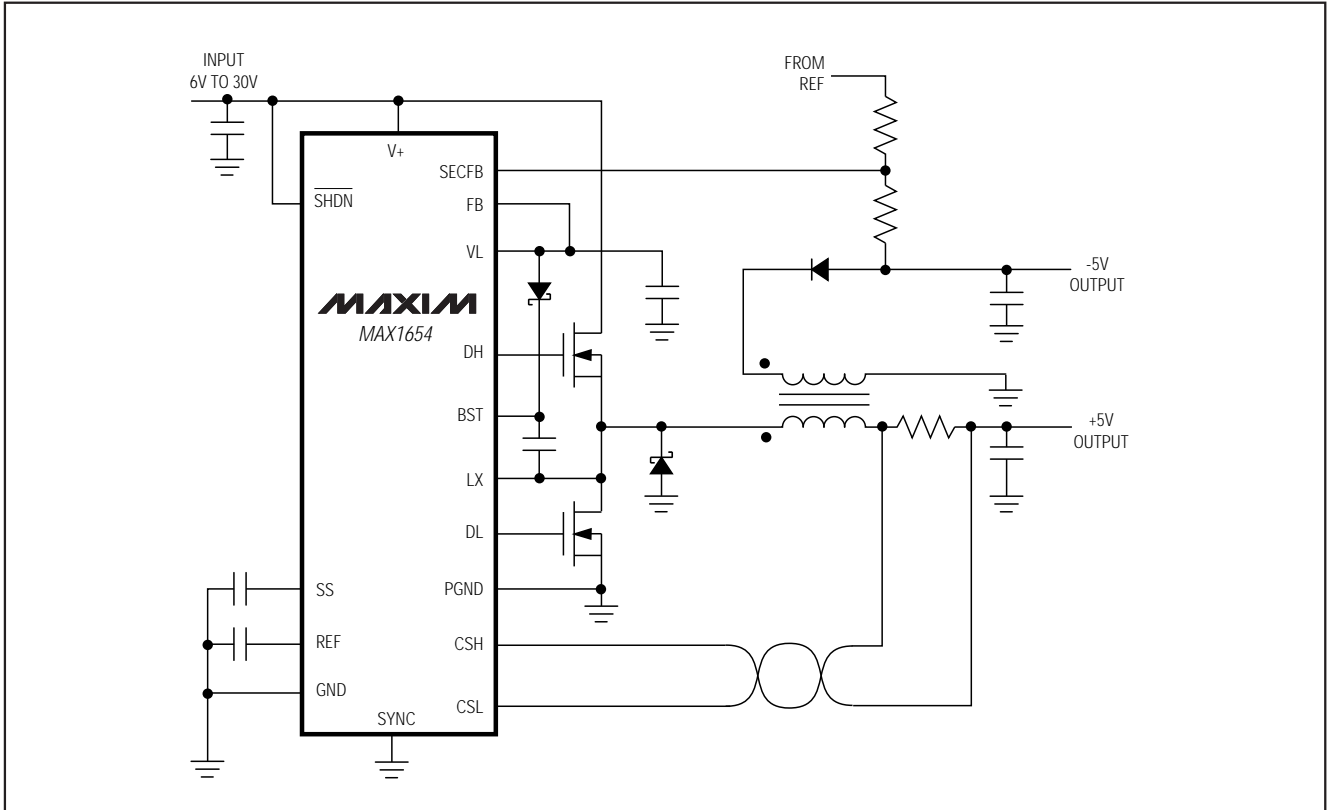
Typical Operating Characteristics

(Circuit of Figure 1, $\overline{\text{SKIP}}$ = GND, T_A = +25°C, unless otherwise noted.)
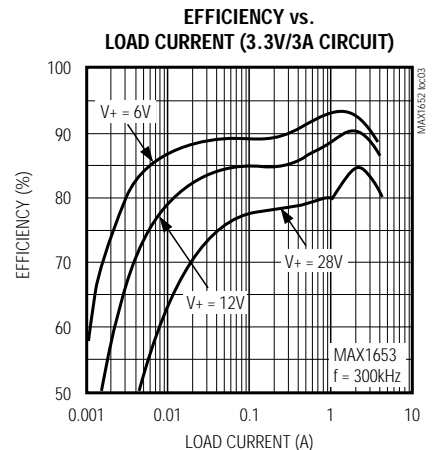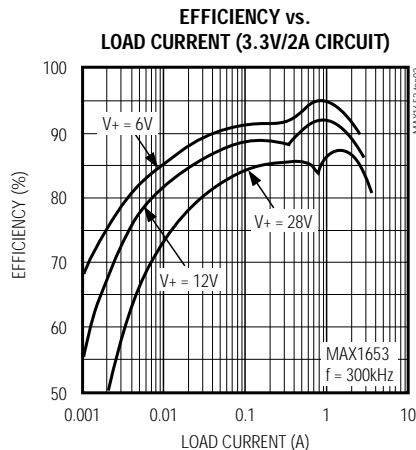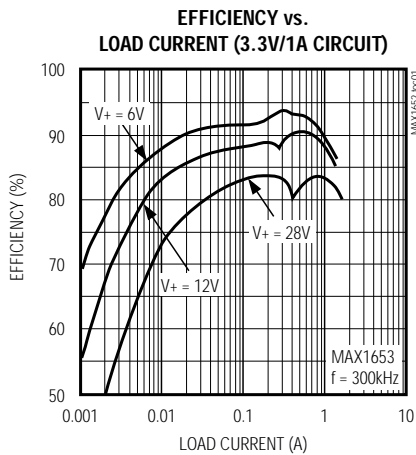
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MAX1652–MAX1655

_____**Typical Operating Characteristics (continued)**

(Circuit of Figure 1, $\overline{SKIP}$ = GND, T_A = +25°C, unless otherwise noted.)

EFFICIENCY vs. LOAD CURRENT (3.3V/5A CIRCUIT)

EFFICIENCY vs. LOAD CURRENT (5V/3A CIRCUIT)

EFFICIENCY vs. LOAD CURRENT (1.8V/2.5A CIRCUIT)

IDLE-MODE SUPPLY CURRENT vs. INPUT VOLTAGE (3.3V/3A CIRCUIT)

PWM-MODE SUPPLY CURRENT vs. INPUT VOLTAGE (3.3V/3A CIRCUIT)

SHUTDOWN SUPPLY CURRENT vs. INPUT VOLTAGE

REF LOAD-REGULATION ERROR vs. REF LOAD CURRENT

VL LOAD-REGULATION ERROR vs. VL LOAD CURRENT

MAX1652 MAXIMUM SECONDARY OUTPUT CURRENT vs. SUPPLY VOLTAGE

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MAX1652–MAX1655

_____**Typical Operating Characteristics (continued)**

(Circuit of Figure 1, $\overline{\text{SKIP}}$ = GND, T_A = +25°C, unless otherwise noted.)

**DROPOUT VOLTAGE vs.
LOAD CURRENT (3.3V/3A CIRCUIT)**
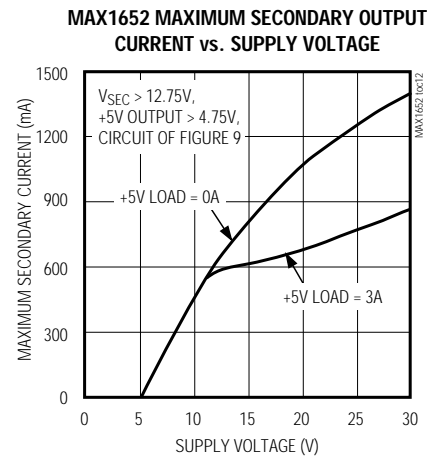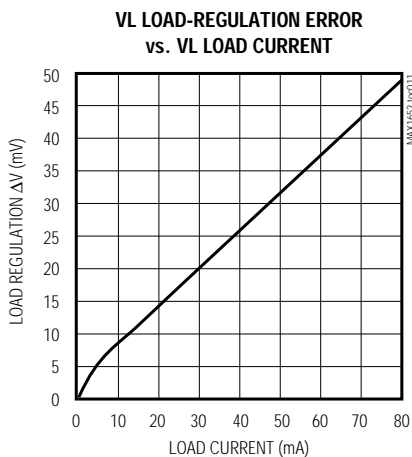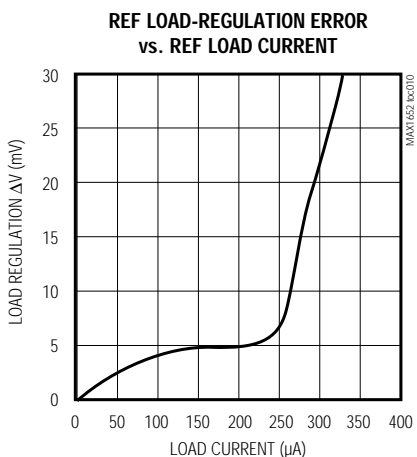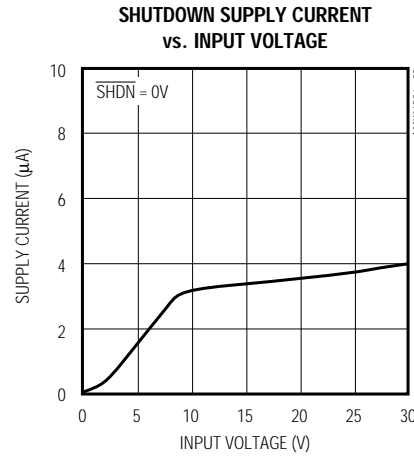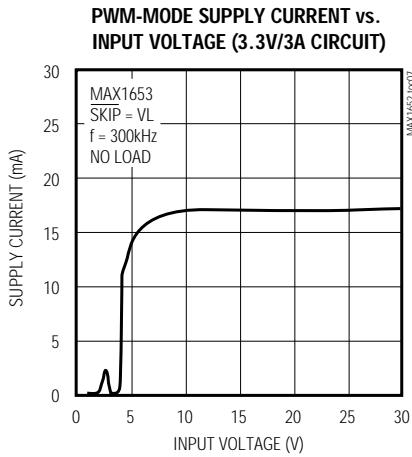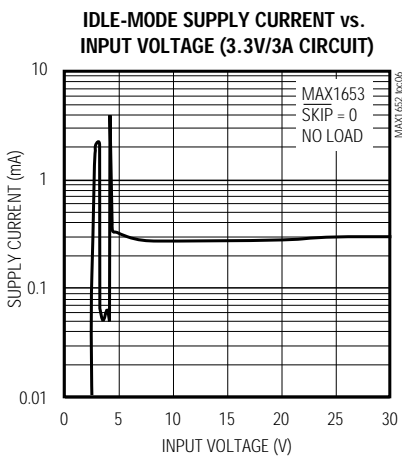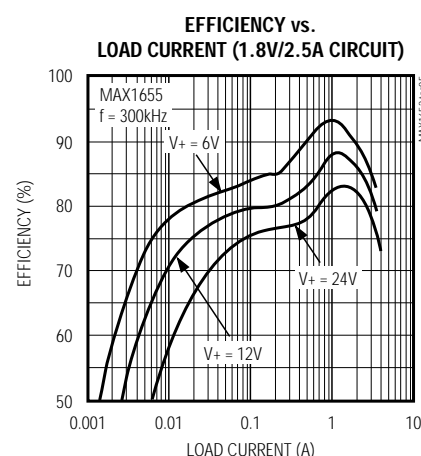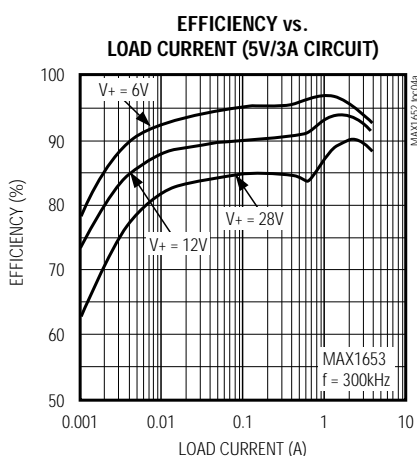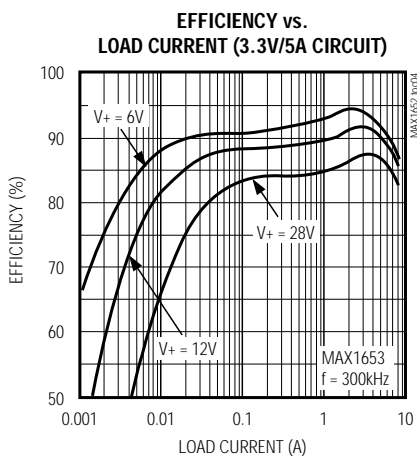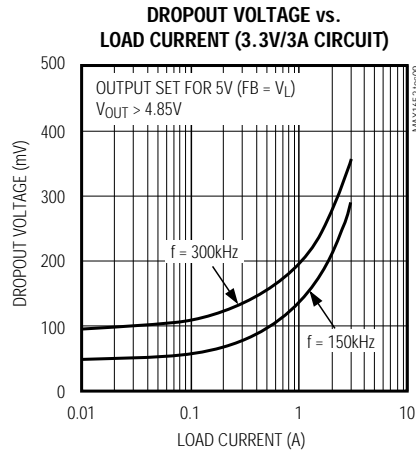
**PULSE-WIDTH-MODULATION
MODE WAVEFORMS**
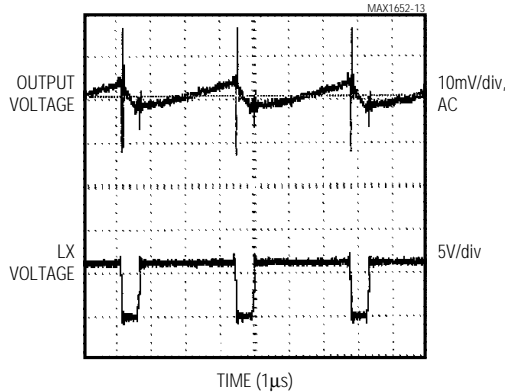
V_{IN} = 6V, 3.3V/3A CIRCUIT

IDLE-MODE WAVEFORMS
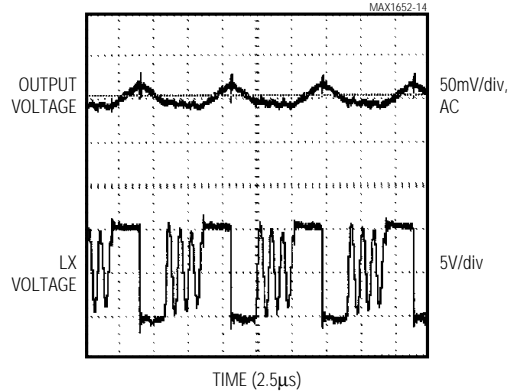
I_{LOAD} = 300mA, V_{IN} = 10V, 3.3V/3A CIRCUIT

DROPOUT WAVEFORMS
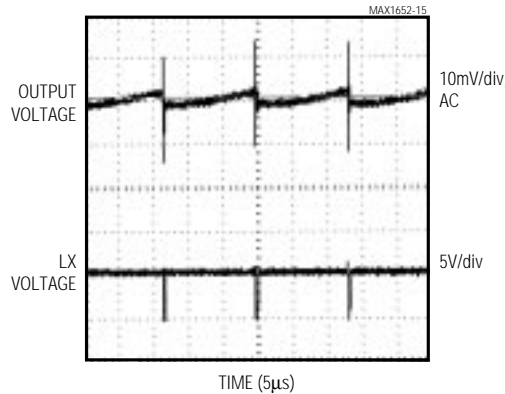
V_{IN} = 5.1V, NO LOAD, 3.3V/3A CIRCUIT,
SET TO 5V OUTPUT (FB = VL)

LOAD-TRANSIENT RESPONSE

V_{IN} = 15V, 3.3V/3A CIRCUIT

MAX1652–MAX1655

PIN	NAME	FUNCTION
1	SS	Soft-Start Timing Capacitor Connection. Ramp time to full current limit is approximately 1ms/nF.
2	SECFB (MAX1652/ MAX1654)	Secondary Winding Feedback Input. Normally connected to a resistor divider from an auxiliary output. **Don't leave SECFB unconnected.** • MAX1652: SECFB regulates at VSECFB = 2.50V. Tie to VL if not used. • MAX1654: SECFB regulates at VSECFB = 0V. Tie to a negative voltage through a high-value current-limiting resistor (I_{MAX} = 100µA) if not used.
	$\overline{SKIP}$ (MAX1653/ MAX1655)	Disables pulse-skipping mode when high. Connect to GND for normal use. **Don't leave $\overline{SKIP}$ unconnected.** With $\overline{SKIP}$ grounded, the device will *automatically* change from pulse-skipping operation to full PWM operation when the load current exceeds approximately 30% of maximum (Table 3).
3	REF	Reference Voltage Output. Bypass to GND with 0.33µF minimum.
4	GND	Low-Noise Analog Ground and Feedback Reference Point
5	SYNC	Oscillator Synchronization and Frequency Select. Tie to GND or VL for 150kHz operation; tie to REF for 300kHz operation. A high-to-low transition begins a new cycle. Drive SYNC with 0 to 5V logic levels (see the *Electrical Characteristics* table for V_{IH} and V_{IL} specifications). SYNC capture range is 190kHz to 340kHz.
6	$\overline{SHDN}$	Shutdown Control Input, active low. Logic threshold is set at approximately 1V (V_{TH} of an internal N-channel MOSFET). Tie $\overline{SHDN}$ to V+ for automatic start-up.
7	FB	Feedback Input. Regulates at the feedback voltage in adjustable mode. FB is a Dual Mode™ input that also selects the fixed output voltage settings as follows: • Connect to GND for 3.3V operation. • Connect to VL for 5V operation. • Connect FB to a resistor divider for adjustable mode. FB can be driven with +5V CMOS logic in order to change the output voltage under system control.
8	CSH	Current-Sense Input, high side. Current-limit level is 100mV referred to CSL.
9	CSL	Current-Sense Input, low side. Also serves as the feedback input in fixed-output modes.
10	V+	Battery Voltage Input (4.5V to 30V). Bypass V+ to PGND close to the IC with a 0.1µF capacitor. Connects to a linear regulator that powers VL.
11	VL	5V Internal Linear-Regulator Output. VL is also the supply voltage rail for the chip. VL is switched to the output voltage via CSL (V_{CSL} > 4.5V) for automatic bootstrapping. Bypass to GND with 4.7µF. VL can supply up to 5mA for external loads.
12	PGND	Power Ground
13	DL	Low-Side Gate-Drive Output. Normally drives the synchronous-rectifier MOSFET. Swings from 0V to VL.
14	BST	Boost Capacitor Connection for High-Side Gate Drive (0.1µF)
15	LX	Switching Node (inductor) Connection. Can swing 2V below ground without hazard.
16	DH	High-Side Gate-Drive Output. Normally drives the main buck switch. DH is a floating driver output that swings from LX to BST, riding on the LX switching-node voltage.

Dual Mode is a trademark of Maxim Integrated Products.

MAXIM _____ **9**

High-Efficiency, PWM, Step-Down DC-DC Controllers in 16-Pin QSOP

_____Standard Application Circuits

It's easy to adapt the basic MAX1653 single-output 3.3V buck converter (Figure 1) to meet a wide range of applications with inputs up to 30V (limited by choice of external MOSFET). Simply substitute the appropriate components from Table 1 (candidate suppliers are provided in Table 2). These circuits represent a good set of trade-offs among cost, size, and efficiency while staying within the worst-case specification limits for stress-related parameters such as capacitor ripple current.

Don't change the frequency of these circuits without first recalculating component values (particularly inductance value at maximum battery voltage).

For a discussion of dual-output circuits using the MAX1652 and MAX1654, see Figure 9 and the *Secondary Feedback-Regulation Loop* section.

_____Detailed Description

The MAX1652 family are BiCMOS, switch-mode power-supply controllers designed primarily for buck-topology regulators in battery-powered applications where high efficiency and low quiescent supply current are critical. The parts also work well in other topologies such as boost, inverting, and Cuk due to the flexibility of their floating high-speed gate driver. Light-load efficiency is enhanced by automatic idle-mode operation—a variable-frequency pulse-skipping mode that reduces losses due to MOSFET gate charge. The step-down power-switching circuit consists of two N-channel MOSFETs, a rectifier, and an LC output filter. The output voltage is the average of the AC voltage at the switching node, which is adjusted and regulated by changing the duty cycle of the MOSFET switches. The gate-drive signal to the N-channel high-side MOSFET must exceed the battery voltage and is provided by a flying capacitor boost circuit that uses a 100nF capacitor connected to BST.
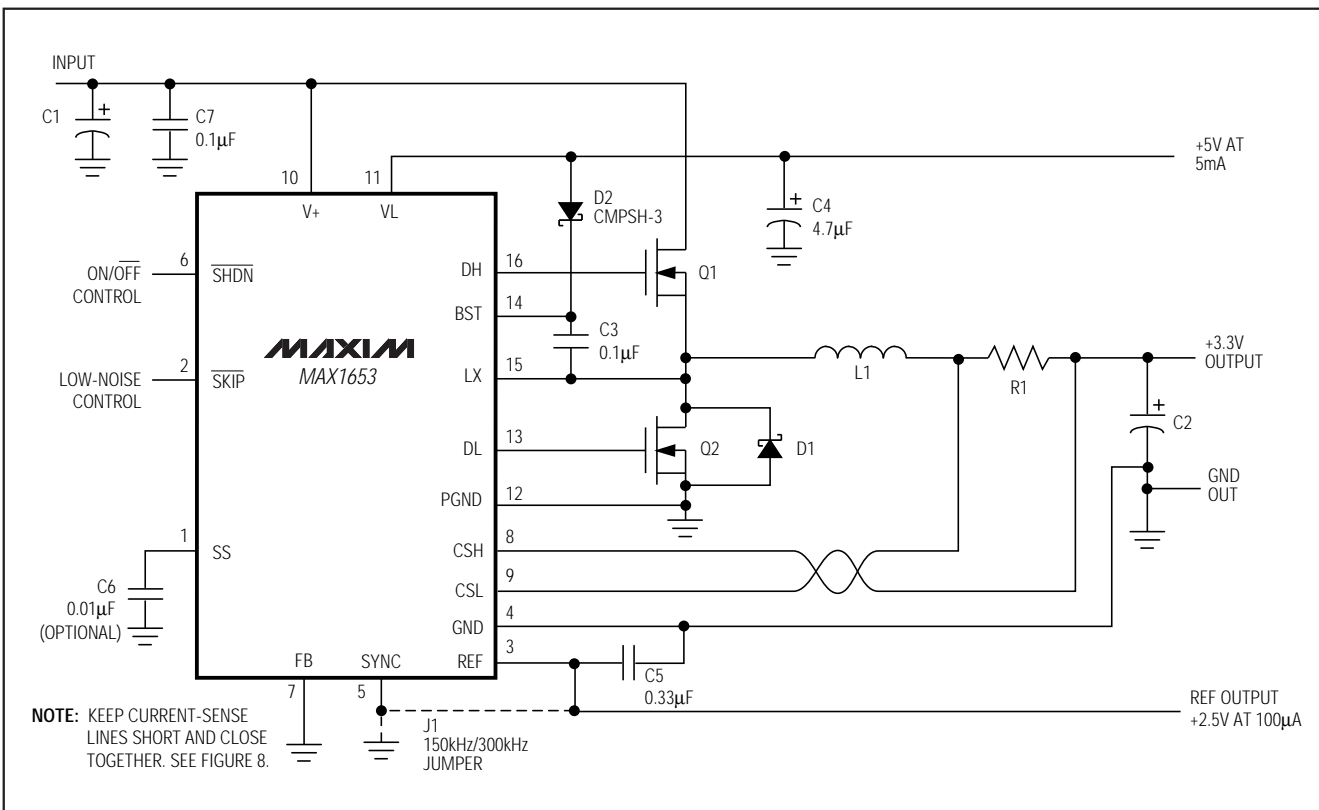
Figure 1. Standard 3.3V Application Circuit (see Table 1 for Component Values)

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MAX1652–MAX1655

Table 1. Component Selection for Standard Applications

COMPONENT	3.3V at 1A	3.3V at 2A	5V/3.3V at 3A	3.3V at 5A	1.8V at 2.5A
Input Range	4.75V to 28V	4.75V to 28V	4.75V to 28V	4.75V to 28V	4.75V to 22V
Frequency	300kHz	300kHz	300kHz	300kHz	150kHz
Q1 High-Side MOSFET	International Rectifier 1/2 IRF7101	International Rectifier 1/2 IRF7303 or Fairchild Semiconductor 1/2 NDS8936	International Rectifier IRF7403 or Fairchild Semiconductor NDS 8410A	Fairchild Semiconductor FDS6680	International Rectifier 1/2 IRF7303 or Fairchild Semiconductor 1/2 NDS8936
Q2 Low-Side MOSFET	International Rectifier 1/2 IRF7101	International Rectifier 1/2 IRF7303 or Fairchild Semiconductor 1/2 NDS8936	International Rectifier IRF7403 or Fairchild Semiconductor NDS 8410A	Fairchild Semiconductor FDS6680	International Rectifier 1/2 IRF7303 or Fairchild Semiconductor 1/2 NDS8936
C1 Input Capacitor	10µF, 35V AVX TPSD106M035R0300	22µF, 35V AVX TPSE226M035R0300	(2) 22µF, 35V AVX TPSE226M035R0300	(3) 22µF, 35V AVX TPSE226M035R0300	10µF, 25V ceramic Taiyo Yuden TMK325F106Z
C2 Output Capacitor	100µF, 6.3V AVX TPSC107M006R	220µF, 10V AVX TPSE227M010R0100 or Sprague 594D227X001002T	470µF, 6V (for 3.3V) Kemet T510X477M006AS **or** (2) 220µF, 10V (for 5V) AVX TPSE227M010R011	(3) 330µF, 10V Sprague 594D337X0010R2T **or** (2) 470µF, 6V Kemet T510X477M006AS	470µF, 4V Sprague 594D477X0004R2T **or** 470µF, 6V Kemet T510X477M006AS
D1 Rectifier	1N5819 or Motorola MBR0520L	1N5819 or Motorola MBRS130LT3	1N5819 or Motorola MBRS130LT3	1N5821 or Motorola MBRS340T3	1N5817 or Motorola MBRS130LT3
R1 Sense Resistor	70mΩ Dale WSL-1206-R070F or IRC LR2010-01-R070	33mΩ Dale WSL-2010-R033F or IRC LR2010-01-R033	25mΩ Dale WSL-2010-R025F or IRC LR2010-01-R025	12mΩ Dale WSL-2512-R012F	30mΩ Dale WSL-2010-R030F or IRC LR2010-01-R030
L1 Inductor	33µH Sumida CDR74B-330	15µH Sumida CDR105B-150	10µH Sumida CDRH125-100	4.7µH Sumida CDRH127-4R7	15µH Sumida CDRH125-150

Table 2. Component Suppliers

MANUFACTURER	USA PHONE	FACTORY FAX [Country Code]
AVX	803-946-0690	[1] 803-626-3123
Central Semiconductor	516-435-1110	[1] 516-435-1824
Coilcraft	847-639-6400	[1] 847-639-1469
Coiltronics	561-241-7876	[1] 561-241-9339
Dale	605-668-4131	[1] 605-665-1627
Fairchild	408-822-2181	[1] 408-721-1635
International Rectifier	310-322-3331	[1] 310-322-3332
IRC	512-992-7900	[1] 512-992-3377
Kemet	408-986-0424	[1] 408-986-1442
Matsuo	714-969-2491	[1] 714-960-6492
Motorola	602-303-5454	[1] 602-994-6430

MANUFACTURER	USA PHONE	FACTORY FAX [Country Code]
Murata	814-237-1431 800-831-9172	[1] 814-238-0490
NIEC	805-867-2555*	[81] 3-3494-7414
Sanyo	619-661-6835	[81] 7-2070-1174
Siliconix	408-988-8000 800-554-5565	[1] 408-970-3950
Sprague	603-224-1961	[1] 603-224-1430
Sumida	847-956-0666	[81] 3-3607-5144
Taiyo Yuden	408-573-4150	[1] 408-573-4159
TDK	847-390-4461	[1] 847-390-4405
Transpower Technologies	702-831-0140	[1] 702-831-3521

Distributor

MAXIM _____ **11**

High-Efficiency, PWM, Step-Down DC-DC Controllers in 16-Pin QSOP

The MAX1652–MAX1655 contain nine major circuit blocks, which are shown in Figure 2:

PWM Controller Blocks:

- Multi-Input PWM Comparator
- Current-Sense Circuit
- PWM Logic Block
- Dual-Mode Internal Feedback Mux
- Gate-Driver Outputs
- Secondary Feedback Comparator

Bias Generator Blocks:

- +5V Linear Regulator
- Automatic Bootstrap Switchover Circuit
- +2.50V Reference

These internal IC blocks aren't powered directly from the battery. Instead, a +5V linear regulator steps down the battery voltage to supply both the IC internal rail (VL pin) as well as the gate drivers. The synchronous-switch gate driver is directly powered from +5V VL, while the high-side-switch gate driver is indirectly powered from VL via an external diode-capacitor boost circuit. An automatic bootstrap circuit turns off the +5V linear regulator and powers the IC from its output voltage if the output is above 4.5V.

PWM Controller Block

The heart of the current-mode PWM controller is a multi-input open-loop comparator that sums three signals: output voltage error signal with respect to the reference voltage, current-sense signal, and slope compensation ramp (Figure 3). The PWM controller is a direct summing type, lacking a traditional error amplifier and the phase shift associated with it. This direct-summing configuration approaches the ideal of cycle-by-cycle control over the output voltage.

Under heavy loads, the controller operates in full PWM mode. Each pulse from the oscillator sets the main PWM latch that turns on the high-side switch for a period determined by the duty factor (approximately V_{OUT}/V_{IN}). As the high-side switch turns off, the synchronous rectifier latch is set. 60ns later the low-side switch turns on, and stays on until the beginning of the next clock cycle (in continuous mode) or until the inductor current crosses zero (in discontinuous mode). Under fault conditions where the inductor current exceeds the 100mV current-limit threshold, the high-side latch resets and the high-side switch turns off.

If the load is light in Idle Mode ($\overline{SKIP}$ = low), the inductor current does not exceed the 25mV threshold set by the Idle Mode comparator. When this occurs, the controller skips most of the oscillator pulses in order to reduce the switching frequency and cut back gate-charge losses. The oscillator is effectively gated off at light loads because the Idle Mode comparator immediately resets the high-side latch at the beginning of each cycle, unless the feedback signal falls below the reference voltage level.

When in PWM mode, the controller operates as a fixed-frequency current-mode controller where the duty ratio is set by the input/output voltage ratio. The current-mode feedback system regulates the peak inductor current as a function of the output voltage error signal. Since the average inductor current is nearly the same as the peak current, the circuit acts as a switch-mode transconductance amplifier and pushes the second output LC filter pole, normally found in a duty-factor-controlled (voltage-mode) PWM, to a higher frequency. To preserve inner-loop stability and eliminate regenerative inductor current "staircasing," a slope-compensation ramp is summed into the main PWM comparator to reduce the apparent duty factor to less than 50%.

The relative gains of the voltage- and current-sense inputs are weighted by the values of current sources that bias three differential input stages in the main PWM comparator (Figure 4). The relative gain of the voltage comparator to the current comparator is internally fixed at K = 2:1. The resulting loop gain (which is relatively low) determines the 2% typical load regulation error. The low loop-gain value helps reduce output filter capacitor size and cost by shifting the unity-gain crossover to a lower frequency.

The output filter capacitor C2 sets a dominant pole in the feedback loop. This pole must roll off the loop gain to unity before the zero introduced by the output capacitor's parasitic resistance (ESR) is encountered (see *Design Procedure* section). A 12kHz pole-zero cancellation filter provides additional rolloff above the unity-gain crossover. This internal 12kHz lowpass compensation filter cancels the zero due to the filter capacitor's ESR. The 12kHz filter is included in the loop in both fixed- and adjustable-output modes.

Synchronous-Rectifier Driver (DL Pin)

Synchronous rectification reduces conduction losses in the rectifier by shunting the normal Schottky diode with a low-resistance MOSFET switch. The synchronous rectifier also ensures proper start-up of the boost-gate driver circuit. If you must omit the synchronous power MOSFET for cost or other reasons, replace it with a small-signal MOSFET such as a 2N7002.

If the circuit is operating in continuous-conduction mode, the DL drive waveform is simply the complement of the DH high-side drive waveform (with controlled dead time to prevent cross-conduction or "shoot-through").

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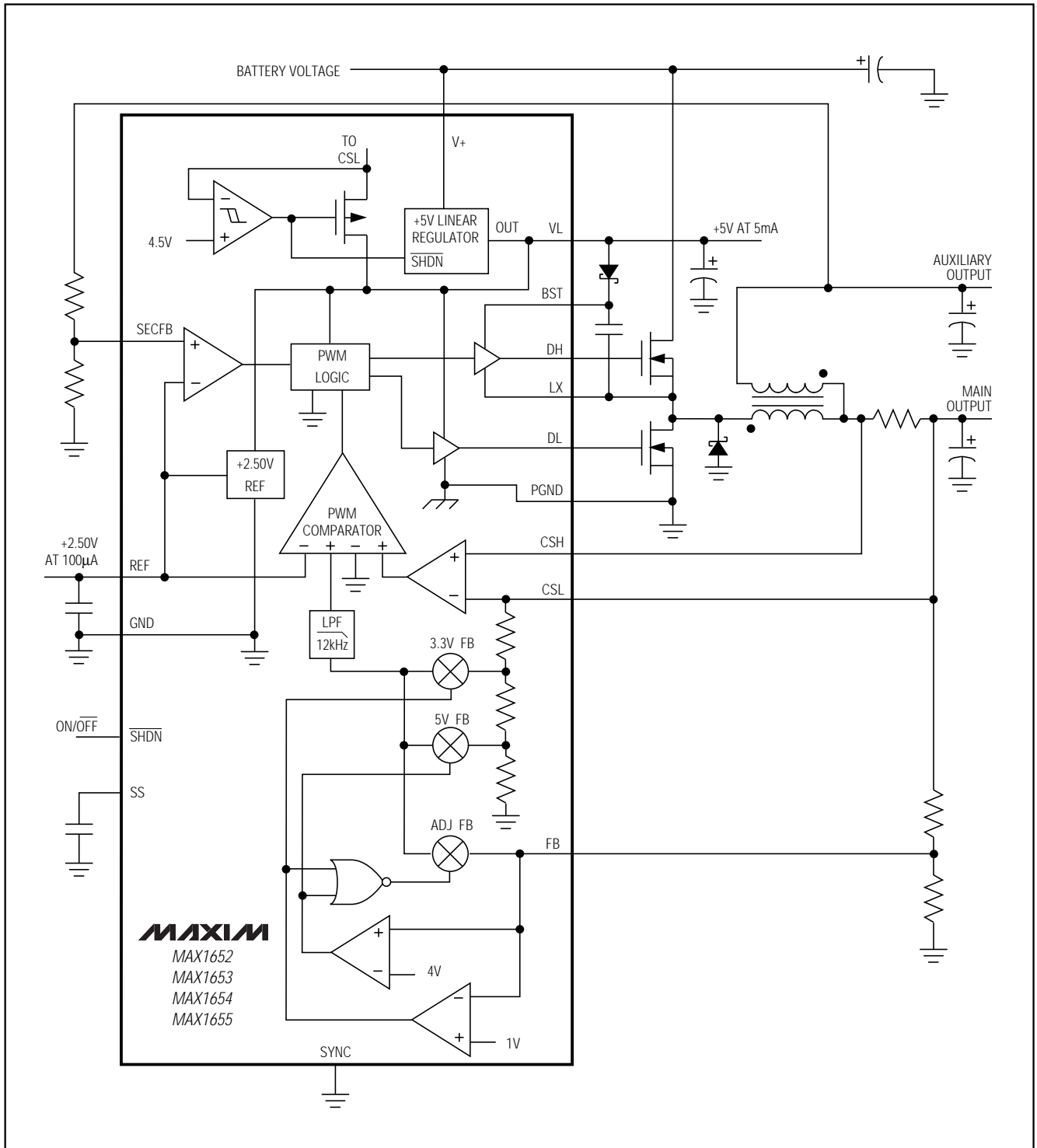
MAX1652–MAX1655

Figure 2. MAX1652–MAX1655 Functional Diagram

MAX1652–MAX1655
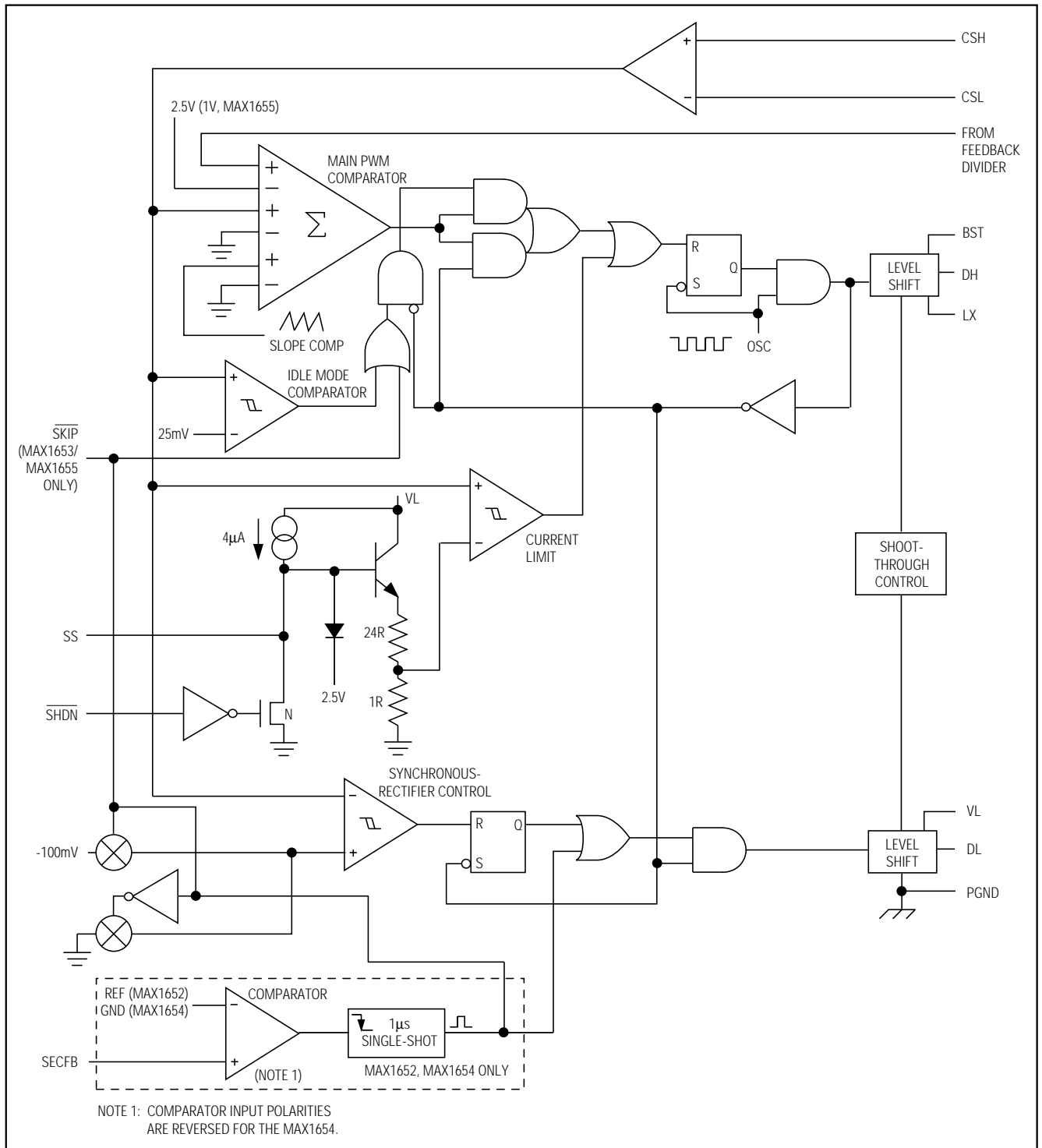
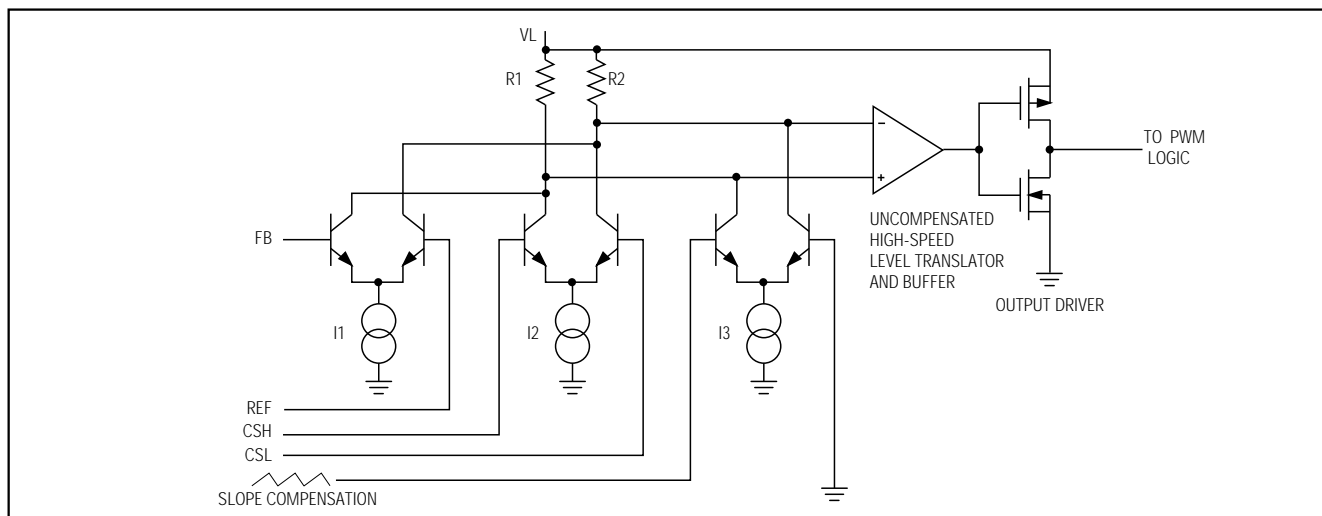Figure 3. PWM Controller Detailed Block Diagram

Figure 4. Main PWM Comparator Block Diagram

In discontinuous (light-load) mode, the synchronous switch is turned off as the inductor current falls through zero. The synchronous rectifier works under all operating conditions, including idle mode. The synchronous-switch timing is further controlled by the secondary feedback (SECFB) signal in order to improve multiple-output cross-regulation (see *Secondary Feedback-Regulation Loop* section).

Internal VL and REF Supplies

An internal regulator produces the 5V supply (VL) that powers the PWM controller, logic, reference, and other blocks. This +5V low-dropout linear regulator can supply up to 5mA for external loads, with a reserve of 20mA for gate-drive power. Bypass VL to GND with 4.7µF. **Important**: VL must not be allowed to exceed 5.5V. Measure VL with the main output fully loaded. If VL is being pumped up above 5.5V, the probable cause is either excessive boost-diode capacitance or excessive ripple at V+. Use only small-signal diodes for D2 (10mA to 100mA Schottky or 1N4148 are preferred) and bypass V+ to PGND with 0.1µF directly at the package pins.

The 2.5V reference (REF) is accurate to ±1.6% over temperature, making REF useful as a precision system reference. Bypass REF to GND with 0.33µF minimum. REF can supply up to 1mA for external loads. However, if tight-accuracy specs for either V_{OUT} or REF are essential, avoid loading REF with more than 100µA. Loading REF reduces the main output voltage slightly, according to the reference-voltage load regulation error. In MAX1654 applications, ensure that the SECFB divider doesn't load REF heavily.

When the main output voltage is above 4.5V, an internal P-channel MOSFET switch connects CSL to VL while simultaneously shutting down the VL linear regulator. This action bootstraps the IC, powering the internal circuitry from the output voltage, rather than through a linear regulator from the battery. Bootstrapping reduces power dissipation caused by gate-charge and quiescent losses by providing that power from a 90%-efficient switch-mode source, rather than from a less efficient linear regulator.

It's often possible to achieve a bootstrap-like effect, even for circuits that are set to $V_{OUT} < 4.5V$, by powering VL from an external-system +5V supply. To achieve this pseudo-bootstrap, add a Schottky diode between the external +5V source and VL, with the cathode to the VL side. This circuit provides a 1% to 2% efficiency boost and also extends the minimum battery input to less than 4V. The external source must be in the range of 4.8V to 5.5V.

Boost High-Side
Gate-Driver Supply (BST Pin)

Gate-drive voltage for the high-side N-channel switch is generated by a flying-capacitor boost circuit as shown in Figure 5. The capacitor is alternately charged from the VL supply and placed in parallel with the high-side MOSFET's gate-source terminals.

On start-up, the synchronous rectifier (low-side MOS-FET) forces LX to 0V and charges the BST capacitor to 5V. On the second half-cycle, the PWM turns on the high-side MOSFET by closing an internal switch between BST and DH. This provides the necessary enhancement voltage to turn on the high-side switch,

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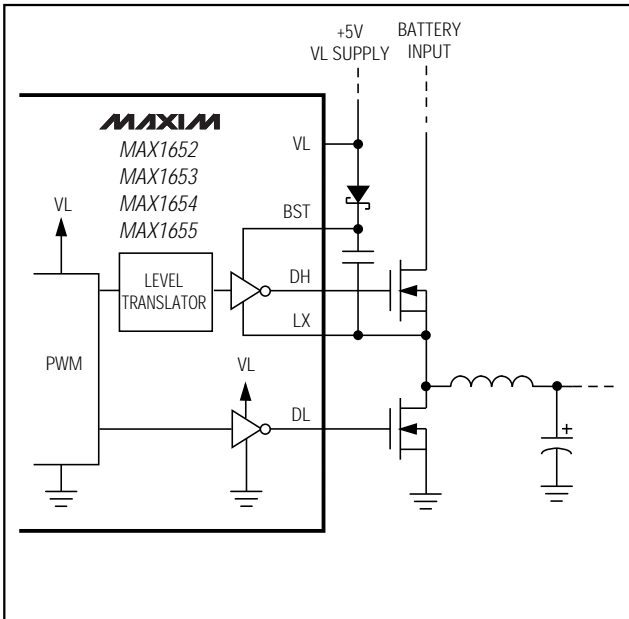
Figure 5. Boost Supply for Gate Drivers

an action that "boosts" the 5V gate-drive signal above the battery voltage.

Ringing seen at the high-side MOSFET gate (DH) in discontinuous-conduction mode (light loads) is a natural operating condition caused by the residual energy in the tank circuit formed by the inductor and stray capacitance at the switching node LX. The gate-driver negative rail is referred to LX, so any ringing there is directly coupled to the gate-drive output.

Current-Limiting and Current-Sense Inputs (CSH and CSL)

The current-limit circuit resets the main PWM latch and turns off the high-side MOSFET switch whenever the voltage difference between CSH and CSL exceeds 100mV. This limiting is effective for both current flow directions, putting the threshold limit at ±100mV. The tolerance on the positive current limit is ±20%, so the external low-value sense resistor must be sized for 80mV/R1 to guarantee enough load capability, while components must be designed to withstand continuous current stresses of 120mV/R1.

For breadboarding purposes or very-high-current applications, it may be useful to wire the current-sense inputs with a twisted pair rather than PC traces.

Oscillator Frequency and Synchronization (SYNC Pin)

The SYNC input controls the oscillator frequency. Connecting SYNC to GND or to VL selects 150kHz operation; connecting SYNC to REF selects 300kHz. SYNC can also be used to synchronize with an external 5V CMOS clock generator. SYNC has a guaranteed 190kHz to 340kHz capture range.

300kHz operation optimizes the application circuit for component size and cost. 150kHz operation provides increased efficiency and improved low-duty factor operation (see *Dropout Operation* section).

Dropout Operation

Dropout (low input-output differential operation) is enhanced by stretching the clock pulse width to increase the maximum duty factor. The algorithm follows: if the output voltage (V_{OUT}) drops out of regulation without the current limit having been reached, the controller skips an off-time period (extending the on-time). At the end of the cycle, if the output is still out of regulation, another off-time period is skipped. This action can continue until three off-time periods are skipped, effectively dividing the clock frequency by as much as four.

The typical PWM minimum off-time is 300ns, regardless of the operating frequency. Lowering the operating frequency raises the maximum duty factor above 98%.

Low-Noise Mode ($\overline{SKIP}$ Pin)

The low-noise mode ($\overline{SKIP}$ = high) is useful for minimizing RF and audio interference in noise-sensitive applications such as audio-equipped systems, cellular phones, RF communicating computers, and electromagnetic pen-entry systems. See the summary of operating modes in Table 3. $\overline{SKIP}$ can be driven from an external logic signal.

The MAX1653 and MAX1655 can reduce interference due to switching noise by ensuring a constant switching frequency regardless of load and line conditions, thus concentrating the emissions at a known frequency outside the system audio or IF bands. Choose an oscillator frequency where harmonics of the switching frequency don't overlap a sensitive frequency band. If necessary, synchronize the oscillator to a tight-tolerance external clock generator.

The low-noise mode ($\overline{SKIP}$ = high) forces two changes upon the PWM controller. First, it ensures fixed-frequency operation by disabling the minimum-current comparator and ensuring that the PWM latch is set at the beginning of each cycle, even if the output is in regulation. Second, it ensures continuous inductor current

Table 3. Operating-Mode Truth Table

$\overline{\text{SHDN}}$	$\overline{\text{SKIP}}$	LOAD CURRENT	MODE NAME	DESCRIPTION
Low	X	X	Shutdown	All circuit blocks turned off; supply current = 3µA typ
High	Low	Low, <10%	Idle	Pulse-skipping; supply current = 300µA typ at V_{IN} = 10V; discontinuous inductor current
High	Low	Medium, <30%	Idle	Pulse-skipping; continuous inductor current
High	Low	High, >30%	PWM	Constant-frequency PWM; continuous inductor current
High	High	X	Low Noise* (PWM)	Constant-frequency PWM regardless of load; continuous inductor current even at no load

* MAX1652/MAX1654 have no $\overline{\text{SKIP}}$ pin and therefore can't go into low-noise mode.
X = Don't care

flow, and thereby suppresses discontinuous-mode inductor ringing by changing the reverse current-limit detection threshold from 0 to -100mV, allowing the inductor current to reverse at very light loads.

In most applications, $\overline{\text{SKIP}}$ should be tied to GND in order to minimize quiescent supply current. Supply current with $\overline{\text{SKIP}}$ high is typically 10mA to 20mA, depending on external MOSFET gate capacitance and switching losses.

Forced continuous conduction via $\overline{\text{SKIP}}$ can improve cross regulation of transformer-coupled multiple-output supplies. This second function of the $\overline{\text{SKIP}}$ pin produces a result that is similar to the method of adding secondary regulation via the SECFB feedback pin, but with much higher quiescent supply current. Still, improving cross regulation by enabling $\overline{\text{SKIP}}$ instead of building in SECFB feedback can be useful in noise-sensitive applications, since SECFB and $\overline{\text{SKIP}}$ are mutually exclusive pins/functions in the MAX1652 family.

Adjustable-Output Feedback (Dual-Mode FB Pin)
The MAX1652–MAX1655 family has both fixed and adjustable output voltage modes. For fixed mode, connect FB to GND for a 3.3V output and to V_L for a 5V out-

put. Adjusting the main output voltage with external resistors is easy for any of the devices in this family, via the circuit of Figure 6. The feedback voltage is nominally 2.5 for all family members except the MAX1655, which has a nominal FB voltage of 1V. The output voltage (given by the formula in Figure 6) should be set approximately 2% high in order to make up for the MAX1652's load-regulation error. For example, if designing for a 3.0V output, use a resistor ratio that results in a nominal output voltage of 3.06V. This slight offsetting gives the best possible accuracy. Recommended normal values for R5 range from 5kΩ to 100kΩ.

Remote sensing of the output voltage, while not possible in fixed-output mode due to the combined nature of the voltage- and current-sense input (CSL), is easy to achieve in adjustable mode by using the top of the external resistor divider as the remote sense point.

Duty-Factor Limitations for Low V_{OUT}/V_{IN} Ratios
The MAX1652/MAX1653/MAX1654's output voltage is adjustable down to 2.5V and the MAX1655's output is adjustable as low as 1V. However, the minimum duty factor may limit the choice of operating frequency, high input voltage, and low output voltage.

$$V_{OUT} = V_{REF} \left(1 + \frac{R4}{R5} \right)$$

WHERE V_{REF} (NOMINAL) = 2.5V (MAX1652–MAX1654)
= 1.0V (MAX1655)
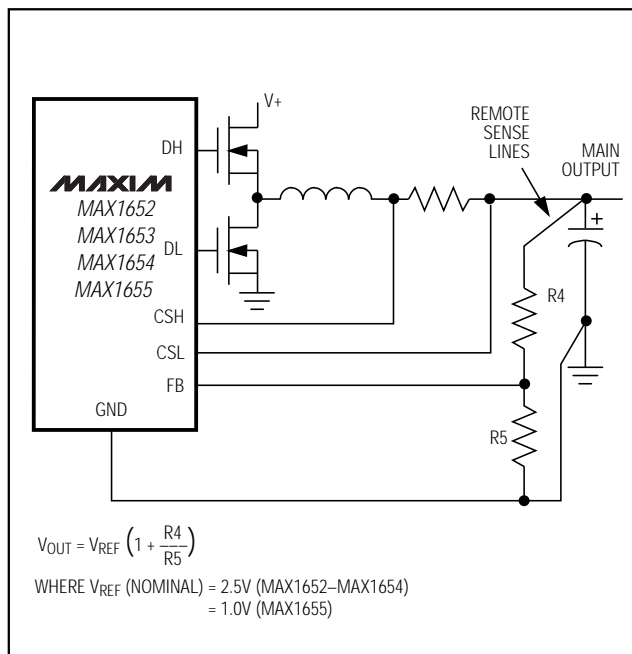
Figure 6. Adjusting the Main Output Voltage

High-Efficiency, PWM, Step-Down
DC-DC Controllers in 16-Pin QSOP

With high input voltages, the required duty factor is approximately $(V_{OUT} + V_{Q2})/V_{IN}$, where V_{Q2} is the voltage drop across the synchronous rectifier. The MAX1652's minimum duty factor is determined by delays through the feedback network, error comparator, internal logic gate drivers, and the external MOSFETs, which typically total 400ns. This delay is about 12% of the switching period at 300kHz and 6% at 150kHz, limiting the typical minimum duty factor to these values.

Even if the circuit can not attain the required duty factor dictated by the input and output voltages, the output voltage will remain in regulation. However, there may be intermittent or continuous half-frequency operation. This can cause a factor-of-two increase in output voltage ripple and current ripple, which will increase noise and reduce efficiency. Choose 150kHz operation for high-input-voltage/low-output-voltage circuits.

Secondary Feedback-Regulation Loop
(SECFB Pin)

A flyback winding control loop regulates a secondary winding output (MAX1652/MAX1654 only), improving cross-regulation when the primary is lightly loaded or when there is a low input-output differential voltage. If SECFB crosses its regulation threshold, a 1µs one-shot is triggered that extends the low-side switch's on-time beyond the point where the inductor current crosses zero (in discontinuous mode). This causes the inductor (primary) current to reverse, which in turn pulls current out of the output filter capacitor and causes the flyback transformer to operate in the forward mode. The low impedance presented by the transformer secondary in the forward mode dumps current into the secondary output, charging up the secondary capacitor and bringing SECFB back into regulation. The SECFB feedback loop does not improve secondary output accuracy in normal flyback mode, where the main (primary) output is heavily loaded. In this mode, secondary output accuracy is determined (as usual) by the secondary rectifier drop, turns ratio, and accuracy of the main output voltage. Hence, a linear post-regulator may still be needed in order to meet tight output accuracy specifications.

The secondary output voltage-regulation point is determined by an external resistor-divider at SECFB. For negative output voltages, the SECFB comparator is referenced to GND (MAX1654); for positive output voltages, SECFB regulates at the 2.50V reference (MAX1652). As a result, output resistor-divider connections and design equations for the two device types differ slightly (Figure 7). Ordinarily, the secondary regulation point is set 5% to 10% below the voltage normally produced by the flyback effect. For example, if the

$$+V_{TRIP} = V_{REF}\left(1 + \frac{R2}{R3}\right)$$ WHERE V_{REF} (NOMINAL) = 2.5V

$$-V_{TRIP} = -V_{REF}\left(\frac{R2}{R3}\right)$$ R3 = 100kΩ (RECOMMENDED)
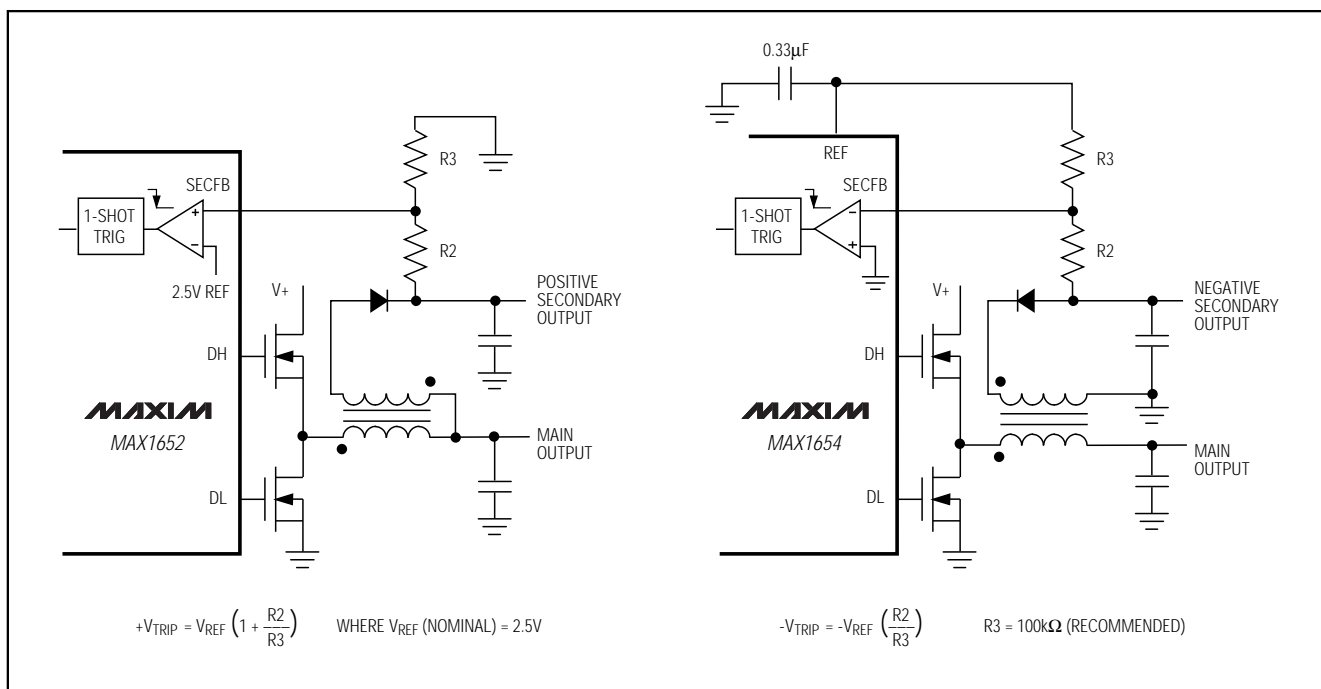
Figure 7. Secondary-Output Feedback Dividers

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output voltage as determined by the turns ratio is +15V, the feedback resistor ratio should be set to produce about +13.5V; otherwise, the SECFB one-shot might be triggered unintentionally, causing an unnecessary increase in supply current and output noise. In negative-output (MAX1654) applications, the resistor-divider acts as a load on the internal reference, which in turn can cause errors at the main output. Avoid overloading REF (see the Reference Load-Regulation Error vs. Load Current graph in the *Typical Operating Characteristics*). 100kΩ is a good value for R3 in MAX1654 circuits.

Output current on secondary winding applications is limited at low input voltages. See the MAX1652 Maximum Secondary Output Current vs. Supply Voltage graph in the Typical Operating Characteristics for data from the application circuit of Figure 8.

Soft-Start Circuit (SS)

Soft-start allows a gradual increase of the internal current-limit level at start-up for the purpose of reducing input surge currents, and perhaps for power-supply sequencing. In shutdown mode, the soft-start circuit holds the SS capacitor discharged to ground. When $\overline{SHDN}$ goes high, a 4µA current source charges the SS capacitor up to 3.2V. The resulting linear ramp waveform causes the internal current-limit level to increase proportionally from 0 to 100mV. The main output capacitor thus charges up relatively slowly, depending on the SS capacitor value. The exact time of the output rise depends on output capacitance and load current and is typically 1ms per nanofarad of soft-start capacitance. With no SS capacitor connected, maximum current limit is reached within 10µs.

Shutdown

Shutdown mode ($\overline{SHDN}$ = 0V) reduces the V+ supply current to typically 3µA. In this mode, the reference and VL are inactive. $\overline{SHDN}$ is a logic-level input, but it can be safely driven to the full V+ range. Connect $\overline{SHDN}$ to V+ for automatic start-up. Do not allow slow transitions (slower than 0.02V/µs) on $\overline{SHDN}$.
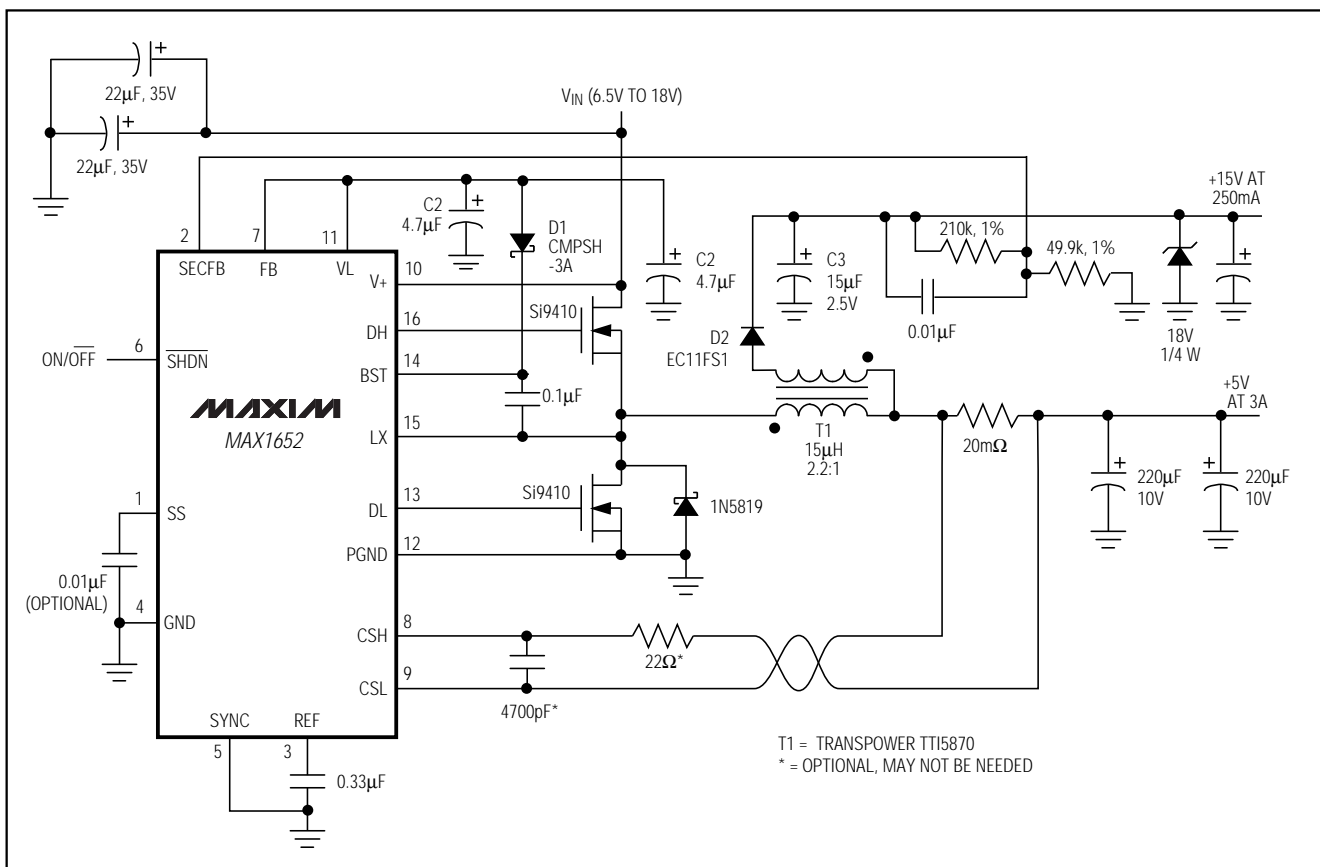
Figure 8. 5V/15V Dual-Output Application Circuit (MAX1652)

High-Efficiency, PWM, Step-Down
DC-DC Controllers in 16-Pin QSOP

_____Design Procedure

The predesigned standard application circuits (Figure 1 and Table 1) contain ready-to-use solutions for common applications. Use the following design procedure to optimize the basic schematic for different voltage or current requirements. Before beginning a design, firmly establish the following:

$V_{IN(MAX)}$, the maximum input (battery) voltage. This value should include the worst-case conditions, such as no-load operation when a battery charger or AC adapter is connected but no battery is installed. $V_{IN(MAX)}$ must not exceed 30V. This 30V upper limit is determined by the breakdown voltage of the BST floating gate driver to GND (36V absolute maximum).

$V_{IN(MIN)}$, the minimum input (battery) voltage. This should be at full-load under the lowest battery conditions. If $V_{IN(MIN)}$ is less than 4.5V, a special circuit must be used to externally hold up VL above 4.8V. If the minimum input-output difference is less than 1V, the filter capacitance required to maintain good AC load regulation increases.

Inductor Value

The exact inductor value isn't critical and can be adjusted freely in order to make trade-offs among size, cost, and efficiency. Although lower inductor values will minimize size and cost, they will also reduce efficiency due to higher peak currents. To permit use of the physically smallest inductor, lower the inductance until the circuit is operating at the border between continuous and discontinuous modes. Reducing the inductor value even further, below this crossover point, results in discontinuous-conduction operation even at full load. This helps reduce output filter capacitance requirements but causes the core energy storage requirements to increase again. On the other hand, higher inductor values will increase efficiency, but at some point resistive losses due to extra turns of wire will exceed the benefit gained from lower AC current levels. Also, high inductor values affect load-transient response; see the V_{SAG} equation in the *Low-Voltage Operation* section.

The following equations are given for continuous-conduction operation since the MAX1652 family is mainly intended for high-efficiency, battery-powered applications. See Appendix A in Maxim's *Battery Management and DC-DC Converter Circuit Collection* for crossover point and discontinuous-mode equations. Discontinuous conduction doesn't affect normal Idle Mode operation.

Three key inductor parameters must be specified: inductance value (L), peak current (I_{PEAK}), and DC resistance (R_{DC}). The following equation includes a constant LIR, which is the ratio of inductor peak-to-peak AC current to DC load current. A higher value of LIR allows smaller inductance, but results in higher losses and ripple. A good compromise between size and losses is found at a 30% ripple current to load current ratio (LIR = 0.3), which corresponds to a peak inductor current 1.15 times higher than the DC load current.

$$L = \frac{V_{OUT} (V_{IN(MAX)} - V_{OUT})}{V_{IN(MAX)} \times f \times I_{OUT} \times LIR}$$

where: f = switching frequency, normally 150kHz or 300kHz

I_{OUT} = maximum DC load current

LIR = ratio of AC to DC inductor current, typically 0.3

The peak inductor current at full load is 1.15 x I_{OUT} if the above equation is used; otherwise, the peak current can be calculated by:

$$I_{PEAK} = I_{LOAD} + \frac{V_{OUT} (V_{IN(MAX)} - V_{OUT})}{2 \times f \times L \times V_{IN(MAX)}}$$

The inductor's DC resistance is a key parameter for efficiency performance and must be ruthlessly minimized, preferably to less than 25mΩ at I_{OUT} = 3A. If a standard off-the-shelf inductor is not available, choose a core with an LI^2 rating greater than $L \times I_{PEAK}^2$ and wind it with the largest diameter wire that fits the winding area. For 300kHz applications, ferrite core material is strongly preferred; for 150kHz applications, Kool-mu (aluminum alloy) and even powdered iron can be acceptable. If light-load efficiency is unimportant (in desktop 5V-to-3V applications, for example) then low-permeability iron-powder cores may be acceptable, even at 300kHz. For high-current applications, shielded core geometries (such as toroidal or pot core) help keep noise, EMI, and switching-waveform jitter low.

Current-Sense Resistor Value

The current-sense resistor value is calculated according to the worst-case, low-current-limit threshold voltage (from the *Electrical Characteristics* table) and the peak inductor current. The continuous-mode peak inductor-current calculations that follow are also useful for sizing the switches and specifying the inductor-current saturation ratings. In order to simplify the calculation, I_{LOAD} may be used in place of I_{PEAK} if the inductor value has been set for LIR = 0.3 or less (high inductor values) and 300kHz operation is selected. Low-inductance resistors, such as surface-mount metal-film resistors, are preferred.

$$R_{SENSE} = \frac{80mV}{I_{PEAK}}$$

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Input Capacitor Value

Place a small ceramic capacitor (0.1µF) between V+ and GND, close to the device. Also, connect a low-ESR bulk capacitor directly to the drain of the high-side MOSFET. Select the bulk input filter capacitor according to input ripple-current requirements and voltage rating, rather than capacitor value. Electrolytic capacitors that have low enough effective series resistance (ESR) to meet the ripple-current requirement invariably have more than adequate capacitance values. Ceramic capacitors or low-ESR aluminum-electrolytic capacitors such as Sanyo OS-CON or Nichicon PL are preferred. Tantalum types are also acceptable but may be less tolerant of high input surge currents. RMS input ripple current is determined by the input voltage and load current, with the worst possible case occurring at $V_{IN} = 2 \times V_{OUT}$:

$$I_{RMS} = I_{LOAD} \times \frac{\sqrt{V_{OUT}\,(V_{IN} - V_{OUT})}}{V_{IN}}$$

$$I_{RMS} = I_{LOAD} / 2 \text{ when } V_{IN} \text{ is } 2 \times V_{OUT}$$

Output Filter Capacitor Value

The output filter capacitor values are determined by the ESR, capacitance, and voltage rating requirements. Electrolytic and tantalum capacitors are generally chosen by voltage rating and ESR specifications, as they will generally have more output capacitance than is required for AC stability. Use only specialized low-ESR capacitors intended for switching-regulator applications, such as AVX TPS, Sprague 595D, Sanyo OS-CON, or Nichicon PL series. To ensure stability, the capacitor must meet *both* minimum capacitance and maximum ESR values as given in the following equations:

$$C_{OUT} > \frac{V_{REF}\,(1 + V_{OUT} / V_{IN(MIN)})}{V_{OUT} \times R_{SENSE} \times f}$$

$$R_{ESR} < \frac{R_{SENSE} \times V_{OUT}}{V_{REF}}$$

(can be multiplied by 1.5, see note below)

These equations are "worst-case" with 45 degrees of phase margin to ensure jitter-free fixed-frequency operation and provide a nicely damped output response for zero to full-load step changes. Some cost-conscious designers may wish to bend these rules by using less expensive (lower quality) capacitors, particularly if the load lacks large step changes. This practice is tolerable if some bench testing over temperature is done to verify acceptable noise and transient response.

There is no well-defined boundary between stable and unstable operation. As phase margin is reduced, the first symptom is a bit of timing jitter, which shows up as blurred edges in the switching waveforms where the scope won't quite sync up. Technically speaking, this (usually) harmless jitter is unstable operation, since the switching frequency is now nonconstant. As the capacitor quality is reduced, the jitter becomes more pronounced and the load-transient output voltage waveform starts looking ragged at the edges. Eventually, the load-transient waveform has enough ringing on it that the peak noise levels exceed the allowable output voltage tolerance. Note that even with zero phase margin and gross instability present, the output voltage noise never gets much worse than $I_{PEAK} \times R_{ESR}$ (under constant loads, at least).

Note: Designers of RF communicators or other noise-sensitive analog equipment should be conservative and stick to the ESR guidelines. Designers of notebook computers and similar commercial-temperature-range digital systems can multiply the R_{ESR} value by a factor of 1.5 without hurting stability or transient response.

The output voltage ripple is usually dominated by the ESR of the filter capacitor and can be approximated as $I_{RIPPLE} \times R_{ESR}$. There is also a capacitive term, so the full equation for ripple in the continuous mode is $V_{NOISE(p-p)} = I_{RIPPLE} \times [R_{ESR} + 1 / (8 \times f \times C_{OUT})]$. In Idle Mode, the inductor current becomes discontinuous with high peaks and widely spaced pulses, so the noise can actually be higher at light load compared to full load. In Idle Mode, the output ripple can be calculated as:

$$V_{NOISE(p-p)} = \frac{0.025 \times R_{ESR}}{R_{SENSE}} +$$

$$\frac{(0.025)^2 \times L \times [1 / V_{OUT} + 1 / (V_{IN} - V_{OUT})]}{(R_{SENSE})^2 \times C_{OUT}}$$

Transformer Design (MAX1652/MAX1654 Only)

Buck-plus-flyback applications, sometimes called "coupled-inductor" topologies, use a transformer to generate multiple output voltages. The basic electrical design is a simple task of calculating turns ratios and adding the power delivered to the secondary in order to calculate the current-sense resistor and primary inductance. However, extremes of low input-output differentials, widely different output loading levels, and high turns ratios can complicate the design due to parasitic transformer parameters such as interwinding capacitance, secondary resistance, and leakage inductance. For examples of what is possible with real-world transformers, see the graphs of Maximum Secondary Current vs. Input Voltage in the *Typical Operating Characteristics*.

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Power from the main and secondary outputs is lumped together to obtain an equivalent current referred to the main output voltage (see *Inductor Value* section for definitions of parameters). Set the value of the current-sense resistor at 80mV / I_{TOTAL}.

P_{TOTAL} = the sum of the output power from all outputs

I_{TOTAL} = P_{TOTAL} / V_{OUT} = the equivalent output current referred to V_{OUT}

$$L(primary) = \frac{V_{OUT} (V_{IN(MAX)} - V_{OUT})}{V_{IN(MAX)} \times f \times I_{TOTAL} \times LIR}$$

$$\text{Turns Ratio N} = \frac{V_{SEC} + V_{FWD}}{V_{OUT(MIN)} + V_{RECT} + V_{SENSE}}$$

where: V_{SEC} is the minimum required rectified secondary-output voltage

V_{FWD} is the forward drop across the secondary rectifier

$V_{OUT(MIN)}$ is the *minimum* value of the main output voltage (from the *Electrical Characteristics*)

V_{RECT} is the on-state voltage drop across the synchronous-rectifier MOSFET

V_{SENSE} is the voltage drop across the sense resistor

In positive-output (MAX1652) applications, the transformer secondary return is often referred to the main output voltage rather than to ground in order to reduce the needed turns ratio. In this case, the main output voltage must first be subtracted from the secondary voltage to obtain V_{SEC}.

_____Selecting Other Components

MOSFET Switches

The two high-current N-channel MOSFETs must be logic-level types with guaranteed on-resistance specifications at V_{GS} = 4.5V. Lower gate threshold specs are better (i.e., 2V max rather than 3V max). Drain-source breakdown voltage ratings must at least equal the maximum input voltage, preferably with a 20% derating factor. The best MOSFETs will have the lowest on-resistance per nanocoulomb of gate charge. Multiplying $R_{DS(ON)}$ x Q_G provides a meaningful figure by which to compare various MOSFETs. Newer MOSFET process technologies with dense cell structures generally give the best performance. The internal gate drivers can tolerate more than 100nC total gate charge, but 70nC is a more practical upper limit to maintain best switching times.

In high-current applications, MOSFET package power dissipation often becomes a dominant design factor. I^2R losses are distributed between Q1 and Q2 according to duty factor (see the equations below). Switching losses affect the upper MOSFET only, since the Schottky rectifier clamps the switching node before the synchronous rectifier turns on. Gate-charge losses are dissipated by the driver and don't heat the MOSFET. Ensure that both MOSFETs are within their maximum junction temperature at high ambient temperature by calculating the temperature rise according to package thermal-resistance specifications. The worst-case dissipation for the high-side MOSFET occurs at the minimum battery voltage, and the worst-case for the low-side MOSFET occurs at the maximum battery voltage.

$$PD \text{ (upper FET)} = I_{LOAD}^2 \times R_{DS(ON)} \times DUTY$$

$$+ V_{IN} \times I_{LOAD} \times f \times \left(\frac{V_{IN} \times C_{RSS}}{I_{GATE}} + 20ns \right)$$

$$PD \text{ (lower FET)} = I_{LOAD}^2 \times R_{DS(ON)} \times (1 - DUTY)$$

$$DUTY = (V_{OUT} + V_{Q2}) / (V_{IN} - V_{Q1} + V_{Q2})$$

where the on-state voltage drop $V_{Q\_}$ = I_{LOAD} x $R_{DS(ON)}$

C_{RSS} = MOSFET reverse transfer capacitance

I_{GATE} = DH driver peak output current capability (1A typically)

20ns = DH driver inherent rise/fall time

Under output short circuit, the synchronous-rectifier MOSFET suffers extra stress and may need to be over-sized if a continuous DC short circuit must be tolerated. During short circuit, Q2's duty factor can increase to greater than 0.9 according to:

Q2 DUTY (short circuit) = 1 - [V_{Q2} / ($V_{IN(MAX)} - V_{Q1} + V_{Q2}$)]

where the on-state voltage drop V_Q = (120mV / R_{SENSE}) x $R_{DS(ON)}$.

Rectifier Diode D1

Rectifier D1 is a clamp that catches the negative inductor swing during the 60ns dead time between turning off the high-side MOSFET and turning on the low-side. D1 must be a Schottky type in order to prevent the lossy parasitic MOSFET body diode from conducting. It is acceptable to omit D1 and let the body diode clamp the negative inductor swing, but efficiency will drop one or two percent as a result. Use an MBR0530 (500mA rated) type for loads up to 1.5A, a 1N5819 type for loads up to 3A, or a 1N5822 type for loads up to 10A. D1's rated reverse breakdown voltage must be at least equal to the maximum input voltage, preferably with a 20% derating factor.

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High-Efficiency, PWM, Step-Down
DC-DC Controllers in 16-Pin QSOP

Boost-Supply Diode D2

A 10mA to 100mA Schottky diode or signal diode such as a 1N4148 works well for D2 in most applications. If the input voltage can go below 6V, use a Schottky diode for slightly improved efficiency and dropout characteristics. Don't use large power diodes such as 1N5817 or 1N4001, since high junction capacitance can cause VL to be pumped up to excessive voltages.

Rectifier Diode D3
(Transformer Secondary Diode)

The secondary diode in coupled-inductor applications must withstand high flyback voltages greater than 60V, which usually rules out most Schottky rectifiers. Common silicon rectifiers such as the 1N4001 are also prohibited, as they are far too slow. This often makes fast silicon rectifiers such as the MURS120 the only choice. The flyback voltage across the rectifier is related to the V_{IN}-V_{OUT} difference according to the transformer turns ratio:

$$V_{FLYBACK} = V_{SEC} + (V_{IN} - V_{OUT}) \times N$$

where: N is the transformer turns ratio SEC/PRI
V_{SEC} is the maximum secondary DC output voltage
V_{OUT} is the primary (main) output voltage

Subtract the main output voltage (V_{OUT}) from $V_{FLYBACK}$ in this equation if the secondary winding is returned to V_{OUT} and not to ground. The diode reverse breakdown rating must also accommodate any ringing due to leakage inductance. D3's current rating should be at least twice the DC load current on the secondary output.

Low-Voltage Operation

Low input voltages and low input-output differential voltages each require some extra care in the design. Low absolute input voltages can cause the VL linear regulator to enter dropout, and eventually shut itself off. Low input voltages relative to the output (low V_{IN}-V_{OUT} differential) can cause bad load regulation in multi-output flyback applications. See *Transformer Design* section. Finally, low V_{IN}-V_{OUT} differentials can also cause the output voltage to sag when the load current changes abruptly. The amplitude of the sag is a function of inductor value and maximum duty factor (D_{MAX} an *Electrical Characteristics* parameter, 98% guaranteed over temperature at f = 150kHz) as follows:

$$V_{SAG} = \frac{(I_{STEP})^2 \times L}{2 \times C_{OUT} \times (V_{IN(MIN)} \times D_{MAX} - V_{OUT})}$$

The cure for low-voltage sag is to increase the value of the output capacitor. For example, at V_{IN} = 5.5V, V_{OUT} = 5V, L = 10µH, f = 150kHz, a total capacitance of 660µF will prevent excessive sag. Note that only the capacitance requirement is increased and the ESR requirements don't change. Therefore, the added capacitance can be supplied by a low-cost bulk capacitor in parallel with the normal low-ESR capacitor. Table 4 summarizes low-voltage operational issues.

Table 4. Low-Voltage Troubleshooting

SYMPTOM	CONDITION	ROOT CAUSE	SOLUTION
Sag or droop in V_{OUT} under step load change	Low V_{IN}-V_{OUT} differential, <1V	Limited inductor-current slew rate per cycle.	Increase bulk output capacitance per formula above. Reduce inductor value.
Dropout voltage is too high (V_{OUT} follows V_{IN} as V_{IN} decreases)	Low V_{IN}-V_{OUT} differential, <0.5V	Maximum duty-cycle limits exceeded.	Reduce f to 150kHz. Reduce MOSFET on-resistance and coil DCR.
Unstable—jitters between two distinct duty factors	Low V_{IN}-V_{OUT} differential, <0.5V	Normal function of internal low-dropout circuitry.	Increase the minimum input voltage or ignore.
Secondary output won't support a load	Low V_{IN}-V_{OUT} differential, V_{IN} < 1.3 x V_{OUT}(main)	Not enough duty cycle left to initiate forward-mode operation. Small AC current in primary can't store energy for flyback operation.	Reduce f to 150kHz. Reduce secondary impedances—use Schottky if possible. Stack secondary winding on main output.
High supply current, poor efficiency	Low input voltage, <5V	VL linear regulator is going into dropout and isn't providing good gate-drive levels.	Use a small 20mA Schottky diode for boost diode D2. Supply VL from an external source.
Won't start under load or quits before battery is completely dead	Low input voltage, <4.5V	VL output is so low that it hits the VL UVLO threshold at 4.2V max.	Supply VL from an external source other than V_{BATT}, such as the system 5V supply.

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High-Efficiency, PWM, Step-Down DC-DC Controllers in 16-Pin QSOP

_____Applications Information

Heavy-Load Efficiency Considerations

The major efficiency loss mechanisms under loads (in the usual order of importance) are:

- $P(I^2R)$, I^2R losses
- P(gate), gate-charge losses
- P(diode), diode-conduction losses
- P(tran), transition losses
- P(cap), capacitor ESR losses
- P(IC), losses due to the operating supply current of the IC

Inductor-core losses are fairly low at heavy loads because the inductor's AC current component is small. Therefore, they aren't accounted for in this analysis. Ferrite cores are preferred, especially at 300kHz, but powdered cores such as Kool-mu can work well.

$$\text{Efficiency} = P_{OUT} / P_{IN} \times 100\%$$
$$= P_{OUT} / (P_{OUT} + P_{TOTAL}) \times 100\%$$
$$P_{TOTAL} = P(I^2R) + P(gate) + P(diode) + P(tran) + P(cap) + P(IC)$$
$$P(I^2R) = (I_{LOAD})^2 \times (R_{DC} + R_{DS(ON)} + R_{SENSE})$$

where R_{DC} is the DC resistance of the coil, $R_{DS(ON)}$ is the MOSFET on-resistance, and R_{SENSE} is the current-sense resistor value. The $R_{DS(ON)}$ term assumes identical MOSFETs for the high- and low-side switches because they time-share the inductor current. If the MOSFETs aren't identical, their losses can be estimated by averaging the losses according to duty factor.

$$P(gate) = \text{gate-driver loss} = q_G \times f \times V_L$$

where V_L is the MAX1652 internal logic supply voltage (5V), and q_G is the sum of the gate-charge values for low- and high-side switches. For matched MOSFETs, q_G is twice the data sheet value of an individual MOSFET. If V_{OUT} is set to less than 4.5V, replace V_L in this equation with V_{BATT}. In this case, efficiency can be improved by connecting V_L to an efficient 5V source, such as the system +5V supply.

$$P(diode) = \text{diode conduction losses}$$
$$= I_{LOAD} \times V_{FWD} \times t_D \times f$$

where t_D is the diode conduction time (120ns typ) and V_{FWD} is the forward voltage of the Schottky.

$$PD(tran) = \text{transition loss} =$$
$$V_{BATT} \times I_{LOAD} \times f \times \left(\frac{V_{BATT} \times C_{RSS}}{I_{GATE}} + 20ns \right)$$

where C_{RSS} is the reverse transfer capacitance of the high-side MOSFET (a data sheet parameter), I_{GATE} is the DH gate-driver peak output current (1A typ), and 20ns is the rise/fall time of the DH driver.

$$P(cap) = \text{input capacitor ESR loss} = (I_{RMS})^2 \times R_{ESR}$$

where I_{RMS} is the input ripple current as calculated in the *Input Capacitor Value* section of the *Design Procedure.*

Light-Load Efficiency Considerations

Under light loads, the PWM operates in discontinuous mode, where the inductor current discharges to zero at some point during the switching cycle. This causes the AC component of the inductor current to be high compared to the load current, which increases core losses and I^2R losses in the output filter capacitors. Obtain best light-load efficiency by using MOSFETs with moderate gate-charge levels and by using ferrite, MPP, or other low-loss core material. Avoid powdered iron cores; even Kool-mu (aluminum alloy) is not as good as ferrite.

__PC Board Layout Considerations

Good PC board layout is *required* to achieve specified noise, efficiency, and stability performance. The PC board layout artist must be provided with explicit instructions, preferably a pencil sketch of the placement of power switching components and high-current routing. See the evaluation kit PC board layouts in the MAX1653, MAX796, and MAX797 EV kit manuals for examples. A ground plane is essential for optimum performance. In most applications, the circuit will be located on a multilayer board, and full use of the four or more copper layers is recommended. Use the top layer for high-current connections, the bottom layer for quiet connections (REF, SS, GND), and the inner layers for an uninterrupted ground plane. Use the following step-by-step guide.

1) Place the high-power components (C1, C2, Q1, Q2, D1, L1, and R1) first, with their grounds adjacent.

   Priority 1: **Minimize current-sense resistor trace lengths** (see Figure 9).

   Priority 2: **Minimize ground trace lengths** in the high-current paths (discussed below).

   Priority 3: **Minimize other trace lengths** in the high-current paths. Use >5mm wide traces. C1 to Q1: 10mm max length. D1 anode to Q2: 5mm max length LX node (Q1 source, Q2 drain, D1 cathode, inductor): 15mm max length

   Ideally, surface-mount power components are butted up to one another with their ground terminals almost touching. These high-current grounds (C1-, C2-, source of Q2, anode of D1, and PGND) are then connected to each other with a wide filled zone

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of top-layer copper, so that they don't go through vias. The resulting top-layer "sub-ground-plane" is connected to the normal inner-layer ground plane at the output ground terminals. This ensures that the analog GND of the IC is sensing at the output terminals of the supply, without interference from IR drops and ground noise. Other high-current paths should also be minimized, **but focusing ruthlessly on short ground and current-sense connections eliminates about 90% of all PC board layout difficulties.** See the evaluation kit PC board layouts for examples.

2) Place the IC and signal components. Keep the main switching node (LX node) away from sensitive analog components (current-sense traces and REF and SS capacitors). Placing the IC and analog components on the opposite side of the board from the power-switching node is desirable. Important: the IC must be no farther than 10mm from the current-sense resistor. Keep the gate-drive traces (DH, DL, and BST) shorter than 20mm and route them away from CSH, CSL, REF, and SS.

3) Employ a single-point star ground where the input ground trace, power ground (subground plane), and normal ground plane all meet at the output ground terminal of the supply.
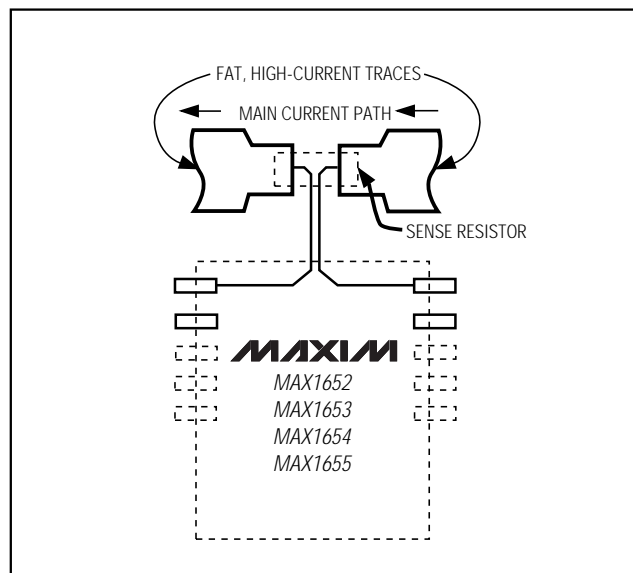
Figure 9. Kelvin Connections for the Current-Sense Resistor

Pin Configurations

TOP VIEW

QSOP

Narrow SO

( ) ARE FOR MAX1652/MAX1654.
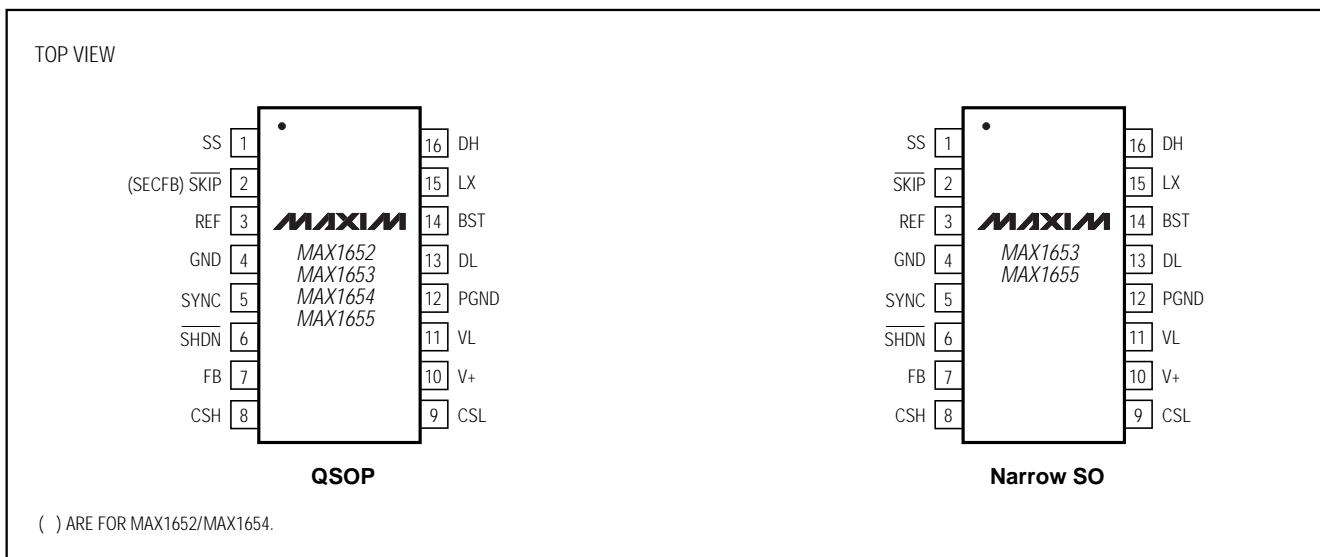
High-Efficiency, PWM, Step-Down
DC-DC Controllers in 16-Pin QSOP

_____Chip Information

TRANSISTOR COUNT: 1990

_____Package Information

QSOP.EPS

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	.061	.068	1.55	1.73
A1	.004	.0098	0.102	0.249
A2	.055	.061	1.40	1.55
B	.008	.012	0.20	0.31
C	.0075	.0098	0.191	0.249
D	SEE VARIATIONS			
E	.150	.157	3.81	3.99
e	.025 BSC		0.635 BSC	
H	.230	.244	5.84	6.20
h	.010	.016	0.25	0.41
L	.016	.035	0.41	0.89
N	SEE VARIATIONS			
X	SEE VARIATIONS			
Y	.071	.087	1.803	2.209
α	0°	8°	0°	8°

VARIATIONS:

	INCHES		MILLIMETERS		
	MIN.	MAX.	MIN.	MAX.	N
D	.189	.196	4.80	4.98	16 AA
S	.0020	.0070	0.05	0.18	
X	.107	.123	2.72	3.12	
D	.337	.344	8.56	8.74	20 AB
S	.0500	.0550	1.270	1.397	
D	.337	.344	8.56	8.74	24 AC
S	.0250	.0300	0.635	0.762	
D	.386	.393	9.80	9.98	28 AD
S	.0250	.0300	0.635	0.762	
X	.271	.287	6.88	7.29	
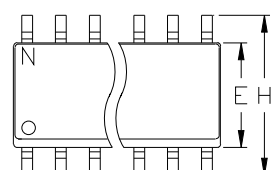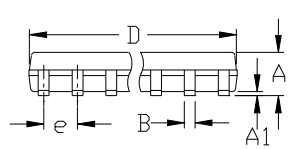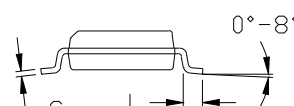
NOTES:
1. D & E DO NOT INCLUDE MOLD FLASH
   OR PROTRUSIONS
2. MOLD FLASH OR PROTRUSIONS NOT TO
   EXCEED .006" PER SIDE.
3. HEAT SLUG DIMENSIONS X AND Y APPLY ONLY
   TO 16 AND 28 LEAD POWER-QSOP PACKAGES.
4. CONTROLLING DIMENSIONS: INCHES.

/\/\ /\ X I /\/

PROPRIETARY INFORMATION
TITLE:
PACKAGE OUTLINE, QSOP, .150", .025" LEAD PITCH

APPROVAL	DOCUMENT CONTROL NO.	REV	
	21-0055	B	1/1

Package Information (continued)

	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.053	0.069	1.35	1.75
A1	0.004	0.010	0.10	0.25
B	0.014	0.019	0.35	0.49
C	0.007	0.010	0.19	0.25
e	0.050		1.27	
E	0.150	0.157	3.80	4.00
H	0.228	0.244	5.80	6.20
h	0.010	0.020	0.25	0.50
L	0.016	0.050	0.40	1.27

	INCHES		MILLIMETERS		N	MS012
	MIN	MAX	MIN	MAX		
D	0.189	0.197	4.80	5.00	8	A
D	0.337	0.344	8.55	8.75	14	B
D	0.386	0.394	9.80	10.00	16	C

NOTES:
1. D&E DO NOT INCLUDE MOLD FLASH
2. MOLD FLASH OR PROTRUSIONS NOT
   TO EXCEED .15mm (.006")
3. LEADS TO BE COPLANAR WITHIN
   .102mm (.004")
4. CONTROLLING DIMENSION: MILLIMETER
5. MEETS JEDEC MS012-XX AS SHOWN
   IN ABOVE TABLE
6. N = NUMBER OF PINS

MAXIM
120 SAN GABRIEL DR. SUNNYVALE CA 94086 FAX (408) 737 7194
PROPRIETARY INFORMATION

PACKAGE FAMILY OUTLINE: SOIC .150"
TITLE

1/1

21-0041 A
DOCUMENT CONTROL NUMBER   REV

High-Efficiency, PWM, Step-Down
DC-DC Controllers in 16-Pin QSOP

NOTES

EXHIBIT 4

MAXIM

MAX1711 Voltage Positioning Evaluation Kit

Evaluates: MAX1711

_____General Description

The MAX1711 evaluation kit (EV kit) demonstrates the high-power, dynamically adjustable notebook CPU application circuit with voltage positioning. Voltage positioning decreases CPU power consumption and reduces output capacitance requirements. This DC-DC converter steps down high-voltage batteries and/or AC adapters, generating a precision, low-voltage CPU core V_{CC} rail.

The MAX1711 EV kit provides a digitally adjustable 0.925V to 2V output voltage from a 7V to 24V battery input range. It delivers sustained output current of 12A and 14.1A peaks, operating at a 550kHz switching frequency, and has superior line- and load-transient response. The MAX1711 EV kit is designed to accomplish output voltage transitions in a controlled amount of time with limited input surge current.

This EV kit is a fully assembled and tested circuit board.

_____Ordering Information

PART	TEMP. RANGE	IC PACKAGE
MAX1711EVKIT	0°C to +70°C	24 QSOP

Quick-PWM is a trademark of Maxim Integrated Products.

_____Features

♦ **Output Voltage Positioned**

♦ **Reduces CPU Power Consumption**

♦ **Lowest Number of Output Capacitors (only 4)**

♦ **High Speed, Accuracy, and Efficiency**

♦ **Fast-Response Quick-PWM™ Architecture**

♦ **7V to 24V Input Voltage Range**

♦ **0.925V to 2V Output Voltage Range**

♦ **12A Load-Current Capability (14.1A peak)**

♦ **550kHz Switching Frequency**

♦ **Power-Good Output**

♦ **24-Pin QSOP Package**

♦ **Low-Profile Components**

♦ **Fully Assembled and Tested**

_____Component List

DESIGNATION	QTY	DESCRIPTION
C1–C4, C20	5	10µF, 25V ceramic capacitors Taiyo Yuden TMK432BJ106KM, Tokin C34Y5U1E106Z, or United Chemi-Con/Marcon THCR50E1E106ZT
C5, C6, C7, C16	4	220µF, 2.5V, 25mΩ low-ESR polymer capacitors Panasonic EEFUEOE 221R
C8	1	10µF, 6.3V ceramic capacitor Taiyo Yuden JMK325BJ106MN or TDK C3225X5R1A106M
C9	1	0.1µF ceramic capacitor
C10	0	0.01µF ceramic capacitor (not installed)
C11, C12	2	0.22µF ceramic capacitors
C13	0	0.1µF ceramic capacitor (not installed)
C14	1	470pF ceramic capacitor
C15	1	1µF ceramic capacitor
C18	1	1000pF ceramic capacitor
D1	1	2A Schottky diode SGS-Thomson STPS2L25U or Nihon EC31QS03L

DESIGNATION	QTY	DESCRIPTION
D2	1	100mA Schottky diode Central Semiconductor CMPSH-3
D3	1	1A Schottky diode Motorola MBRS130LT3, International Rectifier 10BQ040, or Nihon EC10QS03
D4	1	200mA switching diode Central Semiconductor CMPD2838
J1	1	Scope-probe connector Berg Electronics 33JR135-1
JU1	1	2-pin header
JU3–9	0	Not installed
L1	1	0.47µH power inductor Sumida CEP 125 series 4712-T006
N1	1	N-channel MOSFET (SO-8) International Rectifier IRF7811 (11mΩ at V_{GS} = 4.5V)
N2	1	N-channel MOSFET (SO-8) International Rectifier IRF7809 (7.5mΩ at V_{GS} = 4.5V)
N3	0	Not installed

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For free samples and the latest literature, visit www.maxim-ic.com or phone 1-800-998-8800.
For small orders, phone 1-800-835-8769.

MAX1711 Voltage Positioning Evaluation Kit

_____Component List (continued)

DESIGNATION	QTY	DESCRIPTION
N4, N5 (not installed)	0	N-channel MOSFETs Motorola 2N7002 or Central Semiconductor 2N7002
R1	1	20kΩ ±5% resistor
R2	1	10k ±5% resistor (not installed)
R3	1	1MΩ ±5% resistor
R4	1	100kΩ ±5% resistor
R6	1	121kΩ ±1% resistor
R7	1	3Ω ±5% resistor
R9	1	140kΩ ±1% resistor
R10	1	1kΩ ±5% resistor
R11	1	100Ω ±5% resistor
R13	1	1MΩ ±1% resistor
R14	1	10kΩ ±1% resistor
SW1	1	DIP-10 dip switch
SW2	1	Momentary switch, normally open Digi-Key P8006/7S
U1	1	MAX1711EEG (24-pin QSOP)
U2 (not installed)	0	Exclusive-OR gate (5-Pin SSOP) Toshiba TC4S30F
None	1	Shunt (JU1)
None	1	MAX1711 PC board
None	1	MAX1711 data sheet

_____Recommended Equipment

- 7V to 24V, >20W power supply, battery, or notebook AC adapter
- DC bias power supply, 5V at 100mA
- Dummy load capable of sinking 14.1A
- Digital multimeter (DMM)
- 100MHz dual-trace oscilloscope

_____Quick Start

1) Ensure that the circuit is connected correctly to the supplies and dummy load prior to applying power.
2) Ensure that the shunt is connected at JU1 ($\overline{\text{SHDN}}$ = V$_{CC}$).
3) Set switch SW1 per Table 1 to achieve the desired output voltage.
4) Connect +5V or ground to the AC Present pad to disable the transition detector circuit. See the _Dynamic Output Voltage Transitions_ section for more information regarding the transition detector circuit.

_____Component Suppliers

SUPPLIER	PHONE	FAX
Central Semiconductor	516-435-1110	516-435-1824
Dale-Vishay	402-564-3131	402-563-6418
Fairchild	408-721-2181	408-721-1635
International Rectifier	310-322-3331	310-322-3332
Kemet	408-986-0424	408-986-1442
Motorola	602-303-5454	602-994-6430
Nihon	847-843-7500	847-843-2798
Panasonic	714-373-7939	714-373-7183
Sanyo	619-661-6835	619-661-1055
SGS-Thomson	617-259-0300	617-259-9442
Sumida	708-956-0666	708-956-0702
Taiyo Yuden	408-573-4150	408-573-4159
TDK	847-390-4373	847-390-4428
Tokin	408-432-8020	408-434-0375

Note: _Please indicate that you are using the MAX1711 when contacting these component suppliers._

5) Turn on battery power prior to +5V bias power; otherwise, the output UVLO timer will time out and the FAULT latch will be set, disabling the regulator until +5V power is cycled or shutdown is toggled (**press the RESET button**).
6) Observe the output with the DMM and/or oscilloscope. Look at the LX switching-node and MOSFET gate-drive signals while varying the load current.

_____Detailed Description

This 14A buck-regulator design is optimized for a 550kHz frequency and output voltage settings around 1.6V. At V$_{OUT}$ = 1.6V, inductor ripple is approximately 35%, with a resulting pulse-skipping threshold at roughly I$_{LOAD}$ = 2.2A.

Setting the Output Voltage

Select the output voltage using the D0–D4 pins. The MAX1711 uses an internal 5-bit DAC as a feedback resistor voltage divider. The output voltage can be digitally set from 0.925V to 2V using the D0–D4 inputs. Switch SW1 sets the desired output voltage. See Table 1.

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MAX1711 Voltage Positioning Evaluation Kit

Table 1. MAX1710/1711 Output Voltage Adjustment Settings

D4	D3	D2	D1	D0	OUTPUT VOLTAGE (V)
0	0	0	0	0	2.00
0	0	0	0	1	1.95
0	0	0	1	0	1.90
0	0	0	1	1	1.85
0	0	1	0	0	1.80
0	0	1	0	1	1.75
0	0	1	1	0	1.70
0	0	1	1	1	1.65
1	1	0	0	0	1.60
1	1	0	0	1	1.55
1	1	0	1	0	1.50
1	1	0	1	1	1.45
1	1	1	0	0	1.40
1	1	1	0	1	1.35
1	1	1	1	0	1.30
0	1	1	1	1	Shutdown
1	0	0	0	0	1.275
1	0	0	0	1	1.250
1	0	0	1	0	1.225
1	0	0	1	1	1.200
1	0	1	0	0	1.175
1	0	1	0	1	1.150
1	0	1	1	0	1.125
1	0	1	1	1	1.100
1	1	0	0	0	1.075
1	1	0	0	1	1.050
1	1	0	1	0	1.025
1	1	0	1	1	1.000
1	1	1	0	0	0.975
1	1	1	0	1	0.950
1	1	1	1	0	0.925
1	1	1	1	1	Shutdown

Voltage Positioning

The MAX1711 EV kit uses voltage positioning to minimize the output capacitor requirements of the Intel Coppermine CPU's transient voltage specification (-7.5% to +7.5%). The output voltage is initially set slightly high (1.25%) and then allowed to regulate lower as the load current increases. R13 and R14 set the ini-tial output voltage 20mV high, and R12 (5mΩ) causes the output voltage to drop with increasing load (60mV or about 4% of 1.6V at 12A).

Setting the output voltage high allows a larger step-down when the output current increases suddenly, and regulating at the lower output voltage under load allows a larger step-up when the output current suddenly decreases. Allowing a larger step size means that the output capacitance can be reduced and the capaci-tor's ESR can be increased. If voltage positioning is not used, one additional output capacitor is required to meet the same transient specification.

Reduced power consumption at high load currents is an additional benefit of voltage positioning. Because the output voltage is reduced under load, the CPU draws less current. This results in lower power dissipation in the CPU, though some extra power is dissipated in R12. For a 1.6V, 12A nominal output, reducing the output voltage 2.75% (1.25% - 4%) gives an output voltage of 1.556V and an output current of 11.67A. So the CPU power consumption is reduced from 19.2W to 18.16W. The additional power consumption of R12 is 5mΩ · 11.7A^2 = 0.68W, and the overall power savings is 19.2 − (18.16 + 0.68) = 0.36W. In effect, 1W of CPU dissipation is saved and the power supply dissipates much of the savings, but both the net savings and the transfer of dis-sipation away from the hot CPU are beneficial.

Dynamic Output Voltage Transitions

If the DAC inputs (D0–D4) are changed, the output volt-age will change accordingly. However, under some cir-cumstances, the output voltage transition may be slow-er than desired. All transitions to a higher voltage will occur very quickly, with the circuit operating at the cur-rent limit set by the voltage at the ILIM pin. Transitions to a lower output voltage require the circuit or the load to sink current. If $\overline{\text{SKIP}}$ is held low (PFM mode), the cir-cuit won't sink current, so the output voltage will decrease only at the rate determined by the load cur-rent. This is often acceptable, but some applications require output voltage transitions to be completed with-in a set time limit.

Powering CPUs with Intel's Geyserville technology is such an application. The specification requires that out-put voltage transitions occur within 100µs after a DAC code change. This fast transition timing means that the regulator circuit must sink as well as source current.

The simplest way of meeting this requirement is to use the MAX1711's fixed-frequency PWM mode (set $\overline{\text{SKIP}}$ high), allowing the regulator to sink or source currents equally. This EV kit is shipped with $\overline{\text{SKIP}}$ set high. Although this results in a V_{DD} quiescent current to 20mA or more, depending on the MOSFETs and

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MAX1711 Voltage Positioning Evaluation Kit

switching frequency used, it is often an acceptable choice. A similar but more clever approach is to use PWM mode only during transitions. This approach allows the regulator to sink current when needed and to operate with low quiescent current the rest of the time, but it requires that the system know when the transitions will occur. Any system with a changing output voltage must know when its output voltage changes occur. Usually, it is the system that initiates the transition, either by driving the DAC inputs to new levels or by selecting new DAC inputs with a digital mux. While it is possible for the regulator to recognize transitions by watching for DAC code changes, the glue logic needed to add that feature to existing controllers is unnecessarily complicated (refer to the MAX1710/MAX1711 data sheet, Figure 10). It is easier to use the chipset signal that selects DAC codes at the mux, or some other system signal to inform the regulator that a code change is occurring.

For easy modification, the MAX1711 EV kit is designed to use an external chipset signal to indicate DAC code transitions (install U2, R2, C10, C13; short JU9 and cut JU10). This signal connects to the EV kit's AC Present pad and should have 5V logic levels. Logic edges on AC Present are detected by exclusive-OR gate U2, which generates a 60µs pulse on each edge (determined by R2 and C10). These pulses drive $\overline{SKIP}$, allowing the regulator to sink current during transitions.

Because U2 is powered by V_{CC} (5V), the signal connected to AC Present must have 5V logic levels so that U2's output pulses will be symmetric for positive- and negative-going transitions. If the signal that's available to drive AC Present has a different logic level, either level-shift the signal or lift U2's supply pin and power it from the appropriate supply rail.

In addition to controlling $\overline{SKIP}$, the pulses from U2 have two other functions, which are optional. U2's output drives the gates of two small-signal MOSFETs, N4 and N5 (not installed). N4 is used to temporarily reduce the circuit's current limit, in effect soft-starting the regulator. This reduces the battery surge current, which otherwise would discharge (upward transitions) or charge (downward transitions) the regulator input (battery) at a rate determined by the regulator's maximum current limit. N5 pulls down on PGOOD during transitions, indicating that the output voltage is in transition.

Load-Transient Measurement

One interesting experiment is to subject the output to large, fast load transients and observe the output with an oscilloscope. This necessitates careful instrumentation of the output, using the supplied scope-probe jack.

Accurate measurement of output ripple and load-transient response invariably requires that ground clip leads be completely avoided and that the probe hat be removed to expose the GND shield, so the probe can be plugged directly into the jack. Otherwise, EMI and noise pickup will corrupt the waveforms.

Most benchtop electronic loads intended for power-supply testing are unable to subject the DC-DC converter to ultra-fast load transients. Emulating the supply current di/dt at the CPU VCORE pins requires at least 10A/µs load transients. One easy method for generating such an abusive load transient is to solder a MOSFET, such as an MTP3055 or 12N05 directly across the scope-probe jack. Then drive its gate with a strong pulse generator at a low duty cycle (10%) to minimize heat stress in the MOSFET. Vary the high-level output voltage of the pulse generator to adjust the load current.

To determine the load current, you might expect to insert a meter in the load path, but this method is prohibited here by the need for low resistance and inductance in the path of the dummy-load MOSFET. There are two easy alternative methods for determining how much load current a particular pulse-generator amplitude is causing. The first and best is to observe the inductor current with a calibrated AC current probe, such as a Tektronix AM503. In the buck topology, the load current is equal to the average value of the inductor current. The second method is to first put on a static dummy load and measure the battery current. Then, connect the MOSFET dummy load at 100% duty momentarily, and adjust the gate-drive signal until the battery current rises to the appropriate level (the MOSFET load must be well heatsinked for this to work without causing smoke and flames).

Efficiency Measurements and Effective Efficiency

Testing the power conversion efficiency POUT/PIN fairly and accurately requires more careful instrumentation than might be expected. One common error is to use inaccurate DMMs. Another is to use only one DMM, and move it from one spot to another to measure the various input/output voltages and currents. This second error usually results in changing the exact conditions applied to the circuit due to series resistance in the ammeters. It's best to get four 3-1/2 digit, or better, DMMs that have been recently calibrated, and monitor V_{BATT}, V_{OUT}, I_{BATT}, and I_{LOAD} simultaneously, using separate test leads directly connected to the input and output PC board terminals. Note that it's inaccurate to test efficiency at the remote V_{OUT} and ground termi-

MAXIM

nals, because doing this incorporates the parasitic resistance of the PC board output and ground buses in the measurement (a significant power loss).

Remember to include the power consumed by the +5V bias supply when making efficiency calculations:

$$\text{Efficiency} = \frac{V_{OUT} \cdot I_{LOAD}}{(V_{BATT} \cdot I_{BATT}) + (5V \cdot I_{BIAS})}$$

The choice of MOSFET has a large impact on efficiency performance. The International Rectifier MOSFETs used were of leading-edge performance for the 12A application at the time this kit was designed. However, the pace of MOSFET improvement is rapid, so the latest offerings should be evaluated.

Once the actual efficiency data has been obtained, some work remains before an accurate assessment of a voltage-positioned circuit can be made. As discussed in the *Voltage Positioning* section, a voltage-positioned power supply can dissipate additional power while reducing system power consumption. For this reason, we use the concept of effective efficiency, which allows the direct comparison of a positioned and nonpositioned circuit's efficiency. Effective efficien-cy is the efficiency required of a nonvoltage-positioned circuit to equal the total dissipation of a voltage-positioned circuit for a given CPU operating condition.

Calculate effective efficiency as follows:

- Start with the efficiency data for the positioned circuit (V_{IN}, I_{IN}, V_{OUT}, I_{OUT}).

- Model the load resistance for each data point ($R_{LOAD} = V_{OUT} / I_{OUT}$).

- Calculate the output current that would exist for each R_{LOAD} data point in a nonpositioned application ($I_{NP} = V_{NP} / R_{LOAD}$, where $V_{NP} = 1.6V$ in this example).

- Effective efficiency = ($V_{NP} \cdot I_{NP}$) / ($V_{IN} \cdot I_{IN}$) = calculated nonpositioned power output divided by the measured voltage-positioned power input.

- Plot the efficiency data point at the current I_{NP}.

The effective efficiency of the voltage-positioned circuit will be less than that of the nonpositioned circuit at light loads where the voltage-positioned output voltage is higher than the nonpositioned output voltage. It will be greater than that of the nonpositioned circuit at heavy loads where the voltage-positioned output voltage is lower than the nonpositioned output voltage.

MAX1711 Voltage Positioning Evaluation Kit

_____*Jumper and Switch Settings*

Table 2. Jumper JU1 Functions (Shutdown Mode)

SHUNT LOCATION	SHDN PIN	MAX1711 OUTPUT
Installed	Connected to V_{CC}	MAX1711 enabled
Not Installed	Connected to GND	Shutdown mode, $V_{OUT} = 0$

Table 3. Jumpers JU3/JU4/JU5 Functions (Switching-Frequency Selection)

SHUNT LOCATION			TON PIN	FREQUENCY (kHz)
JU3	JU4	JU5		
Installed	Not Installed	Not Installed	Connected to V_{CC}	200
Not Installed	Installed	Not Installed	Connected to REF	400
Not Installed	Not Installed	Installed	Connected to GND	550
Not Installed	Not Installed	Not Installed	Floating	300

IMPORTANT: *Don't change the operating frequency without first recalculating component values because the frequency has a significant effect on the peak current-limit level, MOSFET heating, preferred inductor value, PFM/PWM switchover point, output noise, efficiency, and other critical parameters.*

Table 4. Jumper JU6 Functions (Fixed/Adjustable Current-Limit Selection)

SHUNT LOCATION	ILIM PIN	CURRENT-LIMIT THRESHOLD
Installed	Connected to V_{CC}	100mV
Not Installed	Connected to GND via an external resistor divider, R6/R9. Refer to the Pin Description ILIM section in the MAX1711 data sheet for more information.	Adjustable between 50mV and 200mV

Table 5. Jumpers JU9/JU10 Functions (FBS and FB Integrator Disable Selection)

SHUNT LOCATION		SKIP PIN
JU9	JU10	
Installed	Not Installed	Connected to V_{CC}
Not Installed	Installed	Connected to the output of U2

Table 6. Troubleshooting Guide

SYMPTOM	POSSIBLE PROBLEM	SOLUTION
Circuit won't start when power is applied.	Power-supply sequencing: +5V bias supply was applied first.	Press the RESET button.
Circuit won't start when RESET is pressed, +5V bias supply cycled.	Output overvoltage due to shorted high-side MOSFET.	Replace the MOSFET.
	Output overvoltage due to load recovery overshoot.	Reduce the inductor value, raise the switching frequency, or add more output capacitance.
	Overload condition.	Remove the excessive load.
	Broken connection, bad MOSFET, or other catastrophic problem.	Troubleshoot the power stage. Are the DH and DL gate-drive signals present? Is the 2V V_{REF} present?
On-time pulses are erratic or have unexpected changes in period.	VBATT power source has poor impedance characteristic.	Add a bulk electrolytic bypass capacitor across the benchtop power supply, or substitute a real battery.

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MAX1711 Voltage Positioning Evaluation Kit

Figure 1. MAX1711 Voltage Positioning EV Kit Schematic

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Evaluates: MAX1711
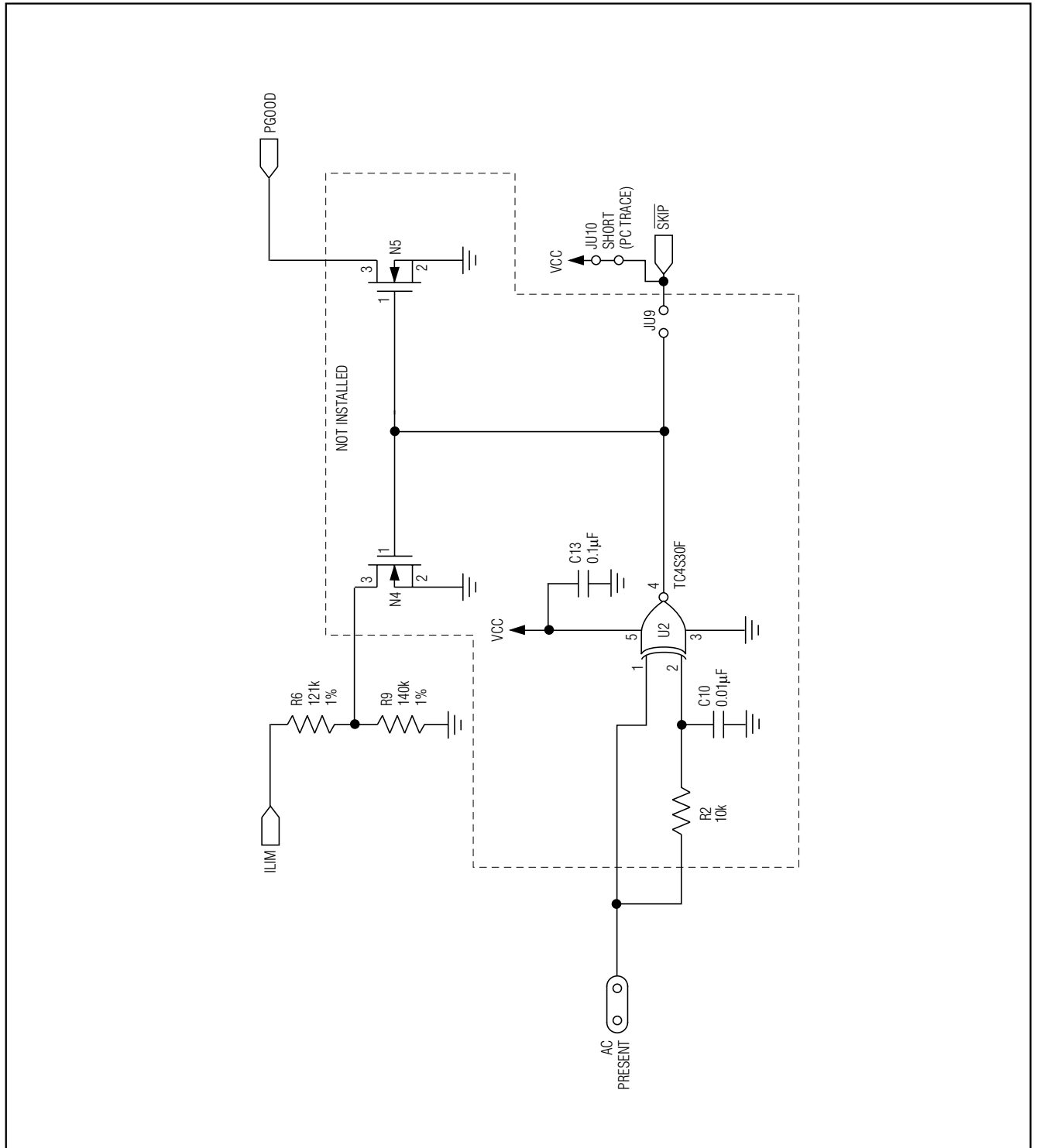
Figure 1. MAX1711 Voltage Positioning EV Kit Schematic (continued)

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MAX1711 Voltage Positioning Evaluation Kit
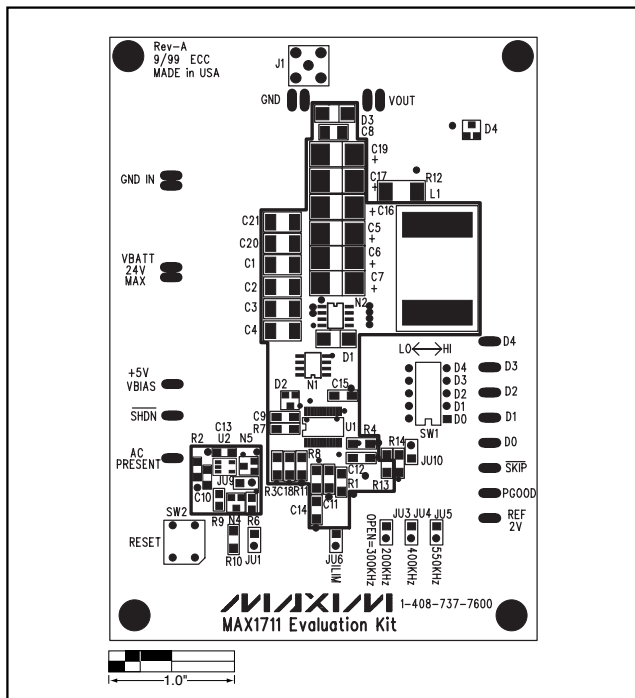
Figure 2. MAX1711 Voltage Positioning EV Kit Component Placement Guide—Component Side
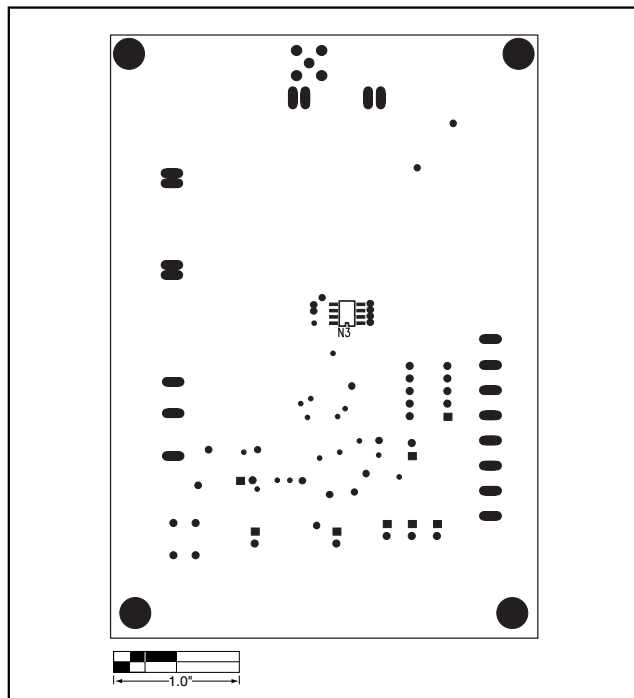
Figure 3. MAX1711 Voltage Positioning EV Kit Component Placement Guide—Solder Side
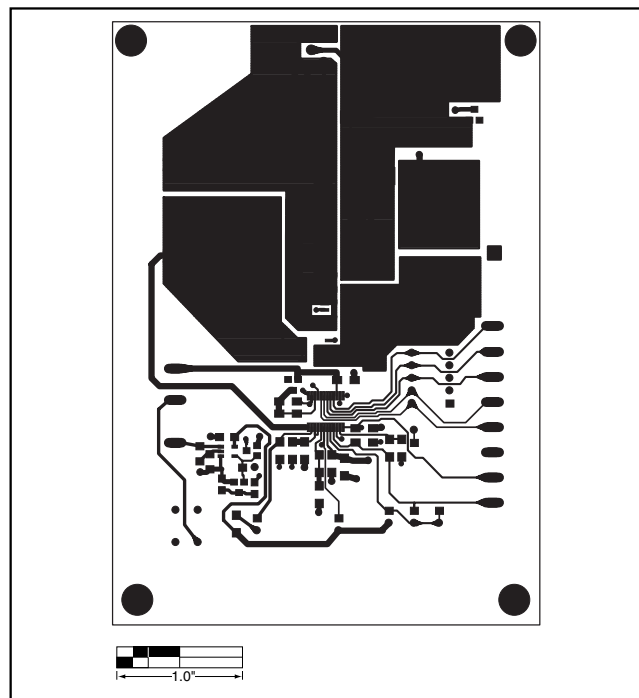
Figure 4. MAX1711 Voltage Positioning EV Kit PC Board Layout—Component Side
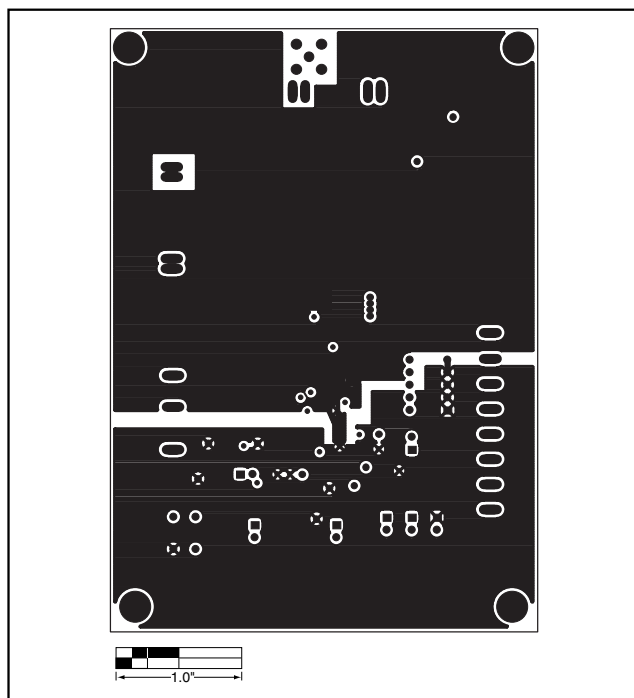
Figure 5. MAX1711 Voltage Positioning EV Kit PC Board Layout—Internal GND Plane (Layer 2)

_____ 9
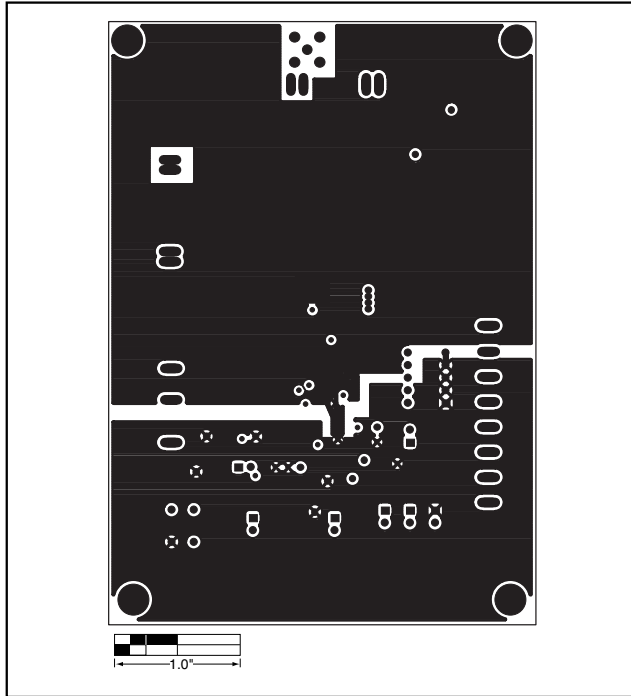
Evaluates: MAX1711

Figure 6. MAX1711 Voltage Positioning EV Kit PC Board Layout—Internal GND Plane (Layer 3)
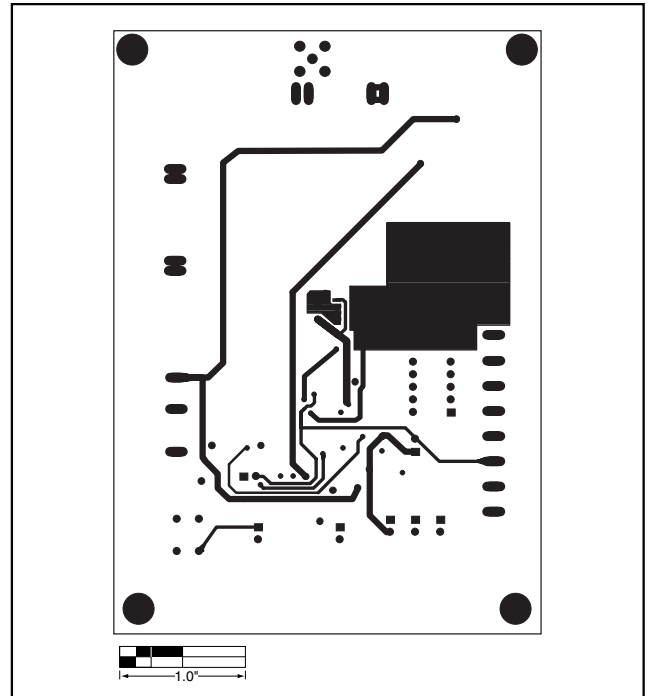
Figure 7. MAX1711 Voltage Positioning EV Kit PC Board Layout—Solder Side

MAX1711 Voltage Positioning Evaluation Kit

NOTES

MAXIM _____ 11

Evaluates: MAX1711

NOTES

EXHIBIT 5

James W. Nilsson

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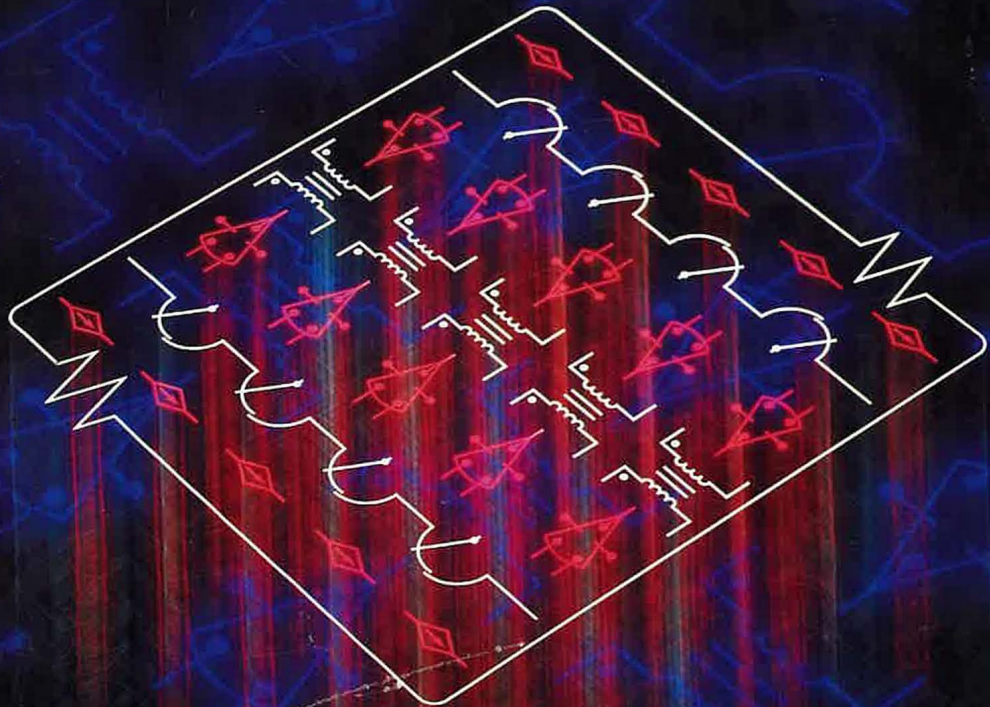
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