

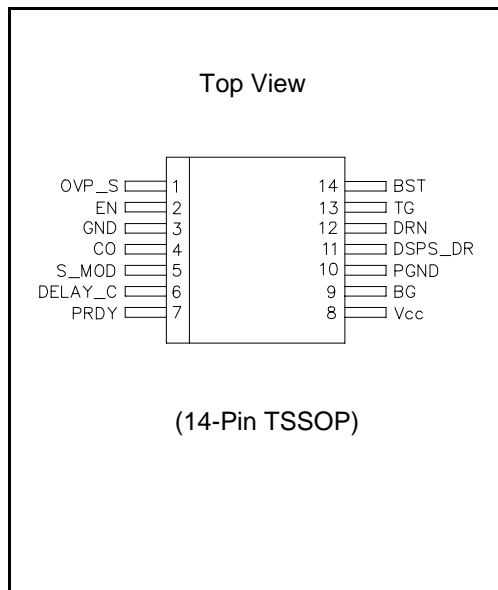
August 31, 2000

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## DESCRIPTION

The SC1405 is a Dual-MOSFET Driver with an internal Overlap Protection Circuit to prevent shoot-through from  $V_{IN}$  to GND in the main switching and synchronous MOSFET's. Each driver is capable of driving a 3000pF load in 20ns rise/fall time and has ULTRA-FAST propagation delay from input transition to the gate of the power FET's. The Overlap Protection circuit ensures that the second FET does not turn on until the top FET source has reached a voltage low enough to prevent shoot-through. The delay between the bottom gate going low to the top gate transitioning to high is externally programmable via a capacitor for optimal reduction of switching losses at the operating frequency. The bottom FET may be disabled at light loads by keeping S\_MOD low to trigger asynchronous operation, thus saving the bottom FET's gate drive current and inductor ripple current. An internal voltage reference allows threshold adjustment for an Output Over-Voltage protection circuitry, independent of the PWM feedback loop. Under-Voltage-Lock-Out circuit is included to guarantee that both driver outputs are low when the 5V logic level is less than or equal to 4.4V (typ) at supply ramp up (4.35V at supply ramp down). A CMOS output provides status indication of the 5V supply. A low enable input places the IC in stand-by mode thereby reducing supply current to less than 10 $\mu$ A. SC1405 is offered in a high pitch (.025" lead spacing) TSSOP package.

## PIN CONFIGURATION



## FEATURES

- Fast rise and fall times (20ns typical with 3000pf load)
- 20ns max. Propagation delay (BG going low)
- Adaptive/programmable shoot-through protection
- Wide input voltage range (4.5-25V)
- Programmable delay between MOSFET's
- Power saving asynchronous mode control
- Output overvoltage protection/overtemp shutdown
- Under-Voltage lock-out and power ready signal
- Less than 10 $\mu$ A stand-by current (EN=low)
- Power ready output signal

## APPLICATIONS

- High Density/Fast transient power supplies
- Motor Drives/Class-D amps
- High frequency (to 1.2 MHz) operation allows use of small inductors and low cost caps in place of electrolytics
- Portable computers

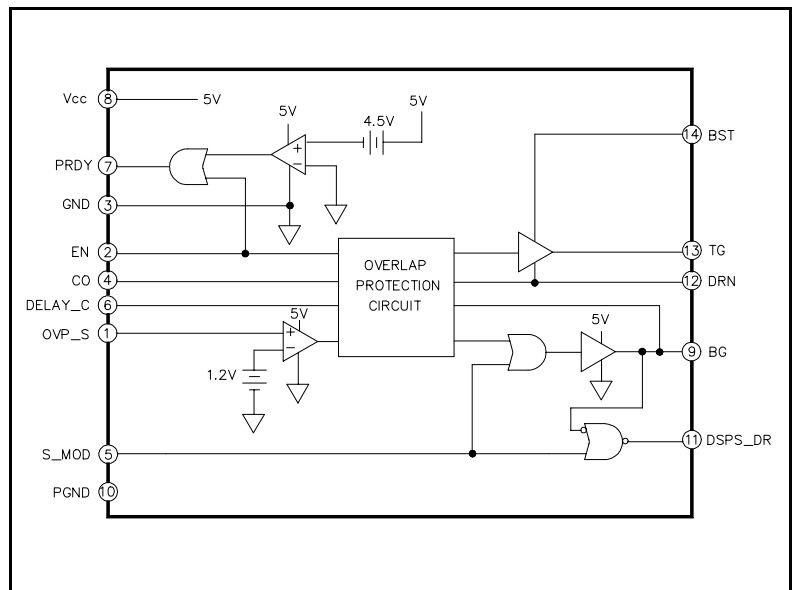
## ORDERING INFORMATION

DEVICE <sup>(1)</sup>	PACKAGE	TEMP. RANGE (T <sub>J</sub> )
SC1405TS.TR	TSSOP-14	0 - 125°C

Note:

(1) Only available in tape and reel packaging. A reel contains 2500 devices.

## BLOCK DIAGRAM



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**ABSOLUTE MAXIMUM RATINGS**

Parameter	Symbol	Conditions	Maximum	Units
V <sub>CC</sub> Supply Voltage	V <sub>MAX5V</sub>		7	V
BST to PGND	V <sub>MAX</sub> <sub>BST-PGND</sub>		30	V
BST to DRN	V <sub>MAX</sub> <sub>BST-DRN</sub>		7	V
DRN to PGND	V <sub>MAX</sub> <sub>DRN-PGN</sub>		25	V
OVP_S to PGND	V <sub>MAX</sub> <sub>OVP_S-PGND</sub>		10	V
Input pin	CO		-0.3 to 7.3	V
Continuous Power Dissipation	P <sub>d</sub>	T <sub>amb</sub> = 25°C, T <sub>J</sub> = 125°C T <sub>case</sub> = 25°C, T <sub>J</sub> = 125°C	0.66 2.56	W
Thermal Resistance Junction to Case	θ <sub>JC</sub>		40	°C/W
Thermal Resistance Junction to Ambient	θ <sub>JA</sub>		150	°C/W
Operating Temperature Range	T <sub>J</sub>		0 to +125	°C
Storage Temperature Range	T <sub>STG</sub>		-65 to +150	°C
Lead Temperature (Soldering) 10 sec	T <sub>LEAD</sub>		300	°C

**NOTE:**

(1) Specification refers to application circuit in Figure 1.

**ELECTRICAL CHARACTERISTICS (DC OPERATING SPECIFICATIONS)**

 Unless specified: -0 < θ<sub>J</sub> < 125°C; V<sub>CC</sub> = 5V; 4V ≤ V<sub>BST</sub> ≤ 26V

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
<b>POWER SUPPLY</b>						
Supply Voltage	V <sub>CC</sub>	V <sub>CC</sub>	4.15	5	6.0	V
Quiescent Current	I <sub>q_stby</sub>	EN = 0V			10	μA
Quiescent Current, operating	I <sub>q_op</sub>	V <sub>CC</sub> = 5V, CO=0V		1		ma
<b>PRDY</b>						
High Level Output Voltage	V <sub>OH</sub>	V <sub>CC</sub> = 4.6V, I <sub>load</sub> = 10mA	4.5	4.55		V
Low Level Output Voltage	V <sub>OL</sub>	V <sub>CC</sub> < UVLO threshold, I <sub>load</sub> = 10μA		0.1	0.2	V
<b>DSPS_DR</b>						
High Level Output Voltage	V <sub>OH</sub>	V <sub>CC</sub> = 4.6V, C <sub>load</sub> = 100pF	4.15			V
Low Level Output Voltage	V <sub>OL</sub>	V <sub>CC</sub> = 4.6V, C <sub>load</sub> = 100pF			0.05	V
<b>UNDER-VOLTAGE LOCKOUT</b>						
Start Threshold	V <sub>START</sub>		4.2	4.4	4.6	V
Hysteresis	V <sub>hys</sub> <sub>UVLO</sub>			0.05		V
Logic Active Threshold	V <sub>ACT</sub>	EN is low			1.5	V

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**ELECTRICAL CHARACTERISTICS (DC OPERATING SPECIFICATIONS) Cont.**

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
<b>OVERVOLTAGE PROTECTION</b>						
Trip Threshold	$V_{TRIP}$		1.145	1.2	1.255	V
Hysteresis	$V_{hys_{OVP}}$			0.8		V
<b>S_MOD</b>						
High Level Input Voltage	$V_{IH}$		2.0			V
Low Level Input Voltage	$V_{IL}$				0.8	V
<b>ENABLE</b>						
High Level Input Voltage	$V_{IH}$		2.0			V
Low Level Input Voltage	$V_{IL}$				0.8	V
<b>CO</b>						
High Level Input Voltage	$V_{IH}$		2.0			V
Low Level Input Voltage	$V_{IL}$				0.8	V
<b>THERMAL SHUTDOWN</b>						
Over Temperature Trip Point	$T_{OTP}$			165		°C
Hysteresis	$T_{HYST}$			10		°C
<b>HIGH-SIDE DRIVER</b>						
Peak Output Current	$I_{PKH}$			1.5		A
Output Resistance	$R_{src_{TG}}$	duty cycle < 2%, t <sub>pw</sub> < 100μs, T <sub>J</sub> = 125°C, V <sub>BST</sub> - V <sub>DRN</sub> = 4.5V, V <sub>TG</sub> = 4.0V (src)+V <sub>DRN</sub> or V <sub>TG</sub> = 0.5V (sink)+V <sub>DRN</sub>		1.4		Ω
	$R_{sink_{TG}}$			1.4		Ω
<b>LOW-SIDE DRIVER</b>						
Peak Output Current	$I_{PKL}$			2		A
Output Resistance	$R_{src_{BG}}$	duty cycle < 2%, t <sub>pw</sub> < 100μs, T <sub>J</sub> = 125°C V <sub>V.5</sub> = 4.6V, V <sub>BG</sub> = 4V (src), or V <sub>LOWDR</sub> = 0.5V (sink)		2		Ω
	$R_{sink_{BG}}$			2		Ω

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**ELECTRICAL CHARACTERISTICS (DC OPERATING SPECIFICATIONS) Cont.**

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
<b>AC OPERATING SPECIFICATIONS</b>						
<b>HIGH-SIDE DRIVER</b>						
rise time	$t_{r_{TG}}$	$C_I = 3nF, V_{BST} - V_{DRN} = 4.6V,$		16	25	ns
fall time	$t_{f_{TG}}$	$C_I = 3nF, V_{BST} - V_{DRN} = 4.6V,$		17	27	ns
propagation delay time, TG going high	$tpd_{h_{TG}}$	$C_I = 3nF, V_{BST} - V_{DRN} = 4.6V,$ <b>C-delay=0</b>		35	56	ns
propagation delay time, TG going low	$tpd_{l_{TG}}$	$C_I = 3nF, V_{BST} - V_{DRN} = 4.6V,$		25	40	ns
<b>LOW-SIDE DRIVER</b>						
rise time	$t_{r_{BG}}$	$C_I = 3nF, V_{V_5} = 4.6V,$		20	32	ns
fall time	$t_{f_{BG}}$	$C_I = 3nF, V_{V_5} = 4.6V,$		18	29	ns
propagation delay time BG going high	$tpd_{h_{BGHI}}$	$C_I = 3nF, V_{V_5} = 4.6V,$ $DRN \leq 1V$		45	72	ns
propagation delay time BG going low	$tpd_{l_{BG}}$	$C_I = 3nF, V_{V_5} = 4.6V,$		12	20	ns
<b>UNDER-VOLTAGE LOCKOUT</b>						
V <sub>5</sub> ramping up	$tpd_{UVLO}$	EN is High			10	us
V <sub>5</sub> ramping down	$tpd_{UVLO}$	EN is High			10	us
<b>PRDY</b>						
EN is transitioning from low to high	$tpd_{PRDY}$	$V_{V_5} \geq UVLO$ threshold, Delay measured from $EN \geq 2.0V$ to $PRDY \geq 3.5V$			10	$\mu s$
EN is transitioning from high to low	$tpd_{UVLO}$	$V_{V_5} \geq UVLO$ threshold. Delay measured from $EN \leq 0.8V$ to $PRDY \leq 10\%$ of $V_{V_5}$			500	$\mu s$
<b>DSPS_DR</b>						
rise/fall time	$t_{r_{DSPS\_DR}},$ $t_{f_{DSPS\_DR}}$	$C_I = 100pf, V_{V_5} = 4.6V,$			20	ns
propagation delay, DSPS_DR going high	$tpd_{DSPS\_DR}$	S_MOD goes high and BG goes high or S_MOD goes low			10	ns
propagation delay DSPS_DR goes low	$tpd_{l_{DSPS\_DR}}$	S_MOD goes high and BG goes low			10	ns
<b>OVERVOLTAGE PROTECTION</b>						
propagation delay OVP_S going high	$tpd_{OVP\_S}$	$V_{V_5} = 4.6V, T_J = 125^\circ C, OVP\_S \geq 1.2V$ to $BG > 90\%$ of $V_{V_5}$			1	$\mu s$

Note:

(1) This device is ESD sensitive. Use of standard ESD handling precautions is required.

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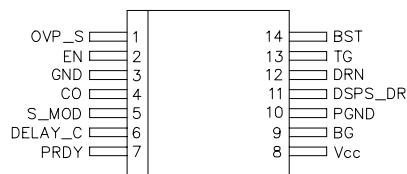
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**PIN DESCRIPTION**

Pin #	Pin Name	Pin Function
1	OVP_S	Overvoltage protection sense. External scaling resistors required to set protection threshold.
2	EN	When high, this pin enables the internal circuitry of the device. When low, TG, BG and PRDY are forced low and the supply current (5V) is less than 10 $\mu$ A.
3	GND	Logic GND.
4	CO	TTL-level input signal to the MOSFET drivers.
5	S_MOD	When low, this signal forces BG to be low. When high, BG is not a function of this signal.
6	DELAY_C	Sets the additional propagation delay for BG going low to TG going high. Total propagation delay= 20ns + 1ns/pF.
7	PRDY	This pin indicates the status of 5V. When 5V is less than 4.4V(typ) this output is driven low. When 5V is greater than or equals to 4.4V(typ) this output is driven to 5V level. This output has a 10mA drive capability and 10 $\mu$ A sink capability.
8	V <sub>cc</sub>	+5V supply. A .22-1 $\mu$ F ceramic capacitor should be connected from 5V to PGND very close to this pin.
9	BG	Output drive for the synchronous MOSFET.
10	PGND	Power ground. Connect to the synchronous FET power ground.
11	DSPS_DR	Dynamic Set Point Switch Drive. TTL level output signal. When S_MOD is high, this pin follows the BG driver pin voltage.
12	DRN	This pin connects to the junction of the switching and synchronous MOSFET's. This pin can be subjected to a -2V minimum relative to PGND without affecting operation.
13	TG	Output gate drive for the switching (high-side) MOSFET.
14	BST	Bootstrap pin. A capacitor is connected between BST and DRN pins to develop the floating bootstrap voltage for the high-side MOSFET. The capacitor value is typically between 0.1 $\mu$ F and 1 $\mu$ F (ceramic).

**NOTE:**

(1) All logic level inputs and outputs are open collector TTL compatible.

**PIN CONFIGURATION**


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