



US005457421A

United States Patent [19]
Tanabe

[11] Patent Number: 5,457,421

[45] Date of Patent: Oct. 10, 1995

[54] VOLTAGE STEPDOWN CIRCUIT INCLUDING A VOLTAGE DIVIDER

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[75] Inventor: Akira Tanabe, Tokyo, Japan

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[73] Assignee: NEC Corporation, Tokyo, Japan

T. Takeshima et al.; "A 55-ns 16-Mb DRAM with Built-in Self-Test Function Using Microprogram ROM"; IEEE Journal of Solid-State Circuits, vol. 25, No. 4, Aug. 1990, pp. 903-911.

[21] Appl. No.: 194,330

[22] Filed: Feb. 8, 1994

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[30] Foreign Application Priority Data

Feb. 10, 1993 [JP] Japan 5-022232

[51] Int. Cl.⁶ H03K 3/01

[52] U.S. Cl. 327/530; 327/306; 327/333; 327/544; 327/546

[58] Field of Search 307/296.1, 296.2, 307/296.3, 296.4, 296.5, 296.6, 353, 532, 350; 328/127; 327/530, 535, 541, 544, 546, 306, 333

[57] ABSTRACT

A voltage step-down circuit to be built in a highly integrated semiconductor IC chip, including a voltage divider and a voltage comparator. A divided output voltage V_{INT} of the voltage divider and a comparison reference voltage V_{REF} are applied to respective input terminals (-) and (+) of the voltage comparator. An output signal of the voltage comparator is supplied to a control signal generator section of the voltage divider to generate control pulses and to control the connection of capacitors of a voltage divider section of the voltage divider with the control pulses so as to supply the divided output voltage V_{INT} to a load circuit. In this case, the capacitors are used as a voltage divider for generating a voltage for an internal circuit from an external power source voltage. Thus, power loss can be reduced and utilization efficiency of the capacitors is raised. Hence, the voltage step-down circuit is suitable for highly integrated semiconductor IC chip.

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15 Claims, 15 Drawing Sheets

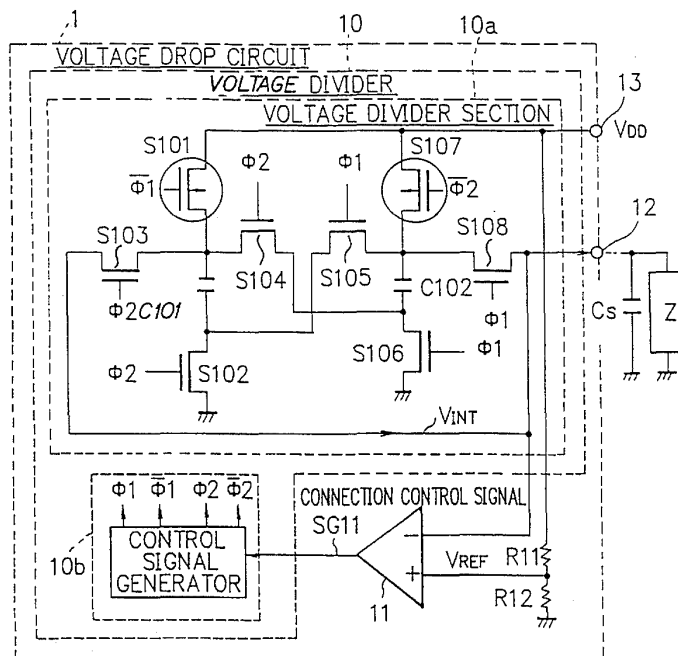


FIG. 1

PRIOR ART

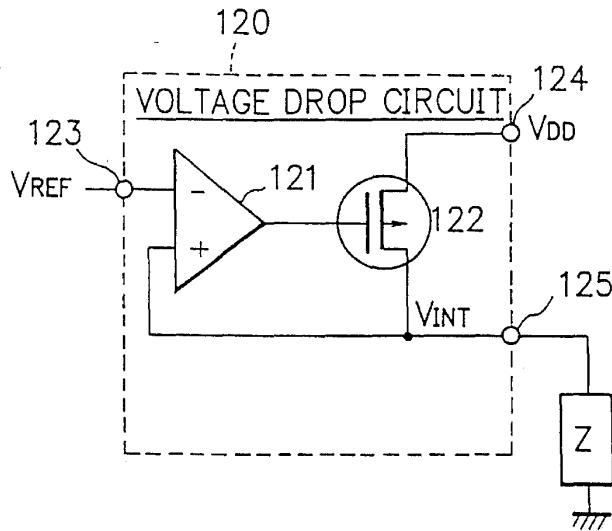


FIG. 2

PRIOR ART

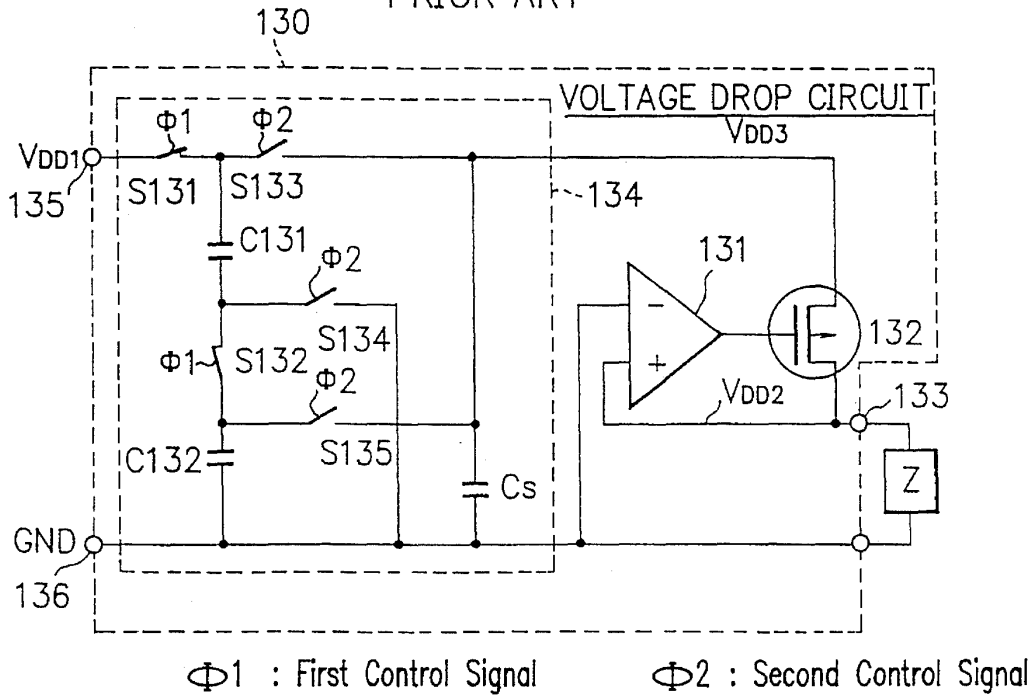


FIG. 3a

PRIOR ART

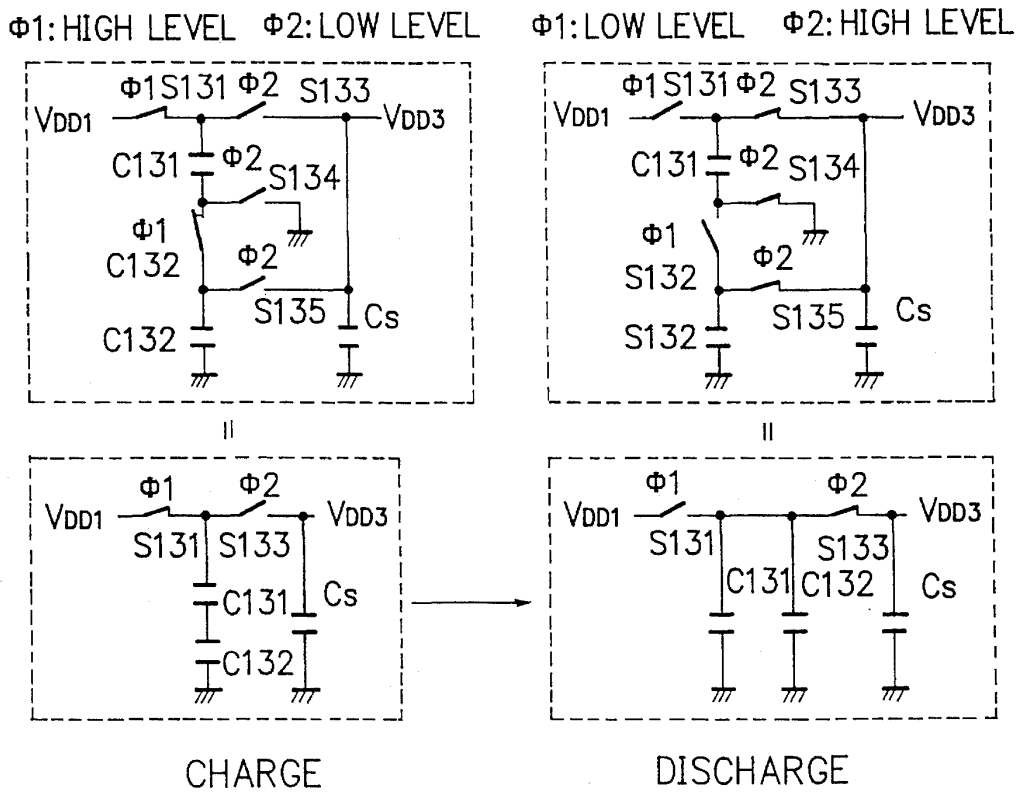


FIG. 3b

PRIOR ART

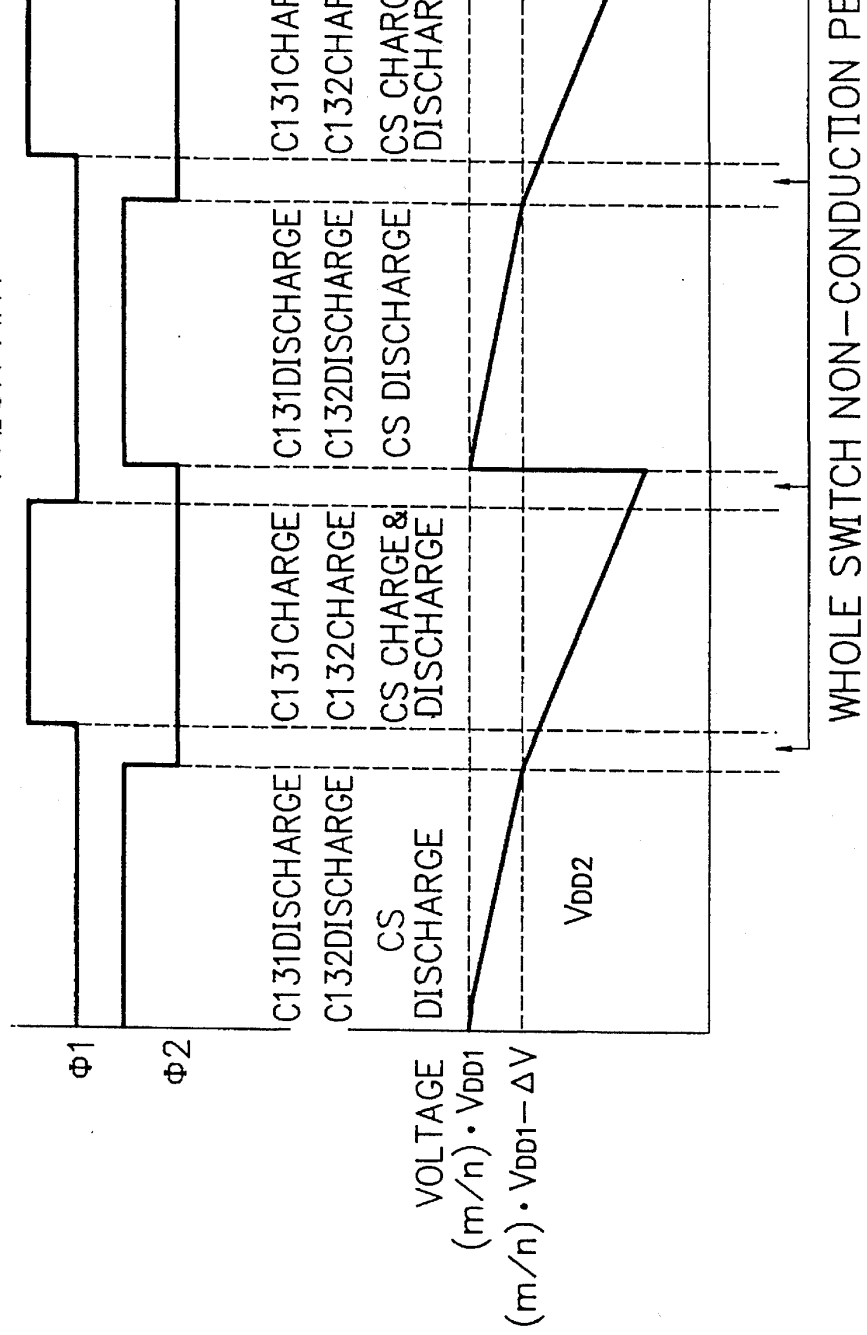


FIG. 4a

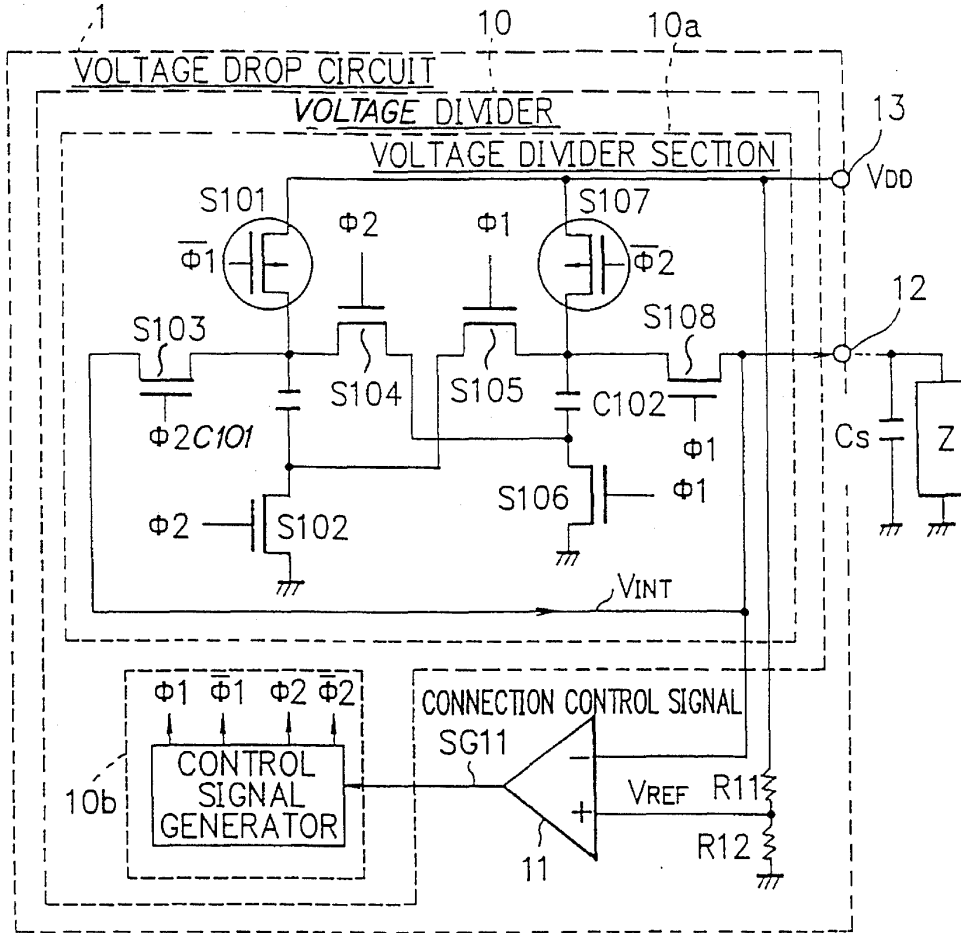
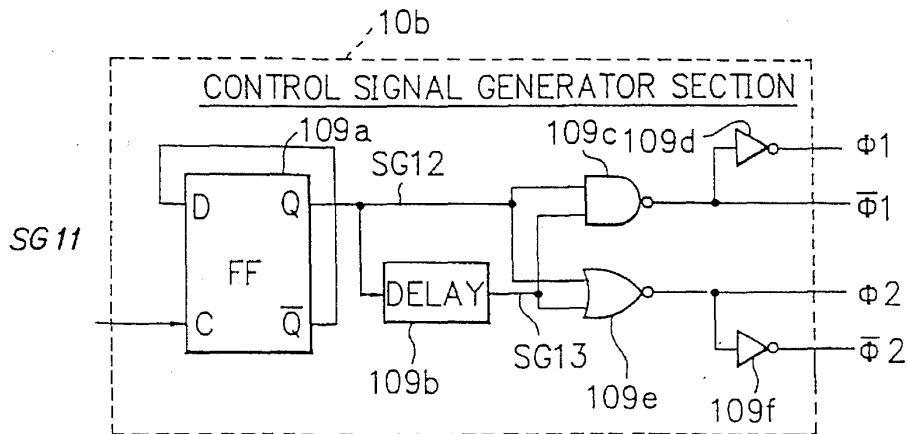


FIG. 4b



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