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Rimondi

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(54) **LOW POWER SRAM MEMORY CELL HAVING A SINGLE BIT LINE**

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(52) **U.S. Cl.** **365/156**; 365/154
(58) **Field of Search** 365/156, 154, 365/203, 69

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(57) **ABSTRACT**

A semiconductor memory cell having a word line, a bit line, a precharge line, an access transistor, and first and second cross-coupled inverters. The first inverter includes a first P-channel transistor and a first N-channel transistor, and the second inverter includes a second P-channel transistor and a second N-channel transistor. The access transistor selectively couples the bit line to an output of the first or second inverter, and one terminal of the first N-channel transistor is connected to the precharge line. In a preferred embodiment, a control circuit is provided that, during a writing operation, supplies data to be written to the memory cell to the bit line, supplies a pulse signal to the precharge line, and activates the word line. A method of writing data to a semiconductor memory cell that is coupled to a word line and single bit line is also provided. According to the method, the level of the bit line is set in accordance with data to be written, the memory cell is precharged so as to force the output of one of the inverters of the memory cell to a predetermined logic level, and the word line is activated to couple the bit line to the memory cell.
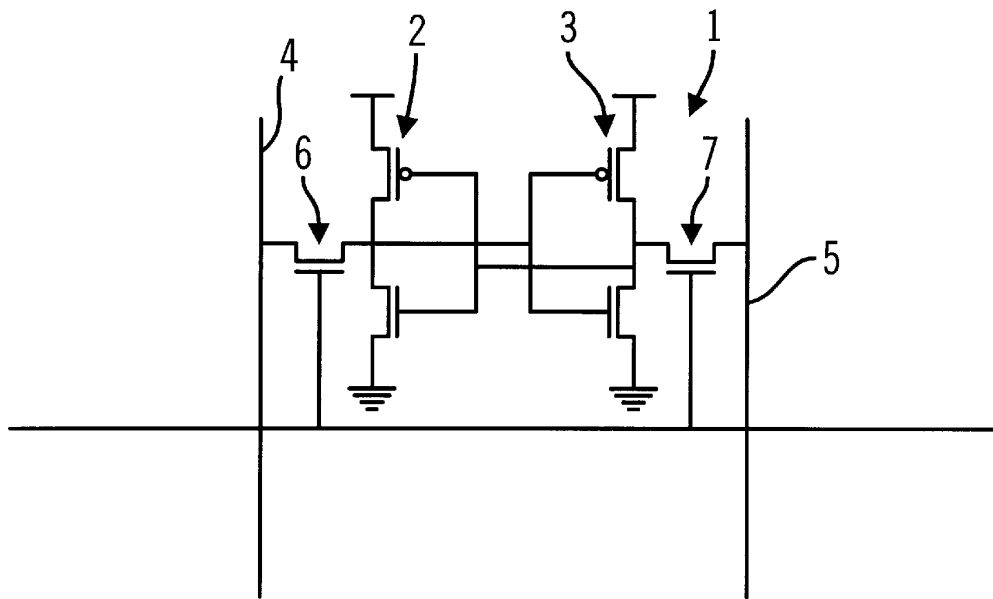
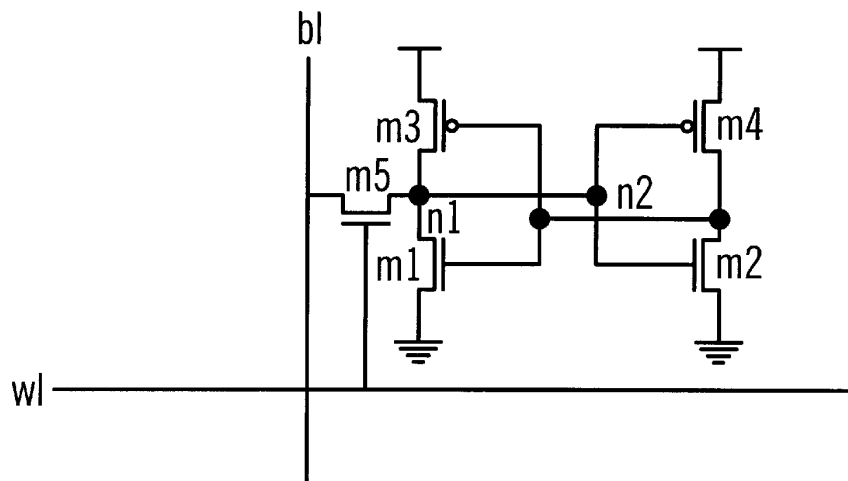**19 Claims, 3 Drawing Sheets**
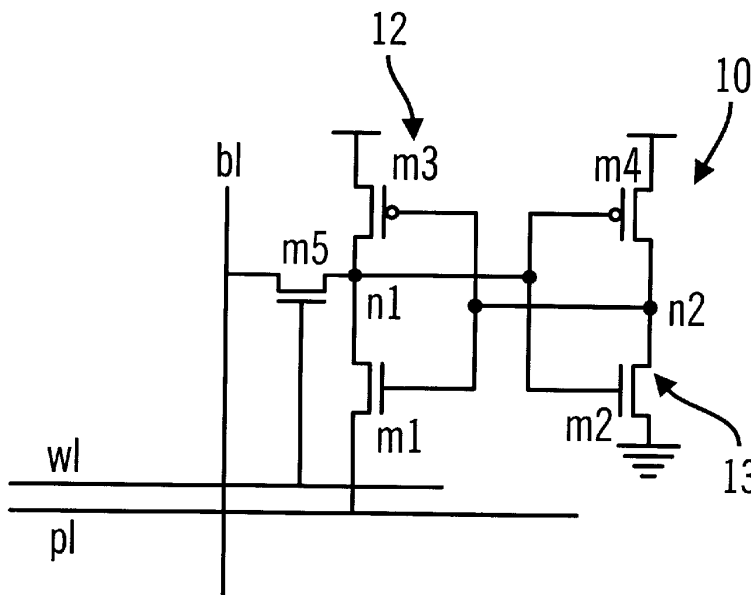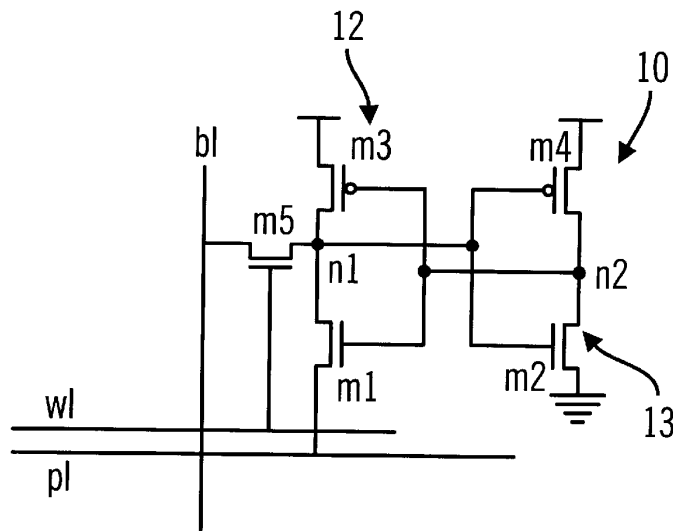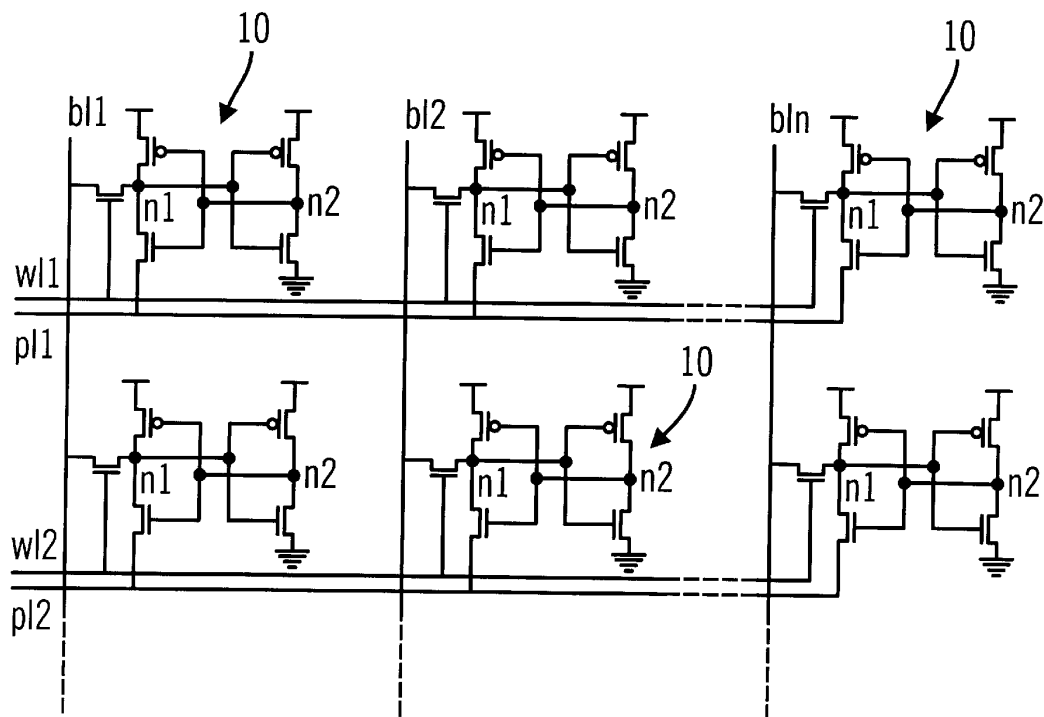
FIG. 1
PRIOR ART

FIG. 2
PRIOR ART

FIG. 3

FIG. 4

initial state: cell1 n1_1=0, cell2 n1_2=0, celln n1_n=1
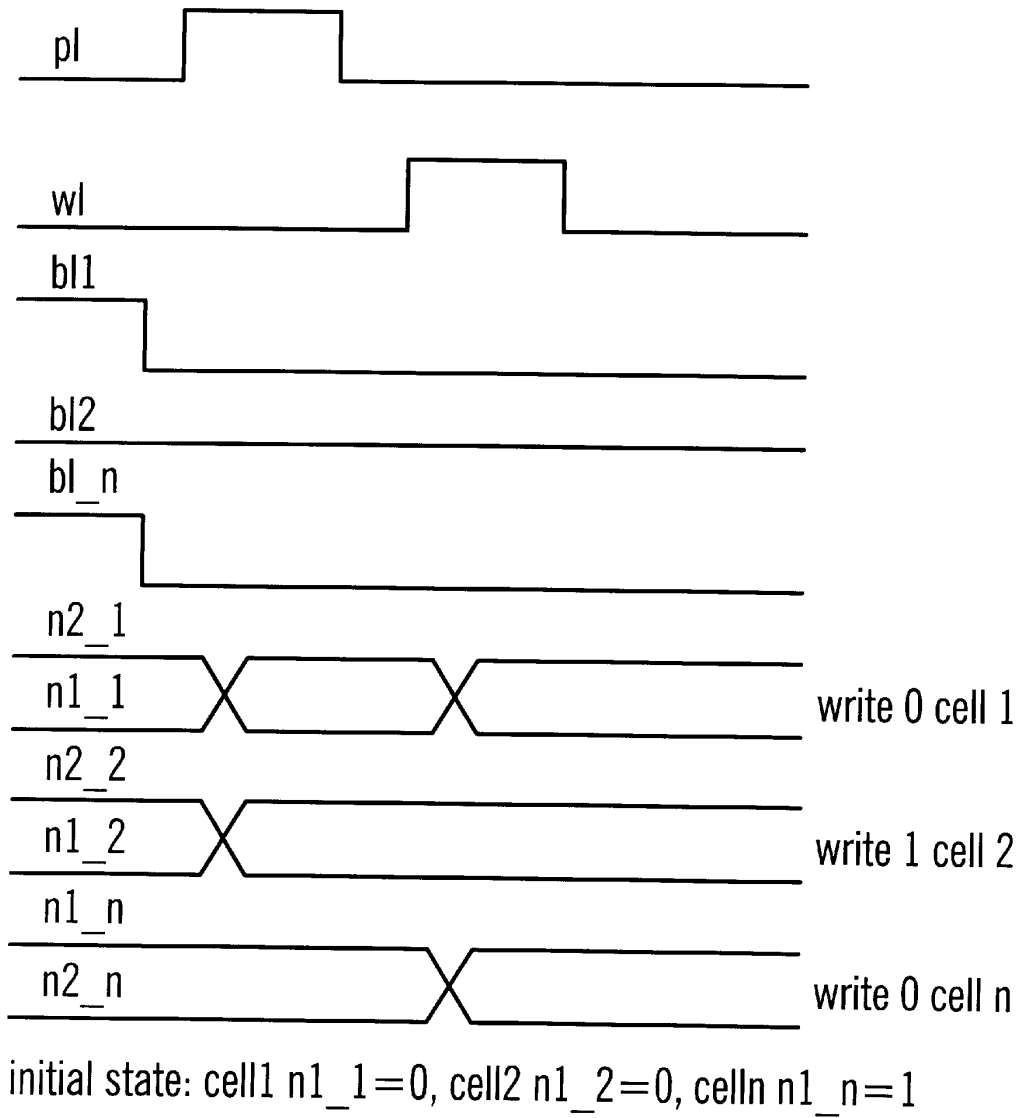
FIG. 5

LOW POWER SRAM MEMORY CELL HAVING A SINGLE BIT LINE

CROSS-REFERENCE TO RELATED APPLICATIONS

This application is based upon and claims priority from prior European Patent Application No. 97-120944.0, filed Nov. 28, 1997, the entire disclosure of which is herein incorporated by reference.

BACKGROUND OF THE INVENTION

1. Field of the Invention

The present invention relates to semiconductor memory devices, and more specifically to a low power SRAM memory cell with cross-coupled CMOS inverters coupled to a single bit line.

2. Description of the Related Art

A conventional semiconductor static random access memory (SRAM) device is formed with static memory cells that each have six transistors. FIG. **1** shows a conventional CMOS six transistor SRAM memory cell. The memory cell **1** includes a pair of cross-coupled CMOS inverters **2** and **3**, each of which is coupled to a bit line **4** and **5**. In particular, the first inverter **2** is coupled to a first bit line **4** through a bi-directional access device **6**, and the second inverter **3** is coupled to an adjacent second bit line **5** through a second access device **7**. During reading and writing operations, different voltages must be applied to the two bit lines **4** and **5**. Thus, this type of access to the storage node of the memory cell can be termed "differential."

More specifically, during reading from the memory cell of FIG. **1**, the bit line voltage swing amplitude is dependent upon the length of time the memory cell has been activated. The voltage difference caused by the swing can be kept quite small and sensed by the sense amplifier of the memory device in order to reduce power consumption. Further, during writing to the memory cell, the bit line voltage swing is made as large as possible (e.g., the full CMOS logic voltage level) in order to toggle (i.e., write to) the memory cell. Thus, in an SRAM six transistor memory cell array with m rows and n columns, the current consumption during reading and writing can be estimated using the following formulas:

$$Idd_r = n*m*Cb*\Delta V_r \tag{1}$$

$$Idd_w = m*m*Cb*\Delta V_w \tag{2}$$

where n is the number of bits in the word being read or written, Cb is the bit line capacitance associated with a given cell, ΔV_r is the bit line voltage swing during a read operation, and ΔV_w is the bit line voltage swing during a write operation. Typically, ΔV_w corresponds to the supply voltage level Vdd.

Previous efforts to reduce the power consumed by such a memory matrix focus on changing one or more of the parameters in the above formulas. One such technique is disclosed by N. Kushiyama et al. in "A 295 MHz CMOS 1M (x256) embedded SRAM using I-directional read/write shared sense amplifiers and self-timed pulsed word-line drivers" (ISSCC Dig. Tech. Papers, February 1995, pages 182–183). According to this technique, power consumption is reduced by reducing the number of cells on the bit line through a hierarchical bit line scheme.

Another power reduction technique is disclosed by B. Amrutur and H. Horowitz in "Technique to reduce power in

fast wide memories" (Dig. Tech. Papers, October 1994, Symp. on Low Power Electronics, pages 92–93). This technique reduces power consumption by limiting the bit line voltage swing during a read by controlling the word line pulse length. Yet another power reduction technique is disclosed by T. Blalock and R. Jager in "A high-speed clamped bit line current-mode sense amplifier" (IEEE J. Solid State Circuits, Vol. 26, No. 4, April 1991, pages 542–548). This solution also reduces power consumption by limiting the bit line voltage swing during a read, but does so using current-mode sense amplifiers so as to reduce ΔV_r. Still another power reduction technique limits the bit line voltage swing during a write to a predetermined value (i.e., Vdd-Vt) using NMOS transistors during precharging.

Further efforts at reducing power consumption have focused on reducing the current consumption by coupling each memory cell to a single bit line instead of the conventional bit line pair. In such devices, the lower bit line capacitance presented by the single bit line cells decreases current consumption. For example, in "A single-bit-line cross-point cell activation (SCPA) architecture for ultra-low-power SRAMs" (IEEE J. Solid State Circuits, Vol. 28, No, 11, November 1992, pages 1114–1118) M. Ukita et al. disclose a single bit line architecture that includes five transistor SRAM cells with a single bit line, as shown in FIG. **2**. Moreover, in "A source sensing technique applied to SRAM cells" (IEEE J. Solid State Circuits, Vol. 30, No. 4, April 1995, pages 500–511), K. J. O'Connor addresses the problem of writing to such a single access SRAM cell.

With such single access (i.e., single bit line) SRAM memory cells, whether or not switching occurs during a read operation is dependent upon the data stored in the memory cell being read. Because switching only occurs when one of the two possible logic values is stored in the memory cell, power consumption (over time) is reduced by one half. Similarly, during a writing operation, the bit lines are only discharged when one of the two possible logic values (e.g., "0") is to be written. Thus, the power consumption during writing (over time) is also reduced by half. Although conventional single access SRAM memory cells offer such significant reductions in power consumption, a serious drawback is presented in that it is difficult to write the other non-discharging logic value (e.g., "1") to the memory cells.

More specifically, when writing a high (1) logic level to a memory cell that is storing a low (0) logic level, the node N1 is low and a high level must be written into the memory cell. When the bit line BL is set high and the word line WL is activated, the transistors M5 and M1 fight one another. In order to make the memory cell stable during such an operation, the O'Connor reference teaches dimensioning the transistor M1 so that it is larger than the transistor M5. However, writing remains quite difficult and the proposed transistor dimension solution requires complex techniques that increase the design complexity of the memory device.

SUMMARY OF THE INVENTION

In view of these drawbacks, it is an object of the present invention to remove the above-mentioned drawbacks and to provide an SRAM memory device with reduced power consumption. An SRAM memory device is formed with memory cells that each have cross-coupled inverters coupled to a single bit line. During operation, one terminal of a pull-down transistor of a memory cell is precharged. Thus, the memory cell is precharged to a logic state that can be easily changed during writing.

In other words, the memory cell is "reset" before a writing operation. In one illustrative embodiment in which five

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