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**Dai et al.**

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(54) **REDUCING POWER CONSUMPTION OF AN ELECTRONIC DEVICE**

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(73) Assignee: **Intel Corporation**, Santa Clara, CA (US)

(\*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 0 days.

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(21) Appl. No.: **09/161,076**

(22) Filed: **Sep. 25, 1998**

(51) **Int. Cl.**<sup>7</sup> ..... **G06F 13/24**

(52) **U.S. Cl.** ..... **713/320; 713/322; 713/340**

(58) **Field of Search** ..... **710/800, 310, 710/320, 323, 324, 330, 340; 365/207; 327/538, 540, 544**

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*Primary Examiner*—Robert Beausoleil

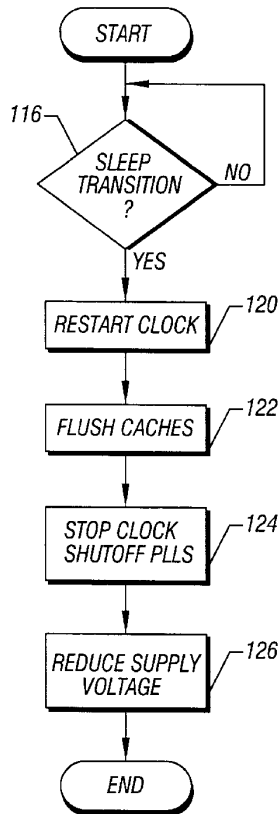
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(57) **ABSTRACT**

Leakage power consumption may be reduced in computers and other devices by providing a state where clocks are off and a low supply voltage is provided to the processor. This voltage may be sufficiently low to prevent adverse consequences while dramatically reducing leakage current. In addition, caches may be flushed to reduce the soft error rate.

**17 Claims, 4 Drawing Sheets**



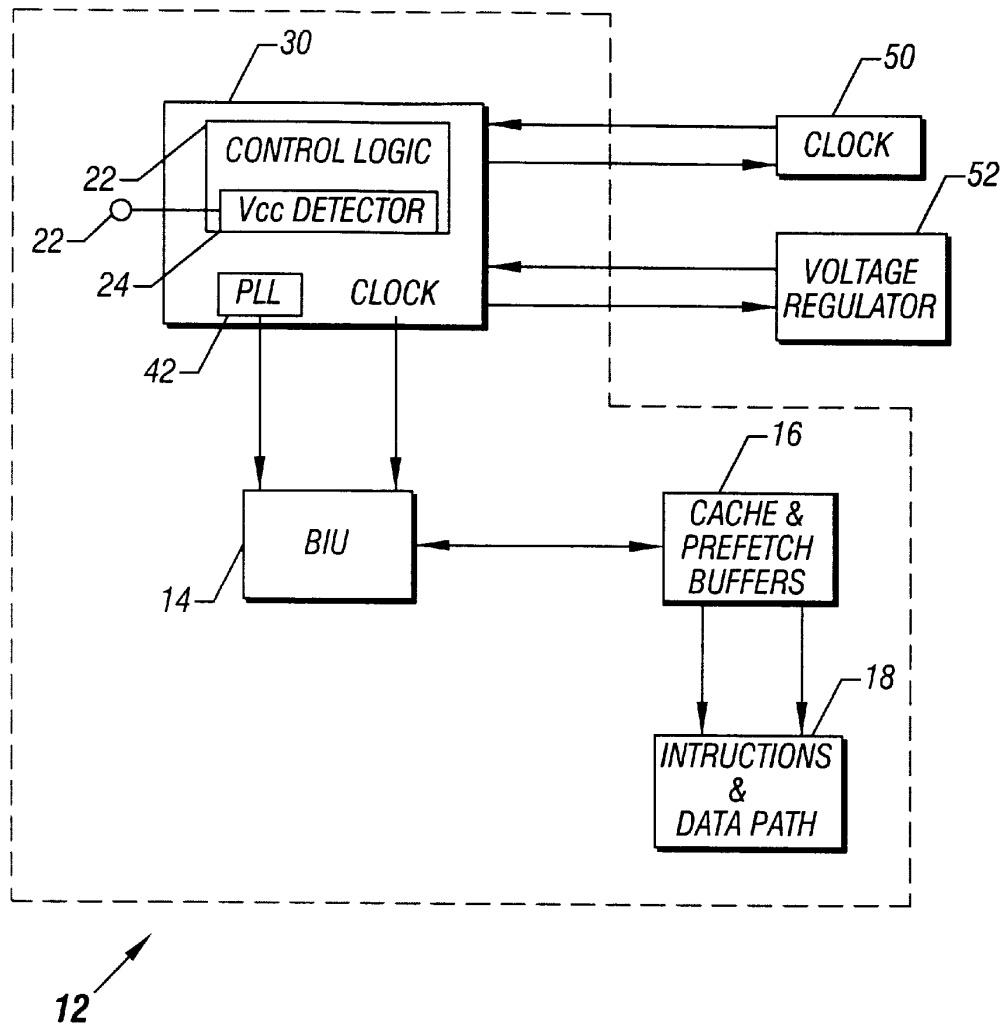


FIG. 1

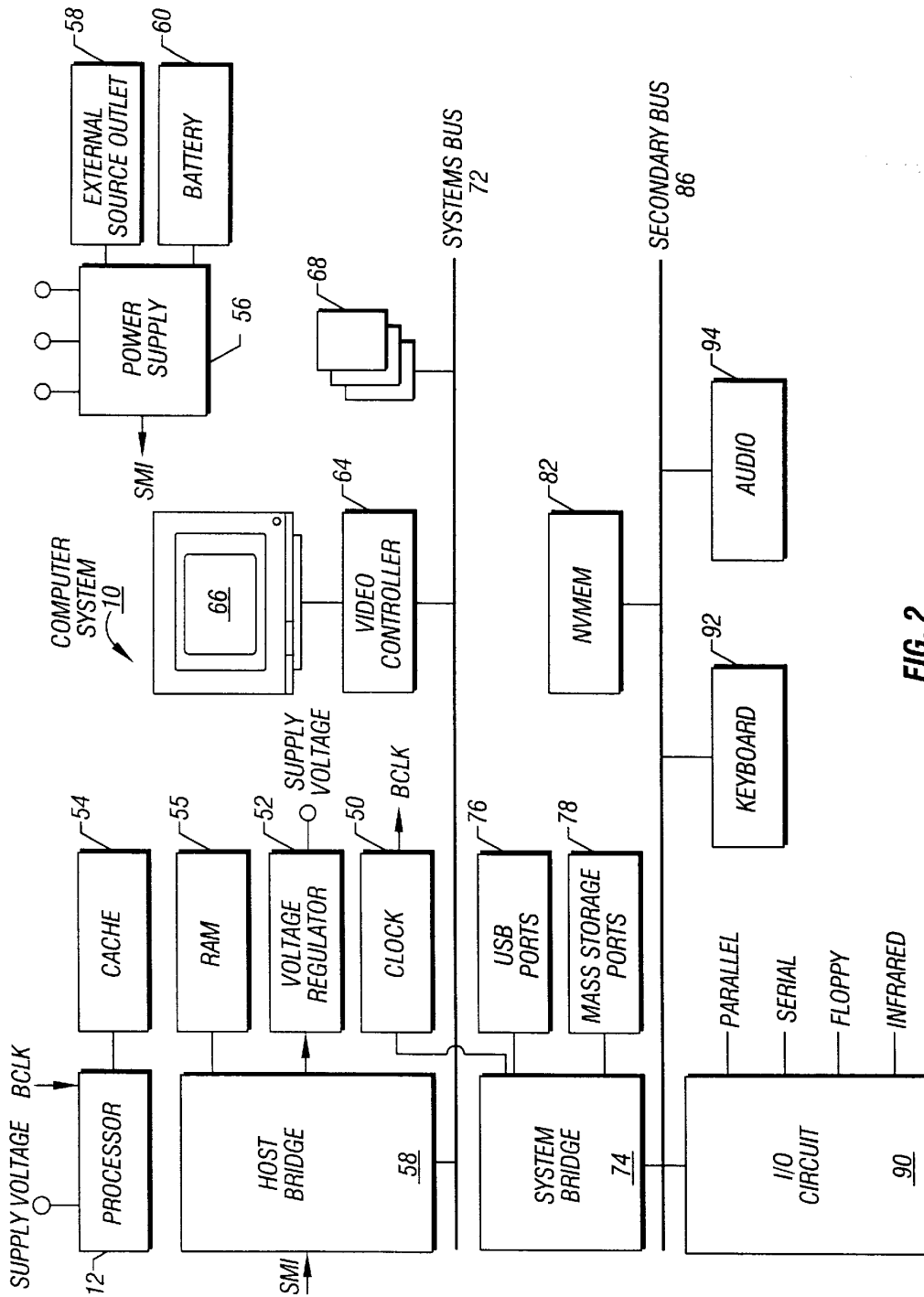


FIG. 2

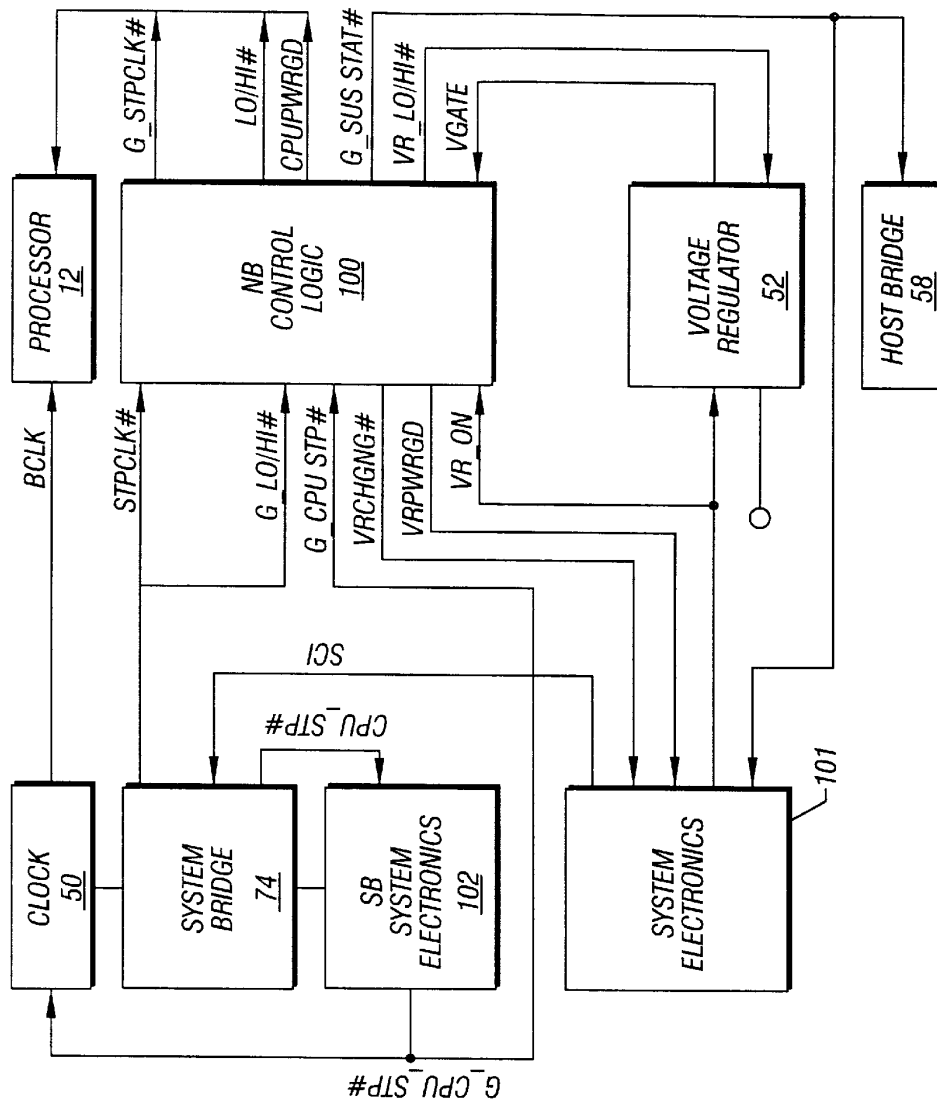


FIG. 3

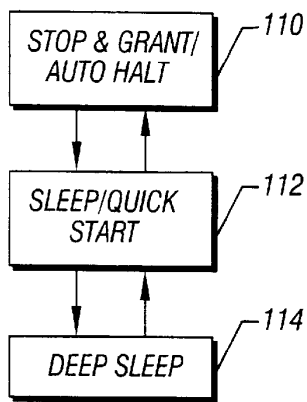


FIG. 4 (PRIOR ART)

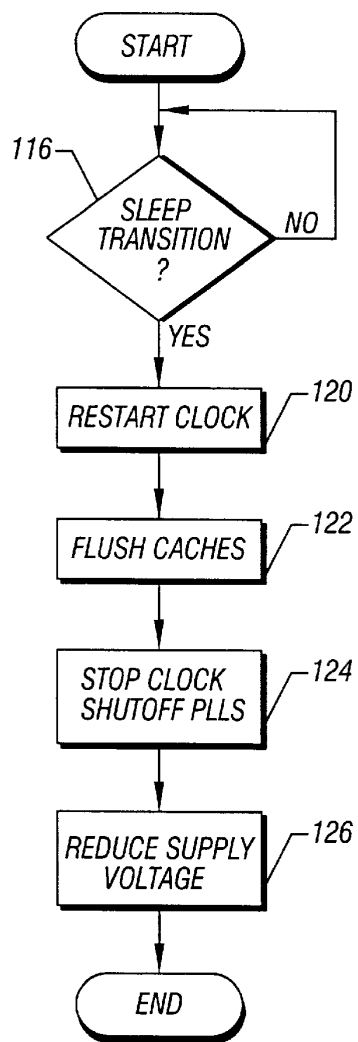


FIG. 5

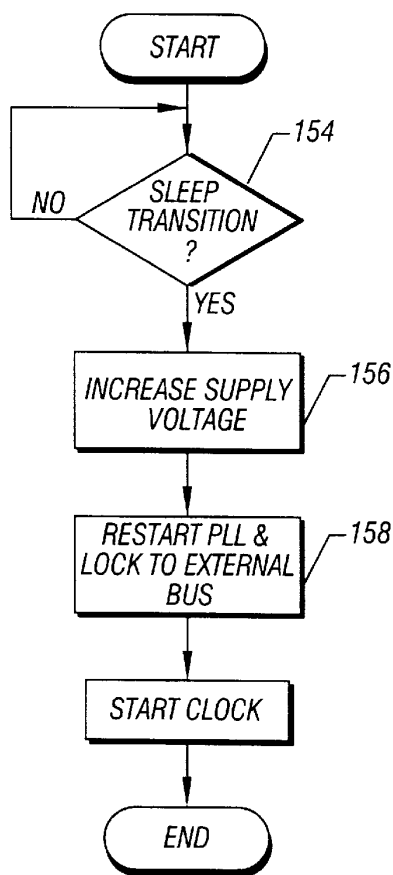


FIG. 6

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