

CMOS, the Ideal Logic Family

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INTRODUCTION

Let's talk about the characteristics of an ideal logic family. It should dissipate no power, have zero propagation delay, controlled rise and fall times, and have noise immunity equal to 50% of the logic swing.

The properties of CMOS (complementary MOS) begin to approach these ideal characteristics.

First, CMOS dissipates low power. Typically, the static power dissipation is 10 nW per gate, which is due to the flow of leakage currents. The active power depends on power supply voltage, frequency, output load, and input rise time, but typically, gate dissipation at 1 MHz with a 50 pF load is less than 10 mW.

Second, the propagation delays through CMOS are short, though not quite zero. Depending on power supply voltage, the delay through a typical gate is on the order of 25 ns to 50 ns.

Third, rise and fall times are controlled, tending to be ramps rather than step functions. Typically, rise and fall times tend to be 20 to 40% longer than the propagation delays.

Last, but not least, the noise immunity approaches 50%, being typically 45% of the full logic swing.

Besides the fact that it approaches the characteristics of an ideal logic family and besides the obvious low power battery applications, why should designers choose CMOS for new systems? The answer is cost.

On a component basis, CMOS is still more expensive than TTL. However, system level cost may be lower. The power supplies in a CMOS system will be cheaper since they can be made smaller and with less regulation. Because of lower currents, the power supply distribution system can be simpler and therefore cheaper. Fans and other cooling equipment are not needed due to the lower dissipation. Because of longer rise and fall times, the transmission of digital signals becomes simpler, making transmission techniques less expensive. Finally, there is no technical reason why CMOS prices cannot approach present day TTL prices as sales volume and manufacturing experience increase. So an engineer about to start a new design should compare the system level cost of using CMOS or some other logic family. He may find that even at today's prices, CMOS is the most economical choice.

Fairchild is building two lines of CMOS. The first is a number of parts of the CD4000A series. The second is the 54C/74C series, which Fairchild introduced and which will become the industry standard in the near future.

The 54C/74C line consists of CMOS parts which are pin and functional equivalents of many of the most popular parts in the 7400 TTL series. This line is typically 50% faster than the 4000A series and sinks 50% more current. For ease of design, it is specified at TTL levels as well as CMOS levels, and there are two temperature ranges available: 54C, -55°C to +125°C or 74C, -40°C to +85°C. Table 1 compares the port parameters of the 54C/74C CMOS line to those of the 54L/74L low power TTL line.

CHARACTERISTICS OF CMOS

The aim of this section is to give the system designer not familiar with CMOS a good feel for how it works and how it behaves in a system. Much has been written about MOS devices in general. Therefore, we will not discuss the design and fabrication of CMOS transistors and circuits.

The basic CMOS circuit is the inverter shown in Figure 1. It consists of two MOS enhancement mode transistors: the upper one a P-channel type, the lower one an N-channel type.

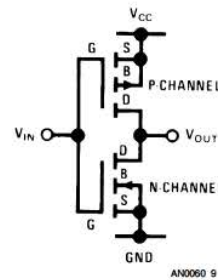


FIGURE 1. Basic CMOS Inverter

The power supplies for CMOS are called V_{DD} and V_{SS} or V_{CC} and Ground, depending on the manufacturer. V_{DD} and V_{SS} are carryovers from conventional MOS circuits and stand for the drain and source supplies. These do not apply directly to CMOS since both supplies are really source supplies. V_{CC} and Ground are carryovers from TTL logic and that nomenclature has been retained with the introduction of the 54C/74C line of CMOS. V_{CC} and Ground is the nomenclature we shall use throughout this paper.

The logic levels in a CMOS system are V_{CC} (logic "1") and Ground (logic "0"). Since "on" MOS transistor has virtually no voltage drop across it if there is no current flowing through it, and since the input impedance to CMOS device is so high (the input characteristic of an MOS transistor is essentially capacitive, looking like a $10^{12}\Omega$ resistor shunted by a 5 pF capacitor), the logic levels seen in a CMOS system will be essentially equal to the power supplies.

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TABLE 1. Comparison of 54L/74L Low Power TTL and 54C/74C CMOS Port Parameters

Family	V _{CC}	V _{IL} Max	I _{IL} Max	V _{IH} Min	I _{IH} 2.4V	V _{OL} Max	I _{OL}	V _{OH} Min	I _{OH}	t _{pd0} Typ	t _{pd1} Typ	P _{DISS} /Gate Static	P _{DISS} /Gate 1 MHz, 50 pF Load
54L/74L	5	0.7	0.18 mA	2.0	10 μA	0.3	2.0 mA	2.4	100 μA	31	35	1 mW	2.25 mW
54C/74C	5	0.8	—	3.5	—	0.4	360 μA (Note 1)	2.4	100 μA (Note 1)	60	45	0.00001 mW	1.25 mW
54C/74C	10	2.0	—	8.0	—	1.0	10 μA (Note 2)	9.0	10 μA (Note 2)	25	30	0.00003 mW	5 mW

Note 1 Assumes interfacing to low power TTL.
 Note 2 Assumes interfacing to CMOS.

Now let's look at the characteristic curves of MOS transistors to get an idea of how rise and fall times, propagation delays and power dissipation will vary with power supply voltage and capacitive loading. Figure 2 shows the characteristic curves of N channel and P channel enhancement mode transistors.

There are a number of important observations to be made from these curves. Refer to the curve of $V_{GS} = 15V$ (Gate to Source Voltage) for the N channel transistor. Note that for a constant drive voltage V_{GS} , the transistor behaves like a current source for V_{DS} s (Drain to Source Voltage) greater than $V_{GS} - V_T$ (V_T is the threshold voltage of a MOS transistor). For V_{DS} s below $V_{GS} - V_T$, the transistor behaves essentially like a resistor. Note also that for lower V_{GS} s, there are similar curves except that the magnitude of the I_{DS} s are significantly smaller and that in fact I_{DS} increases approximately as the square of increasing V_{GS} . The P channel transistor exhibits essentially identical but complemented characteristics.

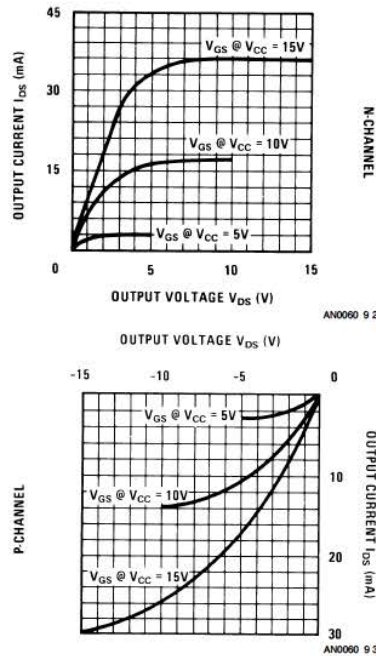


FIGURE 2. Logical "1" Output Voltage vs Source Current

If we try to drive a capacitive load with these devices, we can see that the initial voltage change across the load will be ramp like due to the current source characteristic followed by a rounding off due to the resistive characteristic dominating as V_{DS} approaches zero. Referring this to our basic CMOS inverter in Figure 1, as V_{DS} approaches zero, V_{OUT} will approach V_{CC} or Ground depending on whether the P channel or N channel transistor is conducting.

Now if we increase V_{CC} and therefore V_{GS} , the inverter must drive the capacitor through a larger voltage swing. However, for this same voltage increase, the drive capability (I_{DS}) has increased roughly as the square of V_{GS} and therefore the rise times and the propagation delays through the inverter as measured in Figure 3 have decreased.

So we can see that for a given design and therefore fixed capacitive load, increasing the power supply voltage will increase the speed of the system. Increasing V_{CC} increases speed but it also increases power dissipation. This is true for two reasons. First, CV^2f power increases. This is the power dissipated in a CMOS circuit or any other circuit for that matter when driving a capacitive load.

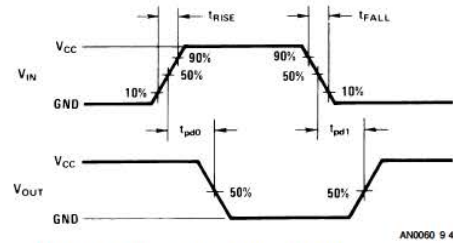


FIGURE 3. Rise and Fall Times and Propagation Delays as Measured in a CMOS System

For a given capacitive load and switching frequency, power dissipation increases as the square of the voltage change across the load.

The second reason is that the power dissipated in the CMOS circuit increases with V_{CC} (for $V_{CC}s > 2V_T$). Each time the circuit switches, a current momentarily flows from V_{CC} to Ground through both output transistors. Since the threshold voltages of the transistors do not change with increasing V_{CC} , the input voltage range through which the upper and lower transistors are conducting simultaneously increases as V_{CC} increases. At the same time, the higher V_{CC} provides higher V_{GS} voltages which also increase the magnitude of the I_{DS} currents. Incidentally, if the rise time of the input signal was zero, there would be no current flow from V_{CC} to Ground through the circuit. This current flows because the input signal has a finite rise time and therefore the input

voltage spends a finite amount of time passing through the region where both transistors conduct simultaneously. Obviously, input rise and fall times should be kept to a minimum to minimize V power dissipation.

Let's look at the transfer characteristics (Figure 5) as they vary with V_{CC} . For the purposes of this discussion we will assume that both transistors in our basic inverter have identical but complementary characteristics and threshold voltages. Assume the threshold voltages V_T to be $2V$. If V_{CC} is less than the threshold voltage of $2V$, neither transistor can ever be turned on and the circuit cannot operate. If V_{CC} is equal to the threshold voltage exactly, then we are on the curve shown on Figure 5a. We appear to have 100% hysteresis. However, it is not truly hysteresis since both output transistors are off and the output voltage is being held on the gate capacitances of succeeding circuits. If V_{CC} is somewhere between one and two threshold voltages (Figure 5b) then we have diminishing amounts of "hysteresis" as we approach V_{CC} equal to $2V_T$ (Figure 5c). At V_{CC} equal to two thresholds we have no "hysteresis" and no current flow through both the upper and lower transistors during switching. As V_{CC} exceeds two thresholds, the transfer curves begin to round off (Figure 5d). As V_{IN} passes through the region where both transistors are conducting, the currents flowing through the transistors cause voltage drops across them, giving the rounded characteristic.

Considering the subject of noise in a CMOS system, we must discuss at least two specs: noise immunity and noise margin.

Fairchild's CMOS circuits have a typical noise immunity of $0.45 V_{CC}$. This means that a spurious input which is $0.45 V_{CC}$ or less away from V_{CC} or Ground typically will not propagate through the system as an erroneous logic level. This does not mean that no signal at all will appear at the output of the first circuit; in fact, there will be an output signal as a result of the spurious input, but it will be reduced in amplitude. As this signal propagates through the system, it will

be attenuated even more by each circuit it passes through until it finally disappears. Typically, it will not change any signal to the opposite logic level. In a typical flip flop, a $0.45 V_{CC}$ spurious pulse on the clock line would not cause the flop to change state.

Fairchild also guarantees that its CMOS circuits have a 1V DC noise margin over the full power supply range and temperature range and with any combination of inputs. This is simply a variation of the noise immunity spec; only now a specific set of input and output voltages have been selected and guaranteed. Stated verbally, the spec says that for the output of a circuit to be within $0.1 V_{CC}$ volts of a proper logic level (V_{CC} or Ground), the input can be as much as $0.1 V_{CC}$ plus 1V away from power supply rail. Shown graphically, we have:

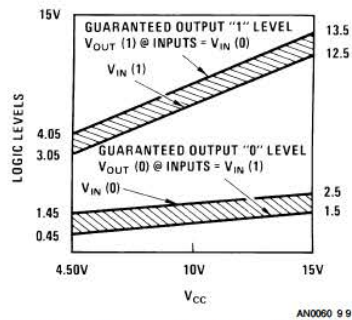


FIGURE 4. Guaranteed CMOS DC margin over temperature as a function of V_{CC} . CMOS Guarantees 1V.

This is similar in nature to the standard TTL noise margin spec which is 0.4V.

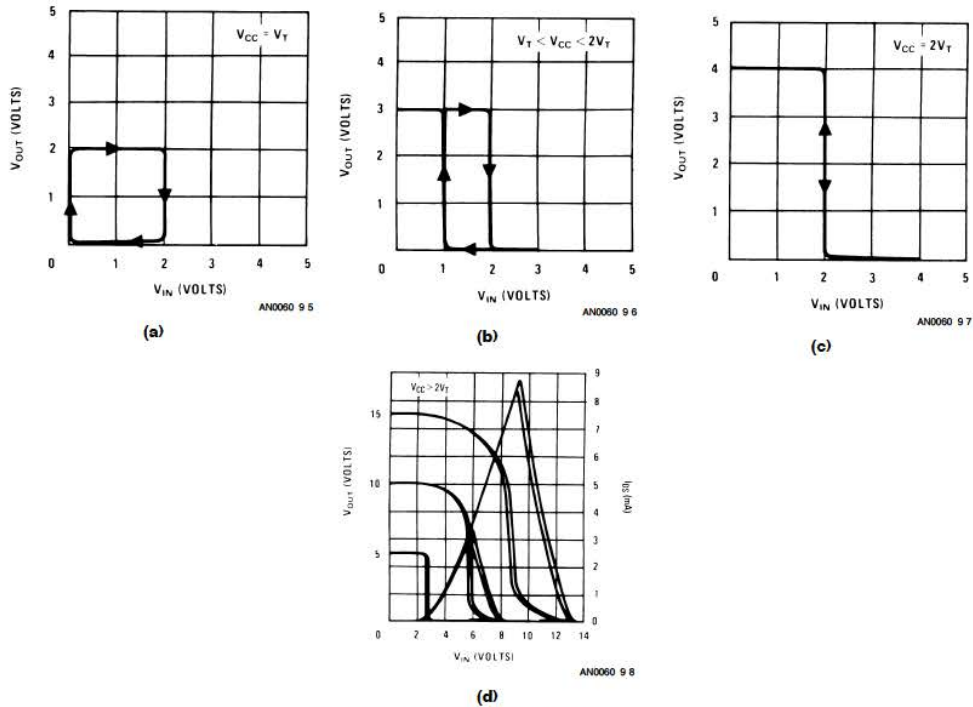


FIGURE 5. Transfer Characteristics vs V_{CC}

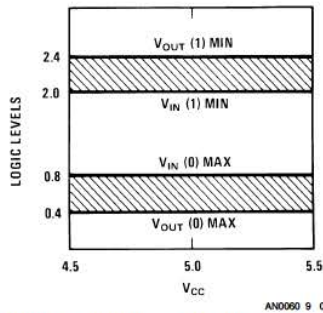


FIGURE 6. Guaranteed TTL DC margin over temperature as a function of V_{CC} .
TTL Guarantees 1V.

For a complete picture of V_{OUT} vs V_{IN} refer to the transfer characteristic curves in Figure 5

SYSTEM CONSIDERATIONS

This section describes how to handle many of the situations that arise in normal system design such as unused inputs paralleling circuits for extra drive data bussing power considerations and interfaces to other logic families

Unused inputs: Simply stated unused inputs should not be left open. Because of the very high impedance ($\sim 10^{12}\Omega$) a floating input may drift back and forth between a "0" and "1" creating some very intriguing system problems. All unused inputs should be tied to V_{CC} , Ground or another used input. The choice is not completely arbitrary however since there will be an effect on the output drive capability of the circuit in question. Take for example a four input NAND gate being used as a two input gate. The internal structure is shown in Figure 7. Let inputs A and B be the unused inputs.

If we are going to tie the unused inputs to a logic level inputs A and B would have to be tied to V_{CC} to enable the other inputs to function. That would turn on the lower A and B transistors and turn off the upper A and B transistors. At most only two of the upper transistors could ever be turned on. However if inputs A and B were tied to input C the input capacitance would triple but each time C went low the upper A, B and C transistors would turn on tripling the available source current. If input D was low also all four of the upper transistors would be on.

So tying unused NAND gate inputs to V_{CC} (Ground for NOR gates) will enable them but tying unused inputs to other used inputs guarantees an increase in source current in the case of NAND gates (sink current in the case of NOR gates)

There is no increase in drive possible through the series transistors. By using this approach a multiple input gate could be used to drive a heavy current load such as a lamp or a relay.

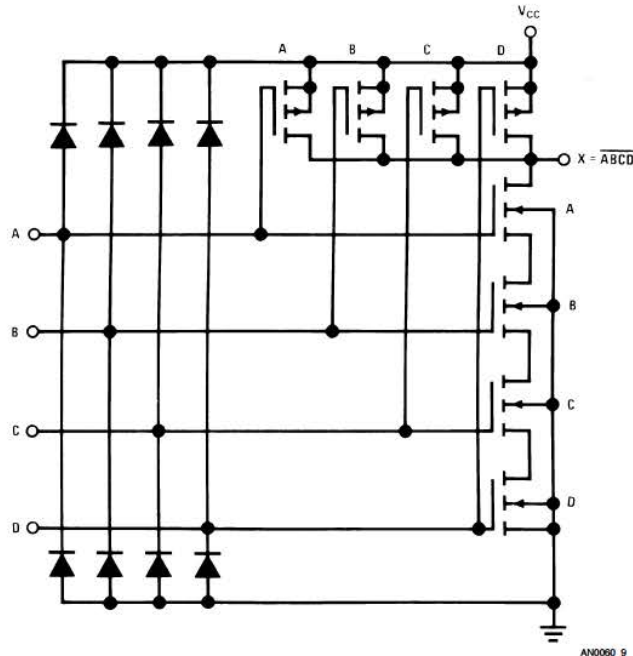


FIGURE 7. MM74C20 Four Input NAND gate

Parallel gates: Depending on the type of gate, tying inputs together guarantees an increase in either source or sink current but not both. To guarantee an increase in both currents, a number of gates must be paralleled as in Figure 8. This insures that there are a number of parallel combinations of the series string of transistors (Figure 7) thereby increasing drive in that direction also.

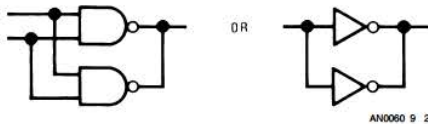


FIGURE 8. Paralleling Gates or Inverters Increases Output Drive in Both Directions.

Data bussing: There are essentially two ways to do this. First, connect ordinary CMOS parts to a bus using transfer gates (Part No. CD4016C). Second, and the preferred way, is to use parts specifically designed with a CMOS equivalent of a 3 STATE output.

Power supply filtering: Since CMOS can operate over a large range of power supply voltages (3V to 15V), the filtering necessary is minimal. The minimum power supply volt

age required will be determined by the maximum frequency of operation of the fastest element in the system (usually only a very small portion of any system operates at maximum frequency). The filtering should be designed to keep the power supply voltage somewhere between this minimum voltage and the maximum rated voltage the parts can tolerate. However, if power dissipation is to be kept to a minimum, the power supply voltage should be kept as low as possible while still meeting all speed requirements.

Minimizing system power dissipation: To minimize power consumption in a given system, it should be run at the minimum speed to do the job with the lowest possible power supply voltage. AC and DC transient power consumption both increase with frequency and power supply voltage. The AC power is described as CV^2f power. This is the power dissipated in a driver driving a capacitive load. Obviously, AC power consumption increases directly with frequency and as the square of the power supply. It also increases with capacitive load, but this is usually defined by the system and is not alterable. The DC power is the V power dissipated during switching in any CMOS device during switching; there is a momentary current path from the power supply to ground (when $V_{CC} > 2V_T$) (Figure 9).

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