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Case/Docket No. TRANS59
Express Mail No.EF338698854US

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Washington, D.C. 20231

Sir:

Transmitted herewith for filing is the patent application of:

Inventors: Andrew Read, Sameer Halepete, and Keith Klayman

For: STATIC POWER CONTROL

Enclosed are:

XXX Two (2) sheet(s) of Formal Drawing(s) including three (5) figures.
XXX An Assignment of the invention to: Transmeta Corporation on , 2000.
XXX A Declaration and Power of Attorney.
XXX A Verified Statement to establish Small Entity Status under 37 CFR 1.9 and 37 CFR 1.27.
XXX Return addressed stamped postcard.

The Filing Fee has been calculated as shown below:

	(Col. 1)	(Col.2)	SMALL ENTITY		OTHER THAN A SMALL ENTITY	
For:	No. Filed	No. Extra	RATE	FEE	RATE	FEE
Basic Fee:	-	-	-	$355.00	-	$710.00
Total Claims:	-13	-0-	x $9.00		x $18.00	-0-
Indep. Claims:	-2	-0-	x $40.00		x $80.00	-0-
☐ Multiple Dep. Claim(s) Presented			+ $135.00		+ $270.00	-0-
* If the difference in (Col. 1) is less than zero, enter "0" in (Col. 2)			Total:	$355.00	Total:	$.00

XXX A check in the amount of $355.00 is enclosed to cover the filing fee.

Respectfully submitted,

Date: Oct. 23, 2000

Stephen L. King, Reg. No. 19,180

30 Sweetbay Road
Rancho Palos Verdes, California 90275
(310) 377-5073

Express Mail No.EF338698854US

Applicant or Patentee: TRANSMETA CORPORATION Attorney's
Serial or Patent No.: _____ Docket No. TRANS59
Filed or Issued: _____

For: STATIC POWER CONTROL

VERIFIED STATEMENT (DECLARATION) CLAIMING SMALL ENTITY STATUS
37 CFR 1.9 (f) and 1.27(c) - - SMALL BUSINESS CONCERN

I hereby declare that I am an official of the small business concern empowered to act on behalf of the concern identified below:

NAME OF CONCERN: TRANSMETA CORPORATION
ADDRESS OF CONCERN: 3940 FREEDOM CIRCLE, SANTA CLARA, CALIFORNIA 95054

I hereby declare that the above identified small business concern qualifies as a small business concern as defined in 13 CFR 121.3-18, and reproduced in 37 CFR 1.9(d), for purposes of paying reduced fees under Section 41(a) and (b) of Title 35, United States Code, in that the number of employees of the concern, including those of its affiliates, does not exceed 500 persons. For purposes of this statement, (1) the number of employees of the business concern is the average over the previous fiscal year of the concern of the persons employed on a full-time, part-time or temporary basis during each of the pay periods of the fiscal year, and (2) concerns are affiliates of each other when either, directly or indirectly, one concern controls or has the power to control the other, or a third party or parties controls or has the power to control both.

I hereby certify that to the best of my knowledge and belief rights under contract or law have been conveyed to and remain with the small business concern identified above with regard to the invention entitled STATIC POWER CONTROL,

by inventor(s) Andrew Read, Sameer Halepete, and Keith Klayman,
described in

[X] the application for United States patent, the specification of which was filed on June 16, 2000, and assigned Serial No. 09/595,196,

and I have reviewed the document that evidences the conveyance of those rights. That document

[X] is being filed herewith.

If the rights held by the above-identified small business concern are not exclusive, each individual, concern or organization having rights to the invention is listed below and **no rights to the invention are held by any person, other than the inventor, who could not qualify as a small business concern under 37 CFR 1.9(d) or by any concern which would not qualify as a small business concern under 347 CFR 1.9(d) or a non-profit organization under 37 CFR 1.9(e)**. NOTE: Separate verified statements are required from each named person, concern or organization having rights to the invention averring to their status as small entities. (37 CFR 1.27)

NAME: _____
ADDRESS: _____
[____] Individual [_____] Small Business Concern [_____] Non-Profit Organization
NAME: _____
ADDRESS: _____
[____] Individual [_____] Small Business Concern [_____] Non-Profit Organization

I acknowledge the duty to file, in this application or patent, notification of any change in status resulting in loss of entitlement to small entity status prior to paying, or at the time of paying, the earliest of the issue fee or any maintenance fee due after the date on which status as a small entity is no longer appropriate. (37 CFR 1.28(b)).

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code, and that such willful false statements may jeopardize the validity of the application, any patent issuing thereon, or any patent to which this verified statement is directed.

NAME OF PERSON SIGNING: MARK ALLEN
TITLE OF PERSON OTHER THAN OWNER: PRESIDENT AND COO
ADDRESS OF PERSON SIGNING: 3940 FREEDOM WAY, SANTA CLARA, CALIFORNIA 95054
SIGNATURE: _____ DATE: _____

METHOD AND APPARATUS FOR REDUCING STATIC POWER LOSS

BACKGROUND OF THE INVENTION

Field Of The Invention

This invention relates to computer systems and, more particularly, to apparatus and methods for reducing power use by a computer system during intervals in which processing is stopped.

History Of The Prior Art

As computer processors have increased in ability, the number of transistors utilized has increased almost exponentially. This increase in circuit elements has drastically increased the power requirements of such processors. As the need of power increases, the temperature at which a computer operates increases and the battery life of portable computers decreases. The loss of battery life with modern portable computers greatly reduces the time during which the computer can function as a portable device. In fact, the power usage has become so great that even with significant reduction in the process size utilized, a plethora of techniques have been implemented to reduce power usage to maintain the efficacy of portable computers.

One of these techniques monitors the use of the various devices within the computer and disables those devices that have not been utilized for some period. Because the processor utilizes a significant amount of the power (e.g., 50%) used by a portable computer, this technique is utilized to disable the processor itself when its processing requirements are unused for some interval. In the typical case, disabling the processor is

accomplished by terminating the system clocks furnished to the processor. When processor clocks have been disabled, controlling circuitry (typically a portion of the "Southbridge" circuitry of an X86-processor-based computer) remains enabled to detect interrupts requiring processor operation. The receipt of such an interrupt causes the controlling circuitry to once again enable clocks to the processor so that the processor may take whatever steps are necessary to handle the basis of the interrupt.

The technique of disabling the processor reduces significantly the dissipation of power caused by the operation of the processor even at a low frequency. In fact, the technique works quite well; and it is estimated that with many portable computers the processor is placed in the state in which system clocks are disabled during approximately ninety percent of the operation of the computer. However, use of this technique emphasizes another aspect of power loss using advanced processors. When system clocks for a processor are disabled, the processor must remain in a state (sometimes called "deep sleep") in which it is capable of rapidly responding to interrupts. Such a state requires the application of core voltage to the various circuits. The application of this voltage generates a power dissipation referred to in this specification as "static power" usage because the processor is in its static state in which clocks are disabled. To date there has been little attention paid to this static power usage. However, the usage is very significant when a processor functions in the deep sleep mode as much as ninety percent of the time. As process technologies continue to shrink

in dimension and lower operating voltages, this static power increases due to lower threshold voltages and thinner gate oxides.

It is desirable to furnish apparatus and methods for reducing the power use of a processor in the state in which its clocks are disabled.

Summary Of The Invention

The present invention is realized by a method for reducing power utilized by a processor including the steps of determining that a processor is transitioning from a computing mode to a mode in which system clock to the processor is disabled, and reducing core voltage to the processor to a value sufficient to maintain state during the mode in which system clock is disabled.

These and other features of the invention will be better understood by reference to the detailed description which follows taken together with the drawings in which like elements are referred to by like designations throughout the several views.

Brief Description Of The Drawings

Figure 1 is a diagram illustrating current-voltage characteristics of CMOS transistor devices utilized in microprocessors.

Figure 2 is another diagram illustrating current-voltage characteristics of CMOS transistor devices utilized in microprocessors.

Figure 3 is a circuit diagram illustrating a first circuit designed in accordance with the present invention for reducing static power usage.

Figure 4 is a circuit diagram illustrating a second circuit designed in accordance with the present invention for reducing static power usage.

Figure 5 is another circuit diagram illustrating a circuit designed in accordance with the present invention for reducing static power usage.

Detailed Description

Figure 1 is a first diagram displaying a number of curves illustrating the current-voltage characteristics of CMOS transistor devices utilized in the circuits of a microprocessor. This first diagram utilizes a linear scale for both current and voltage. As may be seen, each of the curves illustrates that the drain-to-source current of a transistor is essentially nonexistent until the voltage at the gate terminal of the transistor is raised to a threshold voltage. Once the threshold voltage of the transistor is reached, drain-to-source current increases either linearly or quadratically depending on whether the transistor is in the linear region or saturation region of operation.

Although the diagram of Figure 1 appears to illustrate that current flowing below the threshold value of the gate voltage is insignificant, this is not the case in some situations. Figure 2 illustrates current versus voltage curves of the typical transistor device below the threshold voltage with the voltage being plotted on a log scale. As may be seen, current in fact flows below the threshold voltage. If a transistor functions in the state below the threshold voltage for ninety percent of computer processor operation, then this current has a significant affect on power usage by the processor.

Since a processor is not capable of computing in the mode in which its clocks are disabled, it would at first glance appear that the solution would be to terminate the application of voltage to the processor. However, as suggested above, it is necessary that the processor be maintained in a condition in which it can respond rapidly to interrupts provided by the circuitry that controls application of the system clocks. To do this, the processor must maintain state sufficient to immediately return to an operating condition. Thus, prior art processors have been provided sufficient voltage to maintain such state and to keep their transistors ready to immediately respond to interrupts. In general, this has been accomplished by maintaining the processor core voltage at the same level as the operating voltage. With most prior art processors, the core voltage used by a processor is selected by use of motherboard switches or setup software at a level sufficient to provide the highest frequency operations specified for the particular processor. For example, many processors provide 1.8 volts as a core voltage. On the other hand, the voltage required to maintain state in a deep sleep mode may be significantly less, e.g., one volt or less. Since such processors function at the same voltage whether in a computing or a deep sleep mode, a significant amount of unnecessary power may be expended. In one typical state of the art X86 processor, the power usage averages approximately one-half watt in the deep sleep state because of the leakage illustrated by the diagram of Figure 2.

The present invention reduces the voltage applied to the processor significantly below the lowest voltage normally furnished as a core voltage for the processor during the mode in which system clocks are

disabled thereby reducing the power utilized by the processor in the deep sleep state.

Figure 3 is a circuit diagram illustrating a first embodiment of the invention. In the circuit 10 illustrated, a switching voltage regulator 11 receives an input signal at a terminal 12 which determines its output voltage value. Most modern processors utilize a voltage regulator which is capable of furnishing a range of core voltages for operating transistors; a typical regulator may furnish a range of voltages between 2 and 0.925 volts from which a particular core voltage may be selected for operation. Typically, a binary signal is provided a the terminal 12 which selects the particular output voltage level to be furnished by the regulator 11; in such a case, a number of individual pins may be utilized as the terminal 12.

Recently, a new power saving technique has been utilized which dynamically adjusts both the voltage and operating frequency to a level sufficient to maintain computing operations being conducted by a processor. The technique which offers significant power savings is described in detail in U. S. Patent application Serial No. 09/484,516, filed January 18, 2000, entitled Adaptive Power Control, assigned to the assignee of the present invention. A processor which utilizes this technique monitors operations within the processor to determine the frequency level at which the processor should operate. Depending on the particular operations being carried out by the processor, the value furnished at the terminal 12 of a regulator functioning in such a system will cause the regulator to produce an output voltage at some level

between the high and low values necessary for the particular processor to carry out computing functions.

In the circuit of Figure 3, input to the terminal 12 is furnished via a circuit 13 such as a multiplexor that is capable of providing one or more input values. In the embodiment illustrated, a value is provided at a first input 14 to the circuit 13 by the processor (or other circuitry) which determines the operating condition of the processor in its computing range; and a second value is provided at a second input 15 which is selected especially for the deep sleep condition. Either of these input values may be selected by a control signal provided at a control terminal 16 of the circuit 13. In one embodiment, a system control signal normally utilized to signal entry into the deep sleep condition (a stop clock signal) is used as the control signal to be furnished at the control terminal 16. This control signal selects the input value furnished at the input 15 which is especially chosen to cause a typical prior art regulator 11 to produce a voltage output for operating the processor in the deep sleep mode. In one embodiment of the invention, the value furnished for deep sleep mode is chosen to cause the regulator 11 to produce the lowest voltage possible in its range of output voltages. In one exemplary processor that utilizes the technique described in the above-mentioned patent application, the processor is specified as capable of conducting computing operations in a core voltage range from a low voltage of 1.2 volts to a high voltage of 1.6 volts. On the other hand, the processor when operating in deep sleep mode has no problem maintaining that state necessary to resume computing even though functioning at a core voltage of 0.925 volts, the lowest voltage which the regulator can provide.

Thus, although the voltage regulator 11 may typically provide a range of varying output voltage levels, the lowest voltage at which a processor is specified for conducting computing operations is typically significantly above the lowest value which the regulator is capable of furnishing.

In order to reduce power usage in one embodiment of the present invention, in response to a control signal indicating that the processor is about to go into the deep sleep state, the value at the input 15 is furnished by the circuit 13 to the regulator causing the regulator 11 to generate its lowest possible output voltage level for the deep sleep condition. In one exemplary embodiment, the high and low voltages generated in a computing mode are 1.6 volts and 1.2 volts while the deep sleep voltage is 0.925 volts.

Although the voltage level furnished by the regulator 11 for the deep sleep mode of the processor might appear to be only slightly lower than that furnished in the lowest operating condition for the exemplary processor, the reduction in power usage is quite significant. Because both the voltage and the leakage current are reduced, the reduction in power is approximately equal to the ratio in voltage levels raised to the power of about three to four. Over any period of processor use involving the deep sleep state, such a reduction is quite large.

One problem with this approach to reducing power is that it does not reduce the voltage level as far as might be possible and, thus, does not conserve as much power as could be saved. This approach only reduces the voltage level to the lowest level furnished by the regulator. This voltage is significantly greater than appears to be necessary for a

processor which also dynamically regulates voltage furnished during computing operations to save power. Two criteria control the level to which the core voltage may be reduced in deep sleep. The level must be sufficient to maintain state that the processor requires to function after returning from the deep sleep state. The level must be one that can be reached during the times allowed for transition to and from the deep sleep mode.

The first criterion is met so long as values of state stored are not lost during the deep sleep mode. Tests have shown that a core voltage significantly below one-half volt allows the retention of the memory state of a processor. Thus, using this criterion, it would be desirable to reduce the core voltage to a value such as one-half volt or lower.

However, depending on system configuration, the time allowed to transition to and from deep sleep in an X86 processor can be as low as 50 microseconds. Depending on the capacitive load of the particular circuitry, a voltage variation of about 0.5 to 0.6 volts may take place during this time in one exemplary configuration.

Thus, if the exemplary processor is operating at its lowest processing core voltage of 1.2 volts, its core voltage may be lowered in the time available to 0.6 - 0.7 volts. On the other hand, if the processor is operating at a processing core voltage of 1.5 volts, its core voltage may only be lowered in the time available to 0.9 - 1 volts. Consequently, it is desirable that the core voltage furnished during deep sleep be lowered to a level which may be below the level provided by a typical voltage

regulator but which varies depending on the core operating voltage from which it transitions.

This desirable result may be reached utilizing a circuit such as that described in Figure 4. The circuit of Figure 4 includes a feedback network 41 for controlling the level of voltage at the output of the regulator 11. Prior art regulators such as the Maxim 1711 provide a feedback terminal and describe how that terminal may be utilized with a resistor-voltage-divider network joined between the output terminal and ground to raise the output voltage level.

The embodiment of the present invention illustrated in Figure 4 utilizes the same feedback terminal and a similar resistor-voltage-divider network but joins the divider between the output terminal and a source of voltage 42 higher than the normal output voltage of the regulator to force the output voltage level to a lower value rather than a higher level. The particular source voltage and the particular resistor values may be selected to cause the voltage level at the output of the regulator to drop from a particular output value to a desired value such as 0.6 volts when transitioning from a computing level of 1.2 volts.

By appropriate choice of the resistor values of the divider network 41 and the source 42, the voltage drop provided by such a divider network accomplishes the desired result of providing an output voltage for the deep sleep mode of operation that varies from the previous processor computing core voltage by an amount attainable during the transition period available. In one embodiment, resistor 43 was chosen to be 1 Kohms, resistor 45 to be 2.7 Kohms, and source 42 to be 3.3 volts. Such

values cause the voltage drop into deep sleep mode to be between 0.5 and 0.6 volts whether beginning at core voltages of 1.2 or 1.6 volts. On the other hand, by using a higher value of voltage at source 45 and adjusting the values of resistors 41 and 43, the increments of voltage drop reached from different starting voltages to final deep sleep voltage values at the terminal 12 may be brought closer to one another.

It should be noted that the circuitry of Figures 3 and 4 may be combined so that both input selection and output adjustment are both used to adjust the core voltage value produced by a voltage regulator for deep sleep mode in particular instances where the load capacitance is relatively low.

Prior art voltage regulators function in at least two different modes of operation. A first mode of operation is often referred to as "low noise" or "continuous" mode. In this mode, the regulator responds as rapidly as possible to each change in voltage thereby maintaining the output voltage at the desired output level as accurately as possible. In order to maintain this mode of rapid response, regulators consume a certain amount of power. When a regulator is supplying a significant amount of power to the load, the power required to operate in continuous mode is relatively small. But, when a regulator is supplying a small amount of power to the load, the power used to operate the regulator in continuous mode becomes significant, and reduces the efficiency of the regulator significantly. It is common for regulators operating in the continuous mode to transfer charge from the supply capacitors back into the power source when the output voltage is changed from a higher voltage to a

lower voltage. The regulator can later transfer that charge back to the regulator output capacitors. Thus, most of the charge is not wasted.

A second mode of operation by voltage regulators is often referred to as "high efficiency," "burst," or "skip" mode. In this mode, a regulator detects the reduction in load requirements (such as that caused by a transition into the deep sleep state) and switches to a mode whereby the regulator corrects the output voltage less frequently. When there is an increase in load requirements, the regulator switches back to the continuous mode of regulation during which more rapid correction occurs. This has the positive effect of reducing the power consumed by the regulator during deep sleep thereby increasing the regulator efficiency and saving system power. But, as a result of reducing the regulator response rate, there is more noise on the regulator output.

It is common for regulators operating in the high efficiency mode to drain the charge on the supply capacitors during a high to low voltage transition on the power supply output or to allow the load to drain the charge. Thus, the charge is wasted during high to low voltage transitions.

It is typical to operate a voltage regulator in the high efficiency mode. Consequently, there is some waste of power whenever a regulated processor goes into the lower voltage deep sleep mode. If the processor is constantly being placed in deep sleep mode, then the loss of power may be quite high. Different operating systems may increase the waste of power by their operations. For example, an operating system that detects changes in operation through a polling process must constantly

bring a processor out of deep sleep to determine whether a change in operating mode should be implemented. For many such systems, such a system causes an inordinate amount of power waste if a processor would otherwise spend long periods in the deep sleep mode. On the other hand, an operating system that remains in deep sleep until an externally-generated interrupt brings it out of that state wastes power through operating the regulator in the high efficiency mode only when the processor is placed in the deep sleep state.

The present invention utilizes the ability of regulators to function in both the high efficiency mode and the continuous mode to substantially reduce power wasted by transitioning between a computing and a lower voltage deep sleep mode. Although regulators have not been dynamically switched between high efficiency and continuous modes, in one embodiment of the invention, an additional controlling input 50 as shown in Figure 5 is added to the regulator for selecting the mode of operation of the regulator based on whether the processor being regulated is transitioning between states. If the regulator receives a control signal 51 indicating that the processor is to be placed into the deep sleep mode, for example, then a regulator operating in the high efficiency mode immediately switches to the continuous mode during the voltage transition. Assuming that the regulator returns the charge to the battery during continuous mode, this has the effect of reducing the waste of power caused during the transition. Once the transition has completed, the regulator switches back to the high efficiency state for operation during the deep sleep mode of the processor.

For regulators that do not conserve capacitive charge by transferring the charge to the battery, a circuit for accomplishing this may be implemented or a capacitor storage arrangement such as a charge pump 53 for storage may be added. Alternatively, when transitioning to deep sleep, the regulator could switch to a mode where the regulator does not actively drive the voltage low but allows the capacitor charge to drain through the load. The selection of power savings modes is dependent on the processor leakage current, the voltage drop between the operating and deep sleep voltages, and the efficiency of the regulator in transferring charge from the capacitors to the power source and then back. If the leakage current is not sufficient to bring the voltage down more than (1 – efficiency) * (deep sleep voltage drop) during the deep sleep interval, then it is more advantageous to use the load to drain the charge on the capacitors. Otherwise, the charge on the capacitors should be transferred back to the power source.

The control signal utilized may be the same control signal (stop clocks) that signals the transition into the deep sleep state if the method is to be used only for transitions between operating and deep sleep states. Alternatively, a control signal generated by a particular increment of desired change may be utilized for voltage changes within the computing range of the processor as well as the transition to deep sleep mode.

Although the present invention has been described in terms of a preferred embodiment, it will be appreciated that various modifications and alterations might be made by those skilled in the art without departing from the spirit and scope of the invention. The invention should therefore be measured in terms of the claims which follow.

What Is Claimed Is:

Claim 1. A method for reducing power utilized by a processor comprising the steps of:

determining that a processor is transitioning from a computing mode to a mode is which system clock to the processor is disabled, and

reducing core voltage to the processor to a value sufficient to maintain state during the mode in which system clock is disabled.

Claim 2. A method as claimed in Claim 1 in which the step of determining that a processor is transitioning from a computing mode to a mode is which system clock to the processor is disabled comprising monitoring a stop clock signal.

Claim 3. A method as claimed in Claim 1 in which the step of reducing core voltage to the processor to a value sufficient to maintain state during the state in which system clock is disabled comprises furnishing an input to reduce an output voltage provided by a voltage regulator furnishing core voltage to the processor.

Claim 4. A method as claimed in Claim 3 in which the step of reducing core voltage to the processor to a value sufficient to maintain state during the state in which system clock is disabled further comprises providing a feedback signal to the voltage regulator to reduce its output voltage below a specified output voltage.

Claim 5. A method as claimed in Claim 1 further comprising the steps of transferring operation of a voltage regulator furnishing core voltage in

a mode in which power is dissipated during reductions in core voltage to a mode in which power is saved during a voltage transition when it is determined that a processor is transitioning from a computing mode to a mode is which system clock to the processor is disabled.

Claim 6. A method as claimed in Claim 5 further comprising the steps of returning the voltage regulator to its original mode of operation when the lower value of the core voltage is reached.

Claim 7. A circuit for providing a regulated voltage to a processor comprising:

a voltage regulator having:

an output terminal providing a selectable voltage, and

an input terminal for receiving signals indicating the selectable voltage level;

means for providing signals at the input terminal of the voltage regulator for selecting a voltage for operating the processor in a computing mode and a voltage of a level less than that for operating the processor in a computing mode.

Claim 8. A circuit as claimed in Claim 7 in which the means for providing signals at the input terminal of the voltage regulator comprises means for accepting binary signals indicating different levels of voltage.

Claim 9. A circuit as claimed in Claim 7 in which the means for providing signals at the input terminal of the voltage regulator comprises:

selection circuitry,

means for furnishing a plurality of signals at the input to the selection circuitry, and

means for controlling the selection by the selection circuitry.

Claim 10. A circuit as claimed in Claim 9 in which:

the selection circuitry is a multiplexor, and

the means for controlling the selection by the selection circuitry includes a control terminal for receiving signals indicating a system clock to the processor is being terminated.

Claim 11. A circuit as claimed in Claim 7 further comprising means for reducing the selectable voltage below a level provided by the voltage regulator.

Claim 12. A circuit as claimed in Claim 11 in which the means for reducing the selectable voltage below a level provided by the voltage regulator comprises:

a voltage divider network joined between the output terminal and a voltage source furnishing a value higher than the selectable voltage, and

a voltage regulator feedback circuit receiving a value from the voltage divider network.

Claim 13. A circuit as claimed in Claim 7 further comprising:

circuitry for conserving charge stored by the voltage regulator when the selectable voltage decreases, and

means for enabling the circuitry for conserving charge stored by the voltage regulator when the selectable voltage decreases.

Abstract of the Disclosure:

A method for reducing power utilized by a processor including the steps of determining that a processor is transitioning from a computing mode to a mode is which system clock to the processor is disabled, and reducing core voltage to the processor to a value sufficient to maintain state during the mode in which system clock is disabled.

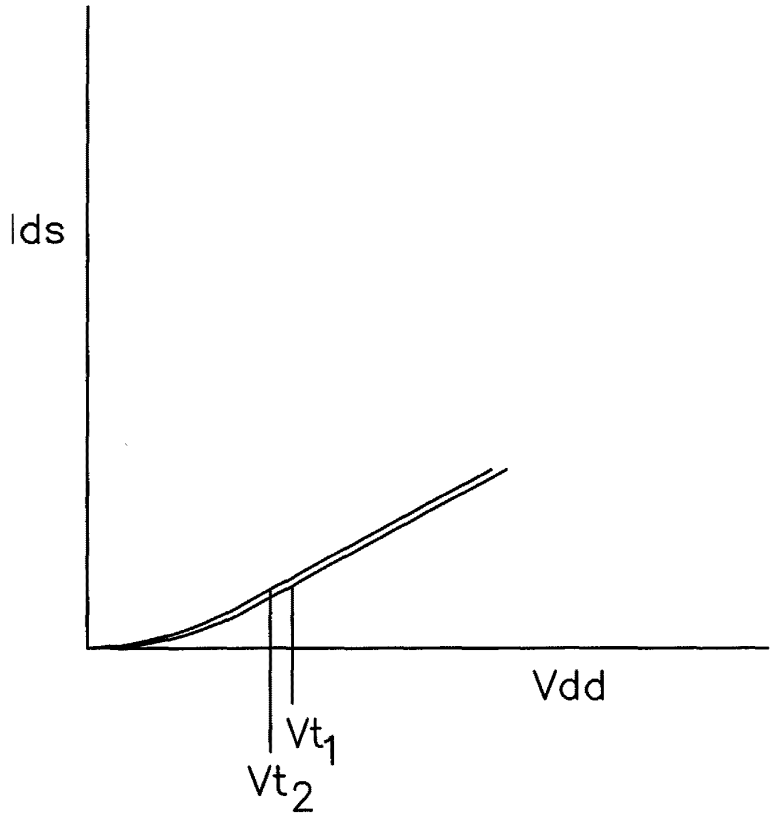


Figure 1

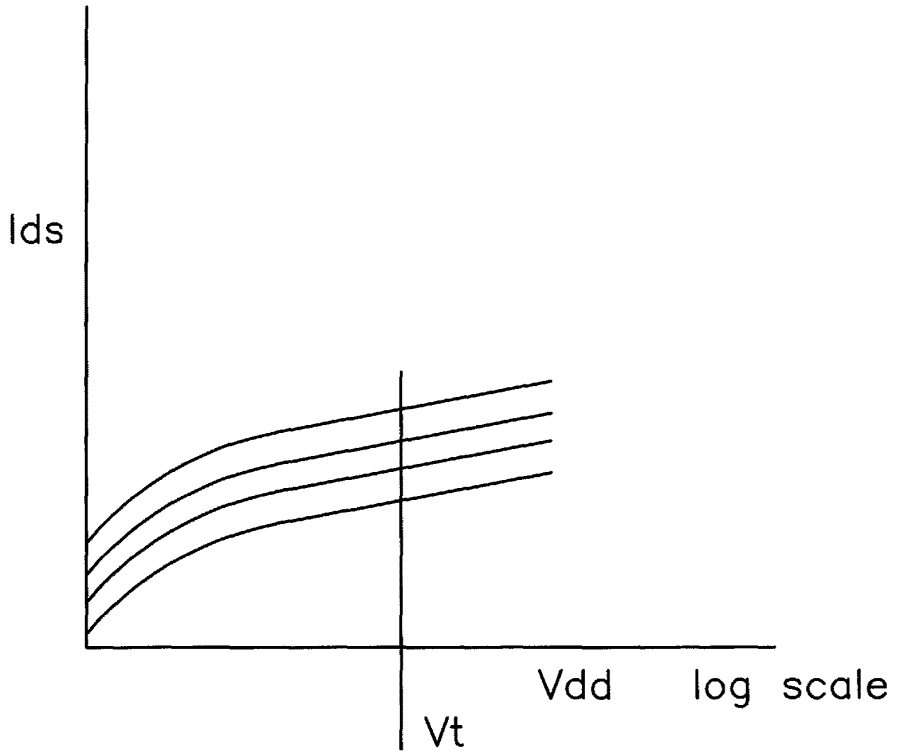


Figure 2

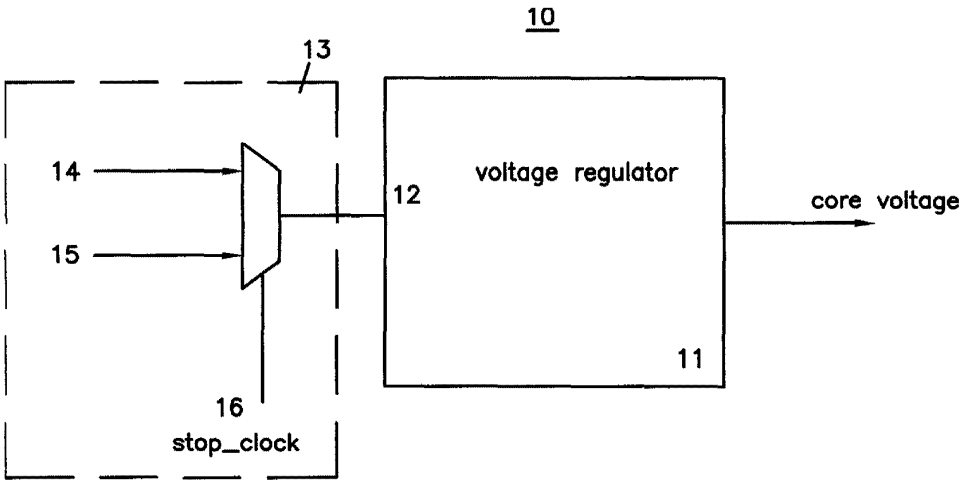


Figure 3

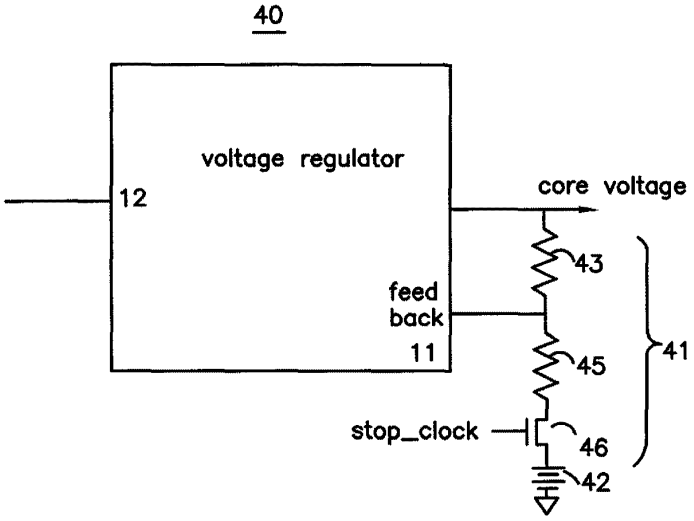


Figure 4

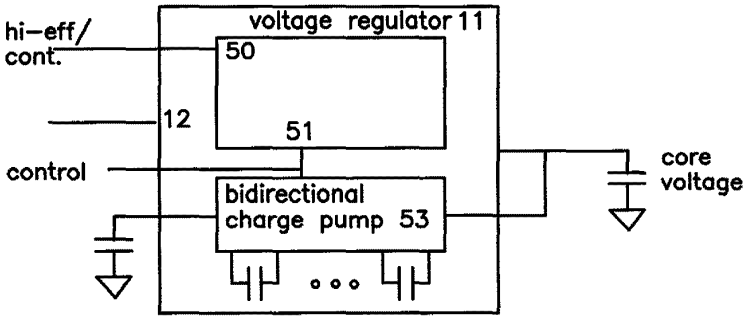


Figure 5

Attorney's Docket No.: Trans59 Patent

DECLARATION AND POWER OF ATTORNEY FOR PATENT APPLICATION

As a below named inventor, I hereby declare that:

My residence, post office address and citizenship are as stated below, next to my name.

I believe I am the original, first, and sole inventor (if only one name is listed below) or an original, first, and joint inventor (if plural names are listed below) of the subject matter which is claimed and for which a patent is sought on the invention entitled

STATIC POWER CONTROL

the specification of which is attached hereto.

I hereby state that I have reviewed and understand the contents of the above-identified specification, including the claim(s), as amended by any amendment referred to above. I do not know and do not believe that the claimed invention was ever known or used in the United States of America before my invention thereof, or patented or described in any printed publication in any country before my invention thereof or more than one year prior to this application, that the same was not in public use or on sale in the United States of America more than one year prior to this application, and that the invention has not been patented or made the subject of an inventor's certificate issued before the date of this application in any country foreign to the United States of America on an application filed by me or my legal representatives or assigns more than twelve months (for a utility patent application) or six months (for a design patent application) prior to this application.

I acknowledge the duty to disclose all information known to me to be material to patentability as defined in Title 37, Code of Federal Regulations, Section 1.56.

I hereby appoint Stephen L. King, Reg. No. 19,180; with offices located at 30 Sweetbay Road, Rancho Palos Verdes, California 90275, telephone (310) 377-5073, with full power of substitution and revocation, to prosecute this application and to transact all business in the Patent and Trademark Office connected herewith.

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of

Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

Full Name of Sole/First Inventor Andrew Read

Inventor's Signature _____ Date _____

Residence Sunnyvale, California (City, State) Citizenship U.S.A. (Country)

Post Office Address: 1621 Eagle Drive
Sunnyvale, California 94087

Full Name of Second/Joint Inventor Sameer Halepete

Inventor's Signature _____ Date _____

Residence San Jose, California (City, State) Citizenship India (Country)

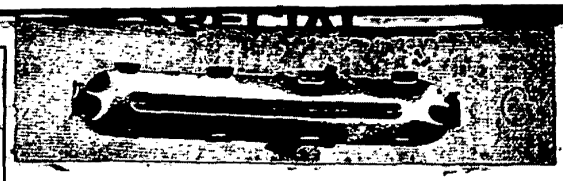
Post Office Address: 373 River Oaks Circle, #1608
San Jose California 95134

Full Name of Third/Joint Inventor Keith Klayman

Inventor's Signature _____ Date _____

Residence Sunnyvale, California (City, State) Citizenship U.S.A. (Country)

Post Office Address: 613 San Conradoter #2
Sunnyvale, California 94086



PATENT NUMBER

ISSUE CLASSIFICATION	Class	Subclass

09/694433 U.S. PTO 10/25/00

U.S. UTILITY Patent Application

O.I.P.E.	PATENT DATE
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APPLICATION NO.	CONT/PRIOR	CLASS	SUBCLASS	ART UNIT	EXAMINER
09/694433		713		2188	

2185

APPLICANTS: Andrew Read
Samser Haleplte
Keith Kiwmer

TITLE: Method and apparatus for reducing static power loss

PTO-2040
12/99

ISSUING CLASSIFICATION

ORIGINAL		CROSS REFERENCE(S)	
CLASS	SUBCLASS	CLASS	SUBCLASS (ONE SUBCLASS PER BLOCK)

INTERNATIONAL CLASSIFICATION

☐ Continued on Issue Slip Inside File Jacket

☐ TERMINAL DISCLAIMER	DRAWINGS			CLAIMS ALLOWED	
	Sheets Drwg.	Figs. Drwg.	Print Fig.	Total Claims	Print Claim for O.G.

☐ The term of this patent subsequent to _____ (date) has been disclaimed.

☐ The term of this patent shall not extend beyond the expiration date of U.S Patent. No. _____

☐ The terminal ____ months of this patent have been disclaimed.

(Assistant Examiner) (Date)

(Primary Examiner) (Date)

(Legal Instruments Examiner) (Date)

NOTICE OF ALLOWANCE MAILED

ISSUE FEE

Amount Due	Date Paid

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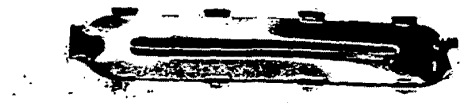

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SEARCHED

Class	Sub.	Date	Exmr.
713	320 322 323 324	7/27/03	cc
327	44 45 99		
363	16 24		
completed all		9/12/04	cc

INTERFERENCE SEARCHED

Class	Sub.	Date	Exmr.

SEARCH NOTES (INCLUDING SEARCH STRATEGY)

	Date	Exmr.
Inventor search	7/26/03	cc
East search		
IEEE search	7/27/03	cc
NPL		
East search	9/3/04	cc

RA 12/18/00

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ISSUE SLIP STAPLE AREA (for additional cross references)

POSITION	INITIALS	ID NO.	DATE
FEE DETERMINATION			
O.I.P.E. CLASSIFIER		21	11/1/00
FORMALITY REVIEW	TM	JCB64	12/15/0
RESPONSE FORMALITY REVIEW	[illegible]	1030	4-16-01

INDEX OF CLAIMS

✓ .... Rejected
= .... Allowed
— (Through numeral)... Canceled
÷ .... Restricted
N .... Non-elected
I .... Interference
A .... Appeal
O .... Objected

Claim Final	Claim Original	Date 7/2/03	Date 4/13/04	Date	Date	Date	Date	Date	Date	Date	Date
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Case/Docket No. TRANS59
Express Mail No.EF338698854US

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Sir:

Transmitted herewith for filing is the patent application of:

Inventors: Andrew Read, Sameer Halepete, and Keith Klayman

For: STATIC POWER CONTROL

Enclosed are:

XXX Two (2) sheet(s) of Formal Drawing(s) including three (5) figures.
XXX An Assignment of the invention to: Transmeta Corporation on , 2000.
XXX A Declaration and Power of Attorney.
XXX A Verified Statement to establish Small Entity Status under 37 CFR 1.9 and 37 CFR 1.27.
XXX Return addressed stamped postcard.

The Filing Fee has been calculated as shown below:

	(Col. 1)	(Col.2)	SMALL ENTITY		OTHER THAN A SMALL ENTITY	
For:	No. Filed	No. Extra	RATE	FEE	RATE	FEE
Basic Fee:	-	-	-	$355.00	-	$710.00
Total Claims:	-13	-0-	x $9.00		x $18.00	-0-
Indep. Claims:	-2	-0-	x $40.00		x $80.00	-0-
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Respectfully submitted,

Date: Oct. 23, 2000

Stephen L. King, Reg. No. 19,180

30 Sweetbay Road
Rancho Palos Verdes, California 90275
(310) 377-5073

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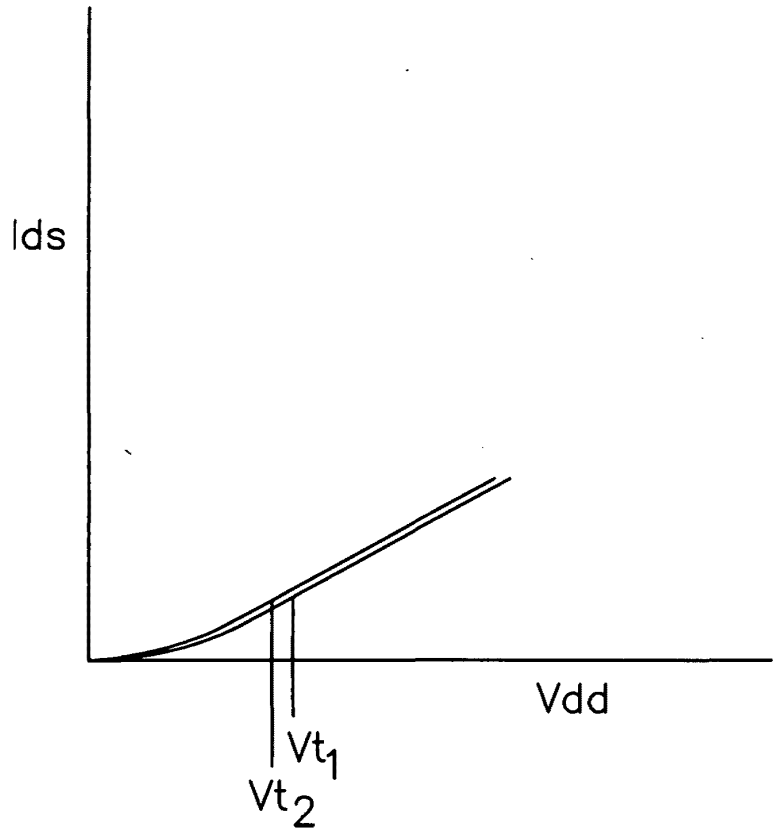

Figure 1

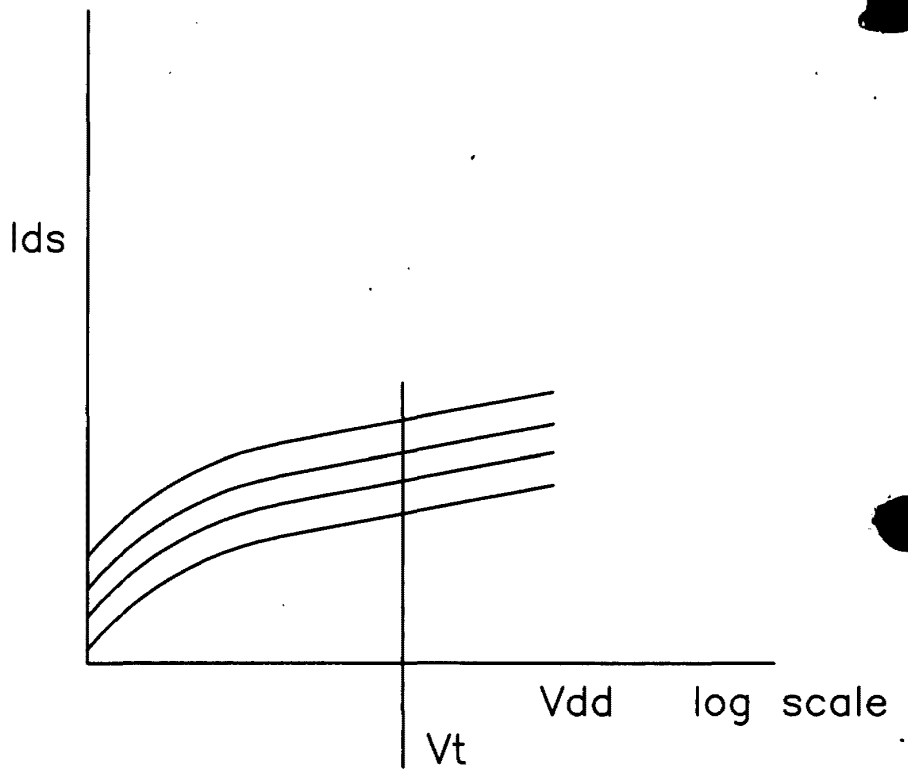

Figure 2

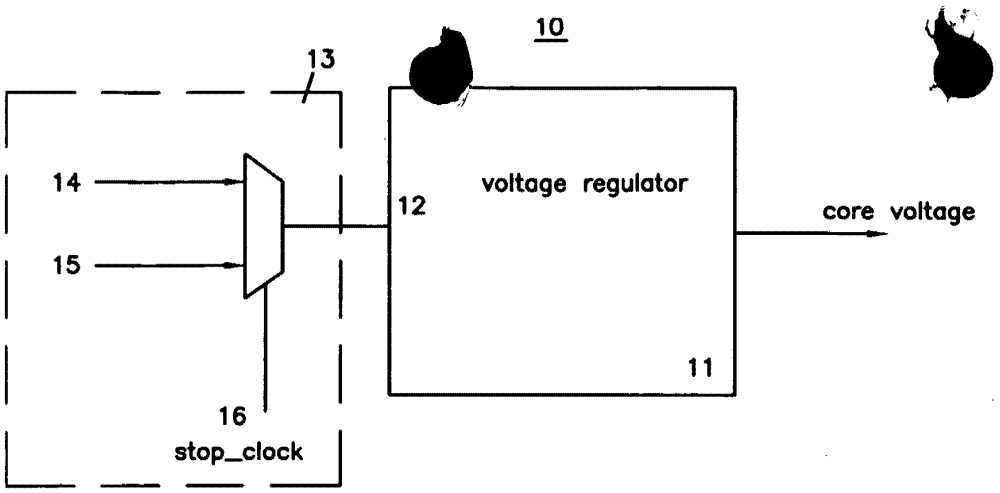

Figure 3

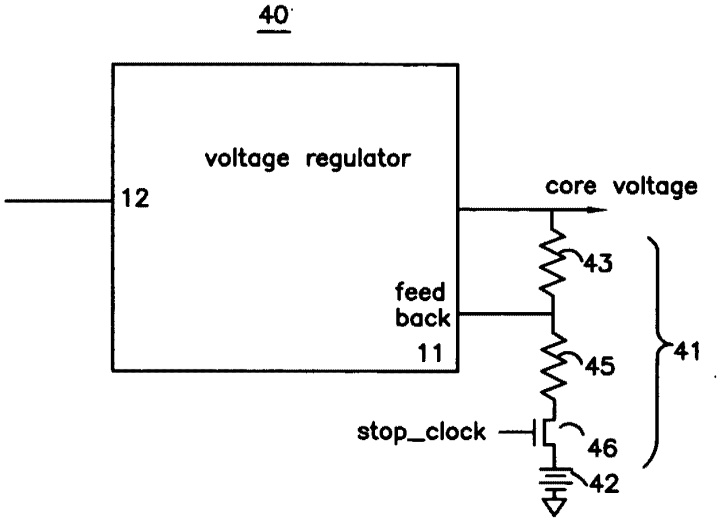

Figure 4

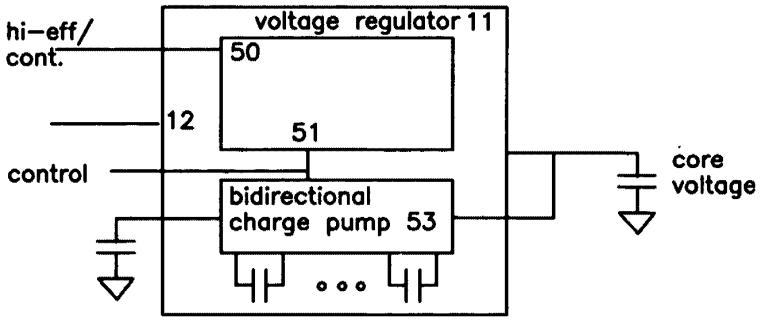

Figure 5

~~METHOD AND APPARATUS FOR REDUCING STATIC POWER LOSS~~
Saving power when in or transitioning to a static mode of a processor

BACKGROUND OF THE INVENTION

Field Of The Invention

This invention relates to computer systems and, more particularly, to apparatus and methods for reducing power use by a computer system during intervals in which processing is stopped.

History Of The Prior Art

As computer processors have increased in ability, the number of transistors utilized has increased almost exponentially. This increase in circuit elements has drastically increased the power requirements of such processors. As the need of power increases, the temperature at which a computer operates increases and the battery life of portable computers decreases. The loss of battery life with modern portable computers greatly reduces the time during which the computer can function as a portable device. In fact, the power usage has become so great that even with significant reduction in the process size utilized, a plethora of techniques have been implemented to reduce power usage to maintain the efficacy of portable computers.

One of these techniques monitors the use of the various devices within the computer and disables those devices that have not been utilized for some period. Because the processor utilizes a significant amount of the power (e.g., 50%) used by a portable computer, this technique is utilized to disable the processor itself when its processing requirements are unused for some interval. In the typical case, disabling the processor is

accomplished by terminating the system clocks furnished to the processor. When processor clocks have been disabled, controlling circuitry (typically a portion of the "Southbridge" circuitry of an X86-processor-based computer) remains enabled to detect interrupts requiring processor operation. The receipt of such an interrupt causes the controlling circuitry to once again enable clocks to the processor so that the processor may take whatever steps are necessary to handle the basis of the interrupt.

The technique of disabling the processor reduces significantly the dissipation of power caused by the operation of the processor even at a low frequency. In fact, the technique works quite well; and it is estimated that with many portable computers the processor is placed in the state in which system clocks are disabled during approximately ninety percent of the operation of the computer. However, use of this technique emphasizes another aspect of power loss using advanced processors. When system clocks for a processor are disabled, the processor must remain in a state (sometimes called "deep sleep") in which it is capable of rapidly responding to interrupts. Such a state requires the application of core voltage to the various circuits. The application of this voltage generates a power dissipation referred to in this specification as "static power" usage because the processor is in its static state in which clocks are disabled. To date there has been little attention paid to this static power usage. However, the usage is very significant when a processor functions in the deep sleep mode as much as ninety percent of the time. As process technologies continue to shrink

in dimension and lower operating voltages, this static power increases due to lower threshold voltages and thinner gate oxides.

It is desirable to furnish apparatus and methods for reducing the power use of a processor in the state in which its clocks are disabled.

Summary Of The Invention

The present invention is realized by a method for reducing power utilized by a processor including the steps of determining that a processor is transitioning from a computing mode to a mode in which system clock to the processor is disabled, and reducing core voltage to the processor to a value sufficient to maintain state during the mode in which system clock is disabled.

These and other features of the invention will be better understood by reference to the detailed description which follows taken together with the drawings in which like elements are referred to by like designations throughout the several views.

Brief Description Of The Drawings

Figure 1 is a diagram illustrating current-voltage characteristics of CMOS transistor devices utilized in microprocessors.

Figure 2 is another diagram illustrating current-voltage characteristics of CMOS transistor devices utilized in microprocessors.

Figure 3 is a circuit diagram illustrating a first circuit designed in accordance with the present invention for reducing static power usage.

Figure 4 is a circuit diagram illustrating a second circuit designed in accordance with the present invention for reducing static power usage.

Figure 5 is another circuit diagram illustrating a circuit designed in accordance with the present invention for reducing static power usage.

Detailed Description

Figure 1 is a first diagram displaying a number of curves illustrating the current-voltage characteristics of CMOS transistor devices utilized in the circuits of a microprocessor. This first diagram utilizes a linear scale for both current and voltage. As may be seen, each of the curves illustrates that the drain-to-source current of a transistor is essentially nonexistent until the voltage at the gate terminal of the transistor is raised to a threshold voltage. Once the threshold voltage of the transistor is reached, drain-to-source current increases either linearly or quadratically depending on whether the transistor is in the linear region or saturation region of operation.

Although the diagram of Figure 1 appears to illustrate that current flowing below the threshold value of the gate voltage is insignificant, this is not the case in some situations. Figure 2 illustrates current versus voltage curves of the typical transistor device below the threshold voltage with the voltage being plotted on a log scale. As may be seen, current in fact flows below the threshold voltage. If a transistor functions in the state below the threshold voltage for ninety percent of computer processor operation, then this current has a significant affect on power usage by the processor.

Since a processor is not capable of computing in the mode in which its clocks are disabled, it would at first glance appear that the solution would be to terminate the application of voltage to the processor. However, as suggested above, it is necessary that the processor be maintained in a condition in which it can respond rapidly to interrupts provided by the circuitry that controls application of the system clocks. To do this, the processor must maintain state sufficient to immediately return to an operating condition. Thus, prior art processors have been provided sufficient voltage to maintain such state and to keep their transistors ready to immediately respond to interrupts. In general, this has been accomplished by maintaining the processor core voltage at the same level as the operating voltage. With most prior art processors, the core voltage used by a processor is selected by use of motherboard switches or setup software at a level sufficient to provide the highest frequency operations specified for the particular processor. For example, many processors provide 1.8 volts as a core voltage. On the other hand, the voltage required to maintain state in a deep sleep mode may be significantly less, e.g., one volt or less. Since such processors function at the same voltage whether in a computing or a deep sleep mode, a significant amount of unnecessary power may be expended. In one typical state of the art X86 processor, the power usage averages approximately one-half watt in the deep sleep state because of the leakage illustrated by the diagram of Figure 2.

The present invention reduces the voltage applied to the processor significantly below the lowest voltage normally furnished as a core voltage for the processor during the mode in which system clocks are

disabled thereby reducing the power utilized by the processor in the deep sleep state.

Figure 3 is a circuit diagram illustrating a first embodiment of the invention. In the circuit 10 illustrated, a switching voltage regulator 11 receives an input signal at a terminal 12 which determines its output voltage value. Most modern processors utilize a voltage regulator which is capable of furnishing a range of core voltages for operating transistors; a typical regulator may furnish a range of voltages between 2 and 0.925 volts from which a particular core voltage may be selected for operation. Typically, a binary signal is provided a the terminal 12 which selects the particular output voltage level to be furnished by the regulator 11; in such a case, a number of individual pins may be utilized as the terminal 12.

Recently, a new power saving technique has been utilized which dynamically adjusts both the voltage and operating frequency to a level sufficient to maintain computing operations being conducted by a processor. The technique which offers significant power savings is described in detail in U. S. Patent application Serial No. 09/484,516, filed January 18, 2000, entitled Adaptive Power Control, assigned to the assignee of the present invention. A processor which utilizes this technique monitors operations within the processor to determine the frequency level at which the processor should operate. Depending on the particular operations being carried out by the processor, the value furnished at the terminal 12 of a regulator functioning in such a system will cause the regulator to produce an output voltage at some level

between the high and low values necessary for the particular processor to carry out computing functions.

In the circuit of Figure 3, input to the terminal 12 is furnished via a circuit 13 such as a multiplexor that is capable of providing one or more input values. In the embodiment illustrated, a value is provided at a first input 14 to the circuit 13 by the processor (or other circuitry) which determines the operating condition of the processor in its computing range; and a second value is provided at a second input 15 which is selected especially for the deep sleep condition. Either of these input values may be selected by a control signal provided at a control terminal 16 of the circuit 13. In one embodiment, a system control signal normally utilized to signal entry into the deep sleep condition (a stop clock signal) is used as the control signal to be furnished at the control terminal 16. This control signal selects the input value furnished at the input 15 which is especially chosen to cause a typical prior art regulator 11 to produce a voltage output for operating the processor in the deep sleep mode. In one embodiment of the invention, the value furnished for deep sleep mode is chosen to cause the regulator 11 to produce the lowest voltage possible in its range of output voltages. In one exemplary processor that utilizes the technique described in the above-mentioned patent application, the processor is specified as capable of conducting computing operations in a core voltage range from a low voltage of 1.2 volts to a high voltage of 1.6 volts. On the other hand, the processor when operating in deep sleep mode has no problem maintaining that state necessary to resume computing even though functioning at a core voltage of 0.925 volts, the lowest voltage which the regulator can provide.

Thus, although the voltage regulator 11 may typically provide a range of varying output voltage levels, the lowest voltage at which a processor is specified for conducting computing operations is typically significantly above the lowest value which the regulator is capable of furnishing.

In order to reduce power usage in one embodiment of the present invention, in response to a control signal indicating that the processor is about to go into the deep sleep state, the value at the input 15 is furnished by the circuit 13 to the regulator causing the regulator 11 to generate its lowest possible output voltage level for the deep sleep condition. In one exemplary embodiment, the high and low voltages generated in a computing mode are 1.6 volts and 1.2 volts while the deep sleep voltage is 0.925 volts.

Although the voltage level furnished by the regulator 11 for the deep sleep mode of the processor might appear to be only slightly lower than that furnished in the lowest operating condition for the exemplary processor, the reduction in power usage is quite significant. Because both the voltage and the leakage current are reduced, the reduction in power is approximately equal to the ratio in voltage levels raised to the power of about three to four. Over any period of processor use involving the deep sleep state, such a reduction is quite large.

One problem with this approach to reducing power is that it does not reduce the voltage level as far as might be possible and, thus, does not conserve as much power as could be saved. This approach only reduces the voltage level to the lowest level furnished by the regulator. This voltage is significantly greater than appears to be necessary for a

processor which also dynamically regulates voltage furnished during computing operations to save power. Two criteria control the level to which the core voltage may be reduced in deep sleep. The level must be sufficient to maintain state that the processor requires to function after returning from the deep sleep state. The level must be one that can be reached during the times allowed for transition to and from the deep sleep mode.

The first criterion is met so long as values of state stored are not lost during the deep sleep mode. Tests have shown that a core voltage significantly below one-half volt allows the retention of the memory state of a processor. Thus, using this criterion, it would be desirable to reduce the core voltage to a value such as one-half volt or lower.

However, depending on system configuration, the time allowed to transition to and from deep sleep in an X86 processor can be as low as 50 microseconds. Depending on the capacitive load of the particular circuitry, a voltage variation of about 0.5 to 0.6 volts may take place during this time in one exemplary configuration.

Thus, if the exemplary processor is operating at its lowest processing core voltage of 1.2 volts, its core voltage may be lowered in the time available to 0.6 - 0.7 volts. On the other hand, if the processor is operating at a processing core voltage of 1.5 volts, its core voltage may only be lowered in the time available to 0.9 - 1 volts. Consequently, it is desirable that the core voltage furnished during deep sleep be lowered to a level which may be below the level provided by a typical voltage

regulator but which varies depending on the core operating voltage from which it transitions.

This desirable result may be reached utilizing a circuit such as that described in Figure 4. The circuit of Figure 4 includes a feedback network 41 for controlling the level of voltage at the output of the regulator 11. Prior art regulators such as the Maxim 1711 provide a feedback terminal and describe how that terminal may be utilized with a resistor-voltage-divider network joined between the output terminal and ground to raise the output voltage level.

The embodiment of the present invention illustrated in Figure 4 utilizes the same feedback terminal and a similar resistor-voltage-divider network but joins the divider between the output terminal and a source of voltage 42 higher than the normal output voltage of the regulator to force the output voltage level to a lower value rather than a higher level. The particular source voltage and the particular resistor values may be selected to cause the voltage level at the output of the regulator to drop from a particular output value to a desired value such as 0.6 volts when transitioning from a computing level of 1.2 volts.

By appropriate choice of the resistor values of the divider network 41 and the source 42, the voltage drop provided by such a divider network accomplishes the desired result of providing an output voltage for the deep sleep mode of operation that varies from the previous processor computing core voltage by an amount attainable during the transition period available. In one embodiment, resistor 43 was chosen to be 1 Kohms, resistor 45 to be 2.7 Kohms, and source 42 to be 3.3 volts. Such

values cause the voltage drop into deep sleep mode to be between 0.5 and 0.6 volts whether beginning at core voltages of 1.2 or 1.6 volts. On the other hand, by using a higher value of voltage at source 45 and adjusting the values of resistors 41 and 43, the increments of voltage drop reached from different starting voltages to final deep sleep voltage values at the terminal 12 may be brought closer to one another.

It should be noted that the circuitry of Figures 3 and 4 may be combined so that both input selection and output adjustment are both used to adjust the core voltage value produced by a voltage regulator for deep sleep mode in particular instances where the load capacitance is relatively low.

Prior art voltage regulators function in at least two different modes of operation. A first mode of operation is often referred to as "low noise" or "continuous" mode. In this mode, the regulator responds as rapidly as possible to each change in voltage thereby maintaining the output voltage at the desired output level as accurately as possible. In order to maintain this mode of rapid response, regulators consume a certain amount of power. When a regulator is supplying a significant amount of power to the load, the power required to operate in continuous mode is relatively small. But, when a regulator is supplying a small amount of power to the load, the power used to operate the regulator in continuous mode becomes significant, and reduces the efficiency of the regulator significantly. It is common for regulators operating in the continuous mode to transfer charge from the supply capacitors back into the power source when the output voltage is changed from a higher voltage to a

lower voltage. The regulator can later transfer that charge back to the regulator output capacitors. Thus, most of the charge is not wasted.

A second mode of operation by voltage regulators is often referred to as "high efficiency," "burst," or "skip" mode. In this mode, a regulator detects the reduction in load requirements (such as that caused by a transition into the deep sleep state) and switches to a mode whereby the regulator corrects the output voltage less frequently. When there is an increase in load requirements, the regulator switches back to the continuous mode of regulation during which more rapid correction occurs. This has the positive effect of reducing the power consumed by the regulator during deep sleep thereby increasing the regulator efficiency and saving system power. But, as a result of reducing the regulator response rate, there is more noise on the regulator output.

It is common for regulators operating in the high efficiency mode to drain the charge on the supply capacitors during a high to low voltage transition on the power supply output or to allow the load to drain the charge. Thus, the charge is wasted during high to low voltage transitions.

It is typical to operate a voltage regulator in the high efficiency mode. Consequently, there is some waste of power whenever a regulated processor goes into the lower voltage deep sleep mode. If the processor is constantly being placed in deep sleep mode, then the loss of power may be quite high. Different operating systems may increase the waste of power by their operations. For example, an operating system that detects changes in operation through a polling process must constantly

bring a processor out of deep sleep to determine whether a change in operating mode should be implemented. For many such systems, such a system causes an inordinate amount of power waste if a processor would otherwise spend long periods in the deep sleep mode. On the other hand, an operating system that remains in deep sleep until an externally-generated interrupt brings it out of that state wastes power through operating the regulator in the high efficiency mode only when the processor is placed in the deep sleep state.

The present invention utilizes the ability of regulators to function in both the high efficiency mode and the continuous mode to substantially reduce power wasted by transitioning between a computing and a lower voltage deep sleep mode. Although regulators have not been dynamically switched between high efficiency and continuous modes, in one embodiment of the invention, an additional controlling input 50 as shown in Figure 5 is added to the regulator for selecting the mode of operation of the regulator based on whether the processor being regulated is transitioning between states. If the regulator receives a control signal 51 indicating that the processor is to be placed into the deep sleep mode, for example, then a regulator operating in the high efficiency mode immediately switches to the continuous mode during the voltage transition. Assuming that the regulator returns the charge to the battery during continuous mode, this has the effect of reducing the waste of power caused during the transition. Once the transition has completed, the regulator switches back to the high efficiency state for operation during the deep sleep mode of the processor.

For regulators that do not conserve capacitive charge by transferring the charge to the battery, a circuit for accomplishing this may be implemented or a capacitor storage arrangement such as a charge pump 53 for storage may be added. Alternatively, when transitioning to deep sleep, the regulator could switch to a mode where the regulator does not actively drive the voltage low but allows the capacitor charge to drain through the load. The selection of power savings modes is dependent on the processor leakage current, the voltage drop between the operating and deep sleep voltages, and the efficiency of the regulator in transferring charge from the capacitors to the power source and then back. If the leakage current is not sufficient to bring the voltage down more than (1 – efficiency) * (deep sleep voltage drop) during the deep sleep interval, then it is more advantageous to use the load to drain the charge on the capacitors. Otherwise, the charge on the capacitors should be transferred back to the power source.

The control signal utilized may be the same control signal (stop clocks) that signals the transition into the deep sleep state if the method is to be used only for transitions between operating and deep sleep states. Alternatively, a control signal generated by a particular increment of desired change may be utilized for voltage changes within the computing range of the processor as well as the transition to deep sleep mode.

Although the present invention has been described in terms of a preferred embodiment, it will be appreciated that various modifications and alterations might be made by those skilled in the art without departing from the spirit and scope of the invention. The invention should therefore be measured in terms of the claims which follow.

What Is Claimed Is:

Sub A1

Claim 1. A method for reducing power utilized by a processor comprising the steps of:

determining that a processor is transitioning from a computing mode to a mode is which system clock to the processor is disabled, and

reducing core voltage to the processor to a value sufficient to maintain state during the mode in which system clock is disabled.

Claim 2. A method as claimed in Claim 1 in which the step of determining that a processor is transitioning from a computing mode to a mode is which system clock to the processor is disabled comprising monitoring a stop clock signal.

Claim 3. A method as claimed in Claim 1 in which the step of reducing core voltage to the processor to a value sufficient to maintain state during the state in which system clock is disabled comprises furnishing an input to reduce an output voltage provided by a voltage regulator furnishing core voltage to the processor.

Claim 4. A method as claimed in Claim 3 in which the step of reducing core voltage to the processor to a value sufficient to maintain state during the state in which system clock is disabled further comprises providing a feedback signal to the voltage regulator to reduce its output voltage below a specified output voltage.

Claim 5. A method as claimed in Claim 1 further comprising the steps of transferring operation of a voltage regulator furnishing core voltage in

a mode in which power is dissipated during reductions in core voltage to a mode in which power is saved during a voltage transition when it is determined that a processor is transitioning from a computing mode to a mode is which system clock to the processor is disabled.

Sub A1

Claim 6. A method as claimed in Claim 5 further comprising the steps of returning the voltage regulator to its original mode of operation when the lower value of the core voltage is reached.

Claim 7. A circuit for providing a regulated voltage to a processor comprising:

a voltage regulator having:

an output terminal providing a selectable voltage, and

an input terminal for receiving signals indicating the selectable voltage level;

means for providing signals at the input terminal of the voltage regulator for selecting a voltage for operating the processor in a computing mode and a voltage of a level less than that for operating the processor in a computing mode.

Claim 8. A circuit as claimed in Claim 7 in which the means for providing signals at the input terminal of the voltage regulator comprises means for accepting binary signals indicating different levels of voltage.

Claim 9. A circuit as claimed in Claim 7 in which the means for providing signals at the input terminal of the voltage regulator comprises:

selection circuitry,

means for furnishing a plurality of signals at the input to the selection circuitry, and

means for controlling the selection by the selection circuitry.

Sub A1

Claim 10. A circuit as claimed in Claim 9 in which:

the selection circuitry is a multiplexor, and

the means for controlling the selection by the selection circuitry includes a control terminal for receiving signals indicating a system clock to the processor is being terminated.

Claim 11. A circuit as claimed in Claim 7 further comprising means for reducing the selectable voltage below a level provided by the voltage regulator.

Claim 12. A circuit as claimed in Claim 11 in which the means for reducing the selectable voltage below a level provided by the voltage regulator comprises:

a voltage divider network joined between the output terminal and a voltage source furnishing a value higher than the selectable voltage, and

a voltage regulator feedback circuit receiving a value from the voltage divider network.

Claim 13. A circuit as claimed in Claim 7 further comprising:

circuitry for conserving charge stored by the voltage regulator when the selectable voltage decreases, and

Sub A1

means for enabling the circuitry for conserving charge stored by the voltage regulator when the selectable voltage decreases.

Abstract of the Disclosure:

A method for reducing power utilized by a processor including the steps of determining that a processor is transitioning from a computing mode to a mode is which system clock to the processor is disabled, and reducing core voltage to the processor to a value sufficient to maintain state during the mode in which system clock is disabled.

Attorney's Docket No.: Trans59 Patent

DECLARATION AND POWER OF ATTORNEY FOR PATENT APPLICATION

As a below named inventor, I hereby declare that:

My residence, post office address and citizenship are as stated below, next to my name.

I believe I am the original, first, and sole inventor (if only one name is listed below) or an original, first, and joint inventor (if plural names are listed below) of the subject matter which is claimed and for which a patent is sought on the invention entitled

STATIC POWER CONTROL

the specification of which is attached hereto.

I hereby state that I have reviewed and understand the contents of the above-identified specification, including the claim(s), as amended by any amendment referred to above. I do not know and do not believe that the claimed invention was ever known or used in the United States of America before my invention thereof, or patented or described in any printed publication in any country before my invention thereof or more than one year prior to this application, that the same was not in public use or on sale in the United States of America more than one year prior to this application, and that the invention has not been patented or made the subject of an inventor's certificate issued before the date of this application in any country foreign to the United States of America on an application filed by me or my legal representatives or assigns more than twelve months (for a utility patent application) or six months (for a design patent application) prior to this application.

I acknowledge the duty to disclose all information known to me to be material to patentability as defined in Title 37, Code of Federal Regulations, Section 1.56.

I hereby appoint Stephen L. King, Reg. No. 19,180; with offices located at 30 Sweetbay Road, Rancho Palos Verdes, California 90275, telephone (310) 377-5073, with full power of substitution and revocation, to prosecute this application and to transact all business in the Patent and Trademark Office connected herewith.

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of

Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

Full Name of Sole/First Inventor Andrew Read

Inventor's Signature _____ Date _____

Residence Sunnyvale, California (City, State) Citizenship U.S.A. (Country)

Post Office Address: 1621 Eagle Drive
Sunnyvale, California 94087

Full Name of Second/Joint Inventor Sameer Halepete

Inventor's Signature _____ Date _____

Residence San Jose, California (City, State) Citizenship India (Country)

Post Office Address: 373 River Oaks Circle, #1608
San Jose California 95134

Full Name of Third/Joint Inventor Keith Klayman

Inventor's Signature _____ Date _____

Residence Sunnyvale, California (City, State) Citizenship U.S.A. (Country)

Post Office Address: 613 San Conradoter #2
Sunnyvale, California 94086

Applicant or Patentee: TRANSMETA CORPORATION Attorney's
Serial or Patent No.: _____ Docket No. TRANS59
Filed or Issued: _____

For: STATIC POWER CONTROL

VERIFIED STATEMENT (DECLARATION) CLAIMING SMALL ENTITY STATUS
37 CFR 1.9 (f) and 1.27(c) - - SMALL BUSINESS CONCERN

I hereby declare that I am an official of the small business concern empowered to act on behalf of the concern identified below:

NAME OF CONCERN: TRANSMETA CORPORATION
ADDRESS OF CONCERN: 3940 FREEDOM CIRCLE, SANTA CLARA, CALIFORNIA 95054

I hereby declare that the above identified small business concern qualifies as a small business concern as defined in 13 CFR 121.3-18, and reproduced in 37 CFR 1.9(d), for purposes of paying reduced fees under Section 41(a) and (b) of Title 35, United States Code, in that the number of employees of the concern, including those of its affiliates, does not exceed 500 persons. For purposes of this statement, (1) the number of employees of the business concern is the average over the previous fiscal year of the concern of the persons employed on a full-time, part-time or temporary basis during each of the pay periods of the fiscal year, and (2) concerns are affiliates of each other when either, directly or indirectly, one concern controls or has the power to control the other, or a third party or parties controls or has the power to control both.

I hereby certify that to the best of my knowledge and belief rights under contract or law have been conveyed to and remain with the small business concern identified above with regard to the invention entitled STATIC POWER CONTROL,

by inventor(s) Andrew Read, Sameer Halepete, and Keith Klayman,
described in

[X] the application for United States patent, the specification of which was filed on June 16, 2000, and assigned Serial No. 09/595,196,

and I have reviewed the document that evidences the conveyance of those rights. That document

[X] is being filed herewith.

If the rights held by the above-identified small business concern are not exclusive, each individual, concern or organization having rights to the invention is listed below and **no rights to the invention are held by any person, other than the inventor, who could not qualify as a small business concern under 37 CFR 1.9(d) or by any concern which would not qualify as a small business concern under 347 CFR 1.9(d) or a non-profit organization under 37 CFR 1.9(e)**. NOTE: Separate verified statements are required from each named person, concern or organization having rights to the invention averring to their status as small entities. (37 CFR 1.27)

NAME: _____
ADDRESS: _____
[____] Individual [_____] Small Business Concern [_____] Non-Profit Organization
NAME: _____
ADDRESS: _____
[____] Individual [_____] Small Business Concern [_____] Non-Profit Organization

I acknowledge the duty to file, in this application or patent, notification of any change in status resulting in loss of entitlement to small entity status prior to paying, or at the time of paying, the earliest of the issue fee or any maintenance fee due after the date on which status as a small entity is no longer appropriate. (37 CFR 1.28(b)).

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code, and that such willful false statements may jeopardize the validity of the application, any patent issuing thereon, or any patent to which this verified statement is directed.

NAME OF PERSON SIGNING: MARK ALLEN
TITLE OF PERSON OTHER THAN OWNER: PRESIDENT AND COO
ADDRESS OF PERSON SIGNING: 3940 FREEDOM WAY, SANTA CLARA, CALIFORNIA 95054
SIGNATURE: ______________________ DATE: ______________________

UNITED STATES PATENT AND TRADEMARK OFFICE

Commissioner for Patents
Washington, DC 20231
www.uspto.gov

Bib Data Sheet

CONFIRMATION NO. 3072

SERIAL NUMBER	FILING DATE	CLASS	GROUP ART UNIT	ATTORNEY DOCKET NO.
09/694,433	10/23/2000 RULE	713	2185	TRANS59

APPLICANTS

Andrew Read, Sunnyvale, CA;
Sameer Halepete, San Jose, CA;
Keith Klayman, Sunnyvale, CA;

** CONTINUING DATA **********

N-C

** FOREIGN APPLICATIONS **********

N-C

IF REQUIRED, FOREIGN FILING LICENSE GRANTED ~~** SMALL ENTITY~~ **
** 12/15/2000

Foreign Priority claimed	STATE OR COUNTRY	SHEETS DRAWING	TOTAL CLAIMS	INDEPENDENT CLAIMS
☐ yes ☑ no	CA	2	13	2
35 USC 119 (a-d) conditions met ☐ yes ☑ no ☐ Met after Allowance				
Verified and Acknowledged Examiner's Signature CAO Initials				

ADDRESS

WAGNER, MURABITO & HAO LLP
TWO NORTH MARKET STREET
THIRD FLOOR
SAN JOSE , CA 95113

TITLE

Method and apparatus for reducing static power loss

FILING FEE RECEIVED		
420	FEES: Authority has been given in Paper No. _____ to charge/credit DEPOSIT ACCOUNT No. _____ for following:	☐ All Fees ☐ 1.16 Fees (Filing) ☐ 1.17 Fees (Processing Ext. of time) ☐ 1.18 Fees (Issue) ☐ Other _____ ☐ Credit

PATENT APPLICATION SERIAL NO. _____

U.S. DEPARTMENT OF COMMERCE
PATENT AND TRADEMARK OFFICE
FEE RECORD SHEET

PTO-1556
(5/87)

*U.S. GPO: 1999-459-082/18144

PATENT APPLICATION FEE DETERMINATION RECORD
Effective October 1, 2000

Application or Docket Number
09 694 433

CLAIMS AS FILED - PART I

	(Column 1)	(Column 2)
TOTAL CLAIMS	13	
FOR	NUMBER FILED	NUMBER EXTRA
TOTAL CHARGEABLE CLAIMS	13 minus 20=	*
INDEPENDENT CLAIMS	2 minus 3 =	*
MULTIPLE DEPENDENT CLAIM PRESENT		☐

* If the difference in column 1 is less than zero, enter "0" in column 2

SMALL ENTITY TYPE ☐		OR	OTHER THAN SMALL ENTITY	
RATE	FEE		RATE	FEE
BASIC FEE	355.00	OR	BASIC FEE	710.00
X$ 9=		OR	X$18=	
X40=		OR	X80=	
+135=		OR	+270=	
TOTAL	355	OR	TOTAL	

CLAIMS AS AMENDED - PART II

AMENDMENT A

	(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA
Total	*	Minus	**	=
Independent	*	Minus	***	=
FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM				☐

SMALL ENTITY		OR	OTHER THAN SMALL ENTITY	
RATE	ADDITIONAL FEE		RATE	ADDITIONAL FEE
X$ 9=		OR	X$18=	
X40=		OR	X80=	
+135=		OR	+270=	
TOTAL ADDIT. FEE		OR	TOTAL ADDIT. FEE	

AMENDMENT B

	(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA
Total	*	Minus	**	=
Independent	*	Minus	***	=
FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM				☐

RATE	ADDITIONAL FEE		RATE	ADDITIONAL FEE
X$ 9=		OR	X$18=	
X40=		OR	X80=	
+135=		OR	+270=	
TOTAL ADDIT. FEE		OR	TOTAL ADDIT. FEE	

AMENDMENT C

	(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA
Total	*	Minus	**	=
Independent	*	Minus	***	=
FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM				☐

RATE	ADDITIONAL FEE		RATE	ADDITIONAL FEE
X$ 9=		OR	X$18=	
X40=		OR	X80=	
+135=		OR	+270=	
TOTAL ADDIT. FEE		OR	TOTAL ADDIT. FEE	

* If the entry in column 1 is less than the entry in column 2, write "0" in column 3.
** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20."
***If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3."
The "Highest Number Previously Paid For" (Total or Independent) is the highest number found in the appropriate box in column 1.

CLAIMS ONLY

SERIAL NO.	FILING DATE
APPLICANT(S)	

CLAIMS

	AS FILED		AFTER 1st AMENDMENT		AFTER 2nd AMENDMENT	
	IND.	DEP.	IND.	DEP.	IND.	DEP.
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TOTAL CLAIMS	3					

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TOTAL IND.						
TOTAL DEP.						
TOTAL CLAIMS						

* MAY BE USED FOR ADDITIONAL CLAIMS OR ADMENDMENTS

FORM PTO-2022 (1-98)

U.S.DEPARTMENT OF COMMERCE
Patent and Trademark Office

UNITED STATES PATENT AND TRADEMARK OFFICE

COMMISSIONER FOR PATENTS
UNITED STATES PATENT AND TRADEMARK OFFICE
WASHINGTON, D.C. 20231
www.uspto.gov

APPLICATION NUMBER	FILING/RECEIPT DATE	FIRST NAMED APPLICANT	ATTORNEY DOCKET NUMBER
09/694,433	10/23/2000	Andrew Read	TRANS59

FORMALITIES LETTER

OC000000005624036

Stephen L. King
30 Sweetbay Road
Rancho Palos Verdes, CA 90275

Date Mailed: 12/15/2000

NOTICE TO FILE MISSING PARTS OF NONPROVISIONAL APPLICATION

FILED UNDER 37 CFR 1.53(b)

Filing Date Granted

An application number and filing date have been accorded to this application. The item(s) indicated below, however, are missing. Applicant is given TWO MONTHS from the date of this Notice within which to file all required items and pay any fees required below to avoid abandonment. Extensions of time may be obtained by filing a petition accompanied by the extension fee under the provisions of 37 CFR 1.136(a).

- The oath or declaration is unsigned.
- To avoid abandonment, a late filing fee or oath or declaration surcharge as set forth in 37 CFR 1.16(e) of $65 for a small entity in compliance with 37 CFR 1.27, must be submitted with the missing items identified in this letter.

- **The balance due by applicant is $ 65.**

A copy of this notice MUST be returned with the reply.

Customer Service Center
Initial Patent Examination Division (703) 308-1202
PART 3 - OFFICE COPY

#8

UNITED STATES PATENT AND TRADEMARK OFFICE

COMMISSIONER FOR PATENTS
UNITED STATES PATENT AND TRADEMARK OFFICE
WASHINGTON, D.C. 20231
www.uspto.gov

APPLICATION NUMBER	FILING/RECEIPT DATE	FIRST NAMED APPLICANT	ATTORNEY DOCKET NUMBER
09/694,433	10/23/2000	Andrew Read	TRANS59

FORMALITIES LETTER

OC000000005624036

Stephen L. King
30 Sweetbay Road
Rancho Palos Verdes, CA 90275

Date Mailed: 12/15/2000

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Filing Date Granted

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- The oath or declaration is unsigned.
- To avoid abandonment, a late filing fee or oath or declaration surcharge as set forth in 37 CFR 1.16(e) of $65 for a small entity in compliance with 37 CFR 1.27, must be submitted with the missing items identified in this letter.

- **The balance due by applicant is $ 65.**

A copy of this notice MUST be returned with the reply.

Customer-Service Center
Initial Patent Examination Division (703) 308-1202
PART 2 - COPY TO BE RETURNED WITH RESPONSE

02/09/2001 TGEDAMU1 00000032 501497 09694433

01 FC:205 65.00 CH

#Sector #3

Case/Docket No. TRANS59

ASSISTANT COMMISSIONER FOR PATENTS
Washington, D.C. 20231

Sir:

Transmitted herewith for filing with respect to the patent application of:

Inventors: A. Read et al
For: STATIC POWER CONTROL
Serial # 09/694,433
Filed : 10/23/00

are:

An executed declaration and power of attorney,
An executed small entity declaration,
An assignment and cover sheet,
A copy of a Notice To File Missing Parts.

The declaration is filed in response to the Notice To File Missing Parts mailed December 15, 2000 in the above-identified patent application. Please file the declaration and power of attorney and the small entity declaration and record the assignment. Please charge the fee of $105 and any additional fees with respect to this transaction to Transmeta deposit account 501497. The fee has been computed as follows: $65 late fee for small entity plus $40 assignment recordation fee totalling $105.

Respectfully submitted,

Date: February 2, 2001

2/2/01

Stephen L. King, Reg. No. 19,180

30 Sweetbay Road
Rancho Palos Verdes, California 90275
(310) 377-5073

I hereby certify that this correspondence is being deposited with sufficient postage with the United States Postal Service as First Class mail in an envelope addressed to: Assistant Commissioner for Patents, Washington, D.C. 20231, on February 2, 2001.

Stephen L. King, registered representative

2-2-01

#7

Attorney's Docket No.: Trans59 Patent

DECLARATION AND POWER OF ATTORNEY FOR PATENT APPLICATION

As a below named inventor, I hereby declare that:

My residence, post office address and citizenship are as stated below, next to my name.

I believe I am the original, first, and sole inventor (if only one name is listed below) or an original, first, and joint inventor (if plural names are listed below) of the subject matter which is claimed and for which a patent is sought on the invention entitled

STATIC POWER CONTROL

the specification of which was filed on October 23, 2000, and assigned Serial No. 09/694,433.

I hereby state that I have reviewed and understand the contents of the above-identified specification, including the claim(s), as amended by any amendment referred to above. I do not know and do not believe that the claimed invention was ever known or used in the United States of America before my invention thereof, or patented or described in any printed publication in any country before my invention thereof or more than one year prior to this application, that the same was not in public use or on sale in the United States of America more than one year prior to this application, and that the invention has not been patented or made the subject of an inventor's certificate issued before the date of this application in any country foreign to the United States of America on an application filed by me or my legal representatives or assigns more than twelve months (for a utility patent application) or six months (for a design patent application) prior to this application.

I acknowledge the duty to disclose all information known to me to be material to patentability as defined in Title 37, Code of Federal Regulations, Section 1.56.

I hereby appoint Stephen L. King, Reg. No. 19,180; with offices located at 30 Sweetbay Road, Rancho Palos Verdes, California 90275, telephone (310) 377-5073, with full power of substitution and revocation, to prosecute this application and to transact all business in the Patent and Trademark Office connected herewith.

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of

Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

Full Name of Sole/First Inventor Andrew Read

Inventor's Signature Andrew J Read Date 25 JAN 01

Residence Sunnyvale, California (City, State) Citizenship U.S.A. (Country)

Post Office Address: 1621 Eagle Drive
Sunnyvale, California 94087

Full Name of Second/Joint Inventor Sameer Halepete

Inventor's Signature _____ Date 25 JAN 2001

Residence San Jose, California (City, State) Citizenship India (Country)

Post Office Address: 373 River Oaks Circle, #1608
San Jose California 95134

Full Name of Third/Joint Inventor Keith Klayman

Inventor's Signature Keith Klayman Date 25 Jan 01

Residence Sunnyvale, California (City, State) Citizenship U.S.A. (Country)

Post Office Address: 613 San Conradoter #2
Sunnyvale, California 94086

Applicant or Patentee: TRANSMETA CORPORATION
Serial or Patent No.: 09/694,433
Filed or Issued: October 23, 2000

Attorney's Docket No. TRANS59

For: STATIC POWER CONTROL

VERIFIED STATEMENT (DECLARATION) CLAIMING SMALL ENTITY STATUS
37 CFR 1.9 (f) and 1.27(c) - - SMALL BUSINESS CONCERN

I hereby declare that I am an official of the small business concern empowered to act on behalf of the concern identified below:

NAME OF CONCERN: TRANSMETA CORPORATION
ADDRESS OF CONCERN: 3940 FREEDOM CIRCLE, SANTA CLARA, CALIFORNIA 95054

I hereby declare that the above identified small business concern qualifies as a small business concern as defined in 13 CFR 121.3-18, and reproduced in 37 CFR 1.9(d), for purposes of paying reduced fees under Section 41(a) and (b) of Title 35, United States Code, in that the number of employees of the concern, including those of its affiliates, does not exceed 500 persons. For purposes of this statement, (1) the number of employees of the business concern is the average over the previous fiscal year of the concern of the persons employed on a full-time, part-time or temporary basis during each of the pay periods of the fiscal year, and (2) concerns are affiliates of each other when either, directly or indirectly, one concern controls or has the power to control the other, or a third party or parties controls or has the power to control both.

I hereby certify that to the best of my knowledge and belief rights under contract or law have been conveyed to and remain with the small business concern identified above with regard to the invention entitled STATIC POWER CONTROL,

by inventor(s) Andrew Read, Sameer Halepete, and Keith Klayman,
described in

[X] the application for United States patent, the specification of which was filed on October 23, 2000, and assigned Serial No. 09/694,433,

and I have reviewed the document that evidences the conveyance of those rights. That document

[X] is being filed herewith.

If the rights held by the above-identified small business concern are not exclusive, each individual, concern or organization having rights to the invention is listed below and **no rights to the invention are held by any person, other than the inventor, who could not qualify as a small business concern under 37 CFR 1.9(d) or by any concern which would not qualify as a small business concern under 347 CFR 1.9(d) or a non-profit organization under 37 CFR 1.9(e)**. NOTE: Separate verified statements are required from each named person, concern or organization having rights to the invention averring to their status as small entities. (37 CFR 1.27)

NAME: _____
ADDRESS: _____
[____] Individual [_____] Small Business Concern [_____] Non-Profit Organization
NAME: _____
ADDRESS: _____
[____] Individual [_____] Small Business Concern [_____] Non-Profit Organization

I acknowledge the duty to file, in this application or patent, notification of any change in status resulting in loss of entitlement to small entity status prior to paying, or at the time of paying, the earliest of the issue fee or any maintenance fee due after the date on which status as a small entity is no longer appropriate. (37 CFR 1.28(b)).

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code, and that such willful false statements may jeopardize the validity of the application, any patent issuing thereon, or any patent to which this verified statement is directed.

NAME OF PERSON SIGNING: MARK ALLEN
TITLE OF PERSON OTHER THAN OWNER: PRESIDENT AND COO
ADDRESS OF PERSON SIGNING: 3940 FREEDOM WAY, SANTA CLARA, CALIFORNIA 95054
SIGNATURE: _____ DATE: 1/25/01

Gp/2188 #4 9-28-02

Attorney Docket No.: TRAN-P059

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Patent

In re Application of:

Inventor(s): Andrew Read, Sameer Halepete, and Keith Klayman

Serial No.: 09/694,433 Examiner:

Filed: 10/23/00 Art Unit: 2188

For: STATIC POWER CONTROL

Patent No.: Issued Date:

Assistant Commissioner for Patents
Washington, D.C. 20231

POWER OF ATTORNEY BY ASSIGNEE OF ENTIRE INTEREST (REVOCATION OF PRIOR POWERS)

As assignee of record of the entire interest of the above identified
- ☒ application,
- ☐ patent,

REVOCATION OF PRIOR POWERS OF ATTORNEY

all powers of attorney previously given are hereby revoked and

NEW POWER OF ATTORNEY

the following attorney(s) and/or agents(s) are hereby appointed to prosecute and transact all business in the Patent and Trademark Office connected herewith.

James P. Hao	Registration No.:	36,398
Anthony C. Murabito	Registration No.:	35,295
John P. Wagner	Registration No.:	35,398
Glenn D. Barnes	Registration No.:	42,293
Thomas M. Catale	Registration No.:	46,434
Jose S. Garcia	Registration No.:	43,628
Eric J. Gash	Registration No.:	46,274
Lin C. Hsu	Registration No.:	46,315
Ronald M. Pomerenke	Registration No.:	43,009
John F. Ryan	Registration No.:	47,050
Matthew J. Blecher	Registration No.:	46,558
Lawrence R. Goerke	Registration No.:	45,927
Reginald A. Ratliff	Registration No.:	48,098

rev. 2/98 dbp

William A. Zarbis	Registration No.:	46,120
Mehlin Dean Matthews	Registration No.:	46,127
Joel D. Youngs	Registration No.:	P-52,389
Bryn C. Ekroot	Registration No.:	38,129

SEND CORRESPONDENCE TO:

WAGNER, MURABITO & HAO LLP
Two North Market Street
Third Floor
San Jose, CA 95113

DIRECT PHONE CALLS TO:

Anthony C. Murabito
(408) 938-9060

Transmeta Corporation
(type or print identity of assignee of entire interest)

3940 Freedom Circle
Santa Clara, CA 95054
Address

☒ Recorded in PTO on 02/05/01
Reel 011536
Frame 0490

☐ Recorded herewith

ASSIGNEE CERTIFICATION

Attached to this power is a "CERTIFICATE UNDER 37 CFR 3.73(b)."

Bryn Ekroot
Signature

9/9/2002
Date

Bryn C. Ekroot
(type or print name of person authorized to sign on behalf of assignee)

Director of Intellectual Property
Title

rev. 2/98 dbp

Docket No.: TRAN-P059
Patent

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of: Read et al.
Serial No.: 09/694,433
Filing Date: 10/23/00
For: STATIC POWER CONTROL

CERTIFICATE UNDER 37 CFR 3.73(b)

TRANSMETA CORPORATION, a corporation, certifies that it is the assignee of the entire right, title and interest in the patent application identified above by virtue of either:

[X] An assignment from the inventor(s) of the patent application identified above. A copy of the assignment is attached.

[ ] A chain of title from the inventor(s), of the patent application identified above, to the current assignees as shown below:

1. From: _____ To: _____
The document was recorded in the Patent and Trademark Office at Reel: _____, Frame: _____, or for which a copy thereof is attached.

2. From: _____ To: _____
The document was recorded in the Patent and Trademark Office at Reel: _____, Frame: _____, or for which a copy thereof is attached.

3. From: _____ To: _____
The document was recorded in the Patent and Trademark Office at Reel: _____, Frame: _____, or for which a copy thereof is attached.

[ ] Additional documents in the chain of title are listed on a supplemental sheet.

[ ] Copies of assignments or other documents in the chain of title are attached.

The undersigned has reviewed all the documents in the chain of title of the patent application identified above and, to the best of undersigned's knowledge and belief, title is in the assignee identified above.

The undersigned (whose title is supplied below) avers that the undersigned is empowered to sign this certificate on behalf of the assignee.

I hereby declare that all statements made herein of my own knowledge are true, and that all statements made on information and belief are believed to be true; and further, that these statements are made with the knowledge that willful false statements, and the like so made, are punishable by fine

or imprisonment, or both, under Section 1001, Title 18 of the United States Code, and that such willful false statements may jeopardize the validity of the application or any patent issuing thereon.

9/9/2002
Date

Signature

Bryn C. Ekroot
Typed or Printed Name

Director of Intellectual Property
Title

Attorney's Docket No.: Trans59

ASSIGNMENT

PATENT

In consideration of good and valuable consideration, the receipt of which is hereby acknowledged, we, the undersigned, Andrew Read, Sameer Halepete, and Keith Klayman hereby sell, assign, and transfer to Transmeta, Corporation, a corporation of Delaware, having a principal place of business at 3940 Freedom Circle, Santa Clara, California 95054, ("Assignee"), and its successors, assigns, and legal representatives, the entire right, title, and interest for the United States and all foreign countries, in and to any and all inventions and improvements that are disclosed in the application for the United States patent, , the specification of which was filed on October 23, 2000, and assigned Serial No. 09/694,433, and is entitled:

STATIC POWER CONTROL

and in and to said application and all divisional, continuing, substitute, renewal, reissue, and all other patent applications that have been or shall be filed in the United States and all foreign countries on any of said improvements; and in and to all original and reissued patents that have been or shall be issued in the United States and all foreign countries on said improvements; and in and to all rights of priority resulting from the filing of said United States application;

agree that said Assignee may apply for and receive a patent or patents for said improvements in its own name; and that, when requested, without charge to, but at the expense of, said Assignee, its successors, assigns, and legal representatives, to carry out in good faith the intent and purpose of this Assignment, the undersigned will execute all divisional, continuing, substitute, renewal, reissue, and all other patent applications on any and all said improvements; execute all rightful oaths, assignments, powers of attorney, and other papers; communicate to said Assignee, its successors, assigns, and representatives all facts known to the undersigned relating to said improvements and the history thereof; and generally do everything possible that said Assignee, its successors, assigns, or representatives shall consider desirable for aiding in securing and maintaining proper patent protection for said improvements and for vesting title to said improvements, and all applications for patents and all patents on said improvements, in said Assignee, its successors, assigns, and legal representatives; and

covenant with said Assignee, its successors, assigns, and legal representatives that no assignment, grant, mortgage, license, or other agreement affecting the rights and property herein conveyed has been made to others by the undersigned, and that full right to convey the same as herein expressed is possessed by the undersigned.

Each Inventor: Please Sign and Date Below:

Date	Name
Jan 25, 2001	Andrew Read
Jan 25, 2001	Sameer Halepete
Jan 25, 2001	Keith Klayman

Each Inventor: Please also list the date that you signed the accompanying Declaration and Power of Attorney:

Date
Jan 25, 2001
Jan 25, 2001
Jan 25, 2001

Assignment Document Return Address:
STEPHEN L. KING
30 SWEETBAY ROAD
RANCHO PALOS VERDES, CA 90275
(310) 377-5073

H5

UNITED STATES
PATENT AND
TRADEMARK OFFICE

Commissioner for Patents
Washington, DC 20231
www.uspto.gov

APPLICATION NUMBER	FILING DATE	FIRST NAMED APPLICANT	ATTY. DOCKET NO./TITLE
09/694,433	10/23/2000	Andrew Read	TRANS59

CONFIRMATION NO. 3072

WAGNER, MURABITO & HAO LLP
TWO NORTH MARKET STREET
THIRD FLOOR
SAN JOSE, CA 95113

OC000000008872573

Date Mailed: 09/30/2002

NOTICE OF ACCEPTANCE OF POWER OF ATTORNEY

This is in response to the Power of Attorney filed 09/16/2002.

The Power of Attorney in this application is accepted. Correspondence in this application will be mailed to the above address as provided by 37 CFR 1.33.

Dale A Hall

DALE A HALL
2100 (703) 305-9633

OFFICE COPY

UNITED STATES
PATENT AND
TRADEMARK OFFICE

Commissioner for Patents
Washington, DC 20231
www.uspto.gov

APPLICATION NUMBER	FILING DATE	FIRST NAMED APPLICANT	ATTY. DOCKET NO./TITLE
09/694,433	10/23/2000	Andrew Read	TRANS59

CONFIRMATION NO. 3072

Stephen L. King
30 Sweetbay Road
Rancho Palos Verdes, CA 90275

OC000000008872560

Date Mailed: 09/30/2002

NOTICE REGARDING CHANGE OF POWER OF ATTORNEY

This is in response to the Power of Attorney filed 09/16/2002.

- The Power of Attorney to you in this application has been revoked by the assignee who has intervened as provided by 37 CFR 3.71. Future correspondence will be mailed to the new address of record(37 CFR 1.33).

Dale A Hall

DALE A HALL
2100 (703) 305-9633

OFFICE COPY

#8/10 Supp 2-14-03

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Attorney Docket No.: TRAN-P059

Inventor(s): Andrew Read, Sameer Halapete and Keith Klayman

Group Art Unit:

Filed: 10/23/00

Examiner:

Serial No.: 09/694,433

Title: STATIC POWER CONTROL

The Commissioner of Patents and Trademarks
Washington, D.C. 20231
Sir:

Information Disclosure Statement Submitted Pursuant to 37 C.F.R. 1.97(b)

The citations referenced herein, copies attached, may be material to the examination of the above-identified application and are, therefore, submitted in compliance with the duty of disclosure as defined in 37 C.F.R. 1.56. The Examiner is requested to make these citations of official record in the application.

This Information Disclosure Statement submitted in accordance with 37 C.F.R. 1.97(b) is not to be construed as a representation that a search has been made, that additional items material to the examination of this application do not exist, or that any one or more of these citations constitute prior art under 35 U.S.C. 102.

The Examiner's attention is respectfully directed to the following U.S. Patents:

Pat. No.	Pat. Title	Grant Date
5,592,173	GPS RECEIVER HAVING A LOW POWER STANDBY MODE	01/07/97
5,757,171	ON-BOARD VOLTAGE REGULATORS WITH AUTOMATIC PROCESSOR TYPE DETECTION	05/26/98
5,848,281	METHOD AND APPARATUS FOR POWDER MANAGEMENT IN A MULTIFUNCTION CONTROLLER WITH AN EMBEDDED MICRO-PROCESSOR	12/08/98
5,923,545	METHOD AND APPARATUS FOR PROVIDING MULTIPLE OUTPUT VOLTAGES FROM A VOLTAGE REGULATOR	07/13/99
6,118,306	CHANGING CLOCK FREQUENCY	09/12/00

The Examiner's attention is respectfully directed to the following documents:

"HIGH-SPEED DIGITALLY ADJUSTED STEP-DOWN CONTROLLERS FOR NOTEBOOK CPUS"; Max1710/Max1711; MAXIM Manual; page 11 and page 21

"OPERATIO U (Refer to Functional Diagram)" LTC1736; Linear Technology Manual page 9

02/05/2003 DEMMANU1 00000050 09694433

01 FC:1806 180.00 OP

rev. 6/97 jpw

Please direct all correspondence concerning the above-identified application to the following address:

WAGNER, MURABITO & HAO LLP
Two North Market Street, Third Floor
San Jose, California 95113
(408) 938-9060

Respectfully submitted,

Date: 27 Jan 2003

By: _____
Matthew J. Blecher
Reg. No. 46,588

2185

Patent

Docket No.: TRAN-P059

Information Disclosure Statement Transmittal

I hereby certify that this transmittal of the below described document is being deposited with the United States Postal Service in an envelope bearing First Class Postage and addressed to the Commissioner of Patents and Trademarks, Washington, D.C., 20231, on the below date of deposit.					
Date of Deposit:	01/27/03	Name of Person Making the Deposit:	KATHERINE RINALDI	Signature of the Person Making the Deposit:	Katherine Rinaldi

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Inventor(s): Andrew Read, Sameer Halapete and Keith Klayman — Group Art Unit:

Filed: 10/23/00 — Examiner:

Serial No.: 09/694,433

Title: STATIC POWER CONTROL

The Commissioner of Patents and Trademarks
Washington, D.C. 20231
Sir:

Information Disclosure Statement Transmittal

Transmitted herewith is the following:

..... Formal drawings, totaling ..... sheets.
..... Informal drawings, totaling ..... sheets.
..... Certification for PTO Consideration
..... Information Disclosure statement (__ sheets)
..X.. Information Disclosure statement and late filing fee
..X.. Form 1449
..... Petition for Extension of Time
..X.. Other: References

Fee Calculation (for other than a small entity)

Fee Items				Fee Rate	Total
Petition for Extension of Time (fee calculated elsewhere				$ .00	$0.00
Information Disclosure Statement, late filing				$180.00	$180.00
Other:					$0.00
Total Fees					$180.00

PAYMENT OF FEES

1. The full fee due in connection with this communication is provided as follows:

[X] The Commissioner is hereby authorized to charge any additional fees associated with this communication or credit any overpayment to Deposit Account No.: 23-0085 .
A duplicate copy of this authorization is enclosed.

[X] A check in the amount of $180.00

[ ] Charge any fees required or credit any overpayments associated with this filing to Deposit Account No.: 23-0085.

kgr 7/98

Please direct all correspondence concerning the above-identified application to the following address:

WAGNER, MURABITO & HAO LLP
Two North Market Street, Third Floor
San Jose, California 95113
(408) 938-9060

Respectfully submitted,

Date: 27 Jan 2003

By: _____
Matthew J. Blecher
Reg. No. 46,558

kgr 7/98

L Number	Hits	Search Text	DB	Time stamp
1	0	((("core voltage" and clock) and (cpu or processor or microprocessor)) and (low or sleep)) and (reduc$3 or cut$4)	JPO	2003/07/27 10:21
2	0	((("core voltage" and clock) and (cpu or processor or microprocessor)) and (low or sleep)) and (reduc$3 or cut$4)	JPO	2003/07/27 10:16
6	0	(("core voltage" and clock) and (cpu or processor or microprocessor)) and (low or sleep)	IBM_TDB	2003/07/27 10:16
3	1	(("core voltage" and clock) and (cpu or processor or microprocessor)) and (low or sleep)	EPO; JPO	2003/07/27 10:22
7	2	(("core voltage") and (cpu or processor or microprocessor)) and (low or sleep)	EPO; JPO	2003/07/27 10:19
10	2	"6202104"	USPAT	2003/07/27 10:19
11	0	(("core voltage" and clock) and (cpu or processor or microprocessor)) and (clock near3 disable)	JPO	2003/07/27 10:21
12	2	(("core voltage" and clock) and (cpu or processor or microprocessor)) and (clock near3 disable)	USPAT	2003/07/27 10:21
13	3381	("central processing unit" or cpu or processor or microprocessor) near4 (stop$3 or disable$1)	EPO; JPO	2003/07/27 10:24
16	12606	("central processing unit" or cpu or processor or microprocessor) near4 (stop$3 or disable$1)	USPAT	2003/07/27 10:24
17	0	(("central processing unit" or cpu or processor or microprocessor) near4 (stop$3 or disable$1)) and ("core voltage")	EPO; JPO	2003/07/27 10:24
20	13	(("central processing unit" or cpu or processor or microprocessor) near4 (stop$3 or disable$1)) and ("core voltage")	USPAT	2003/07/27 10:24
21	315	(stop$3 or disable$1) near4 clock with (cpu or processor or microprocessor or "central processing unit")	JPO	2003/07/27 10:46
22	28	((stop$3 or disable$1) near4 clock with (cpu or processor or microprocessor or "central processing unit")) with (reduc$3 or lower$3)	JPO	2003/07/27 10:39
24	120	(stop$3 or disable$1) near4 clock with (cpu or processor or microprocessor or "central processing unit") with (reduc$3 or lower$3)	USPAT	2003/07/27 10:48
23	20	(stop$3 or disable$1) near4 clock with (cpu or processor or microprocessor or "central processing unit")	EPO	2003/07/27 10:47
25	2	((stop$3 or disable$1) near4 clock with (cpu or processor or microprocessor or "central processing unit") with (reduc$3 or lower$3)) and (voltage adj1 regulator)	USPAT	2003/07/27 11:10
26	3	"5844435"	USPAT	2003/07/27 10:54
27	9	monitoring near6 (stop adj1 clock)	USPAT	2003/07/27 11:10

	Type	Hits	Search Text
1	BRS	321	"core voltage"
2	BRS	30	"core voltage"
3	BRS	1	"core voltage" and clock
4	BRS	73	"core voltage" and clock
5	BRS	47	("core voltage" and clock) and (cpu or processor or microprocessor)
6	BRS	44	(("core voltage" and clock) and (cpu or processor or microprocessor)) and (low or sleep)
7	BRS	41	((("core voltage" and clock) and (cpu or processor or microprocessor)) and (low or sleep)) and (reduc$3 or cut$4)
8	BRS	16	"core voltage" with regulator with (cpu or processor or microprocessor)

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/694,433	10/23/2000	Andrew Read	TRANS59	3072

7590 07/30/2003

WAGNER, MURABITO & HAO LLP
TWO NORTH MARKET STREET
THIRD FLOOR
SAN JOSE, CA 95113

EXAMINER	
CAO, CHUN	
ART UNIT	PAPER NUMBER
2185	7

DATE MAILED: 07/30/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

PTO-90C (Rev. 07-01)

Office Action Summary	Application No.	Applicant(s)	
	09/694,433	READ ET AL.	
	Examiner	Art Unit	
	Chun Cao	2185	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *23 October 2000* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-13* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-13* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) *6* .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

1. Claims 1-13 are presented for examination.

2. The title of the invention is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed. The current title is imprecise.

Claim Rejections - 35 U.S.C. § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless -

(a) the invention was known or used by others in this country, or patented or described in a printed publication in this or a foreign country, before the invention thereof by the applicant for a patent.

(e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371© of this title before the invention thereof by the applicant for patent.

The changes made to 35 U.S.C. 102(e) by the American Inventors Protection Act of 1999 (AIPA) do not apply to the examination of this application as the application being examined was not (1) filed on or after November 29, 2000, or (2) voluntarily published under 35 U.S.C. 122(b). Therefore, this application is examined under 35 U.S.C. 102(e) prior to the amendment by the AIPA (pre-AIPA 35 U.S.C. 102(e)).

4. Claims 1-13 are rejected under 35 U.S.C. 102 (a) or 102(e) as being anticipated by Orton et al. (Orton), US patent no. 6,118,306.

Orton is a prior reference cited by applicant in IDS paper no. 6.

As per claim 1, Orton teaches that a method for reducing power utilized by a processor comprising the steps of:

determining that a processor is transitioning from a computing mode to a mode is which system clock to the processor is disabled [col. 2, lines 44-60]; and

reducing core voltage to the processor to a value sufficient to maintain state during the mode of which system clock is disable; [col. 3, lines 10-20].

As per claim 2, Orton teaches of determining the processor is transitioning from a computing mode to a mode is which system clock to the processor is disabled comprising monitoring a stop clock signal [col. 2, lines 44-60; col. 5, lines 4-11; col. 7, lines 38-43].

As per claims 3 and 4, Orton teaches of reducing an output voltage providing by a voltage regulator furnishing core voltage to the processor and providing a feedback signal to the voltage regulator to reduce its output voltage below a specified output voltage [col. 2, lines 24-27; col. 3, lines 10-19; col. 7, lines 14-19, 44-58].

As per claims 5 and 6, Orton teaches of power dissipation during reductions in core voltage to a mode in which power is saved during the voltage transition [col. 2, lines 11-27, 44-60]; and returning the voltage regulator to its original mode of operation [col. 3, lines 10-14; col. 7, lines 51-58; col. 8, lines 54-65].

As per claims 7-13, Orton teaches the claimed method of steps in claims 1-6. Therefore, Orton teaches the claimed circuit having a voltage regulator to carry out the method of steps [figs. 1, 5; see claims 1-6 rejections state above].

5. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Any response to this action should be mailed to:

Commissioner of Patents and Trademarks

Washington, D.C. 20231

or faxed to:

(703) 746-7239, (for formal communications intended for entry)

Or:

(703) 746-7240 (for informal or draft communications, please label "PROPOSED" or "DRAFT")

Hand-delivered responses should be brought to Crystal Park II, 2121 Crystal Drive, Arlington. VA., Sixth Floor (Receptionist).

6. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Chun Cao at (703) 308-6106. The examiner can normally be reached on Monday-Friday from 7:30 am - 4:00 pm. If attempts to reach the examiner by phone are unsuccessful, the examiner's supervisor Thomas Lee can be reached at (703) 305-9717. The fax number for this Art Unit are followings: After-Final (703) 746-7238; Official (703) 746-7239; Non-Official (703) 746-7240.

Any inquiry of a general nature or relating to the status of this application should be directed to the Group receptionist whose telephone number is (703) 306-5631.

Chun Cao

July 27, 2003

Notice of References Cited	Application/Control No. 09/694,433	Applicant(s)/Patent Under Reexamination READ ET AL.	
	Examiner Chun Cao	Art Unit 2185	Page 1 of 1

U.S. PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Name	Classification
	A	US-6,442,746	08-2002	James et al.	716/14
	B	US-6,314,522	11-2001	Chu et al.	713/322
	C	US-6,304,824	10-2001	Bausch et al.	702/64
	D	US-6,279,048	08-2001	Fadavi-Ardekani et al.	710/15
	E	US-6,272,642	08-2001	Pole et al.	713/300
	F	US-6,202,104	03-2001	Ober, Robert Edmond	710/18
	G	US-5,933,649	08-1999	Lim et al.	713/322
	H	US-5,894,577	04-1999	MacDonald et al.	710/260
	I	US-5,884,049	03-1999	Atkinson, Lee W.	710/303
	J	US-5,825,674	10-1998	Jackson, Robert T.	713/321
	K	US-5,560,020	09-1996	Nakatani et al.	713/322
	L	US-			
	M	US-			

FOREIGN PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Country	Name	Classification
	N	409185589A	07-1997	JPO	Kato	
	O	0501655A2	02-1992	EPO	Suzuki et al.	
	P					
	Q					
	R					
	S					
	T					

NON-PATENT DOCUMENTS

*		Include as applicable: Author, Title Date, Publisher, Edition or Volume, Pertinent Pages)
	U	Madhav P. Desai et al., "Sizing of Clock Distibution Networks for high Performance CPU Chips" Digital Equipment Corporation 1996, pp 389-394.
	V	
	W	
	X	

*A copy of this reference is not being furnished with this Office action. (See MPEP § 707.05(a).)
Dates in MM-YYYY format are publication dates. Classifications may be US or foreign.

PAT-NO: JP409185589A

DOCUMENT-IDENTIFIER: JP 09185589 A

TITLE: INFORMATION PROCESSING SYSTEM AND POWER SAVING METHOD
FOR THE SYSTEM

PUBN-DATE: July 15, 1997

INVENTOR-INFORMATION:
NAME
KATO, MASAYA

ASSIGNEE-INFORMATION:
NAME COUNTRY
TOSHIBA CORP N/A

APPL-NO: JP08000201

APPL-DATE: January 5, 1996

INT-CL (IPC): G06F015/16, G06F015/16 , G06F001/32 , G06F001/04

ABSTRACT:

PROBLEM TO BE SOLVED: To effectively suppress the power consumption of the whole system by positively generating inactive processors even in a state where the number of tasks is over that of processors.

SOLUTION: In this information processing system, OS previously knows the resource request quantity of the processors 11 and 12 of the processing unit of each task including OS itself to centralize the group of tasks to the specific processor 11 within a range in which the resources of the processors 11 and 12 are not short (a range in which the sum of the request quantity of the

processor resources is not over 100). Thereby, the other **processor** 12 is brought into an inactive state so that power source supply for the inactive **processor is stopped or a clock** frequency is **lowered**. Thereby the power consumption of the whole system is effectively suppressed.

(19)日本国特許庁（ＪＰ）　(12) 公開特許公報（A）　(11)特許出願公開番号

特開平9－185589

(43)公開日　平成９年(1997)７月15日

(51)Int.Cl.⁶		識別記号	庁内整理番号	ＦＩ		技術表示箇所
Ｇ０６Ｆ	15/16			Ｇ０６Ｆ	15/16	Ｅ
		４３０				４３０Ｂ
	1/32				1/04	３０１Ｃ
	1/04	３０１			1/00	３３２Ｂ

審査請求　未請求　請求項の数５　ＯＬ　（全７頁）

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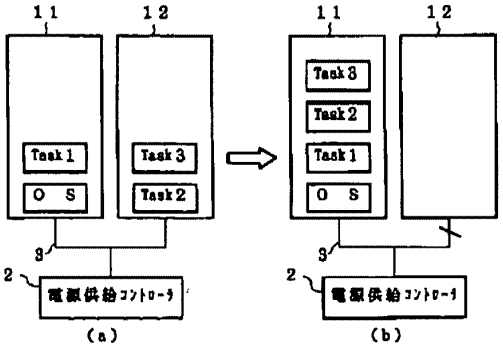
(71)出願人　000003078
株式会社東芝
神奈川県川崎市幸区堀川町72番地
(72)発明者　加藤　雅也
東京都青梅市末広町２丁目９番地　株式会社東芝青梅工場内
(74)代理人　弁理士　須山　佐一

(54)【発明の名称】　情報処理システムと情報処理システムの省電力方法

(57)【要約】
【課題】　従来、複数のプロセッサを有する情報処理システムにおいては、かりにプロセッサ毎にクロック周波数を可変できたとしても、この省電力機構による消費電力の節減効果は十分には得られないと言う課題があった。
【解決手段】　本発明の情報処理システムは、ＯＳが、ＯＳ自身を含め各タスクの処理単位のプロセッサ資源の要求量を事前に知り、プロセッサ資源が不足しない範囲（プロセッサ資源の要求量の和が１００を越えない範囲）でタスク群を特定のプロセッサに集中させる。これにより、他のプロセッサが休止状態となるので、この休止状態のプロセッサに対する電源供給を停止、或いはクロック周波数を下げる。これによりシステム全体の消費電力を効果的に抑制することが可能となる。



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【特許請求の範囲】
【請求項１】　複数のタスクを並列に処理可能な複数のプロセッサと、
前記タスクを構成する処理単位毎のプロセッサ資源の要求量に基づき、休止状態のプロセッサが発生するように前記複数のプロセッサのうちの特定のプロセッサにプロセッサ資源の不足が生じない範囲で複数のタスクを集めるタスク管理手段と、
前記休止状態のプロセッサに対する電源供給を停止する電源供給制御手段とを具備することを特徴とする情報処理システム。
【請求項２】　複数のタスクを並列に処理可能な複数のプロセッサと、
前記タスクを構成する処理単位毎のプロセッサ資源の要求量に基づき、休止状態のプロセッサが発生するように前記複数のプロセッサのうちの特定のプロセッサにプロセッサ資源の不足が生じない範囲で複数のタスクを集めるタスク管理手段と、
前記休止状態のプロセッサの動作クロック周波数を下げる手段とを具備することを特徴とする情報処理システム。
【請求項３】　複数のタスクを並列に処理可能な複数のプロセッサを備えた情報処理システムの省電力方法において、
前記タスクを構成する処理単位毎のプロセッサ資源の要求量に基づき、休止状態のプロセッサが発生するように前記複数のプロセッサのうちの特定のプロセッサにプロセッサ資源の不足が生じない範囲で複数のタスクを集め、前記休止状態のプロセッサに対する電源供給を停止することを特徴とする情報処理システムの省電力方法。
【請求項４】　複数のタスクを並列に処理可能な複数のプロセッサを備えた情報処理システムの省電力方法において、
前記タスクを構成する処理単位毎のプロセッサ資源の要求量に基づき、休止状態のプロセッサが発生するように前記複数のプロセッサのうちの特定のプロセッサにプロセッサ資源の不足が生じない範囲で複数のタスクを集め、前記休止状態のプロセッサの動作クロック周波数を下げることを特徴とする情報処理システムの省電力方法。
【請求項５】　請求項３または４記載の情報処理システムの省電力方法において、
前記タスクの処理単位の処理に要した時間と要求処理時間とから前記処理単位のプロセッサ資源の要求量を求めることを特徴とする情報処理システムの省電力方法。
【発明の詳細な説明】
【０００１】
【発明の属する技術分野】本発明は、複数のプロセッサを備えた情報処理システムとその省電力化の方法に関する。

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【０００２】
【従来の技術】プロセッサの高速化に伴う消費電力の増大を抑えるための手段としてクロックギアシステムがある。このクロックギアシステムは、プロセッサの動作クロック周波数を段階的に可変できるものとし、プロセッサが休止状態にある時はクロック周波数を下げることによってシステム全体の消費電力の節減効果を得るものである。
【０００３】ここで、複数のタスクを並列（時分割多重）に処理することが可能な複数のプロセッサを持つ情報処理システムを考える。また、処理の最大効率を得るため、タスク群は各プロセッサに均等な数で割り当てられるものとする。そして個々のプロセッサのクロック周波数は２段階に可変できるものとする。
【０００４】このような情報処理システムにおいて、全てのプロセッサがタスクを処理している場合、全プロセッサのクロック周波数は同一に設定され、全プロセッサの消費電力もほぼ同じである。また、タスクの数がプロセッサの数を下回った場合、休止状態のプロセッサが発生する。そこでこのプロセッサのクロック周波数を下げることによって、このプロセッサの消費電力が節減される。
【０００５】以下に、かかる省電力機構を備えた情報処理システムの問題点を述べる。
【０００６】上記情報処理システムにおいて消費電力の節減効果が得られるのは、タスクの数がプロセッサの数を下回った場合のような特定の状況に限られる。タスクの数がプロセッサの数以上の場合は、全てのプロセッサがタスク処理を実行するから、全てのプロセッサのクロック周波数は高いほうの値に設定される。タスクの数がプロセッサの数を下回ることは稀れであり、よって、かかる従来方式では、消費電力の十分な節減効果が期待できないと考えられる。
【０００７】
【発明が解決しようとする課題】このように従来、複数のプロセッサを有する情報処理システムにおいては、かりにプロセッサ毎にクロック周波数を可変できたとしても、この省電力機構による消費電力の節減効果は十分には得られないと言う問題があった。
【０００８】本発明はこのような課題を解決するためのもので、タスクの数がプロセッサの数を上回る状況においても休止状態のプロセッサを積極的につくりだすことによって、システム全体の消費電力を効果的に抑制することのできる情報処理システムとその省電力方法の提供を目的としている。
【０００９】
【課題を解決するための手段】本発明の情報処理システムは上記した目的を達成するために、複数のタスクを並列に処理可能な複数のプロセッサと、タスクを構成する処理単位毎のプロセッサ資源の要求量に基づき、休止状

態のプロセッサが発生するように複数のプロセッサのうちの特定のプロセッサにプロセッサ資源の不足が生じない範囲で複数のタスクを集めるタスク管理手段と、休止状態のプロセッサに対する電源供給を停止する電源供給制御手段とを具備することを特徴とする。

【００１０】また、本発明の情報処理システムの省電力方法は、複数のタスクを並列に処理可能な複数のプロセッサを備えた情報処理システムの省電力方法において、タスクを構成する処理単位毎のプロセッサ資源の要求量に基づき、休止状態のプロセッサが発生するように複数のプロセッサのうちの特定のプロセッサにプロセッサ資源の不足が生じない範囲で複数のタスクを集め、休止状態のプロセッサに対する電源供給を停止することを特徴とする。

【００１１】これらの発明においては、タスクを構成する処理単位毎のプロセッサ資源の要求量に基づき、複数のプロセッサのうちの特定のプロセッサにプロセッサ資源の不足が生じない範囲で複数のタスクを集めることで、特定プロセッサをフル稼働に近い状態にする一方、休止状態のプロセッサをつくりだす。この休止状態のプロセッサに対する電源供給を停止することによって、システム全体の消費電力を節減することができる。

【００１２】さらに本発明の情報処理システムは上記した目的を達成するために、複数のタスクを並列に処理可能な複数のプロセッサと、タスクを構成する処理単位毎のプロセッサ資源の要求量に基づき、休止状態のプロセッサが発生するように複数のプロセッサのうちの特定のプロセッサにプロセッサ資源の不足が生じない範囲で複数のタスクを集めるタスク管理手段と、休止状態のプロセッサの動作クロック周波数を下げる手段とを具備することを特徴とする。

【００１３】また、本発明の情報処理システムの省電力方法は、複数のタスクを並列に処理可能な複数のプロセッサを備えた情報処理システムの省電力方法において、タスクを構成する処理単位毎のプロセッサ資源の要求量に基づき、休止状態のプロセッサが発生するように複数のプロセッサのうちの特定のプロセッサにプロセッサ資源の不足が生じない範囲で複数のタスクを集め、休止状態のプロセッサの動作クロック周波数を下げることを特徴とする。

【００１４】これらの発明においては、タスクを構成する処理単位毎のプロセッサ資源の要求量に基づき、複数のプロセッサのうちの特定のプロセッサにプロセッサ資源の不足が生じない範囲で複数のタスクを集めることで、特定プロセッサをフル稼働に近い状態にする一方、休止状態のプロセッサをつくりだす。この休止状態のプロセッサの動作クロック周波数を下げることによって、システム全体の消費電力を節減することができる。

【００１５】

【発明の実施の形態】以下、この発明の実施の形態につ

いて図面を参照して説明する。

【００１６】図１は本実施形態である情報処理システムの全体的な構成を示す図である。

【００１７】同図に示すように、この情報処理システムは複数例えば４つのプロセッサ１１、１２、１３、１４と各プロセッサへの電源供給を制御する電源供給コントローラ２とを備えて構成される。各プロセッサと電源供給コントローラ２とは相互にバス３及び電源線４を通じて接続されている。個々のプロセッサは各々、複数のタスクを並列（時分割多重）に処理することが可能である。

【００１８】この情報処理システムにおいては、タスク群を特定のプロセッサにそのプロセッサの資源が許す範囲で集中させることで、できるだけ多くのプロセッサが休止状態となるように、各プロセッサに対するタスクの割り当てが行われる。

【００１９】その様子を図２に示す。簡単化のため、この例では２つのプロセッサ１１、１２間でのタスクの移動を示す。同図（ａ）はタスク移動前の状態であり、プロセッサ１１はＯＳとタスク（Task１）を有する。またプロセッサ２はタスク（Task２）とタスク（Task３）を有する。

【００２０】ここで、ＯＳ、タスクの“プロセッサ資源の要求量”について説明する。“プロセッサ資源の要求量”とは、ＯＳ、タスクの処理を行う上でプロセッサの能力のどのくらいの割合を必要とするかを示す値であり、プロセッサをフル稼働させてＯＳ、タスク内の処理単位（関数単位、ブロック単位等の各部位、１つのタスクが１つの処理単位となる場合もある。）を実行した場合の処理時間をＴ１とし、その処理単位の要求処理時間をＴ２として、（Ｔ１／Ｔ２）×１００の計算式で求めることができる。例えば、タスク内のある処理単位の要求処理時間Ｔ２を１０ｍｓ、その処理単位をプロセッサをフル稼働させて実行した場合の処理時間Ｔ１を５ｍｓとすれば“プロセッサ資源の要求量”は（５／１０）×１００＝５０（％）となる。

【００２１】図２において、ＯＳの現在の処理単位のプロセッサ資源の要求量は２５、同じくタスク（Task１）は３０、タスク（Task２）は２０、タスク（Task３）は２０とする。また２つのプロセッサ１１、１２の性能は同一とする。図２（ａ）のタスク移動前の状態において、一方のプロセッサ１１が所有するＯＳとタスク（Task１）の現在のプロセッサ資源の要求量の和は５５、他方のプロセッサ１２が所有するタスク（Task２）とタスク（Task３）の現在のプロセッサ資源の要求量の和は４０である。したがって、プロセッサ１１は１００－５５＝４５のプロセッサ資源を余しており、図２（ｂ）に示すように、プロセッサ１２の所有するタスク（Task２）とタスク（Task３）をプロセッサ１１に移動させても、プロセッサ１１においてＯＳと全タスクを並列に処理す

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ることが可能である。

【００２２】本実施形態の情報処理システムは、このようなタスクの移動・割り当て処理をＯＳの管理の下で実行する。ＯＳはＯＳ自身を含め各タスクの処理単位のプロセッサ資源の要求量を事前に知り、プロセッサ資源が不足しない範囲（プロセッサ資源の要求量の和が１００を越えない範囲）でタスク群を特定のプロセッサに集中させるように各プロセッサに対するタスクの割り当てを制御する。各タスクには、プロセッサ資源の要求量を示す情報が処理単位毎に付加されており、これを基にＯＳは現在の各タスクのプロセッサ資源の要求量を知る。勿論、ＯＳ自身にもプロセッサ資源の要求量を示す情報が付加されている。

【００２３】図２に示したように、プロセッサ１２の全てのタスク（Task２，Task３）をプロセッサ１１に移動させたことによって、プロセッサ１２は休止状態となる。ＯＳは、プロセッサ１２が休止状態になったことを知ると、電源供給コントローラ２に命令を出し、プロセッサ１２への電源供給を停止させる。

【００２４】図３は新たなタスク（Task４）が発生した場合を示している。このタスク（Task４）のこれから処理しようとしている処理単位のプロセッサ資源の要求量は２０である。今、プロセッサ１１が所有しているＯＳと３つのタスク（Task１，Task２，Task３）のプロセッサ資源の要求量の和は９５であるから、これに新たなタスク（Task４）のプロセッサ資源の要求量を加えると９５＋２０＝１１５となってプロセッサ１１のプロセッサ資源を越えてしまう。そこでこの場合、ＯＳは電源供給コントローラ２に命令を出してプロセッサ１２への電源供給を復活させると共に、新たなタスク（Task４）をプロセッサ１２に割り当てて、プロセッサ１２にタスク（Task４）の処理を実行させる。

【００２５】また、図２に示すプロセッサ１１がＯＳと３つのタスク（Task１，Task２，Task３）を保有する状態において、いずかのタスクのこれから処理しようとする処理単位のプロセッサ資源の要求量が増加してプロセッサ１１に対するプロセッサ資源の要求量の和が１００を越える場合、ＯＳはこれを判断していずかのタスクを他方のプロセッサ１２に移動させる。

【００２６】例えば、図４に示すように、タスク（Task２）のこれから処理する処理単位のプロセッサ資源の要求量が３０であるとする。この場合、ＯＳと３つのタスク（Task１，Task２，Task３）のプロセッサ資源の要求量の和は２５＋３０＋３０＋２０＝１０５となり、１００を越えてしまため、いずかのタスクを他方のプロセッサ１２に移動させる。この例では、どのタスクを移動させてもプロセッサ１１に要求されるプロセッサ資源量の和は１００未満となるので、どのタスクをプロセッサ１２に移動させてもよい。

【００２７】前述したように、以上のタスク移動・割り当て制御を実現するためには、各タスクにプロセッサ資源の要求量を示す情報を付加しておく必要がある。タスクにプロセッサ資源の要求量を示す情報を付加する方法としては次のようなものを挙げることができる。

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【００２８】図５において、５１はソースプログラム、５２はソースプログラム５１からオブジェクトプログラム５３を生成するコンパイラ、アセンブラ等の言語処理系、５４はオブジェクトプログラム５３を連結編集して一つのプロセッサ実行形式のプログラム（タスク）５５を生成するリンカである。

【００２９】タスクにプロセッサ資源の要求量を示す情報を付加する第１の方法は、プログラム製作者自身がタスクの処理単位毎のプロセッサ資源の要求量を求めることによってソースコード或いはオブジェクコードで記述された資源記述ファイル６を作成し、言語処理時或いはリンカ時に、資源記述ファイル６の記述内容をタスク本体に付加する方法である。また、タスクのソースプログラム１自体にプロセッサ資源の要求量のソースコードを一体化させてもよい。この場合、タスクのソースプログラム１の各部位にＣ言語におけるpragmaのような記述方法でプロセッサ資源の要求量を示す情報を挿入する方法が考えられる。

【００３０】第２の方法は、第１の方法の資源記述ファイル６に代えてタスクの処理単位の要求処理時間を記述した要求処理時間記述ファイルをプログラム製作者自身が作成し、言語処理系が、そのファイルに記述された要求処理時間に基づいて各処理単位のプロセッサ資源の要求量を算出してオブジェクトコード化し、これをタスク本体のオブジェクトコードに付加する方法である。この第２の方法は、第１の方法に比べプログラム製作者の作業負担を軽くすることができる。

【００３１】第３の方法は、プロセッサにおいてタスクの処理を実際に実行してみて、その処理に要した時間と、第２の方法で用いた要求処理時間記述ファイルに記述された要求処理時間とからプロセッサ資源の要求量を計算する方法である。前述したように、プロセッサ資源の要求量は、例えば、プロセッサをフル稼働させてタスク内の処理単位を実行した場合の処理時間をＴ１、その処理単位の要求処理時間をＴ２として（Ｔ１／Ｔ２）×１００の計算式で求めることができる。

【００３２】このプロセッサ資源の要求量の計算は、情報処理システムを実際に運用する前にプロファイリング期間を設け、このプロファイリング期間に全てのタスクの処理単位について行うようにすることが望ましい。

【００３３】かくして本実施形態の情報処理システムによれば、特定のプロセッサにそのプロセッサ資源の不足が生じない範囲で多くのタスクを集中させることで、その他のプロセッサを積極的に休止状態にし、これら休止状態のプロセッサに対する電源供給を停止することによって、システム全体の消費電力を効果的に抑制すること

が可能となる。

【００３４】なお、本実施形態では、休止状態のプロセッサに対する電源供給を停止するようにしたが、プロセッサ毎のクロック周波数を可変できるように構成し、休止状態のプロセッサに対するクロック周波数を下げることによっても消費電力の節減効果が得られる。

【００３５】

【発明の効果】以上説明したように本発明によれば、タスクを構成する処理単位毎のプロセッサ資源の要求量に基づき、複数のプロセッサのうちの特定のプロセッサにプロセッサ資源の不足が生じない範囲で複数のタスクを集めることで、特定プロセッサをフル稼働に近い状態にする一方、休止状態のプロセッサをつくりだし、この休止状態のプロセッサに対する電源供給を停止することによって、システム全体の消費電力を節減することができる。

【００３６】また、本発明によれば、タスクを構成する処理単位毎のプロセッサ資源の要求量に基づき、複数のプロセッサのうちの特定のプロセッサにプロセッサ資源の不足が生じない範囲で複数のタスクを集めることで、特定プロセッサをフル稼働に近い状態にする一方、休止状態のプロセッサをつくりだし、この休止状態のプロセッサの動作クロック周波数を下げることによって、システム全体の消費電力を節減することができる。

【図面の簡単な説明】

【図１】本実施形態である情報処理システムの全体的な構成を示す図

【図２】図１の情報処理システムにおけるタスク移動を説明するための図

【図３】図１の情報処理システムにおいて新たなタスクが発生した場合のタスク割り当てを説明するための図

【図４】図１の情報処理システムにおいて処理単位のプロセッサ資源の要求量が増大した場合のタスク移動を説明するための図

【図５】プロセッサ資源の要求量の情報をタスクに付加する方法を説明するための図

【符号の説明】

２……電源供給コントローラ

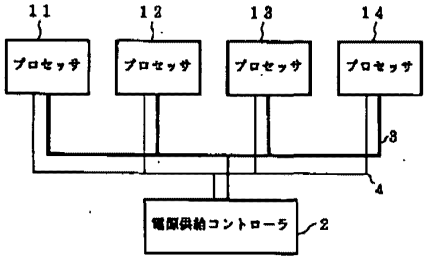
３……バス

４……電源線

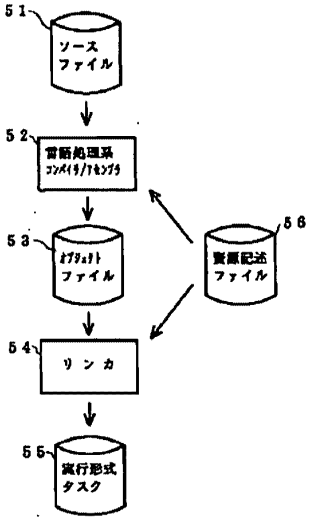
１１、１２、１３、１４……プロセッサ

５６……資源記述ファイル

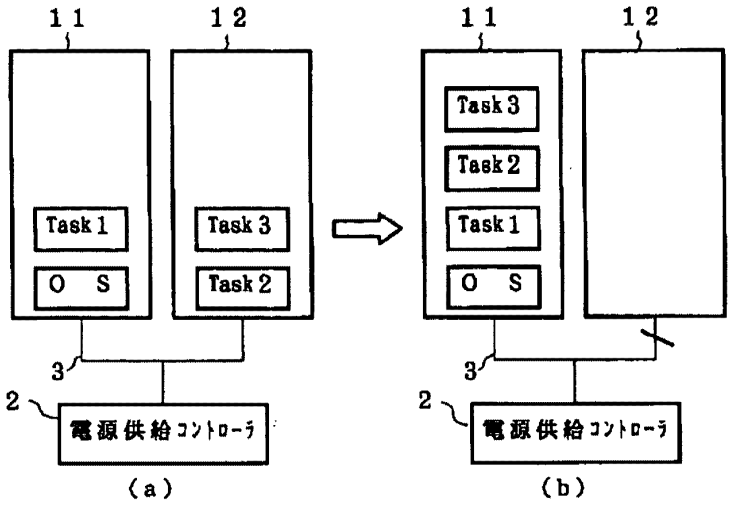
【図１】



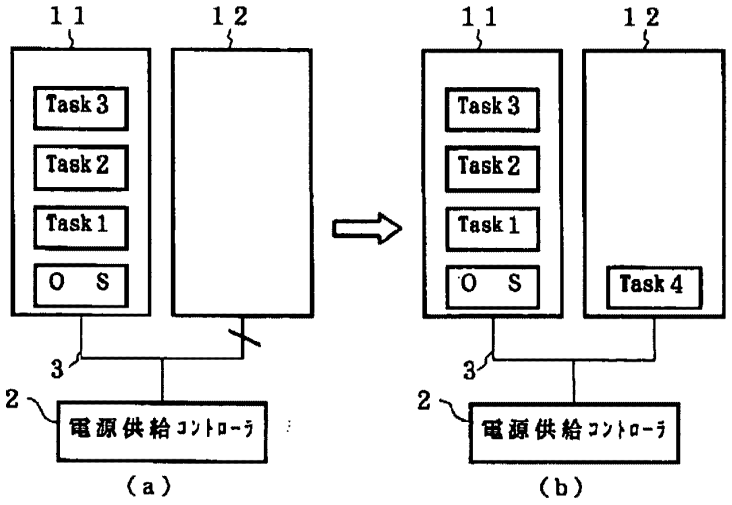
【図５】



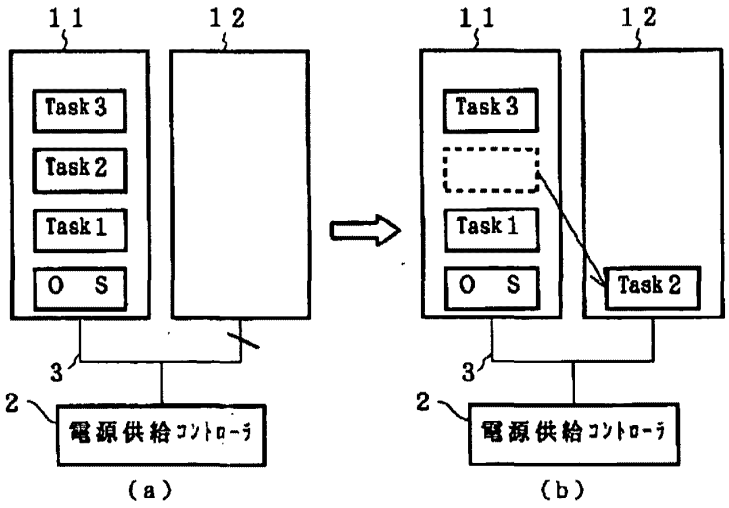
【図2】


11
12
Task 1
O S
Task 3
Task 2
3
2
電源供給コントローラ
(a)
11
12
Task 3
Task 2
Task 1
O S
3
2
電源供給コントローラ
(b)

【図3】


11
12
Task 3
Task 2
Task 1
O S
3
2
電源供給コントローラ
(a)
11
12
Task 3
Task 2
Task 1
O S
Task 4
3
2
電源供給コントローラ
(b)

【図4】


11
12
Task 3
Task 2
Task 1
O S
3
2
電源供給コントローラ
(a)
11
12
Task 3
Task 1
O S
Task 2
3
2
電源供給コントローラ
(b)

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(71) Applicant : **International Business Machines Corporation**
Old Orchard Road
Armonk, N.Y. 10504 (US)

(72) Inventor : **Suzuki, Naoshi**
3-1-2-916 Kyomachi
Kawasaki-ku, Kanagawa-ken (JP)
Inventor : **Uno, Shunya**
Sunwhite M401-13, 4-8-7 Minaminaruse
Machida-shi, Tokyo (JP)

(74) Representative : **Killgren, Neil Arthur**
IBM United Kingdom Limited Intellectual Property Department Hursley Park
Winchester Hampshire SO21 2JN (GB)

(54) Reducing power consumption in a digital processor.

(57) The supply of the clock signal to the processor in a multi-tasking system is controlled by a program (CCP) that runs in the lowest priority under the operating system (OS), so that applications (A,B,) are not affected when clock signals are stopped or slowed to reduce power dissipation.

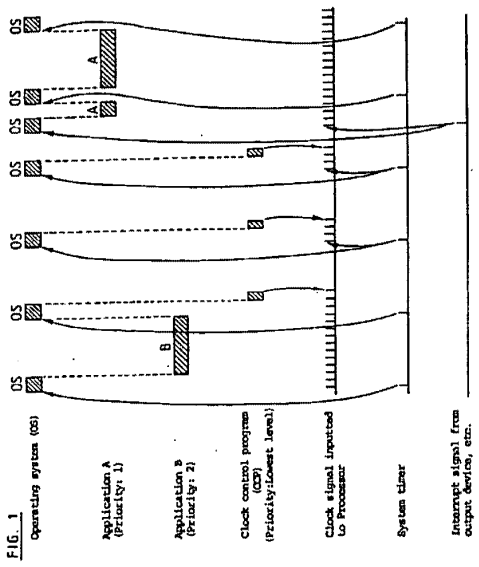


FIG. 1

EP 0 501 655 A2

The present invention relates to reducing the power consumption of a digital processor. Such reduction is desirable particularly to reduce heat dissipation in data processing apparatus including digital processors.

In a known type of processor the contents of its internal registers are not lost even if the supply of a clock signal to the processor is stopped. Operations can be resumed from the stop state by reopening the supply of the clock signal. Such a processor is referred to herein as a full-static processor and, if it uses CMOS logic, power consumption and heat dissipation can be greatly reduced by stopping the supply of a clock signal to the processor, or decreasing the frequency of the clock signal, while the processor idle.

Japanese Published Unexamined Patent Application (PUPA) No.62-169219 (U.S. Pat. No.4,851,987) discloses an information processing system in which the supply of a clock signal to a processor is stopped according to a result of the execution of a program which determines whether the system is currently in a state where it waits for the completion of an operation of an input/output device or key input by an operator. However, even though the system waits for the completion of the operation of the input/output device or key input by the operator, the processor is not always used to be in an idle time. Particularly, in an information processing system using a multi-tasking operating system, possibility that a processor runs a second task while waiting for the completion of an operation of an input/output device or key input by an operator is not insignificant. In such a conventional apparatus there is therefore a danger that the supply of a clock signal to the processor may be stopped while the processor runs the task.

It is accordingly an object of the present invention to provide an information processing system and a method for operating such a system which minimises this danger.

According to the present invention there is provided an information processing apparatus using a multi-tasking operating system, a method for controlling a processor clock signal wherein the supply of a processor clock signal to a processor is controlled by a program which runs in the lowest priority under said multi-tasking operating system.

There is further provided an information processing system including a full static processor, a clock signal generator for supplying the clock signal to said processor, and a clock signal controller for controlling the supply of the clock signal to said processor from said clock signal generator when a program given the lowest priority runs under a multi-tasking operating system.

An information processing system is usually provided with a system timer for synchronising the entire system in addition to a generator or oscillator for generating the clock signal to be supplied to the processor. Under the multi-tasking operating system, tasks to run are switched to one another according to a priority given to each task for each time interval indicated by the system timer. Now in a case where a program (clock control program) that controls the supply of the clock signal to the processor is provided, and the clock control program is given the lowest priority, the clock control program runs if only the clock control program runs and any other tasks does not run, that is, only if the processor may be stopped. Thereby, the supply of the clock signal to the processor can be certainly controlled on or off for each time interval indicated by the system timer. Instead of stopping the supply of the clock signal to the processor, the frequency of the clock signal may be controlled so that it can be decreased.

In order that the invention may be well understood a preferred embodiment thereof will now be described by reference to the accompanying drawings, in which:-

FIG.1 is a time chart showing the operations of the embodiment of an information processing system constructed in accordance with the present invention.

FIG.2 is a block diagram showing the overall construction of said embodiment.

FIG.3 is a flowchart showing a method for controlling processor clock signals and processing steps according to the present invention.

FIG.2 shows the overall construction of an embodiment of an information processing system according to the present invention. Referring to the figure, a processor 10 connects to a clock signal line 21, an interrupt signal line 22, and a signal lines 23. The signal line 23 is comprised of a plurality of signal lines for a control signal, an address signal, and a data signal other than an interrupt signal and connected to a memory 30 and a system timer 70. The signal line 23 and the interrupt signal line 22 may be called a system bus 20. The memory 30 stores a multi-tasking operating system MOS, a clock control program CCP that runs in the lowest priority under the multi-tasking operating system MOS, and application programs A and B.

The clock signal line 21 and the interrupt signal line 22 connect to a clock signal controller 40. The clock signal controller 40 comprises a clock signal on-off switcher 41, a signal transition detector 42, and a register 43. The clock signal on-off switcher 41 is always supplied with a clock signal for the processor from a generator 50, stopping the supply of the clock signal to the processor 10 in response to a clock stopping signal from the register 43, reopening the supply of the clock signal to the processor 10 in response to a clock reopening signal from the signal transition detector 42. The signal transition detector 42 connects to an interrupt signal controller 60. The signal transition detector 42, when receiving an interrupt signal from the interrupt signal controller 60, gives the

interrupt signal to the processor 10 and the clock reopening signal to the clock signal on-off switcher 41.

To the interrupt signal controller 60, in addition to interrupt signals from input/output devices such as a keyboard, a disk storage, a printer, etc., a signal from the system timer are inputted. When receiving these signals, the interrupt signal controller 60 outputs the interrupt signal to the signal transition detector 42. Thereby, except that the interrupt signals from the input/output devices are received, the supply of the clock signal to the processor 10 is reopened when the system timer 70 indicates the lapse of a predetermined time. Under the multi-tasking operating system MOS, task execution is switched for each time interval indicated by the system timer 70. The register 43 is used for receiving and holding a result of the execution of the clock control program CCP given the lowest priority.

Now the operations of the embodiment are described by reference to FIG.1 in addition to FIG.2. Generally, in the multi-tasking operating system, a task scheduler, which is one of the component programs of the operating system, switches tasks on or off based on time slicing in which the task scheduler gives plural tasks the execute right of the processor according to their priority for each predetermined time interval at the completion of a running task or based on a event-driven method in which the execute right of the processor is transferred in response to occurrence of an event such as an interruption, as in the embodiment. Time quanta of time slices are determined by the system timer 70.

FIG.1 shows a state where the execution of plural tasks including the clock control program CCP given the lowest priority is switched under the multi-tasking operating system OS and a condition that the supply of a clock signal to the processor 10 is controlled on or off. Now if the system timer 70 issues a signal indicating the lapse of a predetermined time interval over the signal line 23 while the application program B given priority 2 is running, an object of program execution temporarily changes from the application program B to the operating system OS. The operating system OS not only determines whether the application program B has the execute right of the processor 10 even in the following quantum of time, but also selects any of programs that require the execute right of the processor 10 in the following quantum of time and gives it the execution right.

FIG.1 shows a case where only the clock control program CCP requires the execute right of the processor 10. In this case, the clock control program CCP runs and, as a result, a signal indicating that a clock signal may be stopped is sent to the register 43 of the clock controller 40 through the signal line 23. Since the clock control program CCP does nothing but simple work as described above, its execution time is very short. The register 43 not only holds said signal, but also provides a clock stopping signal to the clock signal on-off switcher 41 to stop the supply of the clock signal to the processor 10.

If the supply of the clock signal to the processor 10 stops and then the system timer 70 issues a signal indicating the lapse of a predetermined time, the interrupt signal controller 60 provides an interrupt signal to the signal transition detector 42 and then the signal transition detector 42 provides a clock reopening signal to the clock signal on-off switcher 41 to not only reopen the supply of the clock signal to the processor 10, but also provide an interrupt signal to the processor 10. The processor 10, on receiving the interrupt signal, prompts a timer interrupt handler and a dispatcher, which are the component programs of the operating system OS, to run and determines a program to be run in the following quantum of time after they run.

FIG.1 shows also a case where a program to be run in the following quantum of time is only the clock control program CCP. Also in this case, the clock control program CCP runs to stop the supply of a clock signal to the processor 10. If the interrupt signal controller 60 issues an interrupt signal while the supply of the clock signal to the processor 10 is stopping, not only the supply of the clock signal to the processor 10 is reopened, but also the operating system OS performs functions to determine a program to be run in the following quantum of time. If the program to be run is the application program A given priority 1, the application program A runs until the system timer 70 issues the following signal. When the system timer 70 issues the signal, the operating system functions to determine a program to be run in the following quantum of time and if the program thus determined is the application program A, the program A runs again until the system timer 70 issues the following signal.

FIG.3 shows processing steps for stopping the supply of a clock signal to the processor under the multi-tasking operating system. In the figure, both an interrupt handler and a task dispatcher are the component programs of a task scheduler of the operating system. The interrupt handler is a program that runs in response to an interrupt signal to do work required for stopping and then reopening an application running before receiving the interrupt signal. The task dispatcher is a program that determines the following task to be run according to priority given to each task and transfers the execute right of the processor to the task thus determined.

Referring to FIG.3, in a step S11 an application program given priority other than the lowest priority runs. In a subsequent step S12, whether said application program is completed or not is determined. If the application program is not completed, the processing proceeds to a step S13 where the application program continues to run. If the application program is completed, the processing proceeds to a step S16.

If an interrupt signal is encountered in a step S14 during the run of the application program, the processing proceeds to a step S15 where the interrupt handler runs and then the task dispatcher is started in the step S16. The task dispatcher determines whether the running application program is authorised to run also in the subsequent quantum of time or not (in a step S17). If the application program is authorised to run in the subsequent quantum of time, the processing returns to the step S11. If the application program is not authorised to run, whether another application program requests authorisation for running or not is determined in a step S18. If another application requests to be authorised to run, the application program runs in a step S19. Otherwise, the processing proceeds to a step S21 where the clock control program (given the lowest priority) for stopping a clock signal is started. In a subsequent step S22, the clock control program runs to send a signal indicating that the supply of the clock signal is stopped, to the register 43 of the clock signal controller 40 and in a step S23 the supply of the clock signal is stopped.

According to the above embodiment, since the clock control program runs only if there is no other tasks to be run, the supply of the clock signal is not in danger of being stopped while some task is running in a background. Further, according to the embodiment, since the on-off control for the clock signal is performed for each timer interval indicated by the system timer, the clock signal is stopped in a small slice of the idle time for the processor and thereby low power dissipation is offered.

It will be recognised that said clock signal controller 40 may be connected to a processor, not the processor 10 and added to another program. It will be appreciated that instead of stopping the supply of a clock signal to the processor 10, the frequency of the clock signal may be decreased to attempt low power dissipation.

As described above, according to the present invention, a method and an information processing system which ensure that an allowed time to stop a processor or an allowed time to delay an operation of the processor is determined to stop the supply of a clock signal to the processor or decrease the frequency of the clock signal, can be provided.

Claims

1 In an information processing apparatus using a multi-tasking operating system, a method for controlling a processor clock signal wherein the supply of a processor clock signal to a processor is controlled by a program which runs in the lowest priority under said multi-tasking operating system.

2 The method for controlling a processor clock signal according to claim 1 wherein said program is adapted to open or to close the supply of clock signals to the processor.

3 The method for controlling a processor clock signal according to claim 1 wherein said program is adapted to change the frequency of the clock signal provided to the processor from an operating frequency to a reduced idle frequency and vice versa.

4 An information processing system including a full static processor, a clock signal generator for supplying the clock signal to said processor, and a clock signal controller for controlling the supply of the clock signal to said processor from said clock signal generator when a program given the lowest priority runs under a multi-tasking operating system.

5 A system as claimed in claim 4 in which said clock signal controller is adapted to change the frequency of said clock signal from an operating frequency to an idling frequency and vice versa.

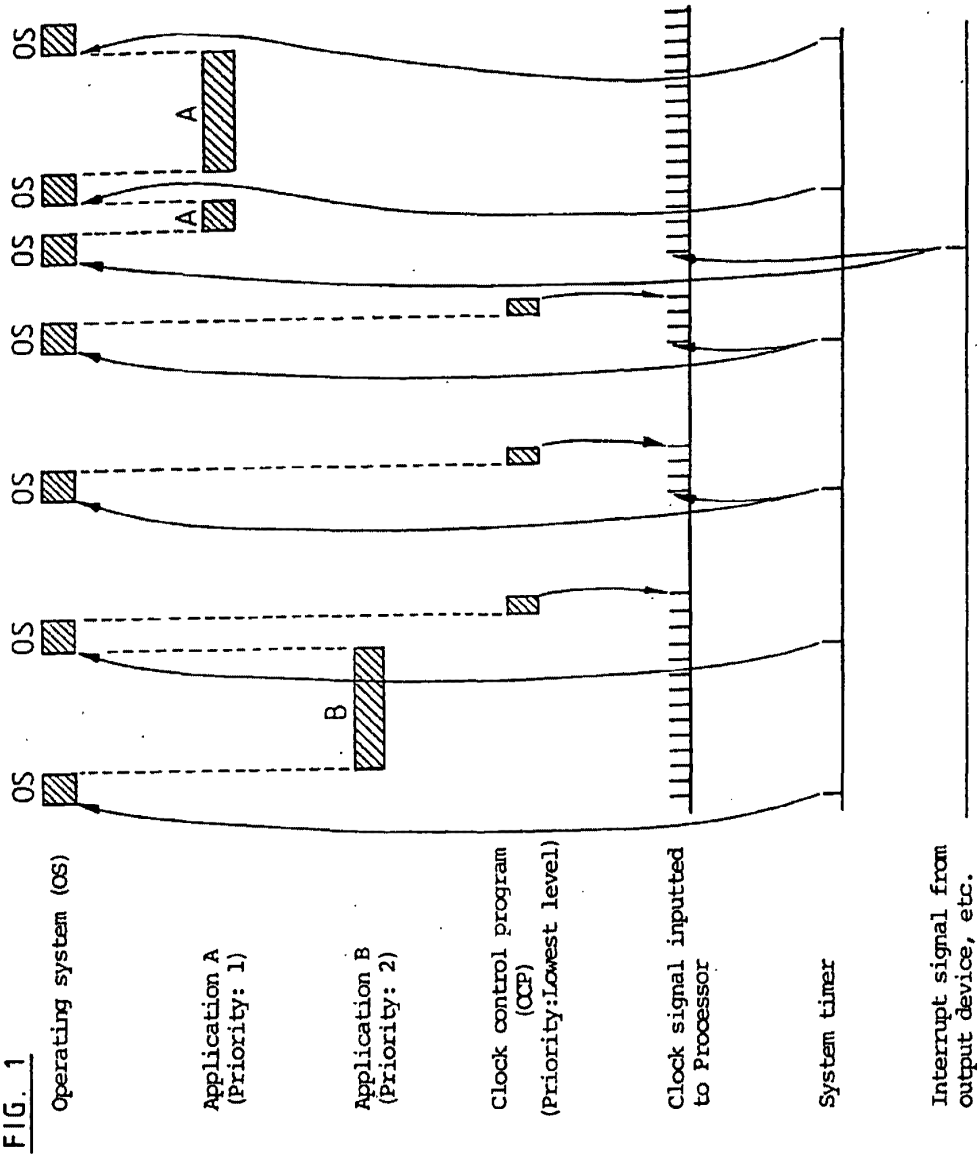
6 A system as claimed in claim 4 in which said clock signal controller is adapted to open or to close the supply of clock signals to said processor.

7 The information processing system according to claim 6 wherein said clock signal controller is adapted to reopen the supply of a clock signal to said processor in response to an interrupt signal to said processor.

8 The information processing system according to claim 7 wherein said interrupt signal is an output signal from a system timer for synchronising the entire information processing system.

9 An information processing system as claimed in any of claims 4 to 8 including a memory, a processor, an input/output device, a generator for supplying a clock signal to said processor, and a system timer for synchronising among the parts of the system, wherein a clock signal controller is provided for the purpose of stopping the supply of the clock signal to the processor by means of a program that runs in the lowest priority under a multi-tasking operating system and reopening the supply of said clock signal in response to an interrupt signal from said input/output device or said system timer.

FIG. 1



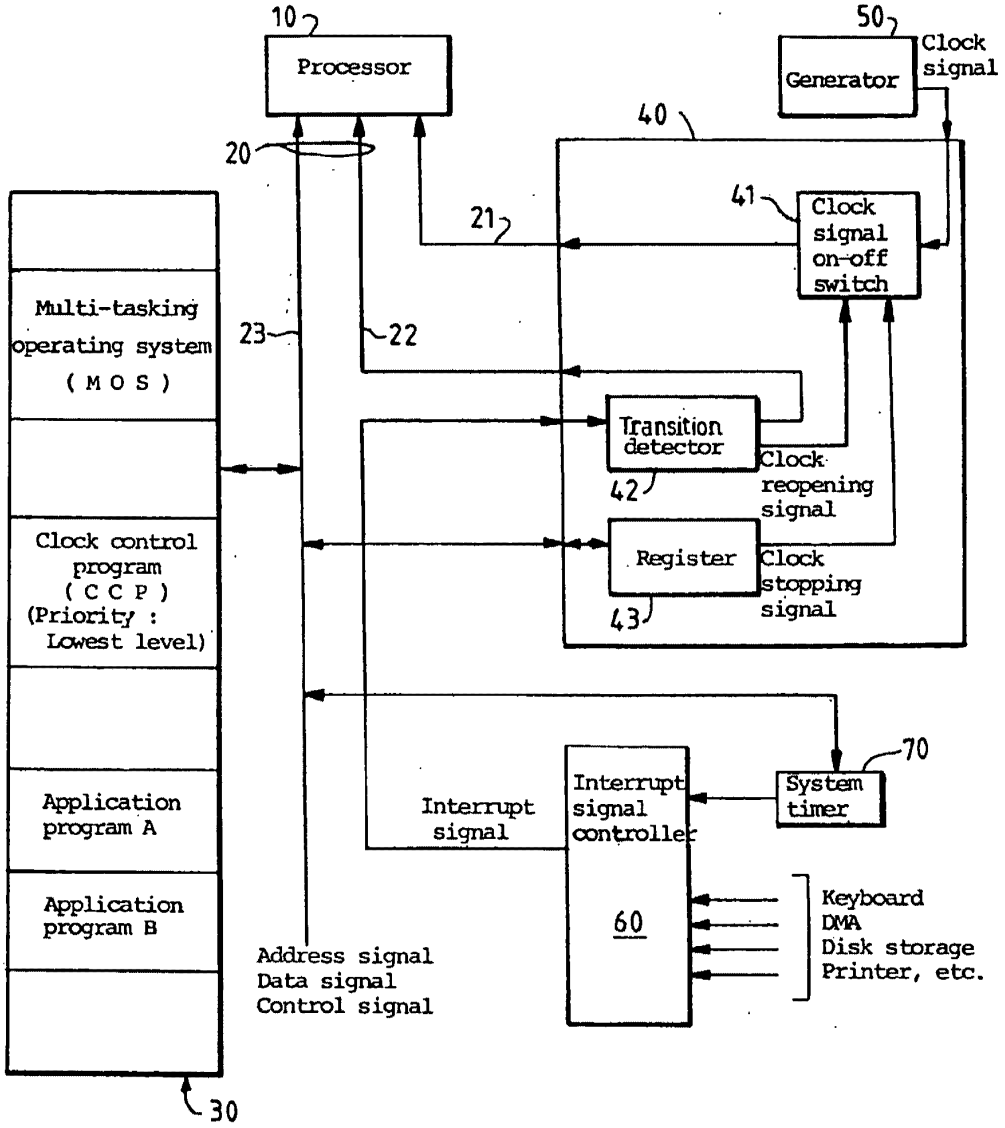


FIG 2

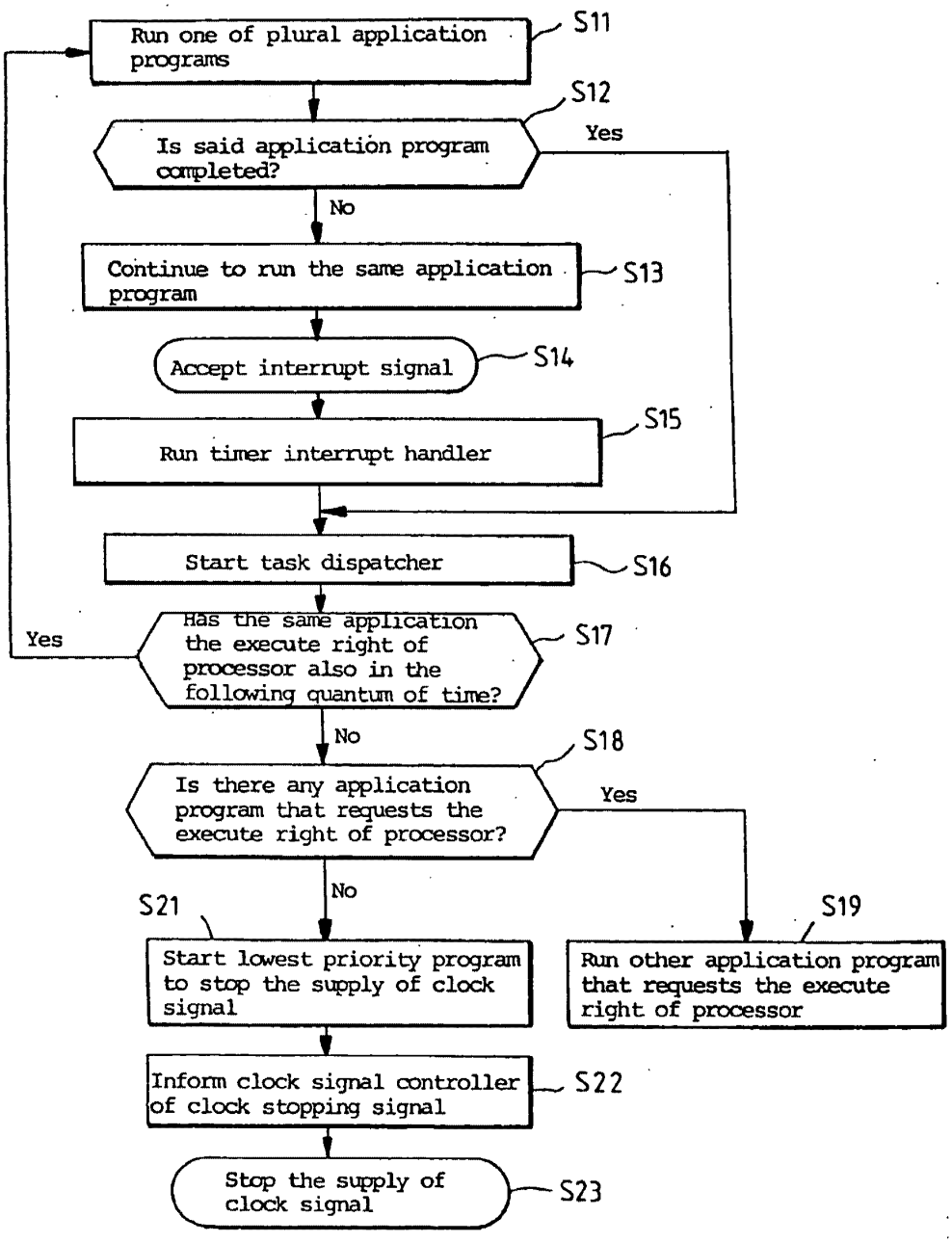


FIG. 3

Attorney Docket No.: TRAN-P059

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Patent Application

Inventor(s): Andrew Read, Sameer Halapete and Keith Klayman

Group Art Unit:

Filed: 10/23/00

Examiner:

Serial No.: 09/694,433

Title: STATIC POWER CONTROL

Form 1449

U.S. Patent Documents

Examiner Initial	No.	Patent No.	Date	Patentee	Class	Sub-class	Filing Date
C	A	5,592,173	01/07/97	Lau et al.	342	357	07/18/94
C	B	5,757,171	05/26/98	Babcock	323	271	12/31/96
C	C	5,848,281	12/08/98	Smalley et al.	395	750.04	07/23/96
C	D	5,923,545	07/13/99	Nguyen	363	24	05/18/98
C	E	6,118,306	09/12/00	Orton et al.	327	44	04/30/99
	F						

Foreign Patent or Published Foreign Patent Application

Examiner Initial	No.	Document No.	Publication Date	Country or Patent Office	Class	Sub-class	Translation Yes	Translation No
	G							
	H							
	I							

Other Documents

Examiner Initial	No.	Author, Title, Date, Place (e.g. Journal) of Publication
C	J	"HIGH-SPEED DIGITALLY ADJUSTED STEP-DOWN CONTROLLERS FOR NOTEBOOK CPUS"; Max1710/Max1711; MAXIM Manual; page 11 and page 21
C	K	"OPERATIO U (Refer to Functional Diagram)" LTC1736; Linear Technology Manual page 9
	L	

Examiner	CW	Date Considered	7/25/03

Examiner: Initial citation considered. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

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M.H.
8-14-03

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Attorney Docket No.: TRAN-P059

Inventor(s): Andrew Read, Sameer Halapete and Keith Klayman

Group Art Unit:

Filed: 10/23/00

Examiner:

Serial No.: 09/694,433

Title: STATIC POWER CONTROL

Commissioner of Patents
P. O. Box 1450
Alexandria, VA 22313-1450
Sir:

Information Disclosure Statement Submitted Pursuant to 37 C.F.R. 1.97(b)

The citations referenced herein, copies attached, may be material to the examination of the above-identified application and are, therefore, submitted in compliance with the duty of disclosure as defined in 37 C.F.R. 1.56. The Examiner is requested to make these citations of official record in the application.

This Information Disclosure Statement submitted in accordance with 37 C.F.R. 1.97(b) is not to be construed as a representation that a search has been made, that additional items material to the examination of this application do not exist, or that any one or more of these citations constitute prior art under 35 U.S.C. 102.

The Examiner's attention is respectfully directed to the following U.S. Patents:

Pat. No.	Pat. Title	Grant Date
6,574,739	DYNAMIC POWER SAVING BY MONITORING CPU UTILIZATION	06/13/03
6,519,706	DSP CONTROL APPARATUS AND METHOD FOR REDUCING POWER CONSUMPTION	02/11/03
6,513,124	METHOD AND APPARATUS FOR CONTROLLING OPERATING SPEED OF PROCESSOR IN COMPUTER	01/28/03
6,510,400	TEMPERATURE CONTROL CIRCUIT FOR CENTRAL PROCESSING UNIT	01/21/03
6,487,668	THERMAL AND POWER MANAGEMENT TO COMPUTER SYSTEMS	11/26/02
6,477,654	MANAGING VT FOR REDUCED POWER USING POWER SETTING COMMANDS IN THE INSTRUCTION STREAM	11/05/02
6,427,211	REAL-TIME POWER CONVERSATION AND THERMAL MANAGEMENT FOR ELECTRONIC DEVICES	07/30/02
6,415,388	METHOD AND APPARATUS FOR POWER THROTTLING IN A MICROPROCESSOR USING A CLOSED LOOP FEEDBACK SYSTEM	07/02/02
6,378,081	POWER CONSERVATION WITHOUT PERFORMANCE REDUCTION IN A POWER MANAGED SYSTEM	04/23/02
6,311,287	VARIABLE FREQUENCY CLOCK CONTROL FOR MICRO-PROCESSOR-BASED COMPUTER SYSTEMS	10/30/02
6,141,762	POWER REDUCTION IN A MULTIPROCESSOR DIGITAL SIGNAL PROCESSOR BASED ON PROCESSOR LOAD	10/31/02
6,119,241	SELF REGULATING TEMPERATURE/PERFORMANCE/VOLTAGE SCHEME FOR MICROS (X86)	09/12/00
6,047,248	PERFORMANCE TEMPERATURE OPTIMIZATION BY COOPERATIVE-LY VARYING THE VOLTAGE AND FREQUENCY OF A CIRCUIT	04/04/00

08/13/2003 SZEUDIE1 00000033 09694433

01 FC:1806 180.00 OP

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5,996,084	METHOD AND APPARATUS FOR REAL-TIME CPU THERMAL MANAGEMENT AND POWER CONSERVATION BY ADJUSTING CPU CLOCK FREQUENCY IN ACCORDANCE WITH CPU ACTIVITY	11/30/99
5,996,083	MICROPROCESSOR HAVING SOFTWARE CONTROLLABLE POWER CONSUMPTION	11/30/99
5974,557	METHOD AND SYSTEM FOR PERFORMING THERMAL AND POWER MANAGEMENT FOR A COMPUTER	10/26/99
5,940,786	TEMPERATURE REGULATED CLOCK RATE FOR MICRO-PROCESSORS	08/17/99
5,940,785	PERFORMANCE-TEMPERATURE OPTIMIZATION BY COOPERATIVE-LY VARYING THE VOLTAGE AND FREQUENCY OF A CIRCUIT	08/17/99
5,815,724	METHOD AND APPARATUS FOR CONTROLLING POWER CONSUMPTION IN A MICROPROCESSOR	09/29/98
5,754,869	METHOD AND APPARATUS FOR MANAGING POWER CONSUMPTION OF THE CPU AND ON-BOARD SYSTEM DEVICES OF PERSONAL COMPUTERS	05/19/98
5,719,800	PERFORMANCE THROTTLING TO REDUCE IC POWER CONSUMPTION	02/17/98
5,692,204	METHOD AND APPARATUS FOR COMPUTER SYSTEM POWER MANAGEMENT	11/25/97
5,502,838	TEMPERATURE MANAGEMENT FOR INTEGRATED CIRCUITS	03/26/96
5,461,266	POWER CONSUMPTION CONTROL SYSTEM	10/24/95
5,422,806	TEMPERATURE CONTROL FOR A VARIABLE FREQUENCY CPU	06/06/95

The Examiner's attention is respectfully directed to the following Published Patent Applications:

US. Published Patent Applications

Examiner Initial	No.	Pub. No.	Filing Date	Applicant	Class	Sub-class	Publication Date
	AA	2003/0074591	10/17/01	McClendon et al.	713	322	04/17/03
	BB	2003/0065960	09/28/01	Rusu et al.	713	300	04/17/03
	CC	2002/0083356	11/26/01	Dai	713	322	06/27/02
	DD	2002/0073348	12/06/01	Tani	713	300	06/13/02

Please direct all correspondence concerning the above-identified application to the following address:

WAGNER, MURABITO & HAO LLP
Two North Market Street, Third Floor
San Jose, California 95113
(408) 938-9060

Respectfully submitted,

Date: 8/5/03

By: Ronald M Pomerenke
Ronald M. Pomerenke
Reg. No. 43,009

rev. 6/97 jpw

Patent 2185

Docket No.: TRAN-P059

Information Disclosure Statement Transmittal

I hereby certify that this transmittal of the below described document is being deposited with the United States Postal Service in an envelope bearing First Class Postage and addressed to the Commissioner of Patents and Trademarks, Washington, D.C., 20231, on the below date of deposit.

Date of Deposit:	08/05/03	Name of Person Making the Deposit:	KATHERINE RINALDI	Signature of the Person Making the Deposit:	Katherine Rinaldi

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Inventor(s): Andrew Read, Sameer Halapete and Keith Klayman

Group Art Unit:

Filed: 10/23/00

Examiner:

Serial No.: 09/694,433

Title: STATIC POWER CONTROL

The Commissioner of Patents and Trademarks
Washington, D.C. 20231
Sir:

Information Disclosure Statement Transmittal

Transmitted herewith is the following:

..... Formal drawings, totaling ..... sheets.
..... Informal drawings, totaling ..... sheets.
..... Certification for PTO Consideration
..... Information Disclosure statement (__ sheets)
..X.. Information Disclosure statement and late filing fee
..X.. Form 1449
..... Petition for Extension of Time
..X.. Other: References

Fee Calculation (for other than a small entity)					
Fee Items				Fee Rate	Total
Petition for Extension of Time (fee calculated elsewhere				$ .00	$0.00
Information Disclosure Statement, late filing				$180.00	$180.00
Other:					$0.00
Total Fees					$180.00

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[X] The Commissioner is hereby authorized to charge any additional fees associated with this communication or credit any overpayment to Deposit Account No.: 23-0085 .
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kgr 7/98

Please direct all correspondence concerning the above-identified application to the following address:

WAGNER, MURABITO & HAO LLP
Two North Market Street, Third Floor
San Jose, California 95113
(408) 938-9060

Respectfully submitted,

Date: 8/5/03

By: Ronald M. Pomerenke
Ronald M. Pomerenke
Reg. No. 43,009

kgr 7/98

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Attorney Docket No.: TRAN-P059

Inventor(s): Andrew Read, Sameer Halapete and Keith Klayman

Group Art Unit:

Filed: 10/23/00

Examiner:

Serial No.: 09/694,433

Title: STATIC POWER CONTROL

The Commissioner of Patents and Trademarks
Washington, D.C. 20231
Sir:

Information Disclosure Statement Submitted Pursuant to 37 C.F.R. 1.97(b)

The citations referenced herein, copies attached, may be material to the examination of the above-identified application and are, therefore, submitted in compliance with the duty of disclosure as defined in 37 C.F.R. 1.56. The Examiner is requested to make these citations of official record in the application.

This Information Disclosure Statement submitted in accordance with 37 C.F.R. 1.97(b) is not to be construed as a representation that a search has been made, that additional items material to the examination of this application do not exist, or that any one or more of these citations constitute prior art under 35 U.S.C. 102.

The Examiner's attention is respectfully directed to the following U.S. Patents:

Pat. No.	Pat. Title	Grant Date
5,812,860	METHOD AND APPARATUS PROVIDING MULTIPLE VOLTAGES AND FREQUENCIES SELETABLE BASED ON REAL TIME CRITERIA TO CONTROL POWER CONSUMPTION	09/22/98
5,726,901	SYSTEM FOR REPORTING COMPUTER ENERGY CONSUMPTION	03/10/98

Please direct all correspondence concerning the above-identified application to the following address:

WAGNER, MURABITO & HAO LLP
Two North Market Street, Third Floor
San Jose, California 95113
(408) 938-9060

Respectfully submitted,

Date: 18 Nov. 2003

By: _____
Matthew J. Blecher
Reg. No. 46,588

12/01/2003 HBIZUNES 00000047 09694433
01 FC:1806 180.00 OP

rev. 6/97 jpw

0623 #9 SP

Patent

Docket No.: TRAN-P059 / 01-28-04

Information Disclosure Statement Transmittal

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Date of Deposit:	11/18/03	Name of Person Making the Deposit:	KATHERINE RINALDI	Signature of the Person Making the Deposit:	Katherine Rinaldi

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Inventor(s): Andrew Read, Sameer Halapete and Keith Klayman

Group Art Unit:

Filed: 10/23/00

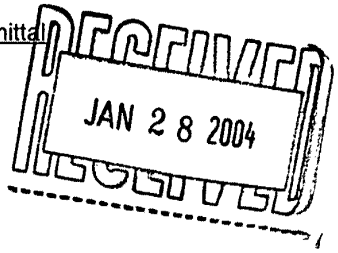
Examiner:

Serial No.: 09/694,433

Title: STATIC POWER CONTROL

The Commissioner of Patents and Trademarks
Washington, D.C. 20231
Sir:

Information Disclosure Statement Transmittal



Transmitted herewith is the following:

..... Formal drawings, totaling ..... sheets.
..... Informal drawings, totaling ..... sheets.
..... Certification for PTO Consideration
..... Information Disclosure statement (__ sheets)
..X.. Information Disclosure statement and late filing fee
..X.. Form 1449
..... Petition for Extension of Time
..X.. Other: References

Fee Calculation (for other than a small entity)					
Fee Items				Fee Rate	Total
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Total Fees					$180.00

PAYMENT OF FEES

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[X] The Commissioner is hereby authorized to charge any additional fees associated with this communication or credit any overpayment to Deposit Account No.: 23-0085 .
A duplicate copy of this authorization is enclosed.

[X] A check in the amount of $180.00

[ ] Charge any fees required or credit any overpayments associated with this filing to Deposit Account No.: 23-0085.

kgr 7/98

Please direct all correspondence concerning the above-identified application to the following address:

WAGNER, MURABITO & HAO LLP
Two North Market Street, Third Floor
San Jose, California 95113
(408) 938-9060

Respectfully submitted,

Date: 18 Nov. 2003

By: _____
Matthew J. Blecher
Reg. No. 46,558

kgr 7/98

TRAN-P059

Patent

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2-12-04

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of

Read et al.

Serial No. 09/694,433

Filing Date: October 23, 2000

For: STATIC POWER CONTROL (As Filed)

Examiner: Cao, Chun

Art Unit: 2185

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

AMENDMENT AND RESPONSE TO OFFICE ACTION

Dear Sir:

In response to the Office Action mailed July 30, 2003, the following amendments and responses to the above captioned patent application are respectfully submitted. Reconsideration of the above captioned patent application is respectfully requested.

02/06/2004 JADD01 00000013 09694433
01 FC:1253 950.00 OP
02 FC:1201 258.00 OP

AMENDMENTS TO THE SPECIFICATION

Please amend the Title of the instant specification as follows.

-- ~~STATIC POWER CONTROL~~ SAVING POWER WHEN IN OR TRANSITIONING TO A STATIC MODE OF A PROCESSOR --

AMENDMENTS TO THE CLAIMS

Please amend Claims 1, 2, 4, 5, 6, 7, 11, and 13 as follows.

A1

1. (Currently Amended) A method for reducing power utilized by a processor comprising the steps of:

determining that a processor is transitioning from a computing mode to a mode [[is]] in which system clock to the processor is disabled, and

reducing core voltage to the processor to a value sufficient to maintain state during the mode in which system clock is disabled, wherein said value of the core voltage is not sufficient to maintain processing activity in said processor.

Claim 2. (Currently Amended) A method as claimed in Claim 1 in which the step of determining that a processor is transitioning from a computing mode to a mode [[is]] in which system clock to the processor is disabled [[comprising]] comprises monitoring a stop clock signal.

Claim 3. (Original) A method as claimed in Claim 1 in which the step of reducing core voltage to the processor to a value sufficient to maintain state during the state in which system clock is disabled comprises furnishing an input to reduce an output voltage provided by a voltage regulator furnishing core voltage to the processor.

Claim 4. (Currently Amended) A method for reducing power utilized by a processor comprising the steps of:

determining that a processor is transitioning from a computing mode to a mode in which system clock to the processor is disabled, and

reducing core voltage to the processor to a value sufficient to maintain state during the mode in which system clock is disabled by:

furnishing an input to reduce an output voltage provided by a voltage regulator furnishing core voltage to the processor, and

~~A method as claimed in Claim 3 in which the step of reducing core voltage to the processor to a value sufficient to maintain state during the state in which system clock is disabled further comprises~~

providing a feedback signal to the voltage regulator to reduce its output voltage below a specified output voltage.

Claim 5. (Currently Amended) A method for reducing power utilized by a processor comprising the steps of:

determining that a processor is transitioning from a computing mode to a mode in which system clock to the processor is disabled,

reducing core voltage to the processor to a value sufficient to maintain state during the mode in which system clock is disabled, and

~~A method as claimed in Claim 1 further comprising the steps of~~

transferring operation of a voltage regulator furnishing core voltage in a mode in which power is dissipated during reductions in core voltage to a mode in which power is saved during a voltage transition when it is determined that a processor is transitioning from a computing mode to a mode is which system clock to the processor is disabled.

Claim 6. (Currently Amended) A method as claimed in Claim 5 further comprising the steps of returning the voltage regulator to its original mode of operation when the [[lower]] value of the core voltage sufficient to maintain state during the mode in which system clock is disabled is reached.

Claim 7. (Currently Amended) A circuit for providing a regulated voltage to a processor comprising:

a voltage regulator having:

an output terminal providing a selectable voltage, and

an input terminal for receiving signals indicating the selectable voltage level;

means for providing signals at the input terminal of the voltage regulator for selecting a voltage for operating the processor in a computing mode and a voltage of a level less than that for operating the processor in a computing mode, wherein the level less than that for operating the processor in a computing mode is sufficient to maintain state of the processor.

Claim 8. (Original) A circuit as claimed in Claim 7 in which the means for providing signals at the input terminal of the voltage regulator comprises means for accepting binary signals indicating different levels of voltage.

Claim 9. (Original) A circuit as claimed in Claim 7 in which the means for providing signals at the input terminal of the voltage regulator comprises:

selection circuitry,

means for furnishing a plurality of signals at the input to the selection circuitry, and

means for controlling the selection by the selection circuitry.

Claim 10. (Original) A circuit as claimed in Claim 9 in which:

the selection circuitry is a multiplexor, and

the means for controlling the selection by the selection circuitry includes a control terminal for receiving signals indicating a system clock to the processor is being terminated.

Claim 11. (Currently Amended) A circuit for providing a regulated voltage to a processor comprising:

a voltage regulator having:

an output terminal providing a selectable voltage, and

an input terminal for receiving signals indicating the selectable voltage level;

means for providing signals at the input terminal of the voltage regulator for selecting a voltage for operating the processor in a computing mode and a voltage of a level less than that for operating the processor in a computing mode; and

~~A circuit as claimed in Claim 7 further comprising~~

means for reducing the selectable voltage below a level provided by the voltage regulator.

Claim 12. (Original) A circuit as claimed in Claim 11 in which the means for reducing the selectable voltage below a level provided by the voltage regulator comprises:

a voltage divider network joined between the output terminal and a voltage source furnishing a value higher than the selectable voltage, and

a voltage regulator feedback circuit receiving a value from the voltage divider network.

Claim 13. (Currently Amended) A circuit for providing a regulated voltage to a processor comprising:

a voltage regulator having:

an output terminal providing a selectable voltage, and

an input terminal for receiving signals indicating the selectable voltage level;

means for providing signals at the input terminal of the voltage regulator for selecting a voltage for operating the processor in a computing mode and a voltage of a level less than that for operating the processor in a computing mode;

~~A circuit as claimed in Claim 7 further comprising:~~

circuitry for conserving charge stored by the voltage regulator when the selectable voltage decreases, and

means for enabling the circuitry for conserving charge stored by the voltage regulator when the selectable voltage decreases.

REMARKS

The claims remaining in the present application are Claims 1-13. Claims 1, 2, 4 - 7, 11, and 13 have been amended. The Title of the instant specification has been amended. No new matter has been added as a result of these amendments.

Title of the Specification

The Title of the instant specification has been amended. Applicants respectfully request that the examiner review and approve of the amended Title.

35 U.S.C. §102

Claims 1-13 are rejected under 35 U.S.C. §102(e) as being anticipated by Orton et al., U.S. Patent No. 6,118,306 (hereinafter, Orton). The rejection is respectfully traversed for the following reasons.

Currently Amended Independent Claim 1 recites, in part:

> reducing core voltage to the processor to a value sufficient to maintain state during the mode in which system clock is disabled, wherein said value of the core voltage is not sufficient to maintain processing activity in said processor.

Amended Independent Claim 1 recites that the core voltage is reduced to a value that is sufficient to maintain state of the processor, but is not sufficient to maintain processing activity in the processor. Applicants assert that reducing a voltage to a processor to a level that is sufficient to maintain state of the processor, but is not sufficient to maintain processing activity in the processor, would not have been obvious to one of ordinary skill in the art at the time of Applicants' invention based on the cited art of record. Applicants do not believe that Orton teaches or suggests reducing the voltage of the processor core to a value that is sufficient to maintain state of the processor, but is not sufficient to maintain processing activity in the processor.

Orton may purport to disclose a system that places a processor into a low activity state. During this state, the frequency of operation may be reduced. Orton may also disclose that a high and a low voltage may be applied to the processor. However, Applicants have found nothing in Orton that expressly teaches or suggests that one of the two voltages is sufficient to maintain state of the processor, but is not sufficient to maintain processing activity in the processor, as Applicants have claimed. Orton does provide exemplary high and low voltage values at col. 7, lines 63-65. Specifically, these values are 1.3V and 1.8V. It is Applicants' understanding that both of these values were typical values that would have been sufficient to maintain processor activity given Orton.

Thus, Orton is silent as to teaching reducing voltage to a value that is sufficient to maintain state of the processor, but is not sufficient to maintain processing activity in the processor. Moreover, Orton's only exemplary voltages would have been sufficient to maintain processor activity, according to Applicants' understanding. Therefore, Applicants respectfully assert that Orton fails to teach or suggest reducing voltage to a value that is sufficient to maintain state of the processor, but is not sufficient to maintain processing activity in the processor, as the Applicants have claimed.

For the foregoing reason, Claim 1 is neither taught nor suggested by Orton. Therefore, Applicants respectfully request allowance of Claim 1.

Currently Amended Independent Claim 7 recites, in part:

> means for providing signals at the input terminal of the voltage regulator for selecting a voltage for operating the processor in a computing mode and a voltage of a level less than that for operating the processor in a computing mode, wherein the level less than that for operating the processor in a computing mode is sufficient to maintain state of the processor (emphasis added).

For at least the reasons discussed in the response to Claim 1, Claim 7 also overcomes Orton. As such, Applicants earnestly request allowance of Claim 7.

Claims 2-3, 8-9, and 10 depend from Claims 1 and 7, which are believed to be allowable for the foregoing reasons. As a result of their dependency on claims believed to be allowable, Claims 2-3, 8-9, and 10 are believed to be allowable. Applicants earnestly request their allowance.

CLAIM 4

Currently Amended Claim 4 recites, in part:

> reducing core voltage to the processor to a value sufficient to maintain state during the mode in which system clock is disabled by
>
> furnishing an input to reduce an output voltage provided by a voltage regulator furnishing core voltage to the processor, and
>
> providing a feedback signal to the voltage regulator to reduce its output voltage below a specified output voltage (emphasis added).

Claim 4 has been rewritten in independent form including all limitations from its base claim and intervening claim. Applicants do not intend that the scope of Claim 4 is narrowed by this amendment. Independent Claim 4 recites that a feedback signal is provided to the voltage regulator to reduce its output voltage below a specified output voltage. Applicants respectfully assert that Orton fails to teach or suggest this claimed limitation.

The passages in Orton to which the rejection refers may teach that a signal is applied to a voltage regulator to alter its output voltage. However, Applicants have claimed that a feedback signal is applied to the voltage regulator. In Figure 1 of Orton,

the voltage regulator (52) is depicted with an input signal from the host bridge (18). However, Applicants do not understand the voltage regulator to receive a feedback signal, as Applicants have claimed.

In Figure 5 of Orton, the voltage regulator (52) has its output voltage controlled by the VR_LO/HI# signal from the NB control logic (400). The voltage regulator also receives a signal from the system electronics (VR_ON), which directs the voltage regulator to settle to the voltage level selected by the VR_LO/HI# signal (col. 7, lines 59-63). Applicants do not understand either of these inputs to the voltage regulator to be feedback signals, as claimed. Furthermore, Applicants do not understand either of these signals to reduce its output voltage below a specified output voltage, as claimed.

For the foregoing reasons, Applicants assert that Independent Claim 4 is neither taught nor suggested by Orton. Consequently, Applicants earnestly request that Claim 4 be allowed.

CLAIMS 5 and 6

Independent Claim 5 recites, in part:

> transferring operation of a voltage regulator furnishing core voltage in a mode in which power is dissipated during reductions in core voltage to a mode in which power is saved during a voltage transition when it is determined that a processor is transitioning from a computing mode to a mode is which system clock to the processor is disabled.

Claim 5 has been rewritten in independent form including all limitations from its base claim and intervening claim. Applicants do not intend that the scope of Claim 5 is narrowed by this amendment. Independent Claim 5 recites that an operation of a voltage regulator is transferred from a mode in which power is dissipated to a mode in

which power is saved. Claim 5 recites an embodiment that operates a voltage regulator in two modes. A first of those modes is one in which power is dissipated and a second mode is one in which power is saved. Claim 5 recites that the voltage regulator is operated in the power saving mode during a voltage transition.

Applicants respectfully assert that Orton fails to teach or suggest the limitations of Claim 5. Orton may discuss reducing power consumption (see, e.g., col. 2, lines 18-20). Orton may achieve a reduction in power by, for example, reducing the operating frequency of the processor. However, power savings can be achieved in manners other than reducing frequency and/or reducing voltage. Applicants have specifically recited in this embodiment that saving power is performed by a choice of mode of operation of the voltage regulator. Orton is silent as to operating the voltage regulator in two different modes, as claimed. Thus, Orton fails to teach or suggest the claimed transferring the operation of a voltage regulator from a mode in which power is dissipated to a mode in which power is saved, during a voltage transition.

For the foregoing reasons, Orton fails to teach or suggest the limitations of Claim 5. Therefore, Applicants earnestly request allowance of Claim 5.

Claim 6 depends from Claim 5. By virtue of its dependency on a claim that is believed to be allowable, Applicants believe Claim 6 to be allowable. Claim 6 is believed to be allowable for the following additional reason.

Claim 6 recites, in part:

> returning the voltage regulator to its original mode of operation when the value of the core voltage sufficient to maintain state during the mode in which system clock is disabled is reached.

Claim 6 recites the limitation of returning the voltage regulator to its original mode of operation when the value of the core voltage sufficient to maintain state during the mode in which system clock is disabled is reached. As Applicants have previous argued, Orton fails to discuss operating a voltage regulator in two modes of operation, one in which power is dissipated and another mode in which power is saved. Therefore, Orton cannot teach or suggest the claimed limitation of "returning the voltage regulator to its original mode of operation when the value of the core voltage sufficient to maintain state during the mode in which system clock is disabled is reached."

For the foregoing reasons, Orton fails to teach or suggest the limitations of Claim 6. Therefore, Applicants earnestly request allowance of Claim 6.

Claims 11 and 12

Amended Independent Claim 11 recites, in part:

> a voltage regulator having:
>
> an output terminal providing a selectable voltage, and
>
> an input terminal for receiving signals indicating the selectable voltage level;
>
> ...
>
> means for reducing the selectable voltage below a level provided by the voltage regulator (emphasis added).

Claim 11 has been rewritten in independent form including all limitations from its base claim and intervening claim. Applicants do not intend that the scope of Claim 11 is narrowed by this amendment. Claim 11 recites a "means for reducing the selectable voltage below a level provided by the voltage regulator." Thus, the voltage regulator is recited as having an output terminal that provides a selectable voltage. Furthermore, Claim 11 recites that the selectable voltage can be reduced below a level that the

voltage regulator provides. This allows embodiments of the present invention to provide a voltage to a processor that is below that which the voltage regulator provides.

Applicants have reviewed Orton and respectfully assert that Orton fails to teach or suggest, "means for reducing the selectable voltage below a level provided by the voltage regulator." The rejection has rejected Claim 11 for the same reasons as Claim 4, according to Applicants understanding of the rejection. The Applicants respectfully assert that Orton fails to teach or suggest a structure that provides the claimed function of reducing the selectable voltage below a level provided by the voltage regulator.

For example, in Figure 5 of Orton, the voltage regulator (52) has its output voltage controlled by the VR_LO/HI# signal from the NB control logic (400). The voltage regulator also receives a signal from the system electronics (VR_ON), which directs the voltage regulator to settle to the voltage level selected by the VR_LO/HI# signal (col. 7, lines 59-63). Applicants do not understand either of these inputs to the voltage regulator to provide the necessary structure to reduce the output voltage of the voltage regulator below a *specified* output voltage, as claimed.

For the foregoing reasons, Orton fails to teach or suggest the limitations of Claim 11. Therefore, Applicants earnestly request allowance of Claim 11.

Claim 12 depends from Claim 11. By virtue of its dependency on a claim that is believed to be allowable, Applicants believe Claim 12 to be allowable. Claim 12 is believed to be allowable for the following additional reasons.

Claim 12 recites:

> A circuit as claimed in Claim 11 in which the means for reducing the selectable voltage below a level provided by the voltage regulator comprises:
>
> a voltage divider network joined between the output terminal and a voltage source furnishing a value higher than the selectable voltage, and
>
> a voltage regulator feedback circuit receiving a value from the voltage divider network.

Claim 12 recites elements coupled to the output terminal and a voltage source that furnishes a higher voltage than the selectable voltage. Applicants have reviewed Orton and respectfully assert that Orton fails to teach or suggest this limitation. Moreover, the rejection fails to point out where Orton teaches or suggests such a limitation. This is because the rejection references the rejection of Claims 1-6 when discussing the rejection to Claim 12. However, the limitation of a voltage divider network joined between the output terminal and a voltage source furnishing a value higher than the selectable voltage are not recited in any of Claims 1-6.

Claim 12 further recites, "a voltage regulator feedback circuit receiving a value from the voltage divider network." Applicants have reviewed Orton and respectfully assert that Orton fails to teach or suggest this limitation. Moreover, the rejection fails to point out where Orton teaches or suggests such a limitation. This is because the rejection references the rejection of Claims 1-6 when discussing the rejection to Claim 12. However, the limitation of a voltage regulator feedback circuit receiving a value from the voltage divider network." is not recited in any of Claims 1-6.

For the foregoing reasons, Orton fails to teach or suggest the limitations of Claim 12. Therefore, Applicants earnestly request allowance of Claim 12.

CLAIM 13

Claim 13 recites, in part:

> a voltage regulator having:
>
> an output terminal providing a selectable voltage, and
>
> an input terminal for receiving signals indicating the selectable voltage level;
>
> ...
>
> circuitry for conserving charge stored by the voltage regulator when the selectable voltage decreases, and
>
> means for enabling the circuitry for conserving charge stored by the voltage regulator when the selectable voltage decreases (emphasis added).

Claim 13 has been rewritten in independent form including all limitations from its base claim and intervening claim. Applicants do not intend that the scope of Claim 13 is narrowed by this amendment. Claim 13 recites circuitry for conserving charge stored by the voltage regulator when the selectable voltage decreases. Claim 13 further recites means for enabling this circuitry.

Applicants respectfully assert that Orton fails to teach or suggest the limitations of Claim 13. Orton may discuss reducing power consumption (see, e.g., col. 2, lines 18-20). Orton may achieve a reduction in power by, for example, reducing the operating frequency of the processor. However, power savings can be achieved in manners other than reducing frequency and/or reducing voltage. Applicants have specifically recited operating the voltage regulator in two different modes. Orton is silent as to circuitry for conserving charge stored by the voltage regulator when the selectable voltage decreases, as claimed.

Applicants further note that the rejection fails to point out where Orton teaches or suggests such a limitation. This is because the rejection references the rejection of

Claims 1-6 when discussing the rejection to Claim 13. However, the limitation of circuitry for conserving charge stored by the voltage regulator when the selectable voltage decreases is not recited in any of Claims 1-6. Therefore, the rejection fails to discuss this claimed limitation.

For the foregoing reasons, Orton fails to teach or suggest the limitations of Claim 13. Therefore, Applicants earnestly request allowance of Claim 13.

CONCLUSION

In light of the above listed amendments and remarks, allowance of Claims 1-13 is requested.

Should the Examiner have a question regarding the instant amendment and response, the Applicants invite the Examiner to contact the Applicants' undersigned representative at the below listed telephone number.

Dated: 1/28, 2004

Respectfully submitted,
WAGNER, MURABITO & HAO LLP
Ronald M. Pomerenke
Registration No. 43,009

Address: WAGNER, MURABITO & HAO LLP
Two North Market Street
Third Floor
San Jose, California 95113

Telephone: (408) 938-9060 Voice
(408) 938-9069 FAX

Attorney Docket No.: TRAN-P059

21858

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

I hereby certify that this transmittal of the below described document is being deposited with the United States Postal Service in an envelope bearing First Class Postage and addressed to the Commissioner for Patents P.O. Box 1450, Alexandria, VA 22313-1450, on the below date of deposit.

Date of Deposit:	01/29/04	Name of Person Making the Deposit:	KATHERINE RINALDI	Signature of the Person Making the Deposit:	Katherine Rinaldi

In re Application of: Andrew Read, Sameer Halapete and Keith Klayman

Serial No.: 09/694,433 Examiner: CAO, CHUN

Filed: 10/23/00 Art Unit: 2185

For: SAVING POWER WHEN IN OR TRASITIONING TO A STATIC MODE OF A PROCESSOR (AS AMENDED)

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

AMENDMENT TRANSMITTAL

1. Transmitted herewith is an amendment for this application

.X. Transmitted herewith is a response to an office action for the above identified patent application. (.17. sheets)
..... Transmitted herewith are ..... sheets of substitute formal drawings.
..... Other:

2. Applicant is other than a small entity

Extension of Term

3. The proceedings herein are for a patent application and the provisions of 37 C.F.R. 1.136 apply.

(a) [X] Applicant petitions for an extension of time under 37 C.F.R. 1.136 (fees: 37 C.F.R. 1.17(a)-(d) for the total number of months checked below:)

Extension	Fee
[ ] one month	$110.00
[ ] two months	$420.00
[X] three months	$950.00
[ ] four months	$1,480.00

Fee $ 950.00

If an additional extension of time is required, please consider this a petition therefor.

(b) [ ] Applicant believes that no extension of term is required. However, this conditional petition is being made to provide for the possibility that applicant has inadvertently overlooked the need for a petition for extension of time.

Fee Calculation

4. The fee for claims (37 C.F.R. 1.16(b)-(d)) has been calculated as shown below:

(for other than a small entity)					
Fee Items	Claims Remaining After Amendment	Highest Number of Claims Previously Paid For	Present Extra Claims	Fee Rate	Total
Total Claims	13	- 20 =	0	x $18.00	$0.00
Independent Claims	6	- 3 =	3	x $86.00	$258.00
Multiple Dependent Claim Fee (one or more, first added by this amendment)				$290.00	$0.00
Total Fees					$258.00

PAYMENT OF FEES

5. The full fee due in connection with this communication is provided as follows:

[x] The Commissioner is hereby authorized to charge any additional fees associated with this communication or credit any overpayment to Deposit Account No.: 23-0085.
A duplicate copy of this authorization is enclosed.

[x] A check in the amount of $1,208.00

[ ] Charge any fees required or credit any overpayments associated with this filing to Deposit Account No.: 23-0085.

Please direct all correspondence concerning the above-identified application to the following address:

WAGNER, MURABITO & HAO LLP
Two North Market Street, Third Floor
San Jose, California 95113
(408) 938-9060

Respectfully submitted,

Date: 1/29/04

By: Ronald M. Pomerenke
Ronald M. Pomerenke
Reg. No. 43,009

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Attorney Docket No.: TRAN-P059

#11 pay 326 of

Inventor(s): Andrew Read, Sameer Halapete and Keith Klayman

Group Art Unit:

Filed: 10/23/00

Examiner:

Serial No.: 09/694,433

Title: STATIC POWER CONTROL

The Commissioner of Patents and Trademarks
Washington, D.C. 20231
Sir:

Information Disclosure Statement Submitted Pursuant to 37 C.F.R. 1.97(b)

The citations referenced herein, copies attached, may be material to the examination of the above-identified application and are, therefore, submitted in compliance with the duty of disclosure as defined in 37 C.F.R. 1.56. The Examiner is requested to make these citations of official record in the application.

This Information Disclosure Statement submitted in accordance with 37 C.F.R. 1.97(b) is not to be construed as a representation that a search has been made, that additional items material to the examination of this application do not exist, or that any one or more of these citations constitute prior art under 35 U.S.C. 102.

The Examiner's attention is respectfully directed to the following U.S. Patents:

Pat. No.	Pat. Title	Grant Date
5,201,059	METHOD FOR REDUCING POWER CONSUMPTION INCLUDES COMPARING VARIANCE IN NUMBER OF TIME MICROPROCESSOR TRIED TO REACT INPUT IN PREDEFINED PERIOD TO PREDEFINED VARIANCE	04/06/93
5,230,055	BATTERY OPERATED COMPUTER OPERATION SUSPENSION IN RESPONSE TO ENVIRONMENTAL SENSOR INPUTS	07/20/93
5,752,011	METHOD AND SYSTEM FOR CONTROLLING A PROCESSOR'S CLOCK FREQUENCY IN ACCORDANCE WITH THE PROCESSOR'S TEMPERATURE	05/12/98
6,216,235	THERMAL AND POWER MANAGEMENT FOR COMPUTER SYSTEMS	04/10/01
5,167,024	POWER MANAGEMENT FOR A LAPTOP COMPUTER WITH SLOW AND SLEEP MODES	11/24/92
5,218,704	REAL-TIME POWER CONSERVATION FOR PORTABLE COMPUTERS	06/08/93
5,239,652	ARRANGMENT FOR REDUCING COMPUTER POWER CONSUMPTION BY TURNING OFF THE MICROPROCESSOR WHEN INACTIVE	08/24/93
5,682,093	APPARATUS AND METHOD FOR REDUCING THE POWER CONSUMPTION OF AN ELECTRONIC DEVICE	10/28/97
5,717,319	METHOD TO REDUCE THE POWER CONSUMPTION OF AN ELECTRONIC DEVICE COMPRISING A VOLTAGE REGULATOR	02/10/98
5,086,501	COMPUTING SYSTEM WITH SELECTIVE OPERATING VOLTAGE AND BUS SPEED	02/04/92
6,157,092	METHOD AND CIRCUIT CONFIGURATION FOR VOLTAGE SUPPLY IN ELECTRIC FUNCTION UNITS	12/05/00
5,222,239	PROCESS AND APPARATUS FOR REDUCING POWER USAGE MICRO-PROCESSOR DEVICES OPERATING FROM STORED ENERGY SOURCES	06/22/93
5,726,901	SYSTEM FOR REPORTING COMPUTER ENERGY CONSUMPTION	03/10/98
5,812,860	METHOD AND APPARATUS PROVIDING MULTIPLE VOLTAGES AND FREQUENCIES SELECTABLE BASED ON REAL TIME CRITERIA TO CONTROL POWER CONSUMPTION	09/22/98

03/23/2004 SMINASS1 00000055 09694433

01 FC:1805 180.00 OP

rev. 6/97 jpw

5,940,785	PERFORMANCE-TEMPERATURE OPTIMIZATION BY COOPERATIVELY VARYING THE VOLTAGE AND FREQUENCY OF A CIRCUIT	08/17/99
6,510,525	METHOD AND APPARATUS TO POWER UP AN INTEGRATED DEVICE FROM A LOW POWER STATE	01/21/03
6,457,135	SYSTEM AND METHOD FOR MANAGING A PLURALITY OF PROCESSOR PERFORMANCE STATES	09/24/02
6,388,432	CPU CORE VOLTAGE SWITCHING CIRCUIT	05/14/02
6,347,379	REDUCING POWER CONSUMPTION OF AN ELECTRONIC DEVICE	02/12/02
6,345,363	MICROPROCESSOR CORE POWER REDUCTION BY NOT RELOADING EXISTING OPERANDS	02/05/02
6,078,319	PROGRAMMABLE COREVOLTAGE SOLUTION FOR A VIDEO CONTROLLER	06/20/00
5,511,203	POWER MANAGEMENT SYSTEM DISTINGUISHING BETWEEN PRIMARY AND SECONDARY SYSTEM ACTIVITY	04/23/96
5,914,996	MULTIPLE CLOCK FREQUENCY DIVIDER WIITH FIFTY PERCENT DUTY CYCLE OUTPUT	06/22/99
5,774,703	DATA PROCESSING SYSTEM HAVING A REGISTER CONTROLLABLE SPEED	06/30/98
6,112,164	COMPUTER SYSTEM THERMAL MANAGEMENT	08/29/00
6,021,500	PROCESSOR WITH SLEEP AND DEEP SLEEP MODES	02/01/00
6,094,367	VOLTAGE REGULATING DEVICE FOR DYNAMICALLY REGULATING VOLTAGE IN A COMPUTER SYSTEM	07/25/00
5,630,110	METHOD AND APPARATUS FOR ENHANCING PERFORMANCE OF A PROCESSOR	05/13/97
5,687,114	INTEGRATED CIRCUIT FOR STORAGE AND RETRIEVAL OF MULTIPLE DIGITAL BITS PER NONVOLATILE MEMORY CELL	11/11/97
5,713,030	THERMAL MANAGEMENT DEVICE AND METHOD FOR A COMPUTER PROCESSOR	01/27/98
5,572,719	CLOCK CONTROL SYSTEM FOR MICROPROCESSOR INCLUDING A DELAY SENSING CIRCUIT	11/05/96
5,832,284	SELF REGULATING TEMPERATURE/PERFORMANCE/VOLTAGE SCHEME FOR MICROS (X86)	11/03/98
5,628,001	POWER SAVING METHOD AND APPARATUS FOR CHANGING THE FREQUENCY OF A CLOCK IN RESPONSE TO A START SIGNAL	05/06/97
5,710,929	MULTI-STATE POWER MANAGEMENT FOR COMPUTER SYSTEMS	01/20/98
5,913,067	APPARATUS FOR DAPTOVE POWER MANAGEMENT OF A COMPUTER SYSTEM	06/15/99
5,701,783	SETTING ANGLE ADJUSTER FOR THE CAR HEADLAMP	12/30/97
5,745,375	APPARATUS AND METHOD FOR CONTROLLING POWER USAGE	04/28/98

The Examiner's attention is respectfully directed to the following Published Patent Applications:

Pub No.	Title	Publication Date
2002/0026597	REDUCING LEAKAGE POWER CONSUMPTION	10/18/01
2002/0138778	CONTROLLING CPU CORE VOLTAGE TO REDUCE POWER CONSUMPTION	03/22/01

The Examiner's attention is respectfully directed to the following Foreign Patent or Published Foreign Patents:

Document No.	Title	Publication Date
EPO474963	COMPUTER SYSTEM HAVING SLEEP MODE FUNCTION	03/18/92
EPO381021	POWER SAVING SYSTEM	08/08/90
WO01/27728 A1	MINIMIZING POWER CONSUMPTION DURING SLEEP MODES BY USING MINIMUM CORE VOLTAGE NECESSARY TO MAINTAIN SYSTEM STATE	04/19/01

The Examiner's attention is respectfully directed to the following related documents:

Weiser et al.; "SCHEDULING FOR REDUCED CPU ENERGY"; Xerox PARC, Palo Alto, CA; Appears in "Proceedings of the First Symposium on operating Systems Design and Implementation; Usenix Assoc. Nov. 1994

Govil; "COMPARING ALGORITHMS FOR DYNAMIC SPEEDSETTING OF A LOW POWER CPU"; International Computer Science Institute; Berkeley, CA; April 1995

Please direct all correspondence concerning the above-identified application to the following address:

WAGNER, MURABITO & HAO LLP
Two North Market Street, Third Floor
San Jose, California 95113
(408) 938-9060

Respectfully submitted,

Date: 3/18/04

By: Ronald M Pomerenke
Ronald M. Pomerenke
Reg. No. 43,009

215 $

Patent

Docket No.: TRAN-P059

Information Disclosure Statement Transmittal

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Date of Deposit:	03/18/04	Name of Person Making the Deposit:	KATHERINE RINALDI	Signature of the Person Making the Deposit:	Katherine Rinaldi

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Inventor(s): Andrew Read, Sameer Halapete and Keith Klayman

Group Art Unit:

Filed: 10/23/00

Examiner:

Serial No.: 09/694,433

Title: STATIC POWER CONTROL

The Commissioner of Patents and Trademarks
Washington, D.C. 20231
Sir:

Information Disclosure Statement Transmittal

Transmitted herewith is the following:

..... Formal drawings, totaling ..... sheets.
..... Informal drawings, totaling ..... sheets.
..... Certification for PTO Consideration
..... Information Disclosure statement (__ sheets)
..X.. Information Disclosure statement and late filing fee
..X.. Form 1449
..... Petition for Extension of Time
..X.. Other: References

Fee Calculation (for other than a small entity)					
Fee Items				Fee Rate	Total
Petition for Extension of Time (fee calculated elsewhere				$ .00	$0.00
Information Disclosure Statement, late filing				$180.00	$180.00
Other:					$0.00
Total Fees					$180.00

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[X] A check in the amount of $180.00

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kgr 7/98

Please direct all correspondence concerning the above-identified application to the following address:

WAGNER, MURABITO & HAO LLP
Two North Market Street, Third Floor
San Jose, California 95113
(408) 938-9060

Respectfully submitted,

Date: 3/18/04

By: Ronald M Pomerenke
Ronald M. Pomerenke
Reg. No. 43,009

kgr 7/98

EP0474963

Publication Title:

Computer system having sleep mode function.

Abstract:

A personal computer having a sleep mode function for reducing power consumption by lowering the frequency of a clock pulse to be supplied to a CPU includes a clock control circuit (18) for generating a high-frequency first clock pulse, and a low-frequency second clock pulse. When a power supply is turned on, an initial program loader (IPL) discriminates whether or not an AC adapter (105) is connected. The computer also includes a sleep mode controller (16) for, when the AC adapter is connected, disabling a signal, to be supplied to the clock control circuit, for instructing generation of the second clock pulse.

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(11) Publication number: **0 474 963 A2**

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(51) Int. Cl.5: **G06F 1/32**

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(84) Designated Contracting States:
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(71) Applicant: **Kabushiki Kaisha Toshiba**
72, Horikawa-cho Saiwai-ku
Kawasaki-shi(JP)

(72) Inventor: **Yamaki, Kazunori, c/o Intellectual Property Div.**
Kabushiki Kaisha Toshiba, 1-1 Shibaura 1-chome
Minato-ku, Tokyo 105(JP)
Inventor: **Nishikawa, Hirofumi, c/o Intellectual Property Div**
Kabushiki Kaisha Toshiba, 1-1 Shibaura 1-chome
Minato-ku, Tokyo 105(JP)

(74) Representative: **Henkel, Feiler, Hänzel & Partner**
Möhlstrasse 37
W-8000 München 80(DE)

(54) Computer system having sleep mode function.

(57) A personal computer having a sleep mode function for reducing power consumption by lowering the frequency of a clock pulse to be supplied to a CPU includes a clock control circuit (18) for generating a high-frequency first clock pulse, and a low-frequency second clock pulse. When a power supply is turned on, an initial program loader (IPL) discriminates whether or not an AC adapter (105) is connected. The computer also includes a sleep mode controller (16) for, when the AC adapter is connected, disabling a signal, to be supplied to the clock control circuit, for instructing generation of the second clock pulse.

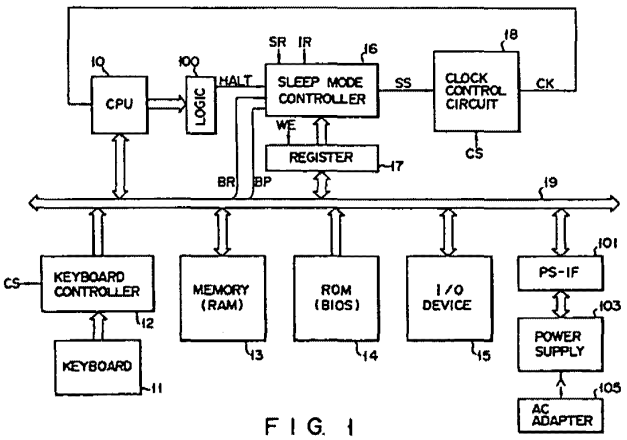

FIG. 1

EP 0 474 963 A2

The present invention relates to a personal computer and, more particularly, to a computer system having a sleep mode function of decreasing a processing speed of a CPU to save power of the system (i.e., to reduce power consumption).

In recent years, a lap-top type personal computer which employs a battery (rechargeable internal battery) as a power supply for a computer system has been developed. Such a computer must have some means for saving power since continuous use of its power supply is limited.

For the purpose of saving power of the power supply, a so-called sleep mode function of decreasing a processing speed of a CPU (microprocessor) under a predetermined condition is known. When no input/output (I/O) operation is performed, the CPU does not require a normal processing speed (relatively high speed), and the processing speed of the CPU can be decreased. The processing speed of the CPU is determined by the frequency of a clock pulse. For this reason, the sleep mode function switches a high-frequency clock pulse normally supplied to the CPU to a low-frequency clock pulse, and supplies it to the CPU.

When the following conditions are satisfied, the sleep mode function is started upon execution of a HALT instruction by a basic input and output system (BIOS).

(1) Although a keyboard control routine of the BIOS is executed, no key input data is set in a key buffer.

(2) No key input data is set in the key buffer, and the CPU is in an idle state.

On the other hand, the sleep mode function is released when an external interrupt, e.g., a timer interrupt occurs, or when the CPU is reset. Once the sleep mode function is released, it will not be enabled unless the BIOS executes a HALT instruction again.

In order to enable the sleep mode function, the BIOS must execute a HALT instruction under the above-mentioned conditions. When the sleep mode function is permitted to be enabled, the BIOS must always monitor whether the above-mentioned conditions are satisfied. More specifically, time is undesirably wasted for processing which is not associated with actual execution of a program.

When the sleep mode function is enabled, and when it is released in response to an interrupt (e.g., a timer interrupt for monitoring a status of the system) or resetting of the CPU, the low-frequency clock (e.g., 4 MHz) must be restored to the high-frequency clock (32 MHz). This operation requires a plurality of cycles, and time is wasted for processing which is not associated with actual execution of the program, as described above.

As described above, the sleep mode function is set to prolong a battery driving time by reducing power consumption. Therefore, when the computer receives an external power supply, e.g., when an AC adapter is connected to the computer, a power supply from the AC adapter has priority over a power supply from the battery. Therefore, the sleep mode function need not be enabled.

However, the sleep mode function of a conventional battery driven personal computer is enabled as long as the conditions are satisfied even when the computer is operated by a mounted battery, and when it receives an external power supply, e.g., when it is operated by an externally connected AC adapter or when it receives power from a master station which can be connected to the battery driven personal computer. Therefore, the processing speed of a program is decreased, and performance of the personal computer cannot be fully exhibited.

It is an object of the present invention to provide a personal computer which can disable a sleep mode function when the personal computer which is battery driven is operated by externally supplied power, and can fully exhibit its performance.

In order to achieve the above object, according to the present invention, a computer system having a sleep mode function, comprises: processor means for performing various data processing operations; clock control means for selecting one of a first clock pulse at a predetermined high frequency required in a normal mode of the processor means, and a second clock pulse at a predetermined low frequency required in a sleep mode of the processor means, and supplying the selected clock pulse to the processor means; discrimination means for discriminating whether or not the computer system receives an external power supply; and sleep operation control means for, when the discrimination means discriminates that the computer system receives an external power supply, prohibiting the clock control means to supply the second clock pulse to the processor means.

According to the present invention, the computer can automatically recognize that power is externally supplied, and can automatically disable the sleep mode function. As a result, a personal computer having a sleep mode function, which can fully exhibit its performance can be provided.

This invention can be more fully understood from the following detailed description when taken in conjunction with the accompanying drawings, in which:

Fig. 1 is a block diagram showing a personal computer having a sleep mode function according to an embodiment of the present invention;

Fig. 2 is a detailed circuit diagram of a sleep mode controller shown in Fig. 1;

Fig. 3 is a detailed circuit diagram of a logic

circuit shown in Fig. 1;

Fig. 4 is a detailed circuit diagram of a clock control circuit shown in Fig. 1;

Fig. 5 is a detailed circuit diagram of a circuit for discriminating connection of an AC adapter; and

Figs. 6A and 6B are flow charts showing an operation of the embodiment shown in Fig. 1.

Fig. 1 is a block diagram showing a personal computer having a sleep mode function according to an embodiment of the present invention. The personal computer shown in Fig. 1 is a lap-top type personal computer which can be operated by a rechargeable battery. As shown in Fig. 1, this system comprises a microprocessor 10 constituting a central processing unit (CPU), a keyboard 11, a keyboard controller (KBC) 12, a memory 13, a read only memory (ROM) 14 for storing a basic input and output system (BIOS), an I/O device 15, and a power supply 103 connected to a system bus 19 via a power supply control interface (PS-IF) 101.

The keyboard 11 and the KBC 12 constitute an input device for inputting data upon various key operations on the keyboard 11. The memory 13 comprising a random access memory (RAM) constitutes various registers such as key buffers for storing data inputted from the keyboard 11. As described above, the ROM 14 stores the BIOS for performing an I/O control operation. The I/O device 15 is an external storage device such as a floppy disk drive.

The system further comprises a sleep mode controller 16 and a control register 17. The sleep mode controller 16 discriminates based on a command outputted from, e.g., the CPU 10 whether or not predetermined conditions for executing a sleep mode are satisfied. If the predetermined conditions are satisfied, the sleep mode controller 16 outputs a control signal SS to a clock control circuit 18. The control register 17 stores mode control data for enabling or disabling execution of a control operation of the sleep mode controller 16.

The clock control circuit 18 generates a clock pulse CK for determining a processing speed of the CPU 10, as shown in Fig. 4. A clock generator 40 generates clock pulses NCK1 and NCK2 necessary for a normal operation (high-speed processing) of the CPU 10, and a low-frequency (e.g., 4 MHz) clock pulse SCK necessary for the sleep mode. The clock pulse NCK1 is a high-frequency (e.g., 32 MHz) pulse, and the clock pulse NCK2 is a high-frequency (e.g., 16 MHz) pulse. The clock control circuit 18 comprises first and second clock switching circuits 41 and 42.

The first clock switching circuit 41 selects one of the clock pulses NCK1 and NCK2 on the basis of a clock switch signal CS outputted from the KBC 12, and outputs the selected pulse as a normal-mode clock pulse NCK. The first clock switching circuit 41 is constituted by a logic circuit comprising AND gates 41a and 41b, an OR gate 41c, and an inverter 41d. The second clock switching circuit 42 selects and outputs the clock pulse SCK in accordance with the clock switch signal SS from the sleep mode controller 16 in the sleep mode, and selects and outputs the clock pulse NCK from the first clock switching circuit 41 in the normal mode. The second clock switching circuit 42 is constituted by a logic circuit comprising AND gates 42a and 42b, an OR gate 42c, and an inverter 42d.

The sleep mode controller 16 has a circuit shown in Fig. 2. More specifically, the controller 16 is a logic circuit comprising AND gates 20a and 20b, flip-flops 21a through 21e, NAND gates 22a and 22b, inverters 23a and 23b, an OR gate 24, and buffer circuits 25a and 25b. The first input terminal of the AND gate 20a receives the mode control data CD stored in the control register 17, and the second input terminal thereof receives a HALT instruction from the CPU 10. When the HALT instruction is at logic level "H" (High), it becomes a significant signal. When the mode control data CD is at logic level "H", the sleep mode is disabled, and when it is at logic level "L" (low), the sleep mode is enabled. Therefore, when the mode control data CD at logic level "L" is stored in the control register 17, and the HALT instruction at logic level "H" is inputted, the AND gate 20a outputs a signal at logic level "H" to the OR gate 24. The control register 17 is set in a write enable state in response to a write enable signal WE generated by decoding an I/O address outputted from the CPU 10. The mode control data CD is set in the control register 17 by the CPU 10 on the basis of a content (whether the sleep mode is enabled or disabled) set in a setup menu or a pop-up menu by a user via the keyboard 11.

The first input terminal of the NAND gate 22a receives a system reset signal SR1, and the second input terminal thereof receives a sleep mode release signal (interrupt request) IR. The system reset signal SR1 is a reset signal (logic level "H") outputted from a gate array (not shown). The gate array generates the reset signal upon reception of a power ON/OFF signal from the power supply 103 or upon reception of a control signal from the keyboard 11. The release signal IR is a power OFF signal (power ON reset signal) outputted from the power supply 103, or an interrupt signal from an interrupt controller (not shown). The first input terminal of the NAND gate 22b receives, e.g., a signal BR outputted from a DMA controller (not shown) to request release of the system bus 19, and the second input terminal thereof receives a signal BP outputted from the CPU 10 to enable use of the system bus 19. The signals BR and BP which are significant at logic level "H" are generated when a

file is to be accessed. For this reason, when a file is not accessed, the signals BR and BP are at logic level "L". The clock terminals of the flip-flops 21a through 21e receive a clock CLK from a clock generator (not shown). The AND gate 20b outputs the control signal SS as an output signal from the controller 16. When the mode control data CD is at logic level "L", the HALT instruction is at logic level "H", and the signals BR and BP are at logic level "L". As a result, the AND gate 20b outputs the "H"-level control signal SS which means to setting of the sleep mode. When one of the system reset signal SR1 and the release signal IR is at logic level "H", the sleep mode is released. When the "H"-level mode control data CD which means prohibition of the control operation of the sleep mode controller 16 is set in the control register 17, the sleep mode is released. In Fig. 2, the flip-flops 21c and 21d are arranged to synchronize the system reset signal SR1 and the interrupt signal IR with the HALT signal. More specifically, the system reset signal SR1 and the interrupt signal IR are generated at arbitrary timings. However, the HALT signal is generated by decoding the HALT instruction by the CPU upon an instruction from the BIOS. Therefore, the HALT signal and the system reset signal SR1 or the interrupt signal IR are synchronized with each other. Fig. 2 shows system result signals SR1 and SR0. The system reset signal SR0 is an inverted signal of SR1. More specifically, the system reset signal SR1 goes active at logic "1" ("H"), and the system reset signal SR0 goes active at logic "0" ("L"). The HALT instruction is generated by a status decode circuit shown in Fig. 3 (a logic circuit 100 shown in Fig. 1). This circuit comprises AND gates 30a through 30c, and inverters 31a and 31b. The CPU 10 outputs various status signals MI, WR, DC, BH, BL, and AS to the status decode circuit. The signal MI means memory access when it is at logic level "H"; and means I/O access when it is at logic level "L". The signal WR means a write mode when it is at logic level "H"; and means a read mode when it is at logic level "L". The signal DC means data when it is at logic level "H"; and means a command when it is a logic level "L". For example, when 16-bit data is to be accessed, the signal BH at logic level "H" means that an upper byte of data is enabled, and the signal BL at logic level "H" means that a lower byte of the data is enabled. When the signal AS is at logic level "H" it means that an address signal is correct. When the status decode circuit receives the "H"-level signal MI, the "H"-level signal WR, the "L"-level signal DC, the "H"-level signal BH, the "L"-level signal BL, and "H"-level signal AS, it causes the AND gate 30a to output the "H"-level HALT instruction.

Fig. 5 is a circuit for discriminating that an AC adapter 105 is connected as an external power supply. An output voltage from the AC adapter 105 is voltage-divided by voltage-dividing resistors 107 and 109, and the divided voltage is supplied to the input terminal of a sub CPU 121 in the power supply 103. An analog divided voltage supplied to the input terminal A is converted into a digital value by an internal first A/D converter 111. An output voltage from a battery 113 is voltage-divided by voltage-dividing resistors 115 and 117, and the divided voltage is supplied to an input terminal B of the sub CPU 121. The sub CPU 121 has a ground terminal. One of the output terminals of the AC adapter 105 and the battery 113 is connected to the ground terminal via the voltage-dividing resistors, and the other output terminal is directly connected to the ground terminal. When the AC adapter 105 is connected, a voltage divided by the voltage-dividing resistors 107 and 109 is supplied to the terminal A, and is converted into a digital value by the A/D converter 111. Therefore, the sub CPU 121 reads an output value from the A/D converter 111 to detect connection of the AC adapter 105. Data indicating connection of the AC adapter 105 is outputted onto the system bus 19 via the PS-IF 101. The CPU 10 receives the connection data of the AC adapter 105 when the BIOS (e.g., an initial program loader (IPL)) stored in the ROM 14 is executed, and sets the "H"-level mode control data CD in the register 17.

The operation of this embodiment will be described below with reference to the flow charts shown in Figs. 6A and 6B.

When the power supply of the battery in the power supply 103 is set ON, the clock generator 40 in the clock control circuit 18 is activated, and generates the clock pulses NCK1, NCK2, and SCK (steps S1 and S3). The first clock switching circuit 41 selects the clock pulse NCK1 or NCK2 in accordance with the clock switch signal CS outputted from the KBC 12, and outputs the selected pulse as a normal-mode clock pulse. When the predetermined conditions for setting the sleep mode are not satisfied, the sleep mode controller 16 outputs the "L"-level control signal SS to the clock control circuit 18. In other words, the second clock switching circuit 42 of the clock control circuit supplies the clock pulse NCK as the clock CK to the CPU in a normal mode. In response to the clock pulse NCK (NCK1 or NCK2), the CPU 10 performs normal high-speed data processing (normal mode).

The CPU 10 checks in step S5 if the AC adapter 105 is connected. If the CPU 10 determines in step S5 that the AC adapter 105 is connected, the flow advances to step S17. On the other hand, if it is determined in step S5 that the AC adapter 105 is not connected, the CPU 10 checks in step S7 if the "H"-level mode control

data CD indicating that the control operation of the sleep mode controller 16 is to be prohibited is set in the control register 17. If YES in step S7, the CPU 10 advances the flow to step S17. On the other hand, if NO in step S7, the CPU 10 enables the sleep mode in step S9. More specifically, the CPU 10 executes the BIOS stored in the ROM 14 to detect a state wherein no key input is made from the keyboard 11 for a predetermined period of time. More specifically, the CPU 10 outputs a HALT instruction when input data from the KBC 12 is not stored in the key buffer of the memory 13 for a predetermined period of time. In other words, if no input data is stored in the key buffer, the logic circuit 100 (Fig. 3) outputs an "H"-level HALT instruction to the controller 16. If there is no file access for the I/O device 15 as an external device via the system bus 19 for a predetermined period of time, "L"-level signals BR and BP are outputted to the controller 16 (NO in step S13). When these conditions are satisfied (YES in step S11 and NO in step S13), the controller 16 outputs an "H"-level control signal SS to the clock control circuit 18. Upon reception of the "H"-level control signal SS, the second clock switching circuit 42 of the clock control circuit 18 supplies the low-frequency clock pulse SCK as the clock CK to the CPU 10. As a result, the mode of the CPU 10 is switched from the normal mode, i.e., a high-speed mode to the sleep mode, and the CPU 10 performs low-speed data processing in accordance with this clock pulse (steps S15 and S23). The sleep mode is released when a signal IR is generated in response to a data input from the keyboard 11 or when file access is made.

When the AC adapter 105 is connected (YES in step S5), or when the mode control data CD at logic level "H" for prohibiting the control operation of the sleep mode controller 16 is inputted from the keyboard 11, the data CD is set in the control register 17 (YES in step S7). As shown in Fig. 2, since the "L"-level signal is supplied from the control register 17 to the first input terminal of the AND gate 20a, setting of the sleep mode is prohibited. Therefore, even when the above-mentioned conditions are satisfied (YES in step S11 and NO in step S13), the sleep mode operation is disabled (step S17). More specifically, the second clock switching circuit 42 of the clock control circuit 18 supplies the clock NCK as the clock CK to the CPU 10 in response to the input "L"-level control signal SS. The CPU 10 executes normal high-speed data processing (normal mode) in response to the clock pulse NCK (step S19 and S21).

According to the present invention, when the power supply of the computer system is turned on, the initial program loader determines whether or not the AC adapter is connected, and if the AC adapter is connected, the clock control circuit prohibits supply of the low-frequency clock pulse to the CPU 10. As a result, the high-speed operation of the CPU can be maintained.

In the above embodiment, data set by a user in the setup menu or the pop-up menu and indicating whether the sleep mode is enabled or disabled is set in the register 17. However, the memory 13 may comprise a battery backup RAM, and the data may be stored in the memory 13.

In the above embodiment, whether or not the AC adapter is connected or whether or not the computer receives a power supply from an expansion unit for expanding a function of the personal computer is determined when the power supply is turned on. However, execution of the sleep mode may be disabled when the AC adapter is connected or when the computer receives a power supply from the expansion unit in a state wherein the personal computer is driven by the battery.

Claims

1. A computer system having a sleep mode function, characterized by comprising:

   processor means (10) for performing various data processing operations;

   clock control means (18) for selecting one of a first clock pulse at a predetermined high frequency required in a normal mode of said processor means, and a second clock pulse at a predetermined low frequency required in a sleep mode of said processor means, and supplying the selected clock pulse to said processor means;

   discrimination means (14) for discriminating whether or not said computer system receives an external power supply; and

   sleep operation control means (16) for, when said discrimination means discriminates that said computer system receives an external power supply, prohibiting said clock control means to supply the second clock pulse to said processor means.

2. A system according to claim 1, characterized in that said discrimination means includes means for discriminating whether or not an AC adapter is connected to said system to check whether or not a power is externally supplied.

3. A system according to claim 1, characterized in that said discrimination means includes means for discriminating whether or not said computer system receives a power supply from an expansion unit for expanding a function of said computer system which is releasably connected to said system.

4. A system according to claim 1, characterized in that said discrimination means includes initial program loader means for, when a power is supplied to said computer system, discriminating whether or not said computer system receives an external power supply.

5. A system according to claim 1, characterized in that said sleep operation control means comprises memory means for storing mode control data indicating that the sleep mode operation is prohibited.

6. A system according to claim 5, characterized in that said memory means comprises a register.

7. A system according to claim 5, characterized in that said memory means comprises a battery-backup random access memory (RAM).

8. A computer system including a main body having a battery and an external terminal for receiving an external power source, comprising:

a central processing unit (CPU) (10) performing data processing operations;

a clock control circuit (18) selecting one of a high clock pulse for operating said CPU at a high speed and a low clock pulse for operating said CPU at a low speed, the clock control circuit supplying the selected clock pulse to said CPU;

determination means (14) for determinating whether or not the main body receives the external power source through the external terminal; and

a sleep mode controller (16) instructing said clock control circuit to supply the high clock pulse to said CPU when said determination means determinates that the main body receives the external power source through the external terminal.

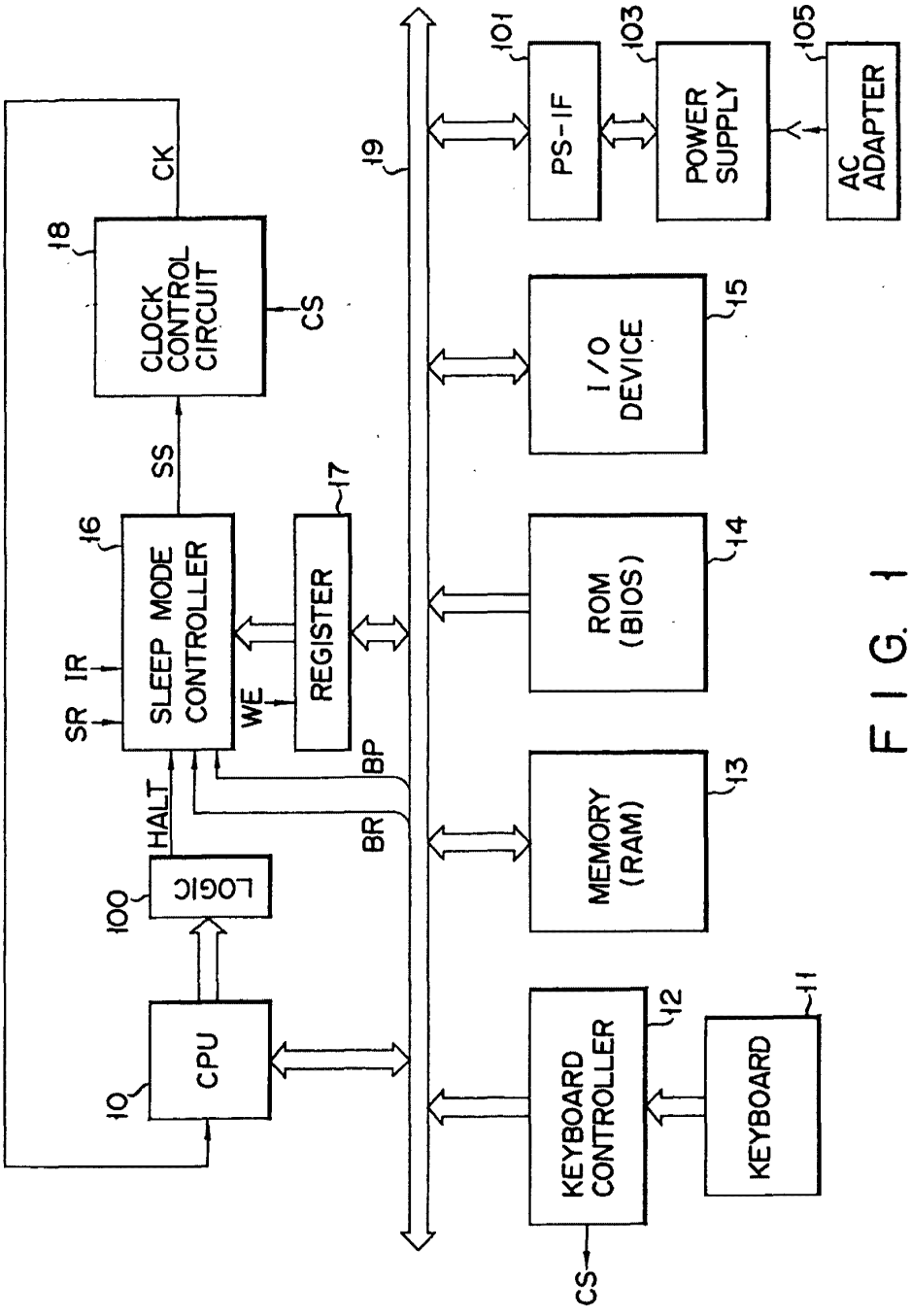

FIG. 1

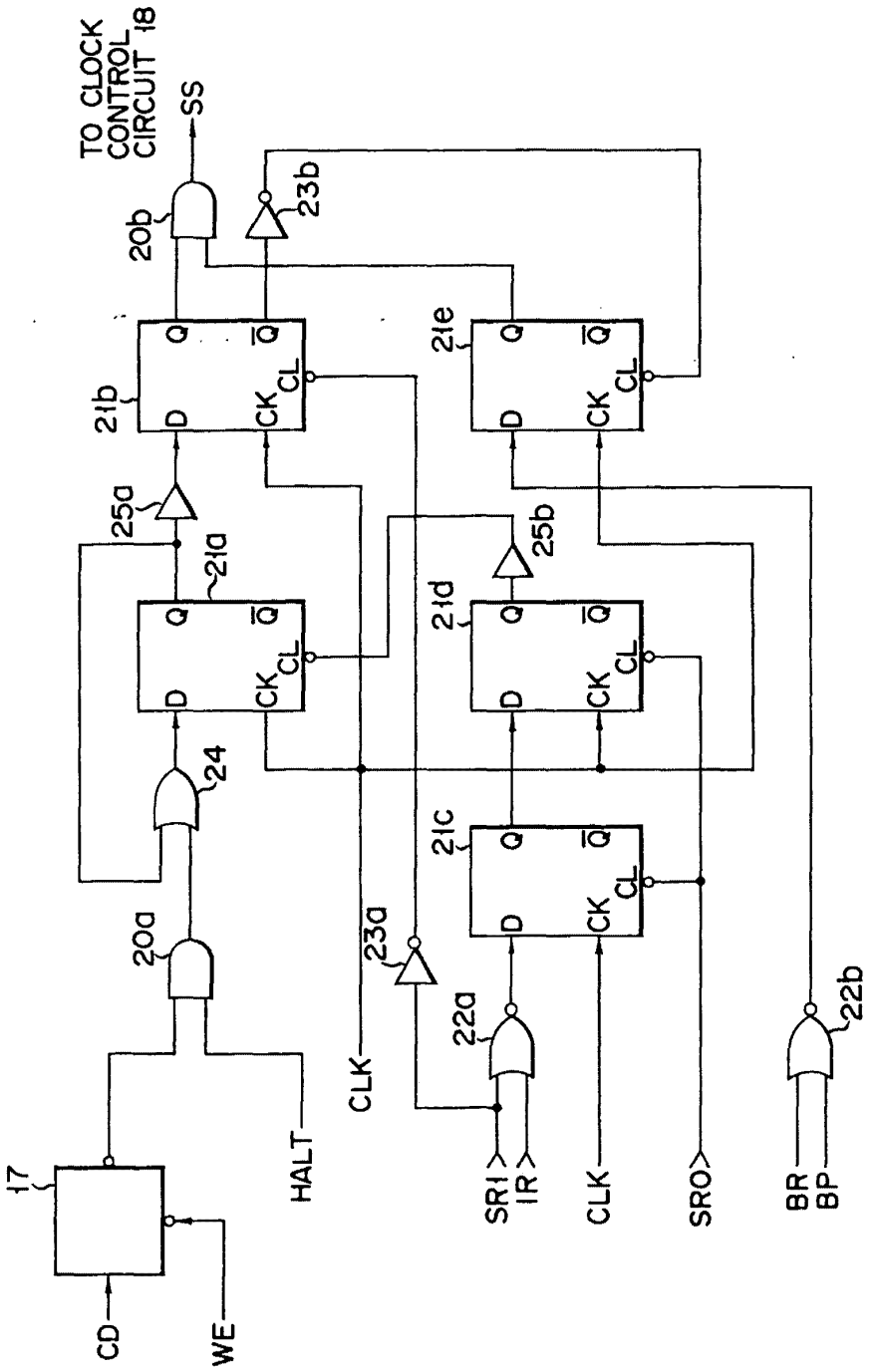

FIG. 2

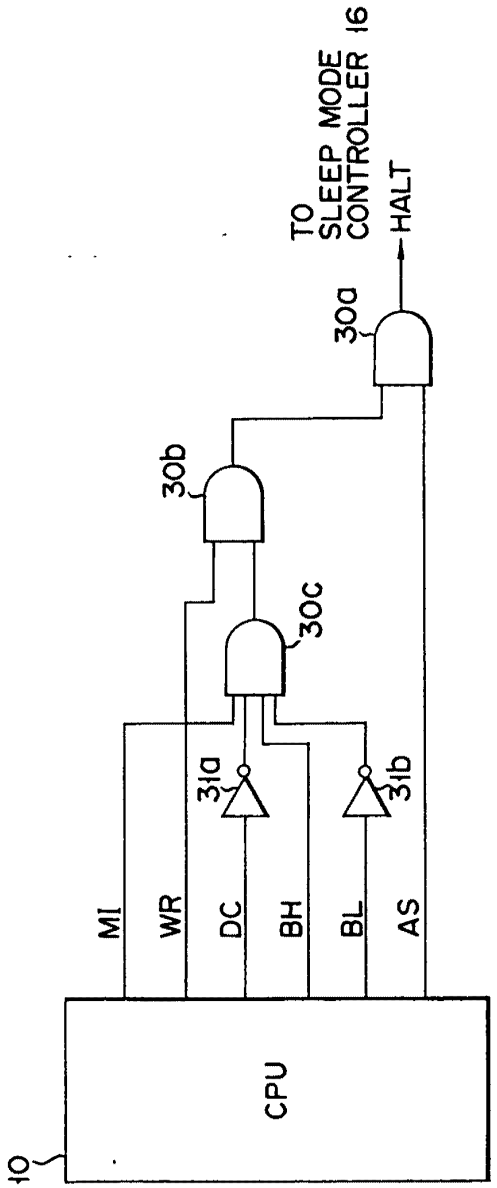

FIG. 3

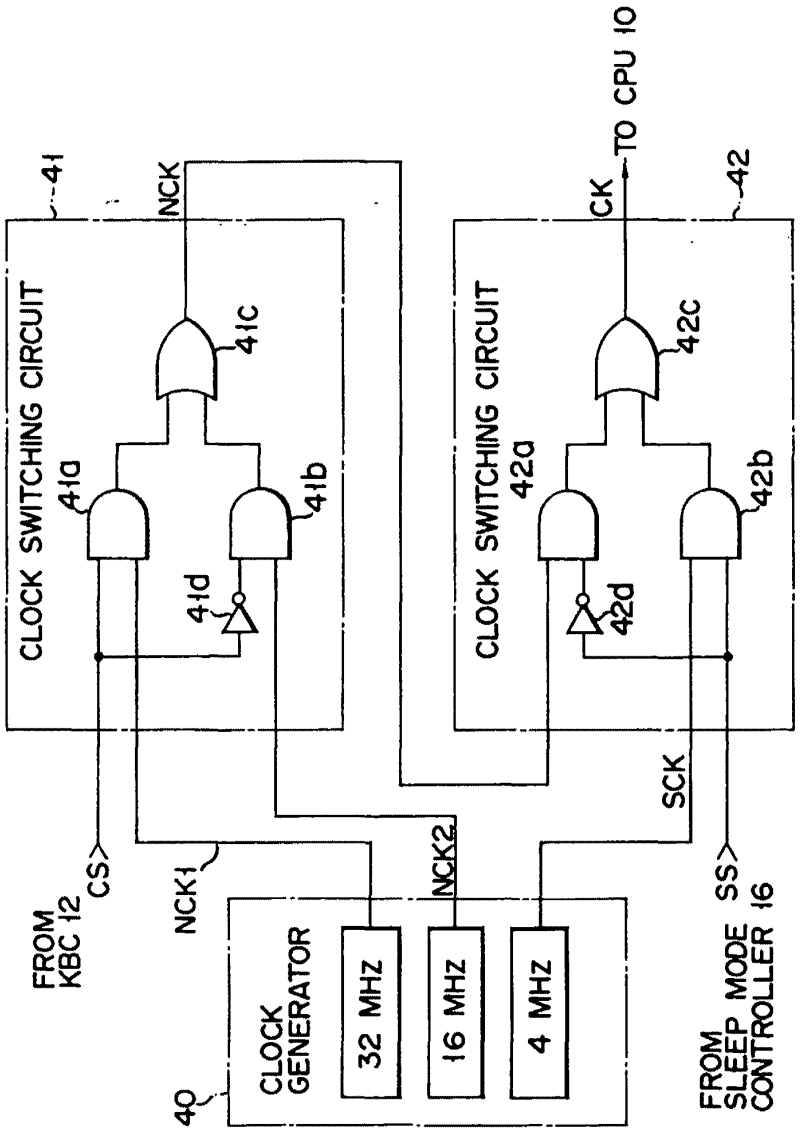

FIG. 4

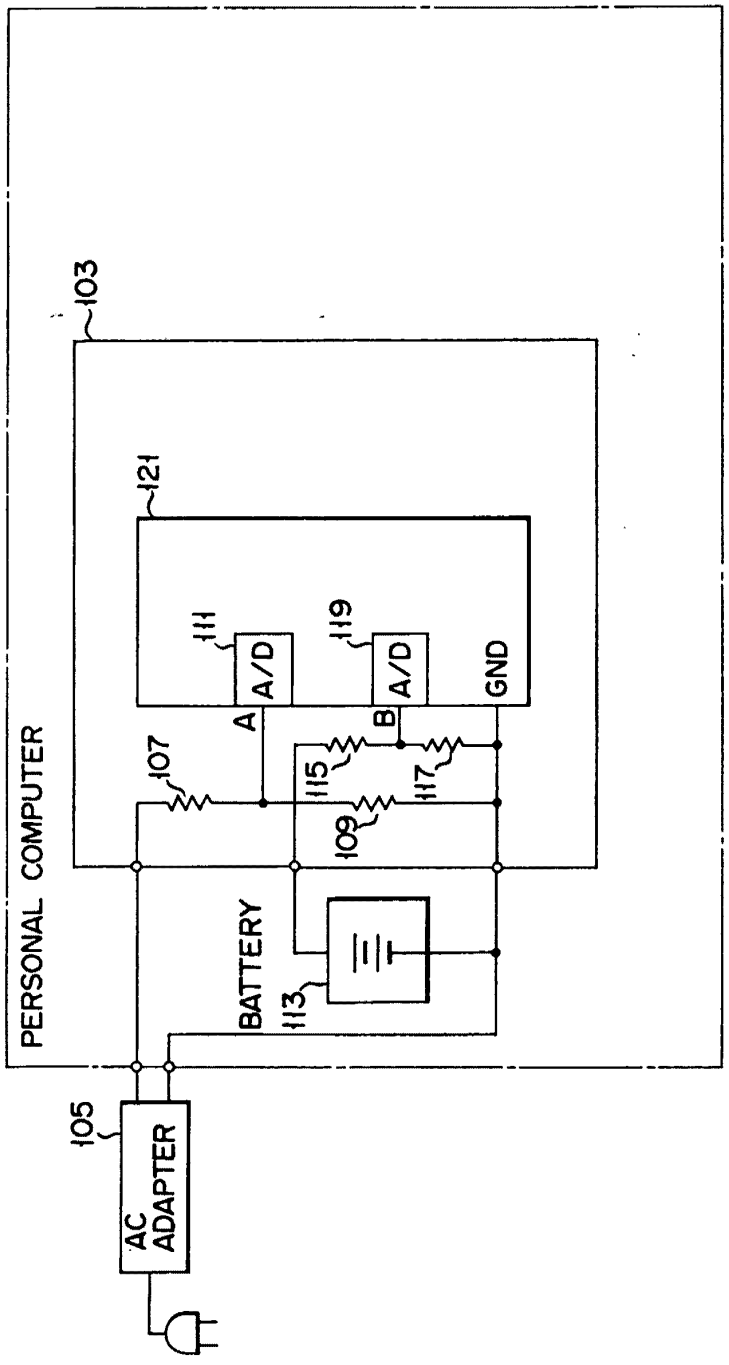
PERSONAL COMPUTER
103
121
111
A/D
119
A/D
GND
A
B
107
115
117
109
BATTERY
113
105
AC ADAPTER

FIG. 5

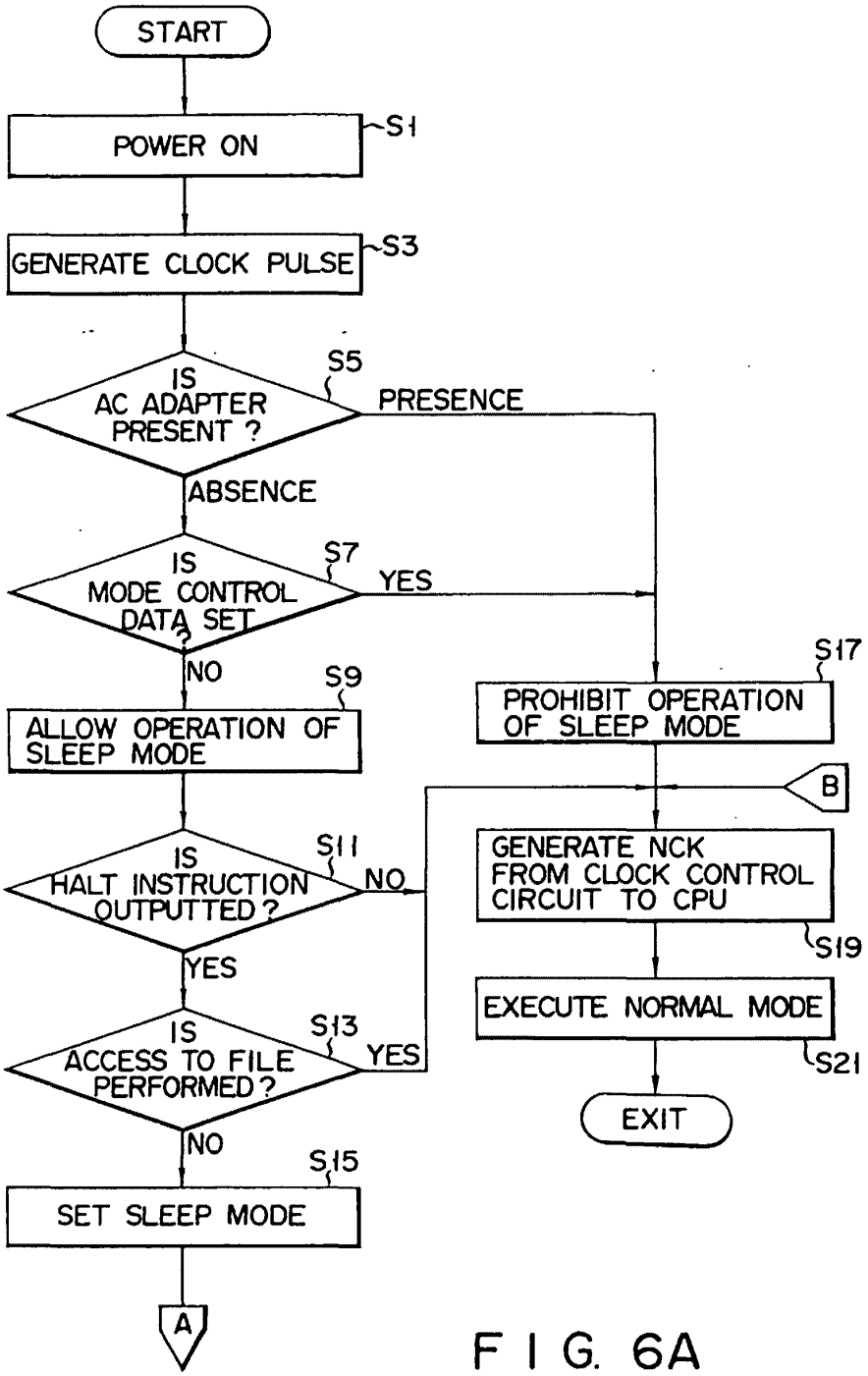

FIG. 6A

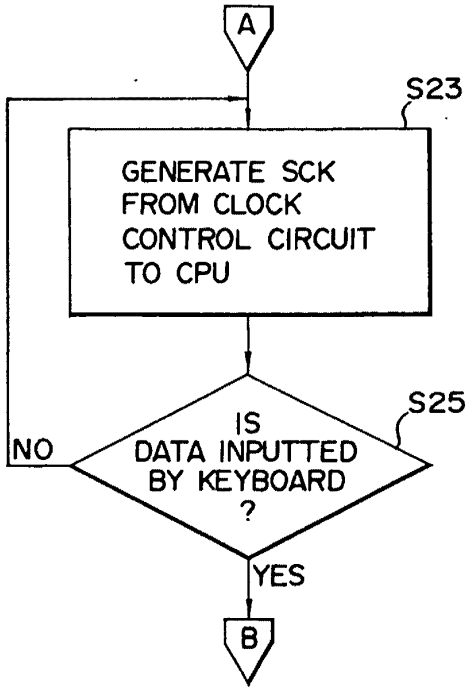

FIG. 6B

EP0381021

Publication Title:

Power saving system.

Abstract:

In a personal computer having a logic circuit constituted by low-power consumption elements such as CMOS elements, a power saving system includes a register (41) in which control data can be set from a keyboard (29) or by software, and switches (43) for allowing and stopping power supply from a power supply to an oscillator on the basis of control data from the register. Supply of clock signals to a disabled logic circuit can be stopped by an operator's decision. In initialization processing of a driver routine of an extended card optionally connected to the personal computer, power supply designation information is set in the register. In the completion routine, power supply stop designation information is set in the register.

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(71) Applicant: **Kabushiki Kaisha Toshiba**
72, Horikawa-cho Saiwai-ku
Kawasaki-shi(JP)

(72) Inventor: **Aihara, Norio, c/o Intellectual Property Division**
Kabushiki Kaisha Toshiba, 1-1 Shibaura 1-chome
Minato-ku, Tokyo 105(JP)

(74) Representative: **Henkel, Feiler, Hänzel & Partner**
Möhlstrasse 37
D-8000 München 80(DE)

(54) **Power saving system.**

(57) In a personal computer having a logic circuit constituted by low-power consumption elements such as CMOS elements, a power saving system includes a register (41) in which control data can be set from a keyboard (29) or by software, and switches (43) for allowing and stopping power supply from a power supply to an oscillator on the basis of control data from the register. Supply of clock signals to a disabled logic circuit can be stopped by an operator's decision. In initialization processing of a driver routine of an extended card optionally connected to the personal computer, power supply designation information is set in the register. In the completion routine, power supply stop designation information is set in the register.

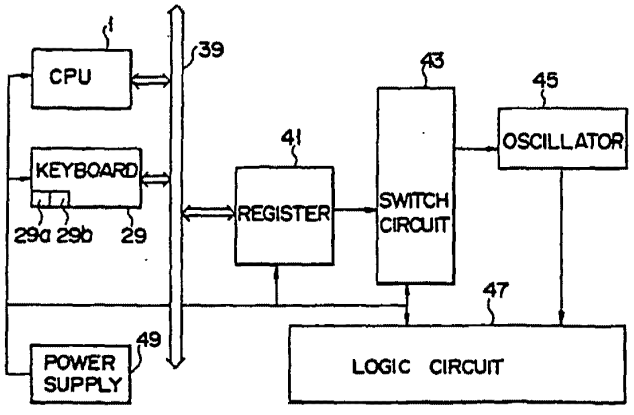

FIG. 2

EP 0 381 021 A2

Power saving system

The present invention relates to a power saving system having a logic circuit constituted by CMOS (Complementary Metal Oxide Semiconductor) elements and applied to, e.g., a personal computer.

In recent years, various types of chips such as microprocessor, memory and LSI chips are manufactured along with developments in semiconductor technologies, and packing densities of these chips are increasing year by year. As a result, compact personal computers have been developed, and for example, compact, light-weight, portable personal computers called lap-top computers have been very popular in place of desk-top personal computers. Most of the lap-top computers are designed as battery-operated computers. For this reason, these computers are designed to minimize power consumption of the internal circuits in order to prolong the operating time.

It is known that power consumption of a CMOS is minimized when a clock pulse is not supplied. A power-saving implementation is proposed wherein LSIs (Large Scale Integration Circuits) used in internal circuits of computers are arranged by CMOS elements.

Wasteful power consumption such as power consumption required for waiting for a key input from a keyboard is still present. Strong demand has arisen for further power saving.

It is an object of the present invention to provide a power saving system which utilizes CMOS characteristics which exhibit minimum power consumption in the absence of input clock pulses, thereby performing power saving in accordance with a software instruction.

According to the first aspect of the present invention, a power saving system for a personal computer which includes a logic circuit constituted by highly integrated semiconductor elements, comprises: a power supply for supplying power; clock signal generating means for receiving the power from the power supply and supplying a clock signal to the logic circuit; keyboard means including at least a power supply designation key for designating power supply to the clock signal generating means and a power supply stop designation key for designating stop of power supply to the clock signal generating means, and for outputting power supply designation information and power supply stop designation information; latch means for latching the power supply designation information or the power supply stop designation information from the keyboard means; and switch means, connected between the latch means and the clock signal generating means, for supplying the power to the clock signal generating means on the basis of the power supply designation information supplied from the latch means and for stopping power supply to the clock signal generating means on the basis of the power supply stop designation information supplied from the latch means.

According to the second aspect of the present invention, a power saving system for a personal computer which includes a logic circuit constituted by highly integrated semiconductor elements and receives an input signal and outputs a predetermined signal, comprises: a power supply for supplying power; clock signal generating means for receiving the power from the power supply and supplying a clock signal to the logic circuit; latch means for latching power supply stop designation information; memory means for storing a control program serving as a logic circuit driver routine executed by the personal computer, the control program determining whether a predetermined signal is output from the logic circuit within a predetermined period of time and setting the power supply stop designation information in the latch means when the predetermined signal is not output within the predetermined period of time; and switch means, connected between the latch means and the clock signal generating means, for stopping power supply to the clock signal generating means on the basis of the power supply stop designation information supplied from the latch means.

According to the third aspect of the present invention, a power saving system for a personal computer, comprises: a power supply for supplying power; extended card means, optionally connectable to the personal computer, for executing a predetermined logical function; clock signal generating means for receiving the power from the power supply and supplying a clock signal to the extended card means; latch means for latching power supply designation information or power supply stop designation information; memory means for storing a program serving as an extended card driver routine executed by the personal computer, the program including an initialization routine for setting the power supply designation information in the latch means and a completion routine for setting the power supply stop designation information in the latch means after a predetermined function is executed by the extended card means; and switch means, connected between the latch means and the clock signal generating means, for supplying the power to the clock signal generating means on the basis of the power supply designation information supplied from the latch means and for stopping power supply to the clock signal generating means on the

basis of the power supply stop designation information supplied from the latch means.

Additional objects and advantages of the invention will be set forth in the description which follows, and in part will be obvious from the description, or may be learned by practice of the invention. The objects and advantages of the invention may be realized and obtained by means of the instrumentalities and combinations particularly pointed out in the appended claims.

Other objects and features of the present invention will be apparent from the following description taken in connection with the accompanying drawings, in which:

Fig. 1 is a block diagram showing an arrangement of a personal computer which employs a power saving system according the present invention;

Fig. 2 is a block diagram of a power saving system according to the first embodiment of the present invention;

Fig. 3 is a data format showing bit assignment of a register shown in Fig. 2;

Fig. 4 is a flow chart for controlling power supply upon operations of power ON and OFF keys arranged on a keyboard;

Fig. 5 is a flow chart for controlling power supply by time-out;

Fig. 6 is a flow chart in which power supply control is utilized in a driver routine of an extended card optionally connected to the power saving system; and

Fig. 7 is a block diagram showing a power saving system according to the second embodiment of the present invention.

Fig. 1 is a block diagram showing an arrangement of a personal computer which employs a power saving system according to the present invention.

Referring to Fig. 1, a CPU (Central Processing Unit) 1 controls the overall system operations of the personal computer. A ROM (Read Only Memory) 3 stores a basic input and output operating system (BIOS) program for controlling inputs/outputs of the personal computer. This BIOS includes programs represented by flow charts of Figs. 4 to 6. A RAM (Random Access Memory) 5 stores application programs executed by this personal computer and various data. A DMAC (Direct Memory Access Controller) 7 comprises a commercially available LSI for controlling DMA. A PIC (Interrupt Controller) 9 comprises a commercially available LSI for controlling various circuit interrupts. A PIT (timer) 11 measures time. An RTC (Real Time Clock) 13 comprises a commercially available LSI for storing date, time, an the like.

An HDC (Hard Disk Controller) 15 comprises a commercially available LSI for controlling an HDD (Hard Disk Driver) 17. The HDD (Hard Disk Drive) 17 serves as an external storage unit for storing programs and data. An FDC (Floppy Disk Controller) 19 comprises a commercially available LSI for controlling an FDD (Floppy Disk Drive) 21. The FDD 21 serves as an external storage unit for storing programs and data as in the HDD 17. A PRTCONT (Printer Controller) 23 controls a printer. An SIO (Serial Input and Output Control Circuit) 25 comprises a commercially available LSI for controlling communication. A KBC (Keyboard Controller) 27 comprises a commercially available LSI for controlling a keyboard 29. The keyboard 29 comprises various keys for inputting various data and includes a power ON command key 29a for designating power supply and a power OFF command key 29b for designating power of power supply. A PDPC (Plasma Display Controller) 31 controls a PDP (Plasma Display) 33. A VRAM (Video RAM) 35 serves as a memory for storing the content displayed on the PDP 33. Data is read out from a kanji ROM 37 to display kanji characters, and the readout kanji information is displayed on the PDP 33. The CPU 1, the ROM 3, the RAM 5, the DMAC 7, the PIC 9, the PIT 11, the RTC 13, the HDC 15, the FDC 19, the PRTC 23, the SIO 25, the KBC 27, the PDPC 31, the VRAM 35, and the kanji ROM 37 are connected to a system bus 39.

Fig. 2 is a block diagram showing a power saving system according to the first embodiment of the present invention.

A register 41 is connected to the system bus 39. The register 41 stores control data for ON/OFF-controlling the power supply. More specifically, the register 41 comprises, e.g., a 16-bit register. As shown in Fig. 3, bit information for controlling power ON/OFF is assigned to, e.g., bit 0. That is, when bit 0 is set at logic "1", the power is supplied to the respective circuits. However, when bit 0 is set at logic "0", the power OFF state is set. A bit output from the register 41 is supplied to a switch circuit 43. This register 41 may be assigned to the RAM 5 in the form of, e.g., a memory mapped I/O. Alternatively, I/O device addresses may be assigned to this register. In either case, the register 41 can be accessed by software.

The switch circuit 43 comprises an electronic switch (constituted by, e.g., transistors) or a relay circuit. When a bit output from the register 41 is set at logic "1", the power is supplied from a power supply 49 to an oscillator 45. However, when the bit output is set at logic "0", the power supply is stopped. When the oscillator 45 receives the power through the switch circuit 43, the oscillator 45 outputs a clock signal to a logic circuit 7. The power supply 49 is connected to supply the power to the CPU 1, the keyboard 29, the register 41, the switch circuit 43, and the logic circuit 47. The logic

circuit 47 comprises a CMOS circuit for performing a predetermined function. For example, in the block diagram of Fig. 1, the logic circuit 47 corresponds to the DMAC 7, the PIC 9, the PIT 11, the RTC 13, the FDC 19, the PRTC 23, the SIO 25, the KBC27, the PDC 31, and the like. Although not illustrated, the logic circuit 47 also includes a LAN (Local Area Network) controller and a MODEM (Modulator Demodulator).

Power supply or stop of power supply can be designated automatically or by an operator. The flow chart shown in Fig. 4 exemplifies an operation for detecting depression of the power OFF or ON command key 29a or 29b arranged on the keyboard 29 and for allowing or stopping power supply from the power supply to the oscillator 45.

The CPU 1 determines in step 51 whether a key input is detected. If YES in step 51, the CPU 1 determines in step 53 whether the depressed key is the power OFF command key 29a. If YES in step 53, data "01" (hex) is set in the register 41 in step 55. As a result, bit data of "1" is supplied from the register 41 to the switch circuit 43, and then the switch circuit 43 supplies the power from the power supply 49 to the oscillator 45. Therefore, the oscillator 45 supplies a clock signal to the logic circuit 47, and the logic circuit is operated.

When the CPU 1 determines in step 57 that the power ON command key 29b is depressed, the CPU 1 sets data "00" (hex) in the register 41 in step 59.

Bit data of "0" is supplied from the register 41 to the switch circuit 43, and the switch circuit 43 does not supply the power to the oscillator 45. In this case, no clock signal is supplied from the oscillator 45 to the logic circuit 47. The power consumption of the logic circuit 47 becomes minimum, and the power can be saved.

Fig. 5 is a flow chart showing an operation for automatically controlling power supply to the KBC (Keyboard Controller) 27.

The CPU 1 determines in step 61 whether a key input is detected. If NO in step 61, a time-measuring software counter is incremented in step 63. The CPU 1 then determines in step 65 whether a predetermined period of time has elapsed. If NO in step 65, the CPU 1 repeats the operations in steps 61, 63, and 65. When the CPU 1 determines in step 65 that the predetermined period of time has elapsed, the CPU 1 sets data "00" (hex) in the register 41 in step 67. As described above, in this case, the switch circuit 43 does not supply the power to the oscillator 45, and the oscillator 45 does not supply the clock signal to the logic circuit 47 accordingly. As a result, the power consumption of the logic circuit 47 becomes minimum, and the power can be saved.

Fig. 6 is a flow chart showing an operation for automatically controlling power supply or stop of power supply when, e.g., a LAN drive routine is loaded or unloaded.

Assume that the system bus of the personal computer shown in Fig. 1 is connected to an external connector (not shown), and that a LAN control card serving as an extended card can be optionally connected to this personal computer. In this case, the LAN driver routine is prestored in the HDD 17. In order to perform LAN control, the LAN driver routine stored in the HDD 17 is loaded in the RAM 5 and is executed by the CPU 1.

In step 71 as an initialization routine, the CPU 1 sets data "01" (hex) in the register 41. The switch circuit 43 supplies the power to the oscillator 45, and the oscillator 45 then supplies a clock signal to the logic circuit 47 (in this case, to the LAN card). The LAN card is then operated. After the predetermined LAN processing routine is executed, the CPU 1 performs completion processing in step 73. In this completion processing, the CPU 1 sets data "00" (hex) in the register 41. In this case, the switch circuit 43 stops supplying the power to the oscillator 45. Therefore, the power consumption of the LAN card becomes minimum, and the power can be saved.

Fig. 7 is a block diagram of a power saving system according to the second embodiment of the present invention. The same reference numerals as in Fig. 1 denote the same parts in Fig. 2, and a detailed description thereof will be omitted.

In the embodiment shown in Fig. 7, power from a power supply 49 is always supplied to an oscillator 45. A clock signal is supplied from the oscillator 45 to a gate circuit 75. The gate circuit 75 comprises, e.g., an AND gate and supplies a clock signal from the oscillator 45 to a logic circuit 47 in response to an enable signal from a CPU 1. The enable signal supplied from the CPU 1 may be supplied from a keyboard as in Fig. 2 or may be obtained by utilizing the concept of time-out, as shown in Fig. 4, or an enable or disable signal may be formed in the initialization and completion routines in the extended load module, as shown in Fig. 6. The same effect as in the embodiment of Fig. 2 can be obtained in the above modifications.

In the second embodiment, the LAN card is exemplified as the extended card. However, the present invention is not limited to this. For example, power supply of various external optional cards such as an SCSI (Small Computer System Interface) control card, various communication boards, a keyboard controller, a printer controller, a display circuit controller, and a modem card can be controlled.

In the above embodiment, the programs shown in Figs. 4 to 6 are stored in the ROM 3. However, these programs may be stored in, e.g., the HDD 17

and the FDD 21.

Additional advantages and modifications will readily occur to those skilled in the art. Therefore, the invention in its broader aspects is not limited to the specific details, representative devices, and illustrated examples shown and described. Accordingly, departures may be made from such details without departing from the spirit or scope of the general inventive concept as defined by the appended claims and their equivalents.

Claims

1. A power saving system for a personal computer having a logic circuit (47) constituted by highly integrated semiconductor elements, a power supply (49) for supplying power, and an oscillator (45) for receiving the power from said power supply and supplying a clock signal to said logic circuit, characterized by comprising:
means (29a, 29b, Figs. 4, 5, and 6) for designating supply and stop of supply of the clock signal to said logic circuit; and
control means (41, 43, 75) for controlling the supply or the stop of supply of the clock signal to said logic circuit in response to designation information from said designating means.

2. A system according to claim 1, characterized in that said designating means comprises a keyboard (29) including at least a power supply designation key (29a) for designating power supply from said power supply to said oscillator and a power supply stop key (29b) for designating stop of power supply from said power supply to said oscillator, said keyboard (29) being arranged to output power supply designation information and power supply stop designation information.

3. A system according to claim 1, characterized in that said logic circuit receives an input signal and outputs a predetermined signal, and
said designating means comprises memory means (3, 17, 21) for storing a control program serving as a logic circuit driver routine executed by said personal computer, the control program setting the power supply stop designation information when the predetermined signal is not output from said logic circuit within a predetermined period of time.

4. A system according to claim 1, characterized in that said logic circuit includes optional extended card means, connectable to said personal computer, for executing a predetermined logic function, and said designating means comprises memory means for storing a program serving as an extended card driver routine executed by said personal computer, the control program including an initialization routine for outputting power supply designation information and a completion routine for outputting the power supply stop designation information after the predetermined function is performed by said extended card means.

5. A system according to any one of claims 1 to 4, characterized in that said control means comprises:
latch means (41) for latching information for designating supply and stop of supply of the clock signal; and
switch means (43), connected between said latch means and said oscillator, for supplying the power to said oscillator on the basis of the clock supply designation information supplied from said latch circuit and for stopping power supply to said oscillator on the basis of the clock supply stop designation information supplied from said latch circuit.

6. A system according to any one of claims 1 to 4, characterized in that said control means comprises gate means (75), connected between said oscillator and said logic circuit, for receiving the clock supply designation information and supplying the clock signal from said oscillator to said logic circuit, and for stopping supply of the clock signal to said logic circuit on the basis of the clock supply stop designation information.

7. A system according to any one of claims 1 to 6, characterized in that said logic circuit comprises CMOS (Complementary Metal Oxide Semiconductor) elements.

8. A system according to any one of claims 1 to 7, characterized in that said logic circuit includes a LAN (Local Area Network) control circuit, an SCSI (Small Computer System Interface) control circuit, a communication board, a keyboard controller, a printer controller, a display controller, and a model control circuit.

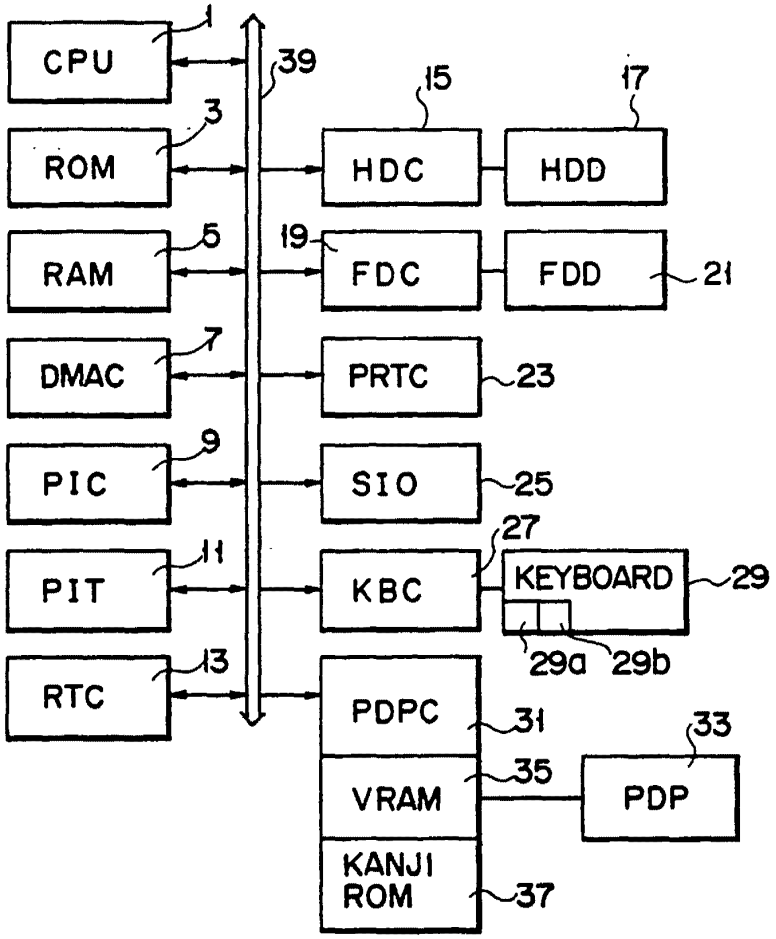
CPU
1
39
ROM
3
HDC
15
HDD
17
RAM
5
19
FDC
FDD
21
DMAC
7
PRTC
23
PIC
9
SIO
25
PIT
11
KBC
27
KEYBOARD
29
29a
29b
RTC
13
PDPC
31
33
VRAM
35
PDP
KANJI ROM
37

FIG. 1

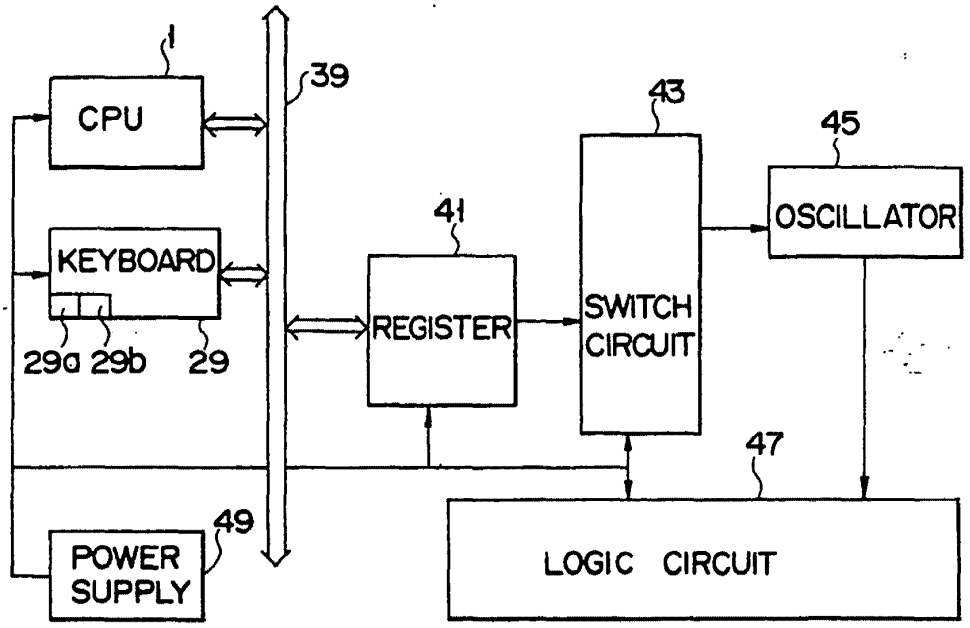
1
39
CPU
43
45
41
KEYBOARD
OSCILLATOR
REGISTER
SWITCH CIRCUIT
29a 29b 29
47
49
POWER SUPPLY
LOGIC CIRCUIT

FIG. 2

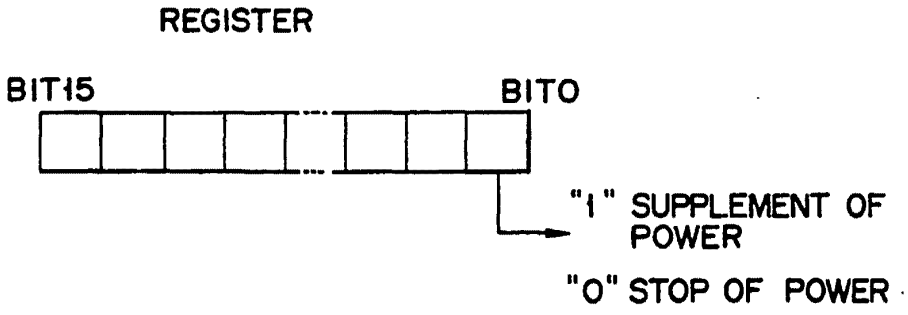
REGISTER
BIT15
BIT0
"1" SUPPLEMENT OF POWER
"0" STOP OF POWER

FIG. 3

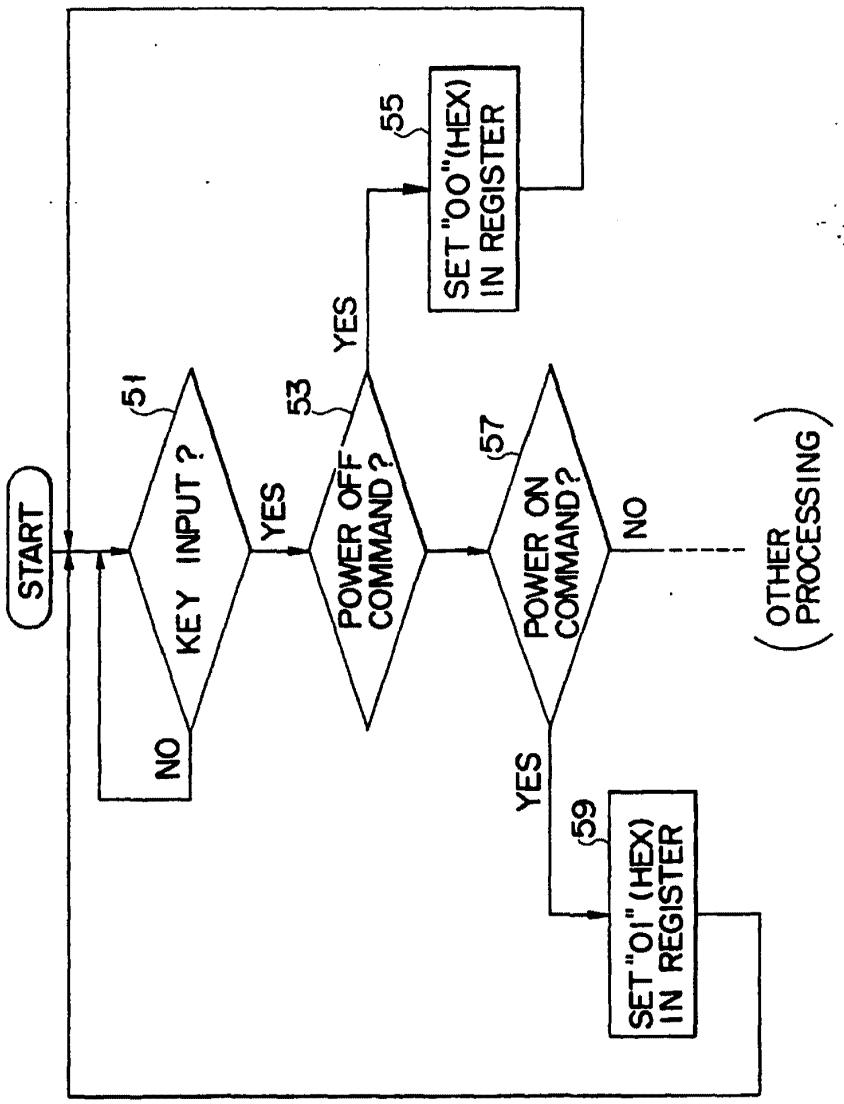
START
KEY INPUT ?
NO
YES
51
POWER OFF COMMAND ?
YES
53
SET "00" (HEX) IN REGISTER
55
POWER ON COMMAND ?
NO
57
OTHER PROCESSING
YES
59
SET "01" (HEX) IN REGISTER

FIG. 4

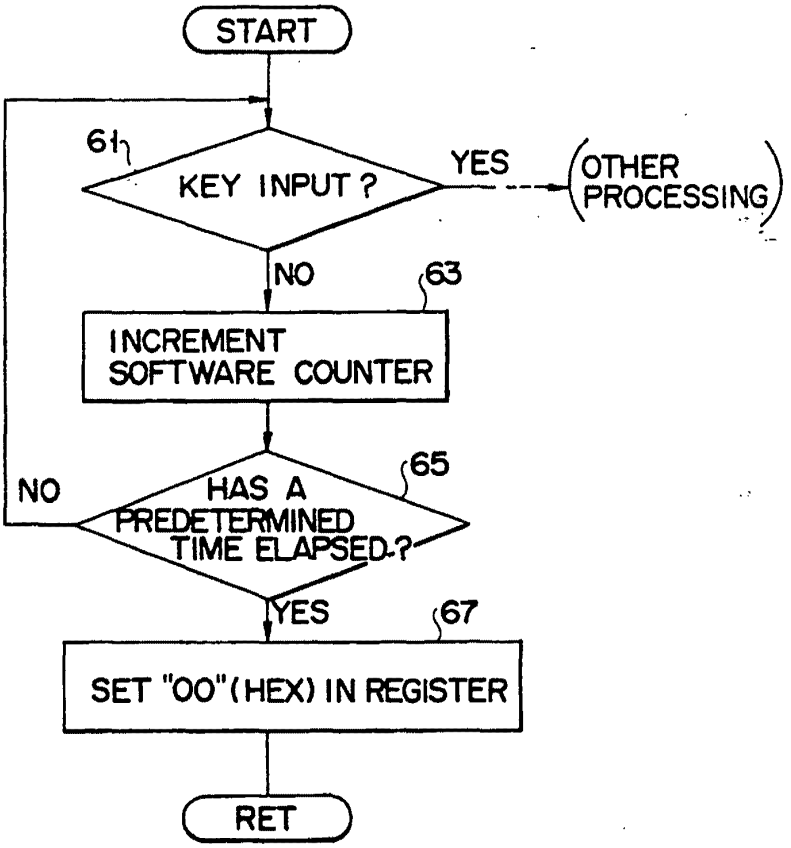

FIG. 5

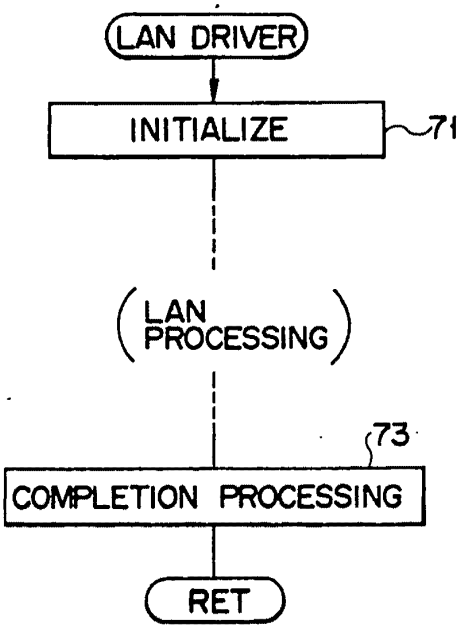
LAN DRIVER
INITIALIZE
71
LAN PROCESSING
73
COMPLETION PROCESSING
RET

FIG. 6

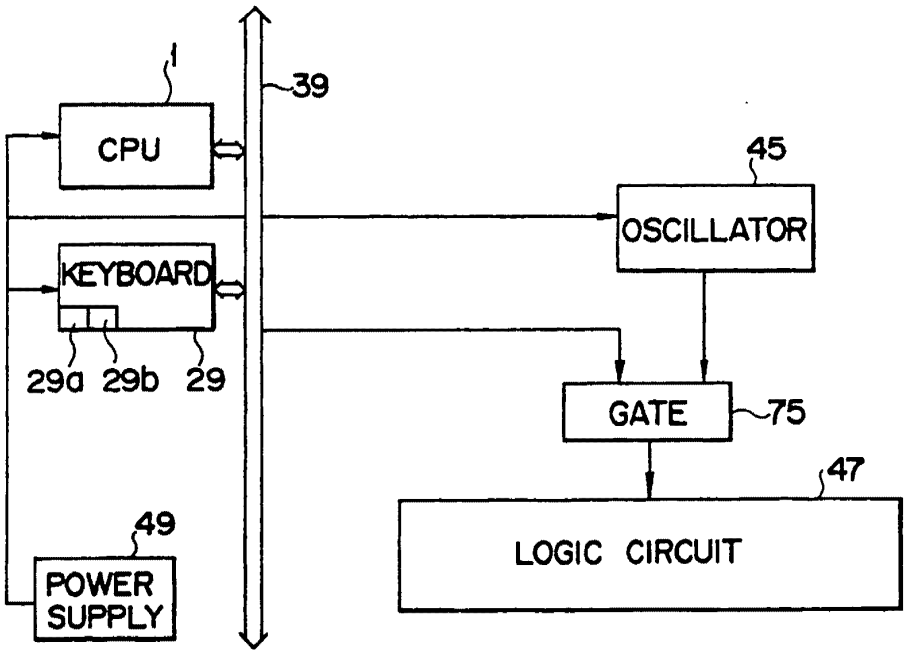
1
39
CPU
45
OSCILLATOR
KEYBOARD
29a
29b
29
GATE
75
47
49
POWER SUPPLY
LOGIC CIRCUIT

FIG. 7

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(71) Applicant: ADVANCED MICRO DEVICES, INC. [US/US]; One AMD Place, Mail Stop 68, Sunnyvale, CA 94088-3453 (US).

(72) Inventors: QURESHI, Qadeer, Ahmad; 16708 Tomcat Drive, Round Rock, TX 78681 (US). MITCHELL, Charles, Weldon; 6501 Skinner Cove, Austin, TX 78759 (US). CALDWELL, Dervinn, Deyual; 3837 Burton Common, Fremont, CA 94536 (US). BAUM, Gary; 189 Ehrlich Road, Austin, TX 78746 (US). ODIORNE, Kyle; 317 Robin Way, Richardson, TX 75080 (US).

(74) Agent: RILEY, Louis, A.; Advanced Micro Devices, Inc., 5204 East Ben White Boulevard, M/S 562, Austin, TX 78741 (US).

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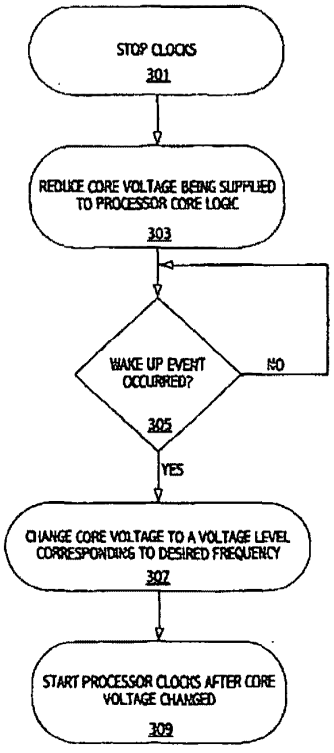
(54) Title: MINIMIZING POWER CONSUMPTION DURING SLEEP MODES BY USING MINIMUM CORE VOLTAGE NECESSARY TO MAINTAIN SYSTEM STATE



(57) Abstract: A control circuit reduces voltage being supplied to an integrated circuit in a sleep mode in which context (e.g. CPU state) is maintained. Because the voltage required to maintain the integrated circuit state intact may be significantly less than the voltage at which the integrated circuit can functionally operate at a predetermined frequency, significant power savings can be achieved by reducing voltage while the clocks are stopped, thereby reducing leakage current and saving power.

WO 01/27728 A1

MINIMIZING POWER CONSUMPTION DURING SLEEP MODES BY USING MINIMUM CORE VOLTAGE NECESSARY TO MAINTAIN SYSTEM STATE

Technical Field

This invention relates to power consumption in integrated circuits and more specifically to reducing power consumption on an integrated circuit while clocks are stopped.

Background Art

A conventional notebook computer has power constraints that cause it to employ techniques to reduce power consumption to conserve battery life. In addition, the conventional notebook computer has thermal constraints due to a small, densely packed system construction that limits its ability to safely dissipate the heat generated by computer operation. The power savings techniques also beneficially reduce the amount of heat needed to be dissipated.

The frequency of operation (clock frequency) of the processor and its operating voltage are primary determinants of power consumption. Since power consumption and dissipation are roughly proportional to the processor's frequency of operation, scaling down the processor's frequency has been a common method of staying within notebook computer power and thermal limitations.

A common power management technique, called "throttling", temporarily stops processor clocks, to reduce power consumption and thus reduce heat generation. Throttling continuously stops and starts processor operation by turning its clocks off and on according to a predefined duty cycle with a period of a few milliseconds. The reduction in the effective speed of the processor reduces power dissipation and thus the processor's temperature. A clock control signal (e.g., STPCLK# in x86 architectures) modulates the duty cycle of processor operation. The clock control signal, when asserted, causes the processor to gate off the clocks being supplied to core logic in the processor. In some current processor designs, e.g., x86 processors, a Stop Grant cycle on a host or system bus is executed to indicate that the stop clock request on the asserted clock control signal has been completed. A temperature sensor placed on or near the processor's heat sink can initiate throttling when needed.

In addition, when operating from its battery, most notebooks take advantage of the processor's idle periods by periodically stopping processor operation to reduce power consumption. Applications like word processors typically leave the processor idle much of the time. For example, in a word processing application, a processor will do a brief burst of work after each letter is typed, then its operation is stopped until the next keystroke. As a result, the typical processor power consumption when running a word processing application, can be as much as 30-50% below the maximum. That idle time can be exploited by the computer system to achieve additional power savings by putting the processor to sleep temporarily.

Current x86 based computer systems utilize an industry supported power management approach described in the Advanced Configuration and Power Interface Specification (ACPI), Revision 1.0a, by Intel, Microsoft and Toshiba dated November 19, 1998, which is incorporated herein by reference. The ACPI is an

operating system (OS) controlled power management scheme that uses features built into the Windows 95, 98 and Windows NT or other compatible operating systems. It defines a standard interrupt (System Control Interrupt or SCI) that handles all ACPI events. System control interrupts are generated by devices to inform the OS about system events.

As part of that power management approach, ACPI specifies sleep and suspend states. Sleep states temporarily halt processor operation and operation can be restored in a few milliseconds. A computer system processor enters the sleep state when internal activity monitors indicate no processing is taking place. When a keystroke is entered, a mouse moves or data is received via a modem, the processor wakes up in order to resume operation, the clocks are turned on and the CPU continues executing from where it left off.

Other modes save processor context external to the processor such as to system memory or even to hard disk. Suspend states shut down more of the notebook's system (e.g. display or hard drive) and take a few seconds for operation to be restored. Suspend states copy the present context of the system (sufficient for the computer to resume processing the application(s) presently opened) into memory (suspend to RAM) or to the hard drive (suspend to disk) and power down peripherals. Obviously in these other modes, longer latency is incurred to resume normal system operation.

When computer systems stop the central processing unit (CPU) clocks during a sleep mode or during throttling, a short latency for resuming processor operation is desirable. One way to achieve that short latency is to ensure that CPU context is not lost. That means that the various latches and other circuit nodes in the CPU that hold information required (e.g., the state of processor registers) for the processor to resume operations where it left off, are maintained in the CPU while clocks are stopped. Maintaining processor context requires that the CPU receive power even though the clocks are stopped.

Note that processors typically have separate regions of the chip that receive separate power supply voltages. For example, such regions may include a core region, as well as a peripheral region where input/output (I/O) circuits are located. The peripheral region often remains powered up even if the core voltage is turned off. Therefore, core voltage which must be maintained to ensure processor context is maintained (assuming I/O voltage is also on). In most current notebook designs, CPU core voltage is typically set during initialization, and is not changed after that.

When power is supplied during the sleep state to maintain CPU context, the CPU still consumes power because of leakage current. The leakage current is generally proportional to the core voltage, and the power consumption is proportional to the square of the core voltage. The leakage current can be significant enough to drain the battery. For example, an AMD-K-6®-2 processor can consume several hundred milliwatts while in sleep mode. Additionally, some circuit designs may be more leaky than others, resulting in even more power being consumed in sleep mode.

It is desirable to reduce power consumption in computers, particularly in portable computers where maximizing battery life and reducing heat generation by reducing power consumption is particularly

advantageous. Therefore it would be desirable to reduce power consumption, if possible, when clocks are stopped and power is being consumed due to leakage current.

DISCLOSURE OF INVENTION

Accordingly, the invention provides a way to save power while a processor (or other integrated circuit) is in a sleep mode in which context is maintained. Because the voltage required to maintain the integrated circuit context (e.g. processor state) intact may be significantly less than the voltage at which the processor can functionally operate at a particular frequency, significant power savings can be achieved by reducing processor voltage while the processor clocks are stopped.

In one embodiment, the invention provides a method of supplying a first voltage to at least a first circuit portion of an integrated circuit during an operational mode. The method further includes stopping clocks which are being supplied to the first circuit portion to place the integrated circuit in a reduced power consumption state and then supplying a second voltage, less than the first voltage, to the first circuit portion while the clocks are stopped, the second voltage being at a voltage sufficient to maintain context of the first circuit portion in existence at a time when the clocks were stopped.

In another embodiment, the invention provides an apparatus that includes an integrated circuit that has a plurality of circuits holding, at least in substantial part, context indicative of a current operational state of the integrated circuit. A power supply circuit supplies variable voltages to the integrated circuit. A control circuit is coupled to the power supply circuit, and supplies the power supply circuit with first voltage control information, indicating a first voltage to be supplied, while clocks are being supplied to the plurality of circuits. The control circuit supplies the power supply circuit with second voltage control information, indicating a second voltage to be supplied, while the clocks are stopped, the second voltage being lower than the first voltage.

BRIEF DESCRIPTION OF DRAWINGS

The present invention may be better understood, and its numerous objects, features, and advantages made apparent to those skilled in the art by referencing the accompanying drawings, wherein:

Fig. 1 illustrates an exemplary system that can exploit the present invention;

Fig. 2 illustrates additional details over a control circuit used in one embodiment of the present invention; and

Fig. 3 is a flow chart of an embodiment of the present invention.

MODE(S) FOR CARRYING OUT THE INVENTION

Additional power savings can be realized in computer systems by reducing the voltage supplied to the processor during a state in which processor clocks are stopped and processor context is maintained. With the

clocks off, the voltage level required to maintain processor context can be reduced to levels below that needed for proper operation of the clocked circuits. Put another way, the voltage required to maintain state, is lower than that needed to change state reliably.

In an exemplary embodiment illustrated in Fig. 1, voltage regulator 101 supplies core voltage 102 to processor (CPU) 103. In the embodiment illustrated, integrated circuit 105 controls the voltage level that is supplied to CPU 103 by supplying voltage control signals VID[0:4] to voltage regulator 101. VID refers to "voltage ID" which is commonly used in the industry to describe the voltage control signals. Integrated circuit 105 may be a south bridge integrated circuit, which is known in the art as one chip of a chipset pair. The south bridge, originally providing a bridge between the Peripheral Component Interconnect (PCI) bus and the ISA bus, also typically incorporates power management functions. The south bridge may also contain integrated legacy functions, as well as interfaces for newer buses such as Universal Serial Bus (USB) and other additional functions. The chipset pair also typically includes a north bridge integrated circuit (not shown) that provides a memory control function as well as a bridge function between the host bus connected to the processor and the Peripheral Component Interconnect (PCI) bus. Clock generator 107 supplies a clock signal 106 used by CPU 103 to generate clocks supplied to core logic in the processor. Clock generator 107 can be controlled by clock stop signal 112 to selectably turn on and off clocks supplied to CPU 103 and other system components.

The variable voltage regulator 101 may be, e.g., the National Semiconductor's LM4130, whose output voltage can be controlled by an external device such as south bridge 105. It is desirable for the voltage regulator to support at least four control bits and for the output voltage to be controllable in steps of 50mV (or smaller) covering a minimum range of from 1.45 to 2.2 volts. A wider range or different granularity may be desirable in some applications.

The CPU clocks can be stopped as follows. The "stop clock" signal refers to STPCLK# signal 110 (where # indicates an active low signal), which causes CPU 103 to stop execution at the end of the current instruction, and turn off internal distribution of the CPU's clock, to most, if not all sections of processor core logic. The CPU executes a "Stop Grant" bus cycle to indicate that the CPU has entered the Stop Grant state.

In addition to stopping distribution internally, clocks to the CPU and other components may be stopped using the "clock stop" signal 112 provided by south bridge 105 to clock generator 107. One typical sequence to stop the clocks is to assert the STPCLK# signal 110 to enter the Stop Grant state, wait for the Stop Grant bus cycle and then turn off the clock generator 107 distribution of clocks using the clock stop signal 112 to enter the Stop Clock state.

Assume that the clocks to the processor are stopped as described above. The particular mechanism to stop clocks may vary in different embodiments and is not critical to the present invention. The clocks may be stopped in association with throttling or because of the processor entering a sleep mode or any other scenario in which clocks are stopped and power is left on. After the clocks are stopped, the south bridge 105 (or any other suitable logic device) supplies new voltage control signals to the CPU core voltage regulator 101 instructing the voltage regulator to supply a reduced voltage to the CPU core. Depending on the sleep mode, it

may still be important that the voltages supplied to other areas of the CPU, such as the I/O circuits are maintained at suitable levels since such circuits may be interfacing with I/O devices, external circuits or buses that may be active when the processor has its core logic clocks stopped.

Because sleep and throttle (and suspend) states require the processor operation to be stopped, it is impossible for system software to control all sleep, and recover operations. To overcome this problem, control logic is typically implemented external to the processor. For example, such control logic may be implemented in the input/output integrated circuit (referred to herein as south bridge 105) to control the final stages of sleep and suspend operations and the resume operation and other common power management features. One such integrated circuit is the Intel Corp. 82371AB PCI-TO-ISA/IDE XCELERATOR (PIIX4). The power management features contained therein reduce power consumption to extend battery life and control heat generation and dissipation to safely operate the processor. While some computer systems use a separate microcontroller for the task, most computer systems, including most notebook computers rely on the south bridge to provide the hardware needed for controlling thermal and power management. South bridge chips from various manufacturers have typically utilized the registers, timers and state machine definitions used in the Intel PIIX4 South Bridge. PIIX4 compatibility in current south bridge chips can be extended to support managing the core voltage during sleep states as described herein.

The control logic to reduce the core voltage after the clocks are turned off may be implemented as a state machine in south bridge 105. It may be particularly advantageous to augment or modify existing power management control logic in the south bridge to provide the enhanced functionality described herein. Once the voltage to the core has been reduced, the control logic waits for a system event that causes the CPU to resume processing. In the meantime the processor is in a quiescent state with the current consumption lower than it otherwise would have been. The system event causing the processor to wake-up, such as mouse movement or depressing a keyboard key, causes the CPU to resume normal operations. The control logic ensures that the core voltage is returned back to an operational level sufficient to support the desired clock frequency prior to the clocks being turned on. Otherwise, unpredictable results may be caused by clocking circuits when the power supply voltage is too low. Thus, the control logic issues new voltage control settings to voltage regulator 101 corresponding to a desired frequency and then the clocks are turned back on by, e.g., enabling clocks at clock generator 107, if necessary, and deasserting STPCLK#.

For a particular processor, the minimum operating core voltage ($V_{coremin}$), which specifies the minimum operating voltage required and the minimum static core voltage ($V_{coremins}$), which specifies the voltage necessary to maintain context with clocks stopped, can be specified over the entire product line. In one embodiment, the voltage control signal (VID) settings corresponding to $V_{coremin}$ and $V_{coremins}$ may be built into BIOS tables. When the system management software determines that the system needs to be put into a mode where clocks are stopped (e.g., a sleep mode or a throttle clock state), the core voltage is reduced to $V_{coremins}$ after the clock has been stopped. Note that if clocks are stopped externally, it may also be possible to reduce the voltage being supplied to I/O regions of the processor under some circumstances. When the system needs to be restored to operating conditions, the system automatically increases the core voltage to the setting needed

for the CPU operation at the desired frequency using the VID settings in the BIOS tables. The control settings may of course be located in any suitable location in the computer system.

Power savings will vary according to the leakage current present in the particular integrated circuit. For example, a processor consuming hundreds milliwatts of power while clocks are stopped in the Stop Grant state (on chip clock multiplier logic is still active) might reduce leakage current by lowering the power supply voltage enough to reduce power consumption by approximately 10%.

The voltage regulator's control pins should be configured for appropriate default operation upon power-up. Accordingly, as shown in Fig. 1, south bridge 105 in one embodiment, has jumper inputs IV[4:0]. The settings of the jumpers 111 (open or short), along with resistors 113, determine the default values for the VID signals. The IBF[2:0] inputs are for frequency control and a description of their use is not critical to understand the present invention. In addition to default modes, the south bridge 105 (or other suitable circuit) supplies the voltage regulator 101 with appropriate voltage control settings during operational modes and during sleep modes in which processor context is maintained.

Referring to Fig. 2, a high level block diagram shows one approach an integrated circuit (such as the south bridge in current x86 based computer systems) may use to provide appropriate voltage control settings for voltage regulator 101 (Fig. 1). In the embodiment illustrated in Fig. 2, multiplexer 201 receives three voltage controls settings as inputs. The first voltage control setting is from VID jumper settings 111, which as previously described, provide for default voltage settings on power-up. Multiplexer 201 also receives inputs from VID stop clock register 202, which provides the voltage control setting for the reduced processor voltage during stop clock modes ($V_{coremin}$). Multiplexer 201 receives inputs from VID operational register 203, which provides VID values for operational modes of the processor, i.e., when core clocks are running. Multiplexer 201 selects between the various voltage control settings according to a select line 204 supplied by control logic 210. Control logic 210 receives reset signal 207 and selects the jumper settings as the appropriate voltage control settings when reset (power on or other hard or soft reset) is asserted. Control logic 210 also receives a stop clock signal 208 which indicates that the processor has or is about to enter a stop clock state with core power maintained. In addition, control logic 210 receives indication 209 that a wakeup event has occurred, i.e., that the processor is going to resume normal operation.

The control logic also supplies load signal 211 to output register 205. During regular operational modes in which clocks are running, multiplexer 201 selects the operational VID register 203. Note that register 203 may be programmable to provide various VID signals during various operational modes. When the processor is in a sleep or throttle mode in which clocks are stopped, the control logic selects the VID stop clock register settings as the source for the voltage control signals VID. Thus, after the clocks are stopped (or simultaneously therewith), the select line selects the VID values from the stop clock VID register 202. The control logic then waits for a wake-up event to occur. When the wake-up event occurs as indicated by wake up signal 209 and before the clocks are started, the control logic causes the operational voltage control signals corresponding to the desired frequency of operation to be loaded into output register 205 from VID operational register 203. The clocks may then be enabled.

A variety of other circuit implementations would be readily apparent to one of skill in the art to accomplish the function of the circuit illustrated in Fig. 2. For example, the multiplexer may only select between jumper settings and a VID register with the VID register being appropriately updated before values in the register are supplied to the voltage regulator 100. That is, south bridge 105 can utilize a programmable register that can be written to update the VID pins with the appropriate voltage control settings available from, e.g., the BIOS tables rather than have separate operational and stop clock registers.

Referring to Fig. 3, a flow chart illustrates the operation of a system incorporating one embodiment for controlling core voltage to effectuate greater power savings according to the present invention. Assume that the clocks are stopped in 301. The clocks may be stopped using the STPCLK# signal 110 or using clock stop signal 112 to turn off the clock signal 106 being supplied to the processor clock multiplier logic, or both, or in any other manner appropriate for the particular implementation. After the clocks are stopped, the system reduces the core voltage being supplied to processor core logic in 303. That is accomplished, e.g., by selecting the appropriate voltage control settings and supplying those settings to the CPU core voltage regulator. Once the processor is maintaining its context with the reduced core voltage, and thereby realizing greater power savings, the control logic waits for a wake-up event in 305. Once the wake-up event occurs, the core logic voltage is changed to a level corresponding to the desired frequency of operation in 307 and then, after the processor is receiving the higher voltage, the clocks are turned on and the processor resumes normal operation.

The description of the invention set forth herein is illustrative, and is not intended to limit the scope of the invention as set forth in the following claims. For instance, while this invention has been described with relation generally to x86 based computer systems and is particularly relevant to notebook computers (which may also be referred to as laptops, portable or mobile computers), the teachings herein may also be utilized in any computing device such as personal digital assistants (PDAs), as well as systems containing any variety of processor in which it is desirable to save power by reducing voltage while clocks are stopped in a power savings mode and still maintain context. Further, while the description herein has focused on reducing core voltages in processors or CPUs, the power savings is equally applicable to any integrated circuit in which clocks are stopped to save power while context is maintained. Other variations and modifications of the embodiments disclosed herein, may be made based on the description set forth herein, without departing from the scope and spirit of the invention as set forth in the following claims

WHAT IS CLAIMED IS:

1. A method comprising:
supplying a first voltage to at least a first circuit portion of an integrated circuit during an operational mode;
stopping clocks which are being supplied to the first circuit portion to place the integrated circuit in a reduced power consumption state; and
then supplying a second voltage, less than the first voltage, to the first circuit portion while the clocks are stopped, the second voltage being at a voltage level sufficient to maintain context of the first circuit portion in existence at a time when the clocks were stopped.

2. The method as recited in claim 1 wherein the integrated circuit is a microprocessor including core logic, the first circuit portion being the core logic.

3. The method as recited in claim 1 further comprising:
supplying a third voltage to the integrated circuit after supplying the integrated circuit with the second voltage, the third voltage being greater than the second voltage; and
then starting the clocks being supplied to the first circuit portion to resume integrated circuit operations.

4. The method as recited in claim 3 wherein the first and third voltages are equal.

5. The method as recited in claim 3 wherein the third voltage is supplied in response to a wake-up event.

6. A computing device comprising:
an integrated circuit including a circuit region holding, at least in substantial part, context indicative of a current operational state of the integrated circuit;
a power supply circuit responsive to control inputs to supply variable voltages to the integrated circuit;
a control circuit coupled to the control inputs of the power supply circuit, wherein the control circuit supplies the control inputs with first voltage control information, indicating an operational voltage, while clocks are being supplied to the circuit region and the control circuit supplies the control inputs with second voltage control information indicating a second voltage, while the clocks are stopped, the second voltage being lower than the operational voltage.

7. The computing device as recited in claim 6 wherein the operational voltage is at a voltage level required to clock the circuit region at a predetermined frequency and the second voltage is below the voltage level required to clock the circuit region at the predetermined frequency.

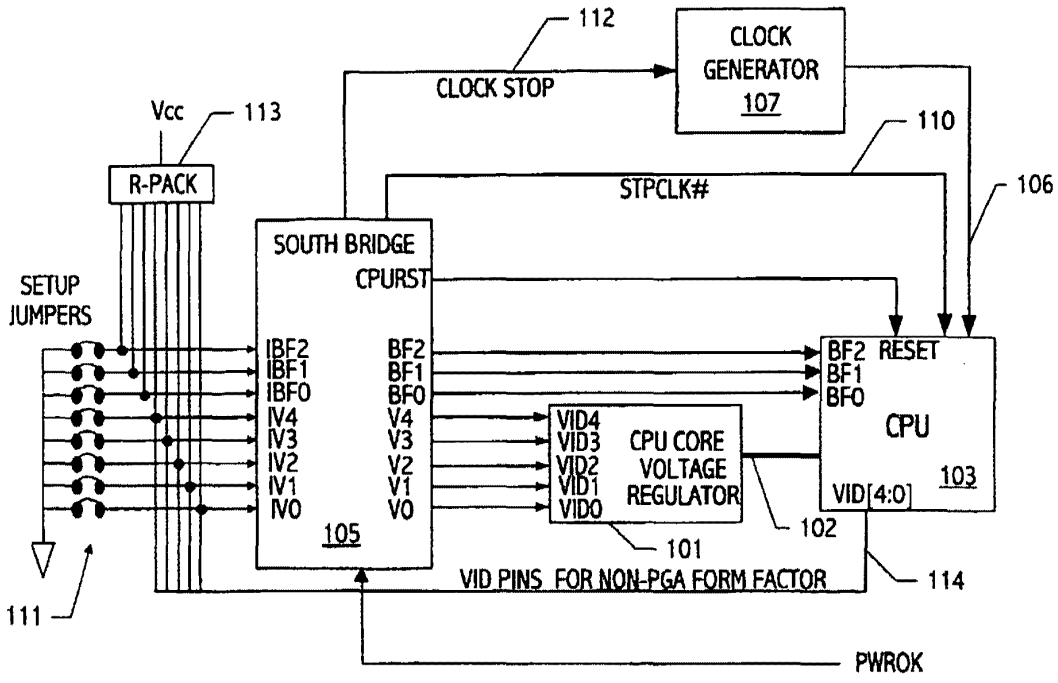
8. An integrated circuit comprising:

a logic circuit responsive to an indication of normal clock operation in which internal clocks are running, to selectably provide first voltage control information indicative of a first voltage level and responsive to an indication of a stop clock state in which internal clocks are stopped to provide second voltage control information indicative of a second voltage level, the second voltage level being lower than the first voltage level; and

an output circuit coupled to receive the selectably provided first and second voltage control information, the first and second voltage control information for coupling to control inputs of a voltage generator.

9. The integrated circuit as recited in claim 8 wherein the logic circuit includes a selector circuit coupled to selectably provide to the output circuit the first or second voltage control information as the control inputs of the voltage generator and further includes at least a first programmable register coupled to the selector circuit and holding at least one of the first voltage control information and the second voltage control information.

10. The integrated circuit as recited in claim 9 further comprising control logic coupled to receive an indication of a wake-up event, an indication of a reset and an indication of the clock stop state, and generating a select signal for the selector circuit in response thereto.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CLOCK GENERATOR
107
CLOCK STOP
Vcc
113
110
R-PACK
STPCLK#
106
SOUTH BRIDGE
CPURST
SETUP JUMPERS
IBF2
IBF1
IBF0
IV4
IV3
IV2
IV1
IV0
105
BF2
BF1
BF0
V4
V3
V2
V1
V0
VID4
VID3
VID2
VID1
VID0
CPU CORE VOLTAGE REGULATOR
101
BF2 RESET
BF1
BF0
CPU
103
VID[4:0]
102
114
VID PINS FOR NON-PGA FORM FACTOR
111
PWROK

FIG. 1

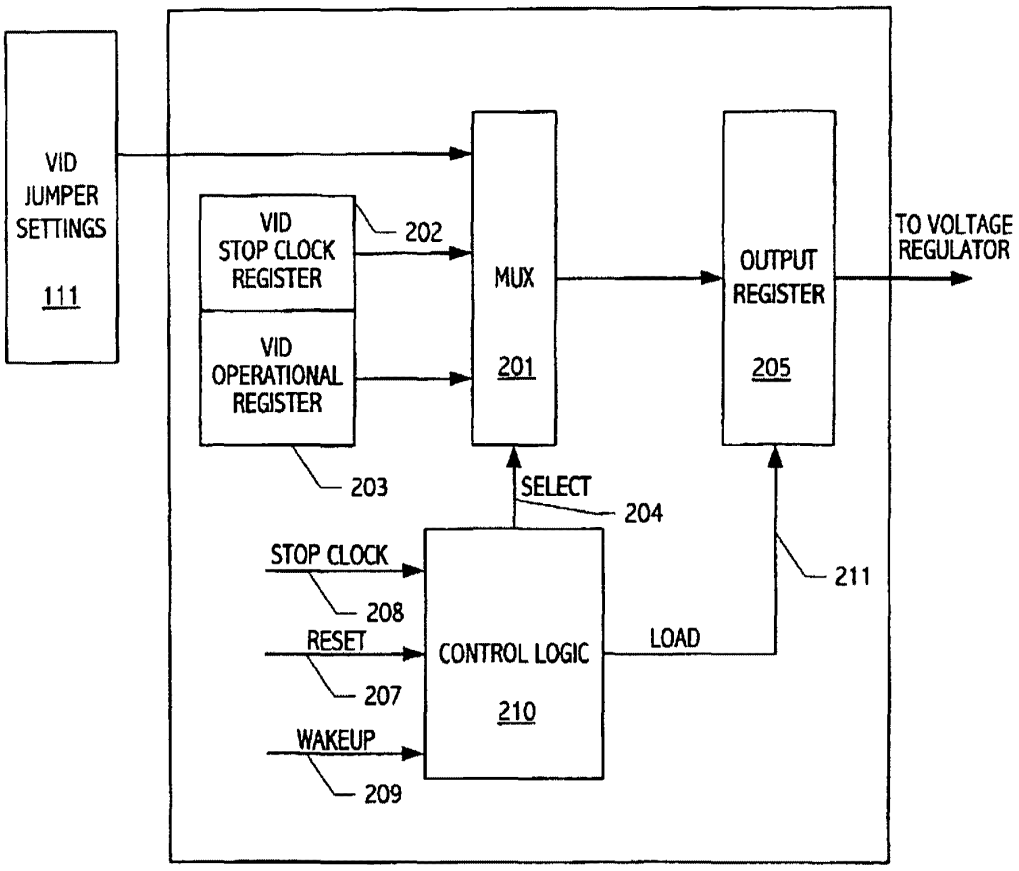

VID JUMPER SETTINGS 111
VID STOP CLOCK REGISTER
202
VID OPERATIONAL REGISTER
203
MUX 201
SELECT
204
OUTPUT REGISTER 205
TO VOLTAGE REGULATOR
211
STOP CLOCK
208
RESET
207
WAKEUP
209
CONTROL LOGIC 210
LOAD

FIG. 2

3/3

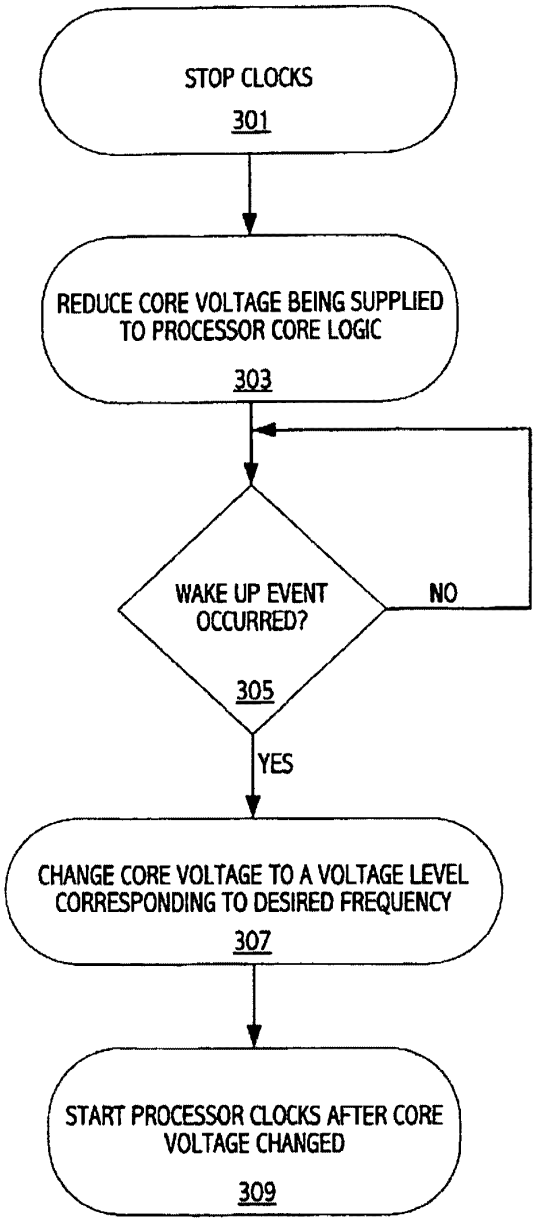

STOP CLOCKS
301
REDUCE CORE VOLTAGE BEING SUPPLIED TO PROCESSOR CORE LOGIC
303
WAKE UP EVENT OCCURRED?
305
NO
YES
CHANGE CORE VOLTAGE TO A VOLTAGE LEVEL CORRESPONDING TO DESIRED FREQUENCY
307
START PROCESSOR CLOCKS AFTER CORE VOLTAGE CHANGED
309

FIG. 3

INTERNATIONAL SEARCH REPORT

Inte onal Application No
PCT/US 00/11062

A. CLASSIFICATION OF SUBJECT MATTER
IPC 7 G06F1/32

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
IPC 7 G06F

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)
EPO-Internal, WPI Data, PAJ, IBM-TDB

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category *	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 5 745 375 A (GUNTHER STEPHEN H ET AL) 28 April 1998 (1998-04-28) column 1, paragraph 3 column 5, paragraph 2 figure 5	1-10
X	EP 0 632 360 A (XEROX CORP) 4 January 1995 (1995-01-04) column 4, paragraph 2 column 7, paragraph 3 figures 1-3	1-10
X	US 5 852 737 A (BIKOWSKY ZEEV) 22 December 1998 (1998-12-22) column 3, line 20 - line 38 column 7, paragraph 2; figures 2,3,6	1-10

☐ Further documents are listed in the continuation of box C.

☒ Patent family members are listed in annex.

* Special categories of cited documents :

"A" document defining the general state of the art which is not considered to be of particular relevance

"E" earlier document but published on or after the international filing date

"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)

"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art.

"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
14 September 2000	22/09/2000

Name and mailing address of the ISA	Authorized officer
European Patent Office, P.B. 5818 Patentlaan 2 NL - 2280 HV Rijswijk Tel. (+31-70) 340-2040, Tx. 31 651 epo nl, Fax: (+31-70) 340-3016	Ciarelli, N

Form PCT/ISA/210 (second sheet) (July 1992)

INTERNATIONAL SEARCH REPORT

Information on patent family members

International Application No
PCT/US 00/11062

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
US 5745375 A	28-04-1998	AU 7247296 A	17-04-1997
		EP 0858634 A	19-08-1998
		WO 9712329 A	03-04-1997
		US 5825674 A	20-10-1998
EP 0632360 A	04-01-1995	JP 7020968 A	24-01-1995
US 5852737 A	22-12-1998	NONE	

Form PCT/ISA/210 (patent family annex) (July 1992)

#12 DA CK (5)

PATENTS
TRAN-P059

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

PATENT

Title : STATIC POWER CONTROL

Patentee : READ et al

Patent No. :

Issued :

On
Application No. : 09/694,433 Confirmation No. :

Filed : 10/23/2000

For : Transmeta Corporation

Group Art Unit :

Examiner :

Hon. Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

NOTIFICATION AND PAYMENT OF FEE DEFICIENCY
PURSUANT TO 37 C.F.R. § 1.28(c)

Sir:

A small entity assertion was made in this case. This assertion of small entity status and any payment of fee(s) as a small entity were made in good faith. It has now been discovered that such status may have been established in error. There was no attempt to fraudulently establish status as a small entity or pay fees as a small entity. Moreover, there was no intent to deceive in establishing status as a small entity or paying fees as a small entity. The Office is hereby notified that status as a small entity is no longer claimed.

03/31/2004 AWONDAF1 00000038 501497 09694433

01 FC:1001 770.00 OP
02 FC:1051 65.00 DA 65.00 OP

Patentee herewith submits $480.00 in payment of a deficiency between fees paid in connection with the above-identified patent application as a small entity, and the fees that were due for other than a small entity. The amount of this deficiency is calculated as follows:

Fee Type	Date Paid as Small Entity	Current Fee (Other than small entity)	Fee Paid (Small entity)	Deficiency Owed
Basic filing fee-Utility	10/23/2000	$770.00	$355.00	$415.00
Surcharge - Late filing fee or oath or declaration	2/2/2001	$130.00	$65.00	$65.00
TOTAL				$480.00

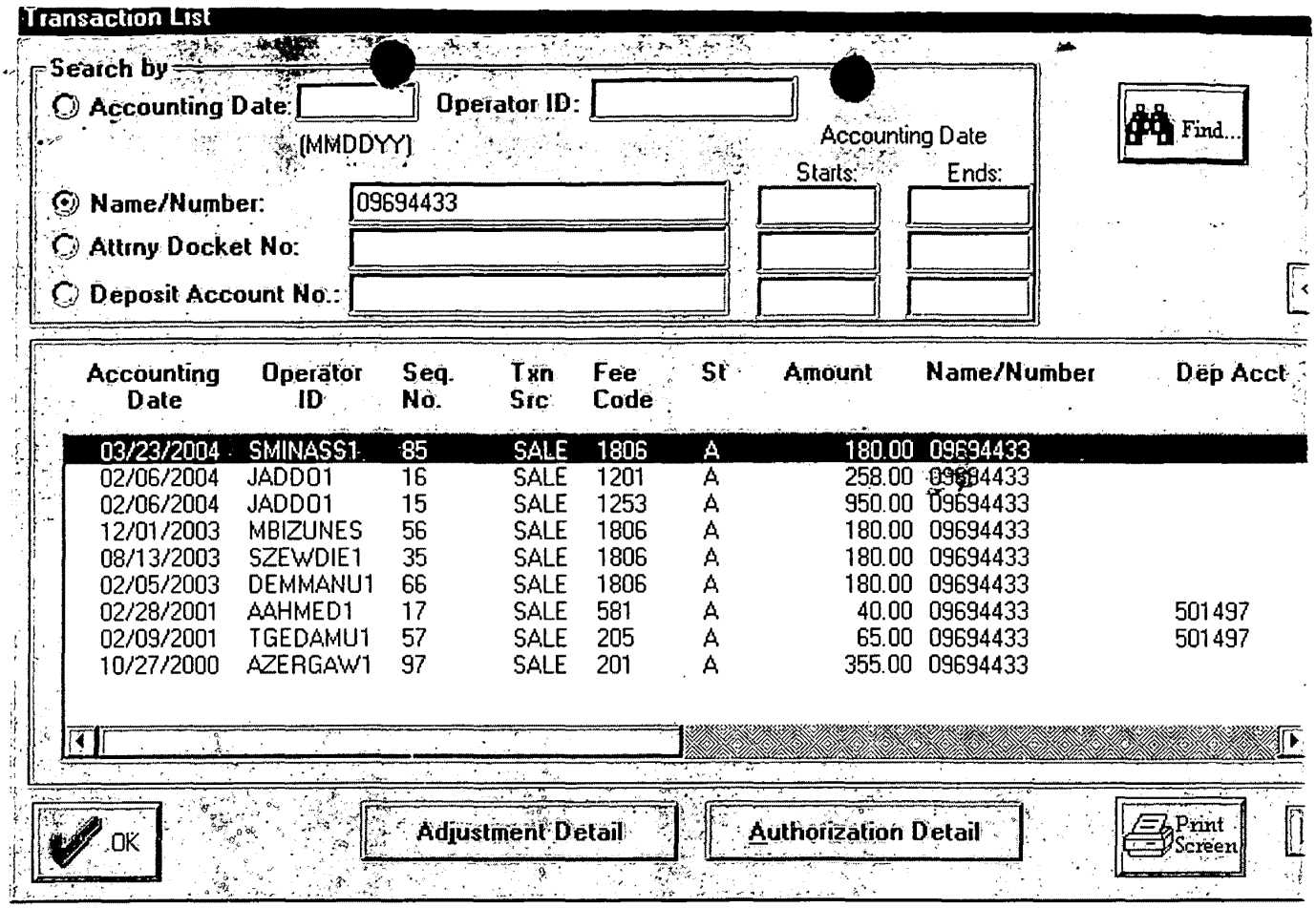
A check in the amount of $480.00 is enclosed in payment of this deficiency. In the event that the enclosed deficiency amount has been miscalculated, the Director is hereby authorized to charge any additional fee that may be due, or to credit any overpayment, in connection with this paper, to Deposit Account No. 23-0085. A duplicate copy of this paper is enclosed herewith.

Date

March 26, 2004

Respectfully submitted,

Anthony C. Murabito
Reg. No. 35,295
Wagner Murabito & Hao
Two North Market Street
Third Floor
San Jose, CA 95113



Adjustment date: 03/31/2004 AHONDAF1
10/27/2000 AZERGAW1 00000054 09694433
01 FC:201 -355.00 DP

Adjustment date: 03/31/2004 AHONDAF1
02/09/2001 TGEDAMU1 00000032 501497 09694433
01 FC:205 65.00 CR

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Paper No. 13

WAGNER MURABITO & HAO
TWO NORTH MARKET STREET
THIRD FLOOR
SAN JOSE, CA 95113

In re Application of	:	
Andrew Read et al	:	
Application No. 09/694,433	:	NOTICE
Filed: October 23, 2000	:	
Attorney Docket No. TRANS59	:	

This is a notice regarding your request for acceptance of a fee deficiency submission under 37 CFR 1.28. On September 1, 1998, the Court of Appeals for the Federal Circuit held that 37 CFR 1.28(c) is the sole provision governing the time for correction of the erroneous payment of the issue fee as a small entity. **See DH Technology v. Synergystex International, Inc. 154 F.3d 1333, 47 USPQ2d 1865 (Fed. Cir. Sept. 1, 1998).**

The Office no longer investigates or rejects original or reissue applications under 37 CFR 1.56. **1098 Off. Gaz. Pat. Office 502 (January 3, 1989).** Therefore, nothing in this Notice is intended to imply that an investigation was done.

Your fee deficiency submission under 37 CFR 1.28 is hereby **ACCEPTED.**

Inquiries related to this communication should be directed to the Office of Petitions Staff at (703) 305-9285.

This file is being forwarded to Technology Center AU 2115.

Wan Laymon
Petitions Examiner
Office of Petitions
Office of the Deputy Commissioner
for Patent Examination Policy

L Number	Hits	Search Text	DB	Time stamp
1	7	"6088807"	USPAT	2004/04/13 08:10
2	0	"20020138778"	USPAT	2004/04/13 08:10
3	1	"20020138778"	US-PGPUB	2004/04/13 08:59
5	0	((core near1 voltage).ti.) and qureshi	US-PGPUB; DERWENT	2004/04/13 09:03
6	0	((core near1 voltage).ti.) and amd.as.	US-PGPUB; DERWENT	2004/04/13 09:05
4	70	(core near1 voltage).ti.	US-PGPUB; DERWENT	2004/04/13 09:06
7	0	qureshi.in. and amd.as.	USPAT	2004/04/13 09:05
8	21	qureshi.in. and advanced.as.	USPAT	2004/04/13 09:03
9	21	qureshi.in. and advanced.as.	USPAT	2004/04/13 10:05
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14	0	qureshi.in. and ((core near1 voltage).ti.)	DERWENT	2004/04/13 09:07
15	7	"5919262"	USPAT	2004/04/13 10:05
16	9	("4419619" | "4509128" | "5294879" | "5429959" | "5481732" | "5550460" | "5552696" | "5596263" | "5774734").PN.	USPAT	2004/04/13 10:06

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/694,433	10/23/2000	Andrew Read	TRANS59	3072

7590 04/19/2004

WAGNER, MURABITO & HAO LLP
TWO NORTH MARKET STREET
THIRD FLOOR
SAN JOSE, CA 95113

EXAMINER	
CAO, CHUN	
ART UNIT	**PAPER NUMBER**
2115	

DATE MAILED: 04/19/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

PTO-90C (Rev. 10/03)

PRG

Office Action Summary	Application No.	Applicant(s)	
	09/694,433	READ ET AL.	
	Examiner	Art Unit	
	Chun Cao	2115	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE ____ MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *29 January 2004*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-13* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _ is/are allowed.

6)☒ Claim(s) *1-11,13* is/are rejected.

7)☒ Claim(s) *12* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *8,9,11*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

FINAL REJECTION

1. Claims 1-13 are presented for examination.

2. The text of those applicable section of Title 35, U.S. Code not included in this action can be found in the prior Office Action.

Claim Rejections - 35 USC § 112

3. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

Claims 1-3 rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the enablement requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention. Applicant fails to adequately teach how to make and/or use the invention, i.e. failing to provide and enabling disclosure. Applicant fails to disclose the detail of "said value of the core voltage is not sufficient to maintain processing activity in said processor". The examiner submits that it would require undue experimentation for one of ordinary skill in the art to make and use the invention for the reason set forth hereinabove. Applicant are reminded that no new matter is allowed in amendment to the specification under 35 U.S.C. 132 and 37 CFR 1.118(a).

Claims 2 and 3 are rejected because they incorporate the deficiencies of claim 1.

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 1-3 are rejected under 35 U.S.C. 103(a) as being unpatentable over Orton et al. (Orton), US patent no. 6,118,306, in view of Horden et al. (Horden), US patent no. 5,812,860.

Orton is a prior art reference cited by applicant in IDS paper no. 6.

Horden is a prior art reference cited by applicant in IDS paper no. 9.

As per claim 1, Orton teaches that a method for reducing power utilized by a processor comprising the steps of:

determining that a processor is transitioning from a computing mode to a mode in which system clock to the processor is disabled [col. 2, lines 44-60]; and

reducing core voltage to the processor to a value sufficient to maintain state during the mode of which system clock is disable [col. 3, lines 10-20].

Orton does not explicitly teach that the value of the core voltage is not sufficient to maintain processing activity in said processor.

Horden teaches that a voltage regulator provides an idle voltage to the processor according to the clock frequency [col. 3, lines 28-34, 40-60; col. 6, lines 27-34]. Inherently, Horden teaches that the value of the core voltage is not sufficient to maintain processing activity in said processor [the processor is idle].

It would have been obvious to one of ordinary skill in the art at time the invention to combine the teachings of Orton and Horden because they are both directed to the problem of reducing the power consumption of a processor core, and the specify teachings of Horden stated above would have allowed for improving power consumption by further reducing the core voltage to a minimum supported voltage.

As per claim 2, Orton teaches of determining the processor is transitioning from a computing mode to a mode in which system clock to the processor is disabled comprises monitoring a stop clock signal [col. 2, lines 44-60; col. 5, lines 4-11; col. 7, lines 38-43].

As per claim 3, Orton teaches of reducing an output voltage providing by a voltage regulator furnishing core voltage to the processor and providing a feedback signal to the voltage regulator to reduce its output voltage below a specified output voltage [col. 2, lines 24-27; col. 3, lines 10-19; col. 7, lines 14-19, 44-58].

6. Claims 4-11 and 13 are rejected under 35 U.S.C. 102 (a) or 102(e) as being anticipated by Orton et al. (Orton), US patent no. 6,118,306.

7. As per claim 4, Orton teaches that a method for reducing power utilized by a processor comprising the steps of:

determining that a processor is transitioning from a computing mode to a mode is which system clock to the processor is disabled [col. 2, lines 44-60];

reducing core voltage to the processor to a value sufficient to maintain state during the mode of which system clock is disable; [col. 3, lines 10-20] by:

furnishing an input to reduce an output voltage provided by a voltage regulator furnishing core voltage to the processor and providing a feedback signal to the voltage regulator to reduce its output voltage below a specified output voltage [col. 2, lines 24-27; col. 3, lines 10-19; col. 7, lines 14-19, 44-58].

8. As per claim 5, Orton teaches a method for reducing power utilized by a processor comprising the steps of:

determining that a processor is transitioning from a computing mode to a mode is which system clock to the processor is disabled [col. 2, lines 44-60];

reducing core voltage to the processor to a value sufficient to maintain state during the mode of which system clock is disable; [col. 3, lines 10-20]; and

transferring operation of a voltage regulator furnishing core voltage in a mode in which power is dissipated during reductions in core voltage to a mode in which power is saved during a voltage transition when it is determined at a processor is transitioning from a computing mode to a mode is which system clock to the processor is disabled [col. 2, lines 11-27, 44-65].

As per claim 6, Orton teaches of returning the voltage regulator to its original mode of operation [col. 3, lines 10-14; col. 7, lines 51-58; col. 8, lines 54-65].

9. As per claim 7, Orton discloses a circuit [fig. 5] for providing a regulated voltage to a processor comprising:

a voltage regulator [52, fig. 1, fig. 5] having: an output terminal [col. 7, lines 50-51; " the output from the voltage regulator 52", inherently, there is an output terminal in the voltage regulator 52] providing a selectable voltage [col. 3, lines 10-12; col. 7, lines

28-31, 46-47, "...adjust the voltage level supplied by the voltage regulator 52 up or down" and "to indicate that the voltage level from the voltage regulator 52 is changing"];

input terminal [fig. 5; col. 7, lines 52-55; "the voltage interface provided the control logic portion 400 allows the voltage regulator 52 to change settings" , inherently, there is an input terminal in the voltage regulator 52] for receiving signals indicating the selectable voltage level;

means for providing signal at the input terminal of the voltage regulator for selecting a voltage for operating the processor in a computing mode and a voltage of a level less than that for operating the processor in computing mode [col. 7, lines 50-65], wherein the level less than that for operating the processor in a computing mode is sufficient to maintain state of the processor [col. 2, lines 44-65; col. 3, lines 10-20].

As per claim 8, Orton discloses that the voltage regulator comprises means for accepting binary signals [LO/HI signals] indicating different voltage level [fig. 5; col. 7, lines 20-37, 63-65; "A signal **VR_LO/HI#**...adjust the voltage level supplied by the voltage regulator 52 up or down"].

As per claim 9, Orton discloses that the voltage regulator comprises:

Selection circuitry, means for furnishing a plurality of signals at the input to the selection circuitry and means for controlling the selection by the selection circuitry [fig. 3A] [col. 5, lines 38-55].

As per claim 10, Orton discloses a multiplexor [col. 5, lines 44-45; fig. 3A] and means for controlling the selection by the selection circuitry including a control terminal

for receiving signals indicating a system clock to the processor is being terminated [col. 5, lines 38-65].

10. As per claim 11, Orton discloses a circuit [fig. 5] for providing a regulated voltage to a processor comprising:

a voltage regulator [52, fig. 1, fig. 5] having: an output terminal [col. 7, lines 50-51; " the output from the voltage regulator 52", inherently, there is an output terminal in the voltage regulator 52] providing a selectable voltage [col. 3, lines 10-12; col. 7, lines 28-31, 46-47, "...adjust the voltage level supplied by the voltage regulator 52 up or down" and "to indicate that the voltage level from the voltage regulator 52 is changing"];

input terminal [fig. 5; col. 7, lines 52-55; "the voltage interface provided the control logic portion 400 allows the voltage regulator 52 to change settings" , inherently, there is an input terminal in the voltage regulator 52] for receiving signals indicating the selectable voltage level;

means for providing signal at the input terminal of the voltage regulator for selecting a voltage for operating the processor in a computing mode and a voltage of a level less than that for operating the processor in computing mode [col. 7, lines 50-65],

means for reducing the selectable voltage below a level provided by the voltage regulator [col. 7, lines 50-65].

11. As per claim 13, Orton discloses a circuit [fig. 5] for providing a regulated voltage to a processor comprising:

a voltage regulator [52, fig. 1, fig. 5] having: an output terminal [col. 7, lines 50-51; " the output from the voltage regulator 52", inherently, there is an output terminal in

the voltage regulator 52] providing a selectable voltage [col. 3, lines 10-12; col. 7, lines 28-31, 46-47, "...adjust the voltage level supplied by the voltage regulator 52 up or down" and "to indicate that the voltage level from the voltage regulator 52 is changing"];

input terminal [fig. 5; col. 7, lines 52-55; "the voltage interface provided the control logic portion 400 allows the voltage regulator 52 to change settings" , inherently, there is an input terminal in the voltage regulator 52] for receiving signals indicating the selectable voltage level;

means for providing signal at the input terminal of the voltage regulator for selecting a voltage for operating the processor in a computing mode and a voltage of a level less than that for operating the processor in computing mode [col. 7, lines 50-65],

circuitry for conserving charge [battery 60] stored by the voltage regulator when the selectable voltage decreases; and means for enabling the circuitry for conserving charge stored by the voltage regulator when the selectable voltage decreases [col. 7, lines 28-58].

Allowable Subject Matter

12. Claim 12 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

13. Applicant's argument with respect to claims 1-13 have been considered but is moot in view of the new ground(s) of rejection.

14. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP

§ 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any response to this action should be mailed to:

Commissioner of Patents and Trademarks

Washington, D.C. 20231

Hand-delivered responses should be brought to Crystal Park II, 2121 Crystal Drive, Arlington. VA., Sixth Floor (Receptionist).

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Chun Cao at (703) 308-6106. The examiner can normally be reached on Monday-Friday from 7:30 am - 4:00 pm. If attempts to reach the examiner by phone are unsuccessful, the examiner's supervisor Thomas Lee can be reached at (703) 305-9717. The fax number for this Art Unit is following: Official (703) 872-9306.

Any inquiry of a general nature or relating to the status of this application should be directed to the Group receptionist whose telephone number is (703) 306-5631.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Chun Cao

Apr. 12, 2004

THOMAS LEE
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100

Notice of References Cited	Application/Control No. 09/694,433	Applicant(s)/Patent Under Reexamination READ ET AL.	
	Examiner Chun Cao	Art Unit 2115	Page 1 of 1

U.S. PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Name	Classification
	A	US-5,919,262	07-1999	Kikinis et al.	713/300
	B	US-			
	C	US-			
	D	US-			
	E	US-			
	F	US-			
	G	US-			
	H	US-			
	I	US-			
	J	US-			
	K	US-			
	L	US-			
	M	US-			

FOREIGN PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Country	Name	Classification
	N					
	O					
	P					
	Q					
	R					
	S					
	T					

NON-PATENT DOCUMENTS

*		Include as applicable: Author, Title Date, Publisher, Edition or Volume, Pertinent Pages)
	U	
	V	
	W	
	X	

*A copy of this reference is not being furnished with this Office action. (See MPEP § 707.05(a).)
Dates in MM-YYYY format are publication dates. Classifications may be US or foreign.

HS

Attorney Docket No.: TRAN-P059

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Patent Application

Inventor(s): Andrew Read, Sameer Halapete and Keith Klayman

Group Art Unit:

Filed: 10/23/00

Examiner:

Serial No.: 09/694,433

Title: STATIC POWER CONTROL

Form 1449

U.S. Patent Documents

Examiner Initial	No.	Patent No.	Date	Patentee	Class	Sub-class	Filing Date
C	A	6,574,739	06/03/03	Kung et al.	713	322	04/14/00
	B	6,519,706	02/11/03	Ogoro	713	322	10/05/99
	C	6,513,124	01/28/03	Furuichi et al.	713	322	05/14/99
	D	6,510,400	01/21/03	Moriyama	702	132	03/28/00
	E	6,487,668	11/26/02	Thomas et al.	713	322	02/12/01
	F	6,477,654	11/05/02	Dean et al.	713	300	04/06/99
	G	6,427,211	07/30/02	Watts, Jr.	713	320	12/01/00
	H	6,415,388	07/02/02	Browning et al.	713	322	10/30/98
	I	6,378,081	04/23/02	Hammond	713	501	10/01/98
	J	6,311,287	10/30/01	Dischler et al.	713	601	10/11/94
	K	6,141,762	10/31/00	Nicol et al.	713	300	08/03/98
	L	6,119,241	09/12/00	Michail et al.	713	322	10/30/98
	M	6,047,248	04/04/00	Georgiou et al.	702	132	10/19/98
	N	5,996,084	11/30/99	Watts	713	323	01/17/97
	O	5,996,083	11/30/99	Gupta et al.	713	322	08/11/95
	P	5,974,557	10/26/99	Thomas et al.	713	322	08/18/97
	Q	5,940,786	08/17/99	Steeby	702	132	11/22/96
	R	5,940,785	08/17/99	Georgiou et al.	702	132	04/29/96
	S	5,815,724	09/29/98	Mates	395	750.04	03/29/96
	T	5,754,869	05/19/98	Holzhammer et al.	395	750.01	01/27/97
	U	5,745,375	04/28/98	Reinhardt et al.	364	492	09/29/95
	V	5,719,800	02/17/98	Mittal et al.	364	707	06/30/95
	W	5,692,204	11/25/97	Rawson et al.	395	750	06/19/96
	X	5,502,838	03/26/96	Kikinis	395	550	04/28/94
	Y	5,461,266	10/24/95	Koreeda et al.	307	125	11/27/91
C	Z	5,422,806	06/06/95	Chen et al.	364	149	03/15/94

US. Published Patent Applications

Examiner Initial	No.	Pub. No.	Filing Date	Applicant	Class	Sub-class	Publication Date
C	AA	2003/0074591	10/17/01	McClendon et al.	713	322	04/17/03
C	BB	2003/0065960	09/28/01	Rusu et al.	713	300	04/17/03
C	CC	2002/0083356	11/26/01	Dai	713	322	06/27/02
C	DD	2002/0073348	12/06/01	Tani	713	300	06/13/02

Foreign Patent or Published Foreign Patent Application

Examiner Initial	No.	Document No.	Publication Date	Country or Patent Office	Class	Sub-class	Translation Yes	Translation No

Other Documents

Examiner Initial	No.	Author, Title, Date, Place (e.g. Journal) of Publication

Examiner	CAO	Date Considered	4/12/04

Examiner: Initial citation considered. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

#11

Attorney Docket No.: TRAN-P059

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Patent Application

Inventor(s): Andrew Read, Sameer Halapete and Keith Klayman

Group Art Unit:

Filed: 10/23/00

Examiner:

Serial No.: 09/694,433

Title: STATIC POWER CONTROL

Form 1449

U.S. Patent Documents

Examiner Initial	No.	Patent No.	Date	Patentee	Class	Sub-class	Filing Date
C	A	5,201,059	04/06/93	Nguyen	395	800	11/13/89
	B	5,230,055	07/20/93	Katz et al.	395	750	01/25/91
	C	5,752,011	05/12/98	Thomas et al.	395	556	06/20/94
	D	6,216,235	04/10/01	Thomas et al.	713	501	07/10/99
	E	5,167,024	11/24/92	Smith et al.	395	375	03/05/92
	F	5,218,704	05/08/93	Watts, Jr. et al.	395	750	10/30/89
	G	5,239,652	08/24/93	Seibert et al.	395	750	02/04/91
	H	5,682,093	10/28/97	Kivela	323	273	04/08/96
	I	5,717,319	02/10/98	Jokinen	323	280	06/08/95
	J	5,086,501	02/04/92	DeLuca et al.	395	550	04/17/89
C	K	6,157,092	12/05/00	Hofmann	307	11	03/18/99
C	L	5,222,239	06/22/93	Rosch	395	750	09/30/92
duplicate	~~M~~	~~5,726,901~~	~~03/10/98~~	~~Brown~~	~~364~~	~~483~~	~~01/25/96~~
	~~N~~	~~5,812,860~~	~~09/22/98~~	~~Horden et al.~~	~~395~~	~~750.04~~	~~02/12/96~~
	~~O~~	~~5,940,785~~	~~08/17/99~~	~~Georgiou et al.~~	702	132	04/29/96
C	P	6,510,525	01/21/03	Nookala et al.	713	324	04/26/99
	Q	6,457,135	09/24/02	Cooper	713	323	08/10/99
	R	6,388,432	05/14/02	Uchida	323	266	12/13/00
	S	6,347,379	02/12/02	Dai et al.	713	320	09/25/98
	T	6,345,363	02/05/02	Levy-Kendler	713	320	06/23/98
	U	6,078,319	06/20/00	Bril et al.	345	211	04/17/95
	V	5,511,203	04/23/96	Wisor et al.	395	750	02/02/94
	W	5,914,996	06/22/99	Huang	377	39	02/12/97
	X	5,774,703	06/30/98	Weiss et al.	395	556	01/05/96
	Y	6,112,164	08/29/00	Hobson	702	132	03/31/98
	Z	6,021,500	02/01/00	Wang et al.	713	320	05/07/97
	AA	6,094,367	07/25/00	Hsu et al.	363	78	06/29/99
	BB	5,630,110	05/13/97	Mote, Jr.	395	556	03/01/96
	CC	5,678,114	11/11/97	Khan	365	185.03	10/06/95
	DD	5,713,030	01/27/98	Evoy	395	750	10/11/95
C	EE	5,572,719	11/05/96	Biesterfeldt	395	555	11/22/94

C	FF	5,832,284	11/03/98	Michail et al.	395	750.04	12/23/96
C	GG	5,628,001	05/06/97	Cepuran	395	556	09/18/95
C	HH	5,710,929	01/20/98	Fung	395	750	06/02/95
C	II	5,913,067	06/15/99	Klein	395	750.01	10/31/97
C	JJ	5,701,783	12/30/97	Lin	74	89.13	08/29/95
Duplicate	~~KK~~	~~5,745,375~~	~~04/28/98~~	~~Reinhardt et al.~~	~~364~~	~~492~~	~~09/29/95~~

US. Published Patent Applications

Examiner Initial	No.	Pub. No.	Date	Applicant	Class	Sub-class	Publication Date
C	LL	2002/0026597	02/28/02	Dai et al.	713	322	10/18/01
C	MM	2002/0138778	09/26/02	Cole et al.	713	330	03/22/01

Foreign Patent or Published Foreign Patent Application

Examiner Initial	No.	Document No.	Publication Date	Country or Patent Office	Class	Sub-class	Translation Yes	Translation No
C	NN	EP0474963A2	03/18/92	EPO	G06F	1/32	X	
C	OO	EP0381021A2	08/08/90	EPO	G06F	1/32	X	
C	PP	WO0127728	04/19/01	PCT	G06F	1/32	X	

Other Documents

Examiner Initial	No.	Author, Title, Date, Place (e.g. Journal) of Publication
C	QQ	Weiser et al.; "SCHEDULING FOR REDUCED CPU ENERGY"; Xerox PARC, Palo Alto, CA; Appears in "Proceedings of the First Symposium on operating Systems Design and Implementation; Usenix Assoc. Nov. 1994
C	RR	Govil; "COMPARING ALGORITHMS FOR DYNAMIC SPEEDSETTING OF A LOW POWER CPU"; International Computer Science Institute; Berkeley, CA; April 1995

Examiner	Date Considered
CAO	4/12/04

Examiner: Initial citation considered. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

#9

Attorney Docket No.: TRAN-P059

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Patent Application

Inventor(s): Andrew Read, Sameer Halapete and Keith Klayman

Group Art Unit:

Filed: 10/23/00

Examiner:

Serial No.: 09/694,433

Title: STATIC POWER CONTROL

Form 1449

U.S. Patent Documents

Examiner Initial	No.	Patent No.	Date	Patentee	Class	Sub-class	Filing Date
C	A	5,812,860	09/22/98	Horden et al.	395	750.04	02/12/96
C	B	5,726,901	03/10/98	Brown	364	483	01/25/96
	C						
	D						
	E						
	F						

Foreign Patent or Published Foreign Patent Application

Examiner Initial	No.	Document No.	Publication Date	Country or Patent Office	Class	Sub-class	Translation Yes	Translation No
	G							
	H							
	I							

Other Documents

Examiner Initial	No.	Author, Title, Date, Place (e.g. Journal) of Publication
	J	

Examiner	CAO	Date Considered	4/12/04

Examiner: Initial citation considered. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

#16 Pauz 8-9-04

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Attorney Docket No.: TRAN-P059 (5TH IDS)

Inventor(s): Andrew Read, Sameer Halapete and Keith Klayman

Group Art Unit:

Filed: 10/23/00

Examiner:

Serial No.: 09/694,433

Title: STATIC POWER CONTROL

The Commissioner of Patents and Trademarks
Washington, D.C. 20231
Sir:

Information Disclosure Statement Submitted Pursuant to 37 C.F.R. 1.97(b)

The citations referenced herein, copies attached, may be material to the examination of the above-identified application and are, therefore, submitted in compliance with the duty of disclosure as defined in 37 C.F.R. 1.56. The Examiner is requested to make these citations of official record in the application.

This Information Disclosure Statement submitted in accordance with 37 C.F.R. 1.97(b) is not to be construed as a representation that a search has been made, that additional items material to the examination of this application do not exist, or that any one or more of these citations constitute prior art under 35 U.S.C. 102.

The Examiner's attention is respectfully directed to the following U.S. Patents:

Pat. No.	Pat. Title	Grant Date
5,204,863	DEVICE FOR MONITORING THE OPERATION OF A MICROPROCESSOR SYSTEM, OR THE LIKE	04/20/93
5,778,237	DATA PROCESSOR AND SINGLE-CHIP MICROPROCESSOR WITH CHANGING CLOCK FREQUENCY AND OPERATING VOLTAGE	07/07/98

Please direct all correspondence concerning the above-identified application to the following address:

WAGNER, MURABITO & HAO LLP
Two North Market Street, Third Floor
San Jose, California 95113
(408) 938-9060

Respectfully submitted,

Date: 6/18/2004

By: _____
Anthony C. Murabito
Reg. No. 35,295

06/24/2004 SSESHE1 00000095 09694433
01 FC:1806 180.00 OP

rev. 6/97 jpw

Attorney Docket No.: TRAN-P059 (5TH IDS)

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Patent Application

Inventor(s): Andrew Read, Sameer Halapete and Keith Klayman

Group Art Unit:

Filed: 10/23/00

Examiner:

Serial No.: 09/694,433

Title: STATIC POWER CONTROL

Form 1449

U.S. Patent Documents

Examiner Initial	No.	Patent No.	Date	Patentee	Class	Sub-class	Filing Date
	A	5,778,237	07/07/98	Yamamoto et al.	395	750.04	12/14/95
	B	5,204,863	04/20/93	Saint-Joigny et al.	371	16.3	02/08/91
	C						

Foreign Patent or Published Foreign Patent Application

Examiner Initial	No.	Document No.	Publication Date	Country or Patent Office	Class	Sub-class	Translation Yes	Translation No
	D							
	E							

Other Documents

Examiner Initial	No.	Author, Title, Date, Place (e.g. Journal) of Publication
	F	
	G	

Examiner	Date Considered

Examiner: Initial citation considered. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

AF/2115
61
Patent

Docket No.: TRAN-P059 (5th IDS)

Information Disclosure Statement Transmittal

I hereby certify that this transmittal of the below described document is being deposited with the United States Postal Service in an envelope bearing First Class Postage and addressed to the Commissioner of Patents and Trademarks, Washington, D.C., 20231, on the below date of deposit.					
Date of Deposit:	06/18/04	Name of Person Making the Deposit:	KATHERINE RINALDI	Signature of the Person Making the Deposit:	Katherine Rinaldi

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Inventor(s): Andrew Read, Sameer Halapete and Keith Klayman

Group Art Unit:

Filed: 10/23/00

Examiner:

Serial No.: 09/694,433

Title: STATIC POWER CONTROL

The Commissioner of Patents and Trademarks
Washington, D.C. 20231
Sir:

Information Disclosure Statement Transmittal

Transmitted herewith is the following:

..... Formal drawings, totaling ..... sheets.
..... Informal drawings, totaling ..... sheets.
..... Certification for PTO Consideration
..... Information Disclosure statement (__ sheets)
..X.. Information Disclosure statement and late filing fee
..X.. Form 1449
..... Petition for Extension of Time
..X.. Other: References

Fee Calculation (for other than a small entity)

Fee Items				Fee Rate	Total
Petition for Extension of Time (fee calculated elsewhere				$ .00	$0.00
Information Disclosure Statement, late filing				$180.00	$180.00
Other:					$0.00
Total Fees					$180.00

PAYMENT OF FEES

1. The full fee due in connection with this communication is provided as follows:

[X] The Commissioner is hereby authorized to charge any additional fees associated with this communication or credit any overpayment to Deposit Account No.: 23-0085. A duplicate copy of this authorization is enclosed.

[X] A check in the amount of $180.00

[ ] Charge any fees required or credit any overpayments associated with this filing to Deposit Account No.: 23-0085.

kgr 7/98

Please direct all correspondence concerning the above-identified application to the following address:

WAGNER, MURABITO & HAO LLP
Two North Market Street, Third Floor
San Jose, California 95113
(408) 938-9060

Respectfully submitted,

Date: 6/18/2004

By: _____
Anthony C. Murabito
Reg. No. 35,295

kgr 7/98

L Number	Hits	Search Text	DB	Time stamp
1	0	((deep near1 sleep) or deep-sleep) with "core voltage"	USPAT	2004/07/08 15:34
2	11	((deep near1 sleep) or deep-sleep) and "core voltage"	USPAT	2004/07/08 17:24
3	1	((deep near1 sleep) or deep-sleep) and "core voltage"	EPO; JPO; DERWENT; IBM_TDB	2004/07/08 15:35
4	16	legend.as.	USPAT	2004/07/08 15:47
5	0	qdi.as.	USPAT	2004/07/08 15:47
6	7	"5852737"	USPAT	2004/07/08 17:24

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/694,433	10/23/2000	Andrew Read	TRANS59	3072

7590 07/09/2004

WAGNER, MURABITO & HAO LLP
TWO NORTH MARKET STREET
THIRD FLOOR
SAN JOSE, CA 95113

EXAMINER	
CAO, CHUN	

ART UNIT	PAPER NUMBER
2115	15

DATE MAILED: 07/09/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

PTO-90C (Rev. 10/03)

Interview Summary	Application No. 09/694,433	Applicant(s) READ ET AL.	
	Examiner Chun Cao	Art Unit 2115	

All participants (applicant, applicant's representative, PTO personnel):

(1) *Chun Cao*.

(2) *ANTHONY MURABITO*.

(3)*Ronald Pomerenke*.

(4)*Thomas Lee (SPE)*.

Date of Interview: *07 July 2004*.

Type: a)☒ Telephonic b)☐ Video Conference
c)☐ Personal [copy given to: 1)☐ applicant 2)☐ applicant's representative]

Exhibit shown or demonstration conducted: d)☐ Yes e)☒ No.
If Yes, brief description: _____.

Claim(s) discussed: *1-3*.

Identification of prior art discussed: *US patents 6,118,306 and 5,812,860* .

Agreement with respect to the claims f)☒ was reached. g)☐ was not reached. h)☐ N/A.

Substance of Interview including description of the general nature of what was agreed to if an agreement was reached, or any other comments: *Final rejection was discussed. Examiner agreed to withdraw the 112 rejection for claims 1-3. Applicant argued that both of cited references do not teach of the value of the core voltage is not sufficient to maintain processing activity in said processor. Examiner agreed to further review the cited references in light of today's discussion upon receiving response from applicant*.

(A fuller description, if necessary, and a copy of the amendments which the examiner agreed would render the claims allowable, if available, must be attached. Also, where no copy of the amendments that would render the claims allowable is available, a summary thereof must be attached.)

THE FORMAL WRITTEN REPLY TO THE LAST OFFICE ACTION MUST INCLUDE THE SUBSTANCE OF THE INTERVIEW. (See MPEP Section 713.04). If a reply to the last Office action has already been filed, APPLICANT IS GIVEN ONE MONTH FROM THIS INTERVIEW DATE, OR THE MAILING DATE OF THIS INTERVIEW SUMMARY FORM, WHICHEVER IS LATER, TO FILE A STATEMENT OF THE SUBSTANCE OF THE INTERVIEW. See Summary of Record of Interview requirements on reverse side or on attached sheet.

Examiner Note: You must sign this form unless it is an Attachment to a signed Office action.

Examiner's signature, if required

Summary of Record of Interview Requirements

Manual of Patent Examining Procedure (MPEP), Section 713.04, Substance of Interview Must be Made of Record
A complete written statement as to the substance of any face-to-face, video conference, or telephone interview with regard to an application must be made of record in the application whether or not an agreement with the examiner was reached at the interview.

Title 37 Code of Federal Regulations (CFR) § 1.133 Interviews
Paragraph (b)
In every instance where reconsideration is requested in view of an interview with an examiner, a complete written statement of the reasons presented at the interview as warranting favorable action must be filed by the applicant. An interview does not remove the necessity for reply to Office action as specified in §§ 1.111, 1.135. (35 U.S.C. 132)

37 CFR §1.2 Business to be transacted in writing.
All business with the Patent or Trademark Office should be transacted in writing. The personal attendance of applicants or their attorneys or agents at the Patent and Trademark Office is unnecessary. The action of the Patent and Trademark Office will be based exclusively on the written record in the Office. No attention will be paid to any alleged oral promise, stipulation, or understanding in relation to which there is disagreement or doubt.

The action of the Patent and Trademark Office cannot be based exclusively on the written record in the Office if that record is itself incomplete through the failure to record the substance of interviews.

It is the responsibility of the applicant or the attorney or agent to make the substance of an interview of record in the application file, unless the examiner indicates he or she will do so. It is the examiner's responsibility to see that such a record is made and to correct material inaccuracies which bear directly on the question of patentability.

Examiners must complete an Interview Summary Form for each interview held where a matter of substance has been discussed during the interview by checking the appropriate boxes and filling in the blanks. Discussions regarding only procedural matters, directed solely to restriction requirements for which interview recordation is otherwise provided for in Section 812.01 of the Manual of Patent Examining Procedure, or pointing out typographical errors or unreadable script in Office actions or the like, are excluded from the interview recordation procedures below. Where the substance of an interview is completely recorded in an Examiners Amendment, no separate Interview Summary Record is required.

The Interview Summary Form shall be given an appropriate Paper No., placed in the right hand portion of the file, and listed on the "Contents" section of the file wrapper. In a personal interview, a duplicate of the Form is given to the applicant (or attorney or agent) at the conclusion of the interview. In the case of a telephone or video-conference interview, the copy is mailed to the applicant's correspondence address either with or prior to the next official communication. If additional correspondence from the examiner is not likely before an allowance or if other circumstances dictate, the Form should be mailed promptly after the interview rather than with the next official communication.

The Form provides for recordation of the following information:
- Application Number (Series Code and Serial Number)
- Name of applicant
- Name of examiner
- Date of interview
- Type of interview (telephonic, video-conference, or personal)
- Name of participant(s) (applicant, attorney or agent, examiner, other PTO personnel, etc.)
- An indication whether or not an exhibit was shown or a demonstration conducted
- An identification of the specific prior art discussed
- An indication whether an agreement was reached and if so, a description of the general nature of the agreement (may be by attachment of a copy of amendments or claims agreed as being allowable). Note: Agreement as to allowability is tentative and does not restrict further action by the examiner to the contrary.
- The signature of the examiner who conducted the interview (if Form is not an attachment to a signed Office action)

It is desirable that the examiner orally remind the applicant of his or her obligation to record the substance of the interview of each case. It should be noted, however, that the Interview Summary Form will not normally be considered a complete and proper recordation of the interview unless it includes, or is supplemented by the applicant or the examiner to include, all of the applicable items required below concerning the substance of the interview.

A complete and proper recordation of the substance of any interview should include at least the following applicable items:
1) A brief description of the nature of any exhibit shown or any demonstration conducted,
2) an identification of the claims discussed,
3) an identification of the specific prior art discussed,
4) an identification of the principal proposed amendments of a substantive nature discussed, unless these are already described on the Interview Summary Form completed by the Examiner,
5) a brief identification of the general thrust of the principal arguments presented to the examiner,
   (The identification of arguments need not be lengthy or elaborate. A verbatim or highly detailed description of the arguments is not required. The identification of the arguments is sufficient if the general nature or thrust of the principal arguments made to the examiner can be understood in the context of the application file. Of course, the applicant may desire to emphasize and fully describe those arguments which he or she feels were or might be persuasive to the examiner.)
6) a general indication of any other pertinent matters discussed, and
7) if appropriate, the general results or outcome of the interview unless already described in the Interview Summary Form completed by the examiner.

Examiners are expected to carefully review the applicant's record of the substance of an interview. If the record is not complete and accurate, the examiner will give the applicant an extendable one month time period to correct the record.

Examiner to Check for Accuracy

If the claims are allowable for other reasons of record, the examiner should send a letter setting forth the examiner's version of the statement attributed to him or her. If the record is complete and accurate, the examiner should place the indication, "Interview Record OK" on the paper recording the substance of the interview along with the date and the examiner's initials.

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of)
)
Read et al.) Examiner: Cao, Chun
)
Serial No. 09/694,433) Art Unit: 2185
)
Filing Date: October 23, 2000)
)
For: STATIC POWER CONTROL)
(As Filed))
)

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

AMENDMENT AND RESPONSE TO OFFICE ACTION

Dear Sir:

In response to the Office Action mailed April 19, 2004, the following amendments and responses to the above captioned patent application are respectfully submitted. A Request for Continued Examination (RCE) has been filed herewith.

AMENDMENTS TO THE CLAIMS IN THE CASE

1. (Previously Presented) A method for reducing power utilized by a processor comprising the steps of:

determining that a processor is transitioning from a computing mode to a mode in which system clock to the processor is disabled, and

reducing core voltage to the processor to a value sufficient to maintain state during the mode in which system clock is disabled, wherein said value of the core voltage is not sufficient to maintain processing activity in said processor.

Claim 2. (Previously Presented) A method as claimed in Claim 1 in which the step of determining that a processor is transitioning from a computing mode to a mode in which system clock to the processor is disabled comprises monitoring a stop clock signal.

Claim 3. (Original) A method as claimed in Claim 1 in which the step of reducing core voltage to the processor to a value sufficient to maintain state during the state in which system clock is disabled comprises furnishing an input to reduce an output voltage provided by a voltage regulator furnishing core voltage to the processor.

Claim 4. (Previously Presented) A method for reducing power utilized by a processor comprising the steps of:

determining that a processor is transitioning from a computing mode to a mode in which system clock to the processor is disabled, and

reducing core voltage to the processor to a value sufficient to maintain state during the mode in which system clock is disabled by:

furnishing an input to reduce an output voltage provided by a voltage regulator furnishing core voltage to the processor, and

providing a feedback signal to the voltage regulator to reduce its output voltage below a specified output voltage.

Claim 5. (Previously Presented) A method for reducing power utilized by a processor comprising the steps of:

determining that a processor is transitioning from a computing mode to a mode in which system clock to the processor is disabled,

reducing core voltage to the processor to a value sufficient to maintain state during the mode in which system clock is disabled, and

transferring operation of a voltage regulator furnishing core voltage in a mode in which power is dissipated during reductions in core voltage to a mode in which power is saved during a voltage transition when it is determined that a processor is transitioning from a computing mode to a mode is which system clock to the processor is disabled.

Claim 6. (Previously Presented) A method as claimed in Claim 5 further comprising the steps of returning the voltage regulator to its original mode of operation when the value of the core voltage sufficient to maintain state during the mode in which system clock is disabled is reached.

Claim 7. (Previously Presented) A circuit for providing a regulated voltage to a processor comprising:

a voltage regulator having:

an output terminal providing a selectable voltage, and

an input terminal for receiving signals indicating the selectable voltage level;

means for providing signals at the input terminal of the voltage regulator for selecting a voltage for operating the processor in a computing mode and a voltage of a level less than that for operating the processor in a computing mode, wherein the level less than that for operating the processor in a computing mode is sufficient to maintain state of the processor.

Claim 8. (Original) A circuit as claimed in Claim 7 in which the means for providing signals at the input terminal of the voltage regulator

comprises means for accepting binary signals indicating different levels of voltage.

Claim 9. (Original) A circuit as claimed in Claim 7 in which the means for providing signals at the input terminal of the voltage regulator comprises:

selection circuitry,

means for furnishing a plurality of signals at the input to the selection circuitry, and

means for controlling the selection by the selection circuitry.

Claim 10. (Original) A circuit as claimed in Claim 9 in which:

the selection circuitry is a multiplexor, and

the means for controlling the selection by the selection circuitry includes a control terminal for receiving signals indicating a system clock to the processor is being terminated.

Claim 11. (Previously Presented) A circuit for providing a regulated voltage to a processor comprising:

a voltage regulator having:

an output terminal providing a selectable voltage, and

an input terminal for receiving signals indicating the selectable voltage level;

means for providing signals at the input terminal of the voltage regulator for selecting a voltage for operating the processor in a computing mode and a voltage of a level less than that for operating the processor in a computing mode; and

means for reducing the selectable voltage below a level provided by the voltage regulator.

Claim 12. (Currently Amended) ~~A circuit as claimed in Claim 11 in which the means for reducing the selectable voltage below a level provided by the voltage regulator comprises:~~

A circuit for providing a regulated voltage to a processor comprising:

a voltage regulator having:

an output terminal providing a selectable voltage;

an input terminal for receiving signals indicating the selectable voltage level; and

a voltage regulator feedback circuit;

means for providing signals at the input terminal of the voltage regulator for selecting a voltage for operating the processor in a computing mode and a voltage of a level less than that for operating the processor in a computing mode; and

means for reducing the selectable voltage below a level provided by the voltage regulator comprising:

a voltage divider network joined between the output terminal and a voltage source furnishing a value higher than the selectable voltage, and [[a]]

the voltage regulator feedback circuit receiving a value from the voltage divider network.

Claim 13. (Previously Presented) A circuit for providing a regulated voltage to a processor comprising:

a voltage regulator having:

an output terminal providing a selectable voltage, and

an input terminal for receiving signals indicating the selectable voltage level;

means for providing signals at the input terminal of the voltage regulator for selecting a voltage for operating the processor in a

computing mode and a voltage of a level less than that for operating the processor in a computing mode;

circuitry for conserving charge stored by the voltage regulator when the selectable voltage decreases, and

means for enabling the circuitry for conserving charge stored by the voltage regulator when the selectable voltage decreases.

Claim 14. (New) A circuit for providing a regulated voltage to a processor comprising:

a voltage regulator having:

an output terminal providing a selectable voltage, and

an input terminal for receiving signals indicating the selectable voltage level; and

a voltage regulator feedback circuit;

circuitry coupled to said input terminal and configured to provide signals to the input terminal for selecting a first voltage for operating the processor in a first mode and a second voltage for operating the processor in a second mode;

a voltage source furnishing a value higher than the selectable voltage; and

a feedback circuit coupled to the voltage source, the output terminal, and the voltage regulator feedback circuit.

15. (New) The circuit of Claim 14, wherein the first voltage is for operating the processor in a computing mode and the second voltage is a level less than that for operating the processor in the computing mode.

16. (New) The circuit of Claim 15, wherein the feedback circuit comprises a voltage divider.

17. (New) The circuit of Claim 14, wherein the feedback circuit comprises a voltage divider.

18. (New) The method of Claim 4, wherein the output voltage to which said voltage regulator is reduced depends upon output voltage of said voltage regulator prior to furnishing the input to reduce the output voltage provided by the voltage regulator.

REMARKS

The claims remaining in the present application are Claims 1-18. Claim 12 has been amended. Claims 14-18 have been added. No new matter has been added as a result of these amendments.

EXAMINER INTERVIEW SUMMARY

On July 7, 2004 Ronald Pomerenke, Anthony Murabito, and Bryn Ekroot, representatives for the Applicants conducted a telephonic interview with Examiners Chun Cao and Thomas Lee. Applicants thank the Examiners for granting this interview. United States Patent No. 5,812,860 to Horden et al. and U.S. Patent No. 6,118,306 to Orton were discussed with respect to Claim 1. The rejection under 35 U.S.C. §112, ¶1 enablement with respect to Claims 1-3 was discussed. The Examiners agreed that the rejection under 35 U.S.C. §112, ¶1 enablement with respect to Claims 1-3 would be removed. Applicants thank the Examiners for removing this rejection.

ALLOWABLE SUBJECT MATTER

Claim 12 is objected to but indicated as allowable if re-written to incorporate limitations from its base claim. Applicants have re-written Claim 12 in independent form, including all limitations from Claim 11, its base claim. Therefore, Applicants request allowance of Claim 12.

CLAIM REJECTIONS

35 U.S.C. §112

Claims 1-3 were rejected in the Office Action under 35 U.S.C. §112, ¶1, as failing to comply with the enablement requirement. This rejection has been removed per agreement in the above-referenced Examiner interview.

35 U.S.C. §103

Claims 1-3 are rejected under 35 U.S.C. §102(e) as being unpatentable over Orton et al., U.S. Patent No. 6,118,306 (hereinafter, Orton) in view of Horden et al., U.S. Patent No. 5,812,860 (hereinafter, Horden). The rejection is respectfully traversed for the following reasons.

Currently Amended Independent Claim 1 recites, in part:

> reducing core voltage to the processor to a value sufficient to maintain state during the mode in which system clock is disabled, wherein said value of the core voltage is not sufficient to maintain processing activity in said processor.

Independent Claim 1 recites that the core voltage is reduced to a value that is sufficient to maintain state of the processor, but is not sufficient to maintain processing activity in the processor.

Applicants respectfully assert that Orton fails to teach or suggest reducing the voltage of the processor core to a value that is sufficient to

maintain state of the processor, but is not sufficient to maintain processing activity in the processor, as claimed. Orton may purport to disclose a system that places a processor into a low activity state during which state may be preserved (col. 2, lines 44-60). However, Applicants respectfully assert that Orton does not teach or suggest that the voltage during this low activity state is insufficient to maintain processing activity. Therefore, Applicants assert that Orton fails to teach or suggest the limitations, "reducing core voltage to the processor to a value sufficient to maintain state during the mode in which system clock is disabled, wherein said value of the core voltage is not sufficient to maintain processing activity in said processor."

The cited combination of also fails because Horden fails to remedy the deficiencies in Orton in that Horden fails to teach or suggest the above claimed limitations. Applicants respectfully assert that the term "idle" in Horden's disclosure as understood by one or ordinary skill in the art does not mean that the processing activity is stopped. By idle, Applicants understand Horden to be referring to executing instructions in the processor at a frequency less than peak frequency. However, Horden is nevertheless executing instructions in the processor when applying Horden's so-called idle frequency/voltage pair and thus is maintaining processing activity. For example, Horden teaches that the operating system accumulates all processor need for all applications and directs a state machine to transition to a state that matches the frequency and voltage to the current application

needs. For example, if the current application mix does not require the peak performance level, the lowest state that will meet the application mix is used. (See., e.g., col. 4, lines 50-54; col. 3, lines 40-47).

Moreover, Horden provides an example of peak performance frequency of 32 MHz and an idle core frequency of 16MHz. Horden teaches that the minimum voltage *required to operate the processor at these frequencies* is provided to the processor (Horden, col. 3, lines 35-42). Applicants understand Horden to be teaching that processor activity is maintained at the idle frequency/voltage pair as the processor is being operated at 16MHz. In contrast, Applicants note that they have claimed that the system clock to the processor is disabled.

Applicants further note that Horden teaches that the operating system identifies whether the *core utilization and throughput* can be handled at the idle frequency or whether a higher frequency is required (Horden, col. 3, lines 48-53). This passage further indicates that Horden's idle frequency and voltage are used to maintain processor activity as Horden indicates that the idle frequency is capable of handling *core utilization and throughput.*

For the foregoing reasons, Claim 1 is neither taught nor suggested by the combination of Orton and Horden. Therefore, Applicants respectfully request allowance of Claim 1.

Claims 2-3 depend from Claim 1, which is believed to be allowable for the foregoing reasons. As a result of their dependency, Claims 2-3 are believed to be allowable. Applicants earnestly request their allowance.

35 U.S.C. §102

Claims 4-11 and 13 are rejected under 35 U.S.C. §102(a) or (e) as being anticipated by Orton. The rejection is respectfully traversed for the following reasons.

CLAIM 4

Currently Amended Claim 4 recites, in part:

> reducing core voltage to the processor to a value sufficient to maintain state during the mode in which system clock is disabled by
>
> furnishing an input to reduce an output voltage provided by a voltage regulator furnishing core voltage to the processor, and
>
> providing a feedback signal to the voltage regulator to reduce its output voltage below a specified output voltage (emphasis added).

Independent Claim 4 recites that a feedback signal is provided to the voltage regulator to reduce its output voltage below a specified output voltage. Applicants respectfully assert that Orton fails to teach or suggest these claim limitations.

Applicants have claimed that a feedback signal is applied to the voltage regulator. In Figure 1 of Orton, the voltage regulator (52) is depicted with an input signal from the host bridge (18). However, Applicants do not understand the voltage regulator to receive a feedback signal, as Applicants have claimed.

In Figure 5 of Orton, the voltage regulator (52) has its output voltage controlled by the VR_LO/HI# signal from the NB control logic (400). The voltage regulator also receives a signal from the system electronics (VR_ON), which directs the voltage regulator to settle to the voltage level selected by the VR_LO/HI# signal (col. 7, lines 59-63). Applicants do not understand either of these inputs to the voltage regulator to be feedback signals, as claimed.

Furthermore, Applicants do not understand either of these signals (VR_LO/HI#, VR_ON) to reduce the output voltage of the voltage regulator below a specified output voltage, as claimed.

For the foregoing reasons, Applicants assert that Independent Claim 4 is neither taught nor suggested by Orton. Consequently, Applicants earnestly request that Claim 4 be allowed.

CLAIMS 5 and 6

Independent Claim 5 recites, in part:

> transferring operation of a voltage regulator furnishing core voltage in a mode in which power is dissipated during reductions in core voltage to a mode in which power is saved during a voltage transition when it is determined that a processor is transitioning from a computing mode to a mode is which system clock to the processor is disabled.

Applicants respectfully assert that Orton fails to teach or suggest the limitations of Claim 5. Orton may discuss reducing power consumption (see, e.g., col. 2, lines 18-20). Orton may achieve a reduction in power by, for example, reducing the operating frequency of the processor. However, power savings can be achieved in manners other than reducing frequency and/or reducing voltage. Applicants have specifically recited in this embodiment that saving power is performed by a choice of mode of operation of the voltage regulator. Orton is silent as to operating the voltage regulator in a mode in which power is dissipated to a mode in which power is saved, as claimed. Thus, Orton fails to teach or suggest the claimed transferring the operation of a voltage regulator from a mode in which power is dissipated to a mode in which power is saved, during a voltage transition.

For the foregoing reasons, Orton fails to teach or suggest the limitations of Claim 5. Therefore, Applicants earnestly request allowance of Claim 5.

Claim 6 depends from Claim 5. By virtue of its dependency on a claim that is believed to be allowable, Applicants believe Claim 6 to be allowable.

Independent Claim 7 recites, in part:

> means for providing signals at the input terminal of the voltage regulator for selecting a voltage for operating the processor in a computing mode and a voltage of a level less than that for operating the processor in a computing mode, wherein the level less than that for operating the processor in a computing mode is sufficient to maintain state of the processor (emphasis added).

For at least the reasons discussed in the response to Claim 1, Claim 7 is neither taught nor suggested by Orton. As such, Applicants earnestly request allowance of Claim 7.

Claims 8-10 depend from Claim 7. By virtue of their dependency from a claim that is believed to be allowable, Applicants believe Claims 8-10 to be allowable.

Claim 11

Amended Independent Claim 11 recites, in part:

> a voltage regulator having:
>
> an output terminal providing a selectable voltage, and
>
> an input terminal for receiving signals indicating the selectable voltage level;
>
> ...

means for reducing the selectable voltage below a level provided by the voltage regulator (emphasis added).

The limitations "the selectable voltage below a level provided by the voltage regulator" describe a selectable voltage level that is below the lowest voltage level which the voltage regulator is specified to output.

Orton may describe causing the voltage regulator to output different voltages. However, Applicants respectfully assert that Orton is silent as to causing the voltage regulator to output a voltage below the lowest voltage level that the voltage regulator is specified to output. Applicants respectfully assert that one of ordinary skill in the art would understand Orton to teach that the output voltage of the voltage regulator to be within a range specified by the voltage regulator, as Orton is silent as to causing the voltage regulator to output a voltage outside of that range.

For the foregoing reasons, Applicants respectfully assert that Orton fails to teach or suggest the limitations, "reducing the selectable voltage below a level provided by the voltage regulator." Therefore, Applicants earnestly request allowance of Claim 11.

CLAIM 13

Claim 13 recites, in part:

> a voltage regulator having:
>
> an output terminal providing a selectable voltage, and
>
> an input terminal for receiving signals indicating the selectable voltage level;
>
> ...
>
> circuitry for conserving charge stored by the voltage regulator when the selectable voltage decreases, and
>
> means for enabling the circuitry for conserving charge stored by the voltage regulator when the selectable voltage decreases (emphasis added).

Claim 13 recites circuitry for conserving charge stored by the voltage regulator when the selectable voltage decreases. Claim 13 further recites means for enabling this circuitry. Thus, limitations of Claim 13 recite that the circuitry for conserving charge stores charge from the voltage regulator.

Applicants respectfully assert that Orton fails to teach or suggest the limitations of Claim 13. The rejection asserts that Orton teaches a battery (60) as a charge storage unit. However, while a battery may be capable of storing charge, Applicants respectfully assert that Orton does not teach or suggest how charge from the voltage regulator is stored in the battery, as claimed. Moreover, Applicants respectfully assert that Orton fails to teach or suggest how charge from the voltage regulator is stored in the battery when the selectable voltage decreases, as claimed.

For the foregoing reasons, Orton fails to teach or suggest the limitations of Claim 13. Therefore, Applicants earnestly request allowance of Claim 13.

NEW CLAIMS

Claims 14-18 have been added. Support for Claims 14-18 may be found in the instant specification at least at page 7, line 3 - page 11, line 11. No new matter has been added as a result of these claim amendments.

Claim 14 recites:

> A circuit for providing a regulated voltage to a processor comprising:
>
> a voltage regulator having:
> an output terminal providing a selectable voltage, and
> an input terminal for receiving signals indicating the selectable voltage level; and
> a voltage regulator feedback circuit;
>
> circuitry coupled to said input terminal and configured to provide signals to the input terminal for selecting a first voltage for operating the processor in a first mode and a second voltage for operating the processor in a second mode;
>
> a voltage source furnishing a value higher than the selectable voltage; and
>
> a feedback circuit coupled to the voltage source, the output terminal, and the voltage regulator feedback circuit.

Applicants respectfully assert that the prior art fails to teach or suggest the limitations, "a voltage source furnishing a value higher than the

selectable voltage; and a feedback circuit coupled to the voltage source, the output terminal, and the voltage regulator feedback circuit."

Claims 15-17 depend from Claim 14, which is believed to be allowable for the foregoing reasons. Therefore, Claims 15-17 are believed to be allowable by virtue of this dependency.

Claim 18 depends from Claim 4, which is believed to be allowable for the foregoing reasons. Therefore, Claim 18 is believed to be allowable by virtue of this dependency.

CONCLUSION

In light of the above listed amendments and remarks, allowance of Claims 1-18 is requested.

Should the Examiner have a question regarding the instant amendment and response, the Applicants invite the Examiner to contact the Applicants' undersigned representative at the below listed telephone number.

Respectfully submitted,
WAGNER, MURABITO & HAO LLP

Dated: 8/3, 2004

Ronald M. Pomerenke
Registration No. 43,009

Address: WAGNER, MURABITO & HAO LLP
Two North Market Street
Third Floor
San Jose, California 95113

Telephone: (408) 938-9060 Voice
(408) 938-9069 FAX

08-05-04

RCE

2185

Docket Number: TRAN-P059

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Patent Application

I hereby certify that this transmittal of the below described documents is being deposited with the United States Postal Service in an envelope bearing Express Mail Postage and an Express Mail label, with the below serial number, addressed to the Commissioner for Patents P.O. Box 1450 Alexandria, VA 22313-1450, on the below date of deposit.			
Express Mail Label No.:	EV516369256US	Name of Person Making the Deposit:	ANTHONY CHOU
Date of Deposit:	08/03/04	Signature of the Person Making the Deposit:	Anthony Chou

In re Application of: Andrew Read, Sameer Halapete and Keith Klayman

Serial No.: 09/694,433 Examiner: CAO, CHUN

Filed: 10/23/00 Art Unit: 2185

Confirmation No.: 3072

For: SAVING POWER WHEN IN OR ON TRANSITIONING TO A STATIC MODE OF A PROCESSOR (AS AMENDED)

Mail Stop RCE
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

REQUEST FOR CONTINUED EXAMINATION (RCE) TRANSMITTAL (SUBSECTION(B) OF 35 U.S.C. § 132)

This is a Request for Continued Examination (RCE) under 37 C.F.R. § 1.114 for the above-identified application.

1. Submission required under a filing under 37 C.F.R. § 1.114

   a. [ ] Previously submitted

   i. [ ] Consider the amendment(s)/ reply under 37 C.F.R. § 1.116 previously filed on _____
   (Any unentered amendment(s) referred to above will be entered)

   ii. [ ] Consider the arguments in the Appeal Brief or Reply Brief previously filed on _____

   b. [X] Enclosed

   i. [X] Amendment/Reply

   ii. [ ] Affidavit(s)/Declaration(s)

   iii. [X] Information Disclosure Statement (IDS) & Form 1449

   iv. [X] Other References

2. Miscellaneous

   a. [ ] Suspension of action on the above-identified application is requested under 37 C.F.R. § 1.103(c) for a period of _____ months.
   (period of suspension shall not exceed 3 months: Fee under 37 C.F.R. § 1.17(l) required)

08/06/2004 HALI11 00000059 09694433
01 FC:1801 770.00 OP
02 FC:1201 172.00 OP

rev. 1/00 kgr

Extension of Term

3. The proceedings herein are for a patent application and the provisions of 37 C.F.R. 1.136 apply.

(a) [X] Applicant petitions for an extension of time under 37 C.F.R. 1.136 (fees: 37 C.F.R. 1.17(a)-(d) for the total number of months checked below:)

Extension	Fee
[ ] one month	$110.00
[ ] two months	$420.00
[ ] three months	$950.00
[ ] four months	$1,480.00

Fee $ 110.00

If an additional extension of time is required, please consider this a petition therefor.

(b) [ ] Applicant believes that no extension of term is required. However, this conditional petition is being made to provide for the possibility that applicant has inadvertently overlooked the need for a petition for extension of time.

FEES DUE

The RCE fee under 37 C.F.R. § 1.17(e) is required by 37 C.F.R. § 1.114 when the RCE is filed.

CLAIMS					
	NO. OF CLAIMS		EXTRA CLAIMS	RATE	FEES
Basic Application Fee					$770.00
Total Claims	18	Minus 20=	0	X $18 =	$0.00
Independent Claims	8	Minus 6=	2	X $86 =	$172.00
If multiple dependent claims are presented, add $290.00					$0.00
TOTAL APPLICATION FEE DUE					$942.00

PAYMENT OF FEES

1. The full fee due in connection with this communication is provided as follows:

[X] The Commissioner is hereby authorized to charge any additional fees associated with this communication or credit any overpayment to Deposit Account No.: 23-0085. A duplicate copy of this authorization is enclosed.

[**X**] A check in the amount of $942.00

[ ] Charge any fees required or credit any overpayments associated with this filing to Deposit Account No.: 23-0085.

Please direct all correspondence concerning the above-identified application to the following address:

WAGNER, MURABITO & HAO LLP
Two North Market Street, Third Floor
San Jose, California 95113
(408) 938-9060
Customer No: 45590

Respectfully submitted,

Date: 8/3/04

By: Ronald M. Pomerenke
Ronald M. Pomerenke
Reg. No. 43,009

rev. 1/00 kgr

Patent

Docket No.: TRAN-P059

Information Disclosure Statement Transmittal

I hereby certify that this transmittal of the below described document is being deposited with the United States Postal Service in an envelope bearing First Class Postage and addressed to the Commissioner of Patents and Trademarks, Washington, D.C., 20231, on the below date of deposit.

Date of Deposit:	08/03/04	Name of Person Making the Deposit:	ANTHONY CHOU	Signature of the Person Making the Deposit:	

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Inventor(s): Andrew Read, Sameer Halapete and Keith Klayman

Group Art Unit:

Filed: 10/23/00

Examiner:

Application No.: 09/694,433

Title: SAVING POWER WHEN IN OR ON TRANSITIONING TO A STATIC MODE OF A PROCESSOR (AS AMENDED)

The Commissioner of Patents and Trademarks
Washington, D.C. 20231
Sir:

Information Disclosure Statement Transmittal

Transmitted herewith is the following:

..... Formal drawings, totaling ..... sheets.
..... Informal drawings, totaling ..... sheets.
..... Certification for PTO Consideration
..X.. Information Disclosure statement (1 sheet)
..... Information Disclosure statement and late filing fee
..X.. Form 1449
..... Petition for Extension of Time
..X.. Other: References

Fee Calculation (for other than a small entity)

Fee Items				Fee Rate	Total
Petition for Extension of Time (fee calculated elsewhere				$ .00	$0.00
Information Disclosure Statement, late filing				$180.00	$0.00
Other:					$0.00
Total Fees					$0.00

PAYMENT OF FEES

1. The full fee due in connection with this communication is provided as follows:

[X] The Commissioner is hereby authorized to charge any additional fees associated with this communication or credit any overpayment to Deposit Account No.: 23-0085 .
A duplicate copy of this authorization is enclosed.

[ ] A check in the amount of $0.00

[ ] Charge any fees required or credit any overpayments associated with this filing to Deposit Account No.: 23-0085.

kgr 7/98

Please direct all correspondence concerning the above-identified application to the following address:

WAGNER, MURABITO & HAO LLP
Two North Market Street, Third Floor
San Jose, California 95113
(408) 938-9060
Customer No: 45590

Respectfully submitted,

Date: 8/3/04

By: Ronald M. Pomerenke
Ronald M. Pomerenke
Reg. No. 43,009

kgr 7/98

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Attorney Docket No.: TRAN-P059

Inventor(s): Andrew Read, Sameer Halapete and Keith Klayman

Group Art Unit:

Filed: 10/23/00

Examiner:

Serial No.: 09/694,433

Title: SAVING POWER WHEN IN OR ON TRANSITIONING TO A STATIC MODE OF A PROCESSOR (AS AMENDED)

The Commissioner of Patents and Trademarks
Washington, D.C. 20231
Sir:

Information Disclosure Statement Submitted Pursuant to 37 C.F.R. 1.97(b)

The citations referenced herein, copies attached, may be material to the examination of the above-identified application and are, therefore, submitted in compliance with the duty of disclosure as defined in 37 C.F.R. 1.56. The Examiner is requested to make these citations of official record in the application.

This Information Disclosure Statement submitted in accordance with 37 C.F.R. 1.97(b) is not to be construed as a representation that a search has been made, that additional items material to the examination of this application do not exist, or that any one or more of these citations constitute prior art under 35 U.S.C. 102.

The Examiner's attention is respectfully directed to the following U.S. Patents:

Pat. No.	Pat. Title	Grant Date
5,832,205	MEMORY CONTROLLER FOR A MICROPROCESSOR FOR DETECTING A FAILURE OF SPECULATION ON THE PHYSICAL NATURE OF A COMPONENT BEING ADDRESSED	11/03/98

The Examiner's attention is respectfully directed to the following document:

Intel Corporation; "Intel 82801 CAM I/O CONTROLLER HUB (ICH3-M)" Datasheet; July 2001

Please direct all correspondence concerning the above-identified application to the following address:

WAGNER, MURABITO & HAO LLP
Two North Market Street, Third Floor
San Jose, California 95113
(408) 938-9060
Customer Number: 45590

Respectfully submitted,

Date: 8/3/04

By: Ronald M. Pomerenke
Ronald M. Pomerenke
Reg. No. 43,009

rev. 6/97 jpw

Attorney Docket No.: TRAN-P059

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Patent Application

Inventor(s): Andrew Read, Sameer Halapete and Keith Klayman

Group Art Unit:

Filed: 10/23/00

Examiner:

Serial No.: 09/694,433

Title: SAVING POWER WHEN IN OR ON TRANSITIONING TO A STATIC MODE OF A PROCESSOR (AS AMENDED)

Form 1449

U.S. Patent Documents

Examiner Initial	No.	Patent No.	Date	Patentee	Class	Sub-class	Filing Date
	A	5,832,205	11/03/98	Kelly et al.	395	185.06	08/20/96
	B						

Foreign Patent or Published Foreign Patent Application

Examiner Initial	No.	Document No.	Publication Date	Country or Patent Office	Class	Sub-class	Translation Yes	Translation No
	C							

Other Documents

Examiner Initial	No.	Author, Title, Date, Place (e.g. Journal) of Publication
	D	Intel Corporation; "Intel 82801 CAM I/O CONTROLLER HUB (ICH3-M)" Datasheet; July 2001

Examiner	Date Considered

Examiner: Initial citation considered. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

PATENT APPLICATION FEE DETERMINATION RECORD
Effective October 1, 2000

Application or Docket Number
09 644 433

CLAIMS AS FILED - PART I

	(Column 1)	(Column 2)
TOTAL CLAIMS	13	
FOR	NUMBER FILED	NUMBER EXTRA
TOTAL CHARGEABLE CLAIMS	13 minus 20=	*
INDEPENDENT CLAIMS	2 minus 3 =	*
MULTIPLE DEPENDENT CLAIM PRESENT		☐

* If the difference in column 1 is less than zero, enter "0" in column 2

SMALL ENTITY TYPE ☐		OR	OTHER THAN SMALL ENTITY	
RATE	FEE		RATE	FEE
BASIC FEE	355.00	OR	BASIC FEE	710.00
X$ 9=		OR	X$18=	
X40=		OR	X80=	
+135=		OR	+270=	
TOTAL	355	OR	TOTAL	

CLAIMS AS AMENDED - PART II

AMENDMENT A

	(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA
Total	* 18	Minus	** 20	= 0
Independent	* 8	Minus	*** 3	= 2
FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM				☐

SMALL ENTITY		OR	OTHER THAN SMALL ENTITY	
RATE	ADDITIONAL FEE		RATE	ADDITIONAL FEE
X$ 9=		OR	X$18=	
X40=		OR	X80=	172
+135=		OR	+270=	
TOTAL ADDIT. FEE		OR	TOTAL ADDIT. FEE	

AMENDMENT B

	(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA
Total	*	Minus	**	=
Independent	*	Minus	***	=
FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM				☐

RATE	ADDITIONAL FEE		RATE	ADDITIONAL FEE
X$ 9=		OR	X$18=	
X40=		OR	X80=	
+135=		OR	+270=	
TOTAL ADDIT. FEE		OR	TOTAL ADDIT. FEE	

AMENDMENT C

	(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA
Total	*	Minus	**	=
Independent	*	Minus	***	=
FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM				☐

RATE	ADDITIONAL FEE		RATE	ADDITIONAL FEE
X$ 9=		OR	X$18=	
X40=		OR	X80=	
+135=		OR	+270=	
TOTAL ADDIT. FEE		OR	TOTAL ADDIT. FEE	

* If the entry in column 1 is less than the entry in column 2, write "0" in column 3.
** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20."
***If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3."
The "Highest Number Previously Paid For" (Total or Independent) is the highest number found in the appropriate box in column 1.

PRL

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
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P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/694,433	10/23/2000	Andrew Read	TRANS59	3072

7590 09/22/2004

WAGNER, MURABITO & HAO LLP
TWO NORTH MARKET STREET
THIRD FLOOR
SAN JOSE, CA 95113

EXAMINER	
CAO, CHUN	
ART UNIT	PAPER NUMBER
2115	

DATE MAILED: 09/22/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

PTO-90C (Rev. 10/03)

Office Action Summary	Application No.	Applicant(s)	
	09/694,433	READ ET AL.	
	Examiner	Art Unit	
	Chun Cao	2115	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *03 August 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-18* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-18* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *6/22/04, 8/3/04*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAIL ACTION

1. Claims 1-18 are presented for examination.

2. The text of those applicable section of Title 35, U.S. Code not included in this action can be found in the prior Office Action.

Continued Examination Under 37 CFR 1.114

3. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 8/3/04 has been entered.

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 1-3 are rejected under 35 U.S.C. 103(a) as being unpatentable over Orton et al. (Orton), US patent no. 6,118,306, in view of "Re: AX64Pro or AK72?", NewsReader, June 15, 2000, pages 1-2; (hereinafter, "Newsreader").

Orton is a prior art reference cited by applicant in IDS paper no. 6.

As per claim 1, Orton teaches a method for reducing power utilized by a processor comprising the steps of:

determining that a processor is transitioning from a computing mode to a mode in which system clock to the processor is disabled [col. 2, lines 44-60]; and

reducing core voltage to the processor to a value sufficient to maintain state during the mode of which system clock is disable [col. 3, lines 10-20].

Orton does not explicitly teach that the value of the core voltage is not sufficient to maintain processing activity in said processor. In other words, Orton does not teach reducing the core voltage to one Volt or less during deep sleep mode.

Newsreader teaches of reducing the core voltage to one Volt or less during deep sleep mode [page 2, paragraph 3]. Therefore, Newsreader teaches that the value of the core voltage is not sufficient to maintain processing activity in said processor.

It would have been obvious to one of ordinary skill in the art at time the invention to combine the teachings of Orton and Newsreader because they are both directed to the problem of reducing the power consumption of a processor core, and the specify teachings of Newsreader stated above would improve power consumption by further reducing the core voltage to a minimum supported voltage.

As per claim 2, Orton teaches of determining the processor is transitioning from a computing mode to a mode in which system clock to the processor is disabled comprises monitoring a stop clock signal [col. 2, lines 44-60; col. 5, lines 4-11; col. 7, lines 38-43].

As per claim 3, Orton teaches of reducing an output voltage providing by a voltage regulator furnishing core voltage to the processor and providing a feedback signal to the voltage regulator to reduce its output voltage below a specified output voltage [col. 2, lines 24-27; col. 3, lines 10-19; col. 7, lines 14-19, 44-58].

6. Claims 4, 12 and 14-18 are rejected under 35 U.S.C. 103 (a) as being unpatentable over Orton et al. (Orton), US patent no. 6,118,306 in view of Applicant Admitted Prior Art (AAPA).

7. As per claim 4, Orton teaches that a method for reducing power utilized by a processor comprising the steps of:

determining that a processor is transitioning from a computing mode to a mode is which system clock to the processor is disabled [col. 2, lines 44-60];

reducing core voltage to the processor to a value sufficient to maintain state during the mode of which system clock is disable by [col. 3, lines 10-20]:

furnishing an input to reduce an output voltage provided by a voltage regulator furnishing core voltage to the processor [col. 2, lines 24-27; col. 3, lines 10-19; col. 7, lines 14-19, 44-58]; and

providing a control signal to the voltage regulator to reduce its output voltage below a specified output voltage [col. 2, lines 24-27; col. 3, lines 10-19; col. 7, lines 14-19, 44-58].

Orton does not explicitly teach of providing a feedback to the voltage regulator.

AAPA teaches of providing a feedback to the voltage regulator [page 5, lines 6-9].

It would have been obvious to one of ordinary skill in the art at time the invention to combine the teachings of Orton and AAPA because the specify teachings of AAPA stated above would allow the processor to run stable and reliable by adjusting the core voltage accordingly.

As per claim 18, Orton teaches that the output voltage to which said voltage regulator is reduced depends upon output voltage of said voltage regulator prior to furnishing the input to reduce the output voltage provided by the voltage regulator [col. 7, lines 14-58].

8. As per claim 12, Orton discloses a circuit [fig. 5] for providing a regulated voltage to a processor comprising:

a voltage regulator [52, fig. 1, fig. 5] having: an output terminal [col. 7, lines 50-51; " the output from the voltage regulator 52", inherently, there is an output terminal in the voltage regulator 52] providing a selectable voltage [col. 3, lines 10-12; col. 7, lines 28-31, 46-47, "...adjust the voltage level supplied by the voltage regulator 52 up or down" and "to indicate that the voltage level from the voltage regulator 52 is changing"];

input terminal [fig. 5; col. 7, lines 52-55; "the voltage interface provided the control logic portion 400 allows the voltage regulator 52 to change settings", inherently, there is an input terminal in the voltage regulator 52] for receiving signals indicating the selectable voltage level;

means for providing signal at the input terminal of the voltage regulator for selecting a voltage for operating the processor in a computing mode and a voltage of a level less than that for operating the processor in computing mode [col. 7, lines 50-65],

means for reducing the selectable voltage below a level provided by the voltage regulator [col. 7, lines 50-65].

Orton does not explicitly disclose a voltage regulator feedback circuit and a voltage divider network.

AAPA discloses a voltage regulator including a voltage regulator feedback circuit and a voltage divider network [page 5, lines 6-9].

It would have been obvious to one of ordinary skill in the art at time the invention to combine the teachings of Orton and AAPA because the specify teachings of AAPA stated above would allow the processor to run stable and reliable by adjusting the core voltage accordingly.

9. As per claim 14, is contained same limitations as set forth in claim 12. Therefore, same rejection is applied.

As per claim 15, Orton teaches that the first voltage is for operating the processor in a computing mode and the second voltage is a level less than that for operating the processor in the computing mode [col. 7, lines 50-65].

As to claims 16 and 17, AAPA discloses that the feedback circuit comprises a voltage divider [page 5, lines 6-9].

10. Claims 5-11 and 13 are rejected under 35 U.S.C. 102 (a) or 102(e) as being anticipated by Orton et al. (Orton), US patent no. 6,118,306.

As per claim 5, Orton teaches a method for reducing power utilized by a processor comprising the steps of:

determining that a processor is transitioning from a computing mode to a mode is which system clock to the processor is disabled [col. 2, lines 44-60];

reducing core voltage to the processor to a value sufficient to maintain state during the mode of which system clock is disable; [col. 3, lines 10-20]; and

transferring operation of a voltage regulator furnishing core voltage in a mode in which power is dissipated during reductions in core voltage to a mode in which power is saved during a voltage transition when it is determined at a processor is transitioning from a computing mode to a mode is which system clock to the processor is disabled [col. 2, lines 11-27, 44-65; col. 7, line 59-col. 8, line 5].

As per claim 6, Orton teaches of returning the voltage regulator to its original mode of operation [col. 3, lines 10-14; col. 7, lines 51-58; col. 8, lines 54-65].

11. As per claim 7, Orton discloses a circuit [fig. 5] for providing a regulated voltage to a processor comprising:

a voltage regulator [52, fig. 1, fig. 5] having: an output terminal [col. 7, lines 50-51; " the output from the voltage regulator 52", inherently, there is an output terminal in the voltage regulator 52] providing a selectable voltage [col. 3, lines 10-12; col. 7, lines 28-31, 46-47, "...adjust the voltage level supplied by the voltage regulator 52 up or down" and "to indicate that the voltage level from the voltage regulator 52 is changing"];

input terminal [fig. 5; col. 7, lines 52-55; "the voltage interface provided the control logic portion 400 allows the voltage regulator 52 to change settings" , inherently, there is an input terminal in the voltage regulator 52] for receiving signals indicating the selectable voltage level;

means for providing signal at the input terminal of the voltage regulator for selecting a voltage for operating the processor in a computing mode and a voltage of a level less than that for operating the processor in computing mode [col. 7, lines 50-65], wherein the level less than that for operating the processor in a computing mode is sufficient to maintain state of the processor [col. 2, lines 44-65; col. 3, lines 10-20; col. 7, line 59-col. 8, line 5].

As per claim 8, Orton discloses that the voltage regulator comprises means for accepting binary signals [LO/HI signals] indicating different voltage level [fig. 5; col. 7, lines 20-37, 63-65; "A signal **VR_LO/HI#**...adjust the voltage level supplied by the voltage regulator 52 up or down"].

As per claim 9, Orton discloses that the voltage regulator comprises:

Selection circuitry, means for furnishing a plurality of signals at the input to the selection circuitry and means for controlling the selection by the selection circuitry [fig. 3A] [col. 5, lines 38-55].

As per claim 10, Orton discloses a multiplexor [col. 5, lines 44-45; fig. 3A] and means for controlling the selection by the selection circuitry including a control terminal for receiving signals indicating a system clock to the processor is being terminated [col. 5, lines 38-65].

12. As per claim 11, Orton discloses a circuit [fig. 5] for providing a regulated voltage to a processor comprising:

a voltage regulator [52, fig. 1, fig. 5] having: an output terminal [col. 7, lines 50-51; " the output from the voltage regulator 52", inherently, there is an output terminal in the voltage regulator 52] providing a selectable voltage [col. 3, lines 10-12; col. 7, lines 28-31, 46-47, "...adjust the voltage level supplied by the voltage regulator 52 up or down" and "to indicate that the voltage level from the voltage regulator 52 is changing"];

input terminal [fig. 5; col. 7, lines 52-55; "the voltage interface provided the control logic portion 400 allows the voltage regulator 52 to change settings" , inherently, there is an input terminal in the voltage regulator 52] for receiving signals indicating the selectable voltage level;

means for providing signal at the input terminal of the voltage regulator for selecting a voltage for operating the processor in a computing mode and a voltage of a level less than that for operating the processor in computing mode [col. 7, lines 50-65],

means for reducing the selectable voltage below a level provided by the voltage regulator [col. 7, lines 50-65].

13. As per claim 13, Orton discloses a circuit [fig. 5] for providing a regulated voltage to a processor comprising:

a voltage regulator [52, fig. 1, fig. 5] having: an output terminal [col. 7, lines 50-51; " the output from the voltage regulator 52", inherently, there is an output terminal in the voltage regulator 52] providing a selectable voltage [col. 3, lines 10-12; col. 7, lines

28-31, 46-47, "...adjust the voltage level supplied by the voltage regulator 52 up or down" and "to indicate that the voltage level from the voltage regulator 52 is changing"];

input terminal [fig. 5; col. 7, lines 52-55; "the voltage interface provided the control logic portion 400 allows the voltage regulator 52 to change settings" , inherently, there is an input terminal in the voltage regulator 52] for receiving signals indicating the selectable voltage level;

means for providing signal at the input terminal of the voltage regulator for selecting a voltage for operating the processor in a computing mode and a voltage of a level less than that for operating the processor in computing mode [col. 7, lines 50-65],

circuitry for conserving charge [battery 60] stored by the voltage regulator when the selectable voltage decreases; and means for enabling the circuitry for conserving charge stored by the voltage regulator when the selectable voltage decreases [col. 7, lines 28-58].

14. Applicant's argument with respect to claims 1-13 have been considered but is moot in view of the new ground(s) of rejection.

15. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

AMD Athlon; "Processor Module" datasheet, discloses a table of core voltage operating ranges for a processor module [page 28, table 8].

Intel, "Pentium III Processor for the SC242 at 450 MHz to 866 MHz and 1.0 GHz", Datasheet, teaches of a processor is incapable of responding to snoop transactions or latching interrupt signals in deep sleep state [page 16, paragraph 2.2.6].

Any response to this action should be mailed to:

Commissioner of Patents and Trademarks

Washington, D.C. 20231

Hand-delivered responses should be brought to Crystal Park II, 2121 Crystal Drive, Arlington. VA., Sixth Floor (Receptionist).

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Chun Cao at (703) 308-6106 (571-272-3664, effective 10/14/2004). The examiner can normally be reached on Monday-Friday from 7:30 am - 4:00 pm. If attempts to reach the examiner by phone are unsuccessful, the examiner's supervisor Thomas Lee can be reached at (703) 305-9717 (571-272-3667, effective 10/14/2004). The fax number for this Art Unit is following: Official (703) 872-9306.

Any inquiry of a general nature or relating to the status of this application should be directed to the Group receptionist whose telephone number is (703) 306-5631 (571-272-2100, effective 10/14/2004).

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Chun Cao

Sep. 17, 2004

Attorney Docket No.: TRAN-P059

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Patent Application

Inventor(s): Andrew Read, Sameer Halapete and Keith Klayman

Group Art Unit:

Filed: 10/23/00

Examiner:

Serial No.: 09/694,433

Title: SAVING POWER WHEN IN OR ON TRANSITIONING TO A STATIC MODE OF A PROCESSOR (AS AMENDED)

Form 1449

U.S. Patent Documents

Examiner Initial	No.	Patent No.	Date	Patentee	Class	Sub-class	Filing Date
C	A	5,832,205	11/03/98	Kelly et al.	395	185.06	08/20/96
	B						

Foreign Patent or Published Foreign Patent Application

Examiner Initial	No.	Document No.	Publication Date	Country or Patent Office	Class	Sub-class	Translation Yes	Translation No
	C							

Other Documents

Examiner Initial	No.	Author, Title, Date, Place (e.g. Journal) of Publication
C	D	Intel Corporation; "Intel 82801 CAM I/O CONTROLLER HUB (ICH3-M)" Datasheet; July 2001

Examiner	CAO	Date Considered	9/16/04

Examiner: Initial citation considered. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

Attorney Docket No.: TRAN-P059 (5TH IDS)

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Patent Application

Inventor(s): Andrew Read, Sameer Halapete and Keith Klayman

Group Art Unit:

Filed: 10/23/00

Examiner:

Serial No.: 09/694,433

Title: STATIC POWER CONTROL

Form 1449

U.S. Patent Documents

Examiner Initial	No.	Patent No.	Date	Patentee	Class	Sub-class	Filing Date
[illegible]	A	5,778,237	07/07/98	Yamamoto et al.	395	750.04	12/14/95
[illegible]	B	5,204,863	04/20/93	Saint-Joigny et al.	371	16.3	02/08/91
	C						

Foreign Patent or Published Foreign Patent Application

Examiner Initial	No.	Document No.	Publication Date	Country or Patent Office	Class	Sub-class	Translation Yes	Translation No
	D							
	E							

Other Documents

Examiner Initial	No.	Author, Title, Date, Place (e.g. Journal) of Publication
	F	
	G	

Examiner	CAO	Date Considered	9/16/04

Examiner: Initial citation considered. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

Notice of References Cited	Application/Control No. 09/694,433	Applicant(s)/Patent Under Reexamination READ ET AL.	
	Examiner Chun Cao	Art Unit 2115	Page 1 of 1

U.S. PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Name	Classification
	A	US-5,852,737	12-1998	Bikowsky, Zeev	713/323
	B	US-6,675,304	01-2004	Pole et al.	713/322
	C	US-6,704,880	03-2004	Dai et al.	713/323
	D	US-			
	E	US-			
	F	US-			
	G	US-			
	H	US-			
	I	US-			
	J	US-			
	K	US-			
	L	US-			
	M	US-			

FOREIGN PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Country	Name	Classification
	N					
	O					
	P					
	Q					
	R					
	S					
	T					

NON-PATENT DOCUMENTS

*		Include as applicable: Author, Title Date, Publisher, Edition or Volume, Pertinent Pages)
	U	"Re: AX64Pro or AK72?", NewsReader, June 15, 2000, pages 1-2.
	V	AMD Athlon; "Processor Module" datasheet, June 2000, pages 1-64.
	W	Intel, "Pentium III Processor for the SC242 at 450 MHz to 866 MHz and 1.0 GHz", Datasheet, March 2000, pages 1-30.
	X	

*A copy of this reference is not being furnished with this Office action. (See MPEP § 707.05(a).)
Dates in MM-YYYY format are publication dates. Classifications may be US or foreign.

Index of Claims

Application No.	Applicant(s)
09/694,433	READ ET AL.
Examiner	**Art Unit**
Chun Cao	2115

√	Rejected	–	(Through numeral) Cancelled	N	Non-Elected	A	Appeal
=	Allowed	÷	Restricted	I	Interference	O	Objected

Claim		Date
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Search Notes

Application No.	Applicant(s)	
09/694,433	READ ET AL.	
Examiner	**Art Unit**	
Chun Cao	2115	

SEARCHED			
Class	Subclass	Date	Examiner
updated all		9/17/04	cc

INTERFERENCE SEARCHED			
Class	Subclass	Date	Examiner

SEARCH NOTES (INCLUDING SEARCH STRATEGY)		
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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of	)	
	)	
Read et al.	)	Examiner: Cao, Chun
	)	
Serial No. 09/694,433	)	Art Unit: 2115
	)	
Filing Date: October 23, 2000	)	
	)	
For: STATIC POWER CONTROL	)	
(As Filed)	)	
	)	

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

AMENDMENT AND RESPONSE TO NON-FINAL OFFICE ACTION

Dear Sir:

In response to the Office Action mailed September 22, 2004, the following amendments and responses to the above captioned patent application are respectfully submitted. Reconsideration of the application is respectfully requested.

03/28/2005 MWOLDGE1 00000043 09694433

01 FC:1253	~~1020.00~~ OP
02 FC:1201	800.00 OP
03 FC:1202	850.00 OP

AMENDMENTS TO THE CLAIMS

LISTING OF CLAIMS IN THE CASE

The following listing of Claims replaces all previous listings:

1. (Previously Presented) A method for reducing power utilized by a processor comprising the steps of:

determining that a processor is transitioning from a computing mode to a mode in which system clock to the processor is disabled, and

reducing core voltage to the processor to a value sufficient to maintain state during the mode in which system clock is disabled, wherein said value of the core voltage is not sufficient to maintain processing activity in said processor.

Claim 2. (Previously Presented) A method as claimed in Claim 1 in which the step of determining that a processor is transitioning from a computing mode to a mode in which system clock to the processor is disabled comprises monitoring a stop clock signal.

Claim 3. (Original) A method as claimed in Claim 1 in which the step of reducing core voltage to the processor to a value sufficient to maintain state during the state in which system clock is disabled comprises

furnishing an input to reduce an output voltage provided by a voltage regulator furnishing core voltage to the processor.

Claim 4. (Previously Presented) A method for reducing power utilized by a processor comprising the steps of:

determining that a processor is transitioning from a computing mode to a mode in which system clock to the processor is disabled, and

reducing core voltage to the processor to a value sufficient to maintain state during the mode in which system clock is disabled by:

furnishing an input to reduce an output voltage provided by a voltage regulator furnishing core voltage to the processor, and

providing a feedback signal to the voltage regulator to reduce its output voltage below a specified output voltage.

Claim 5. (Previously Presented) A method for reducing power utilized by a processor comprising the steps of:

determining that a processor is transitioning from a computing mode to a mode in which system clock to the processor is disabled,

reducing core voltage to the processor to a value sufficient to maintain state during the mode in which system clock is disabled, and

transferring operation of a voltage regulator furnishing core voltage in a mode in which power is dissipated during reductions in core voltage to a mode in which power is saved during a voltage transition

when it is determined that a processor is transitioning from a computing mode to a mode is which system clock to the processor is disabled.

Claim 6. (Previously Presented) A method as claimed in Claim 5 further comprising the steps of returning the voltage regulator to its original mode of operation when the value of the core voltage sufficient to maintain state during the mode in which system clock is disabled is reached.

Claim 7. (Previously Presented) A circuit for providing a regulated voltage to a processor comprising:

a voltage regulator having:

an output terminal providing a selectable voltage, and

an input terminal for receiving signals indicating the selectable voltage level;

means for providing signals at the input terminal of the voltage regulator for selecting a voltage for operating the processor in a computing mode and a voltage of a level less than that for operating the processor in a computing mode, wherein the level less than that for operating the processor in a computing mode is sufficient to maintain state of the processor.

Claim 8. (Original) A circuit as claimed in Claim 7 in which the means for providing signals at the input terminal of the voltage regulator comprises means for accepting binary signals indicating different levels of voltage.

Claim 9. (Original) A circuit as claimed in Claim 7 in which the means for providing signals at the input terminal of the voltage regulator comprises:

selection circuitry,

means for furnishing a plurality of signals at the input to the selection circuitry, and

means for controlling the selection by the selection circuitry.

Claim 10. (Original) A circuit as claimed in Claim 9 in which:

the selection circuitry is a multiplexor, and

the means for controlling the selection by the selection circuitry includes a control terminal for receiving signals indicating a system clock to the processor is being terminated.

Claim 11. (Currently Amended) A circuit for providing a regulated voltage to a processor comprising:

a voltage regulator having:

an output terminal providing a selectable voltage, and

an input terminal for receiving signals indicating the selectable voltage level;

means for providing signals at the input terminal of the voltage regulator for selecting a voltage for operating the processor in a computing mode and a voltage of a level less than that for operating the processor in a computing mode; and

means for reducing the selectable voltage below a lowest level ~~provided by~~ the voltage regulator is specified to output.

Claim 12. (Previously Presented) A circuit for providing a regulated voltage to a processor comprising:

a voltage regulator having:

an output terminal providing a selectable voltage;

an input terminal for receiving signals indicating the selectable voltage level; and

a voltage regulator feedback circuit;

means for providing signals at the input terminal of the voltage regulator for selecting a voltage for operating the processor

in a computing mode and a voltage of a level less than that for operating the processor in a computing mode; and

means for reducing the selectable voltage below a level provided by the voltage regulator comprising:

a voltage divider network joined between the output terminal and a voltage source furnishing a value higher than the selectable voltage, and

the voltage regulator feedback circuit receiving a value from the voltage divider network.

Claim 13. (Previously Presented) A circuit for providing a regulated voltage to a processor comprising:

a voltage regulator having:

an output terminal providing a selectable voltage, and

an input terminal for receiving signals indicating the selectable voltage level;

means for providing signals at the input terminal of the voltage regulator for selecting a voltage for operating the processor in a computing mode and a voltage of a level less than that for operating the processor in a computing mode;

circuitry for conserving charge stored by the voltage regulator when the selectable voltage decreases, and

means for enabling the circuitry for conserving charge stored by the voltage regulator when the selectable voltage decreases.

Claim 14. (Previously Presented) A circuit for providing a regulated voltage to a processor comprising:

a voltage regulator having:

an output terminal providing a selectable voltage, and

an input terminal for receiving signals indicating the selectable voltage level; and

a voltage regulator feedback circuit;

circuitry coupled to said input terminal and configured to provide signals to the input terminal for selecting a first voltage for operating the processor in a first mode and a second voltage for operating the processor in a second mode;

a voltage source furnishing a value higher than the selectable voltage; and

a feedback circuit coupled to the voltage source, the output terminal, and the voltage regulator feedback circuit.

15. (Previously Presented) The circuit of Claim 14, wherein the first voltage is for operating the processor in a computing mode and the second voltage is a level less than that for operating the processor in the computing mode.

16. (Previously Presented) The circuit of Claim 15, wherein the feedback circuit comprises a voltage divider.

17. (Previously Presented) The circuit of Claim 14, wherein the feedback circuit comprises a voltage divider.

18. (Previously Presented) The method of Claim 4, wherein the output voltage to which said voltage regulator is reduced depends upon output voltage of said voltage regulator prior to furnishing the input to reduce the output voltage provided by the voltage regulator.

19. (New) A computer system comprising:

a processing unit;

circuitry coupled to the processor unit, said circuitry configured to provide to said processing unit:

a sleep voltage;

a first operating voltage; and

a second operating voltage that is less than the first operating voltage;

wherein said computer system has a first transition time for transitioning from said sleep voltage to said first operating voltage;

wherein said computer system has a second transition time for transitioning from said sleep voltage to said second operating voltage;

wherein said second transition time is within an allowed time for transitioning from a sleep state to an operating state; and

wherein said first transition time is greater than said allowed time.

20. (New) A computer system as recited in Claim 19 wherein said allowed time is based on a configuration of said computer system.

21. (New) A computer system as recited in Claim 19 wherein said allowed time is based on timing requirements of said computer system.

22. (New) A computer system as recited in Claim 21, wherein said timing requirements are based on interrupt response times.

23. (New) A computer system as recited in Claim 19 wherein said first and second transition times are based on respective first and second voltage ramp times.

24. (New) A computer system as recited in Claim 19 wherein said sleep voltage is sufficient to maintain state of said processing unit but is not sufficient to maintain processing activity in said processing unit.

25. (New) A method of operating a computer processor, said method comprising:

transitioning from providing a sleep voltage to said computer processor to providing a first operating voltage to said computer processor within an allowed time for transitioning from a sleep state to an operating state; and

transitioning from said providing said first operating voltage to said computer processor to providing a second operating voltage to said computer processor, wherein a transition time for changing from said sleep voltage directly to said second operating voltage is greater than said allowed time for transitioning from said sleep state to said operating state.

26. (New) A method in accordance with Claim 25 wherein said second operating voltage is greater than said first operating voltage.

27. (New) A method in accordance with Claim 25 further comprising:

enabling a system clock to said computer processor when providing said first operating voltage to said computer processor; and

disabling said system clock to said computer processor when providing said sleep voltage to said computer processor.

28. (New) A method in accordance with Claim 25, wherein said sleep voltage is sufficient to maintain state of said computer processor but is not sufficient to maintain processing activity in said computer processor.

29. (New) A computer system comprising:

a processor;

an adjustable voltage supply configured to output to said processor:

a sleep voltage; and

a first operating voltage that, based on a rate of transitioning from said sleep voltage to said first operating voltage, is not achievable

from said sleep voltage within an allowed time for transitioning from a sleep state to an operating state.

30. (New) A computer system as recited in Claim 29, wherein said adjustable voltage supply is further configured to output to said processor a second operating voltage that, based on a rate of transitioning from said sleep voltage to said second operating voltage, is achievable from said sleep voltage within said allowed time for transitioning from said sleep state to said operating state.

31. (New) A computer system as recited in Claim 29 wherein said allowed time is based on a configuration of said computer system.

32. (New) A computer system as recited in Claim 29 wherein said adjustable voltage supply comprises a voltage regulator.

33. (New) A computer system comprising:

a processing unit;

circuitry coupled to the processor unit, said circuitry configured to provide to said processing unit:

a first sleep voltage and a second sleep voltage;

a first operating voltage when transitioning from said first sleep voltage; and

a second operating voltage when transitioning from said second sleep voltage.

34. (New) A computer system as recited in Claim 33, wherein said circuitry is further configured to provide to said processing unit:

said first sleep voltage when transitioning from said first operating voltage; and

said second sleep voltage when transitioning from said second operating voltage.

35. (New) A computer system as recited in Claim 33 wherein a voltage difference between said first operating voltage and said first sleep voltage is approximately equal to a voltage difference between said second operating voltage and said second sleep voltage.

36. (New) A computer system as recited in Claim 33 wherein said first operating voltage is greater than said second operating voltage and wherein said first sleep voltage is greater than said second sleep voltage.

37. (New) A computer system as recited in Claim 36 wherein a voltage transition from said second sleep voltage to said first operating voltage is greater than a time allowed for transition from a sleep state to an operating state of said computer system.

REMARKS

The claims remaining in the present application are Claims 1-36. Claim 11 has been amended. Claims 19-37 have been added. No new matter has been added as a result of these amendments.

CLAIM REJECTIONS

35 U.S.C. §103

CLAIMS 1-3

Claims 1-3 are rejected under 35 U.S.C. §102(e) as being unpatentable over Orton et al., U.S. Patent No. 6,118,306 (hereinafter, Orton) in view of "AX64PRO OR AK72?," Newsreader, June 15, 2000 (hereinafter, Newsreader). The rejection is respectfully traversed for the following reasons.

Independent Claim 1 recites, in part:

> reducing core voltage to the processor to a value sufficient to maintain state during the mode in which system clock is disabled, wherein said value of the core voltage is not sufficient to maintain processing activity in said processor.

The cited combination does not teach or suggest these limitations. Orton may teach a mode in which the processor is not clocked, but Orton is nevertheless silent as to whether or not, in this mode, the processor would be capable of processing activity based on this mode's processor

voltage. Newsreader may disclose a deep-sleep function for a system having an AMD processor but is totally silent as to whether or not the processor is clocked in deep-sleep. In fact, relevant AMD specifications are clear that the processor used by Newsreader is clocked in all power management modes thereby implying that the Newsreader processor is clocked in deep-sleep. Regardless of whether or not the processor in Newsreader is clocked, like Orton, Newsreader is totally silent as to the processor's capability to perform processing activity while in the voltage level of its deep-sleep. Therefore, Newsreader, like Orton, does not teach or suggest the above claim limitations. These arguments are presented more fully below.

The rejection concedes that Orton fails to explicitly teach a method for reducing power used by a processor where the core voltage is set to a value that is not sufficient to maintain processing activity in said processor (when at a reduced voltage that is sufficient to maintain state). Applicants agree and respectfully assert that Orton fails to suggest these limitations.

Applicants respectfully assert that Newsreader fails to remedy these deficiencies in Orton in that Newsreader fails to teach or suggest the claim limitations missing in Orton. The rejection asserts that what is missing from Orton's teaching is reducing the processor core voltage to one Volt or less during deep sleep mode. Applicants respectfully disagree. Applicants

respectfully assert that, at a minimum, what is missing from Orton's teaching, among other things, is the claim limitation of "wherein said value of the core voltage is not sufficient to maintain processing activity in said processor."

Newsreader may disclose reducing core voltage to one Volt during a "deep sleep" function of a KineitiZ 7T mainboard, which Newsreader asserts is used with AMD Socket A Athlon™ processors. However, the deep sleep function is not described in any detail within Newsreader. Newsreader is silent as to the clocking of the processor during the deep sleep function. However, AMD's own specifications of the relevant time period specify that AMD processors are to be clocked while in all power management modes (see below). This implies that the Newsreader article discloses processor clocking during the deep sleep function. Moreover, regardless of the processor clocking state, Newsreader nevertheless does not disclose whether the processor is *capable* of executing instructions or not when held at the deep-sleep voltage level. Therefore, Newsreader does not teach the claim limitations of the core voltage being not sufficient to maintain processing activity in the processor.

For the foregoing reasons, the cited combination does not teach or suggest the claim limitations of reducing core voltage to a value sufficient to maintain state but not sufficient to maintain processing activity.

Next, Applicants respectfully assert the art does not suggest combining Orton and Newsreader in such a fashion to arrive at the claimed invention. Newsreader asserts that the KineitiZ 7T mainboard has a "deep-sleep" function in which the voltage to the processor is 1.0 Volt. Newsreader asserts that the KineitiZ 7T mainboard is used with AMD Socket A Athlon™ processors. It is Applicants understanding, which is based on AMD specifications, that AMD Athlon™ processors at approximately that time (both Socket A and Slot A) were required to clock to the processor in all power management states, as discussed above (see e.g., page 14 of AMD Athlon™ processor module datasheet, Publication # 21016, Revision M, June 2000 (Slot A); and page 14 of AMD Athlon™ processor model 4 datasheet, Publication # 23792 Revision K, November 2001 (Socket A)).

However, Claim 1 recites that the system clock is disabled when the value of the core voltage is not sufficient to maintain processing activity in said processor. Thus, the art does not suggest combining Newsreader's teaching of reducing processor voltage to 1.0 Volt (while clocking the processor because an AMD processor is required) with Orton's teaching of disabling the clock. Therefore, the art does not suggest combining Orton and Newsreader in such a fashion to arrive at the claimed invention. In fact, the cited art teaches away from the claimed combination.

Moreover, even if it is assumed that Orton's teaching is modified to drop the core voltage to Newsreader's 1.0 Volt, Applicants respectfully assert that the rejection has not established what would be the effect on the processor. For example, the rejection has not established what would be the effect of reducing the voltage to the processor in Orton (e.g., processor 12 in Figs. 1, 2, and 5) to any particular voltage during sleep mode. Applicants assert that it is understood that different processors have different operational characteristics. Therefore, Applicants do not understand the evidence in the record to establish that operating Orton's processor (12) at 1.0 Volt as being "not sufficient to maintain processing activity," as claimed.

For the foregoing reasons, the art does not suggest combining Orton and Newsreader in such a fashion to arrive at the claimed invention.

For all of the foregoing reasons, Claim 1 is neither taught nor suggested by Orton and Newsreader, alone or in combination. Therefore, Applicants respectfully request allowance of Claim 1.

Claims 2-3 depend from Claim 1, which is believed to be allowable for the foregoing reasons. As a result of their dependency, Claims 2-3 are believed to be allowable. Applicants earnestly request their allowance.

CLAIMS 4, 12 and 14-18

Claims 4, 12 and 14-18 are rejected under 35 U.S.C. §103(a) as being unpatentable over the combination of Orton and Applicant Admitted Prior Art (AAPA). The rejection is respectfully traversed for the following reasons.

CLAIM 4

Independent Claim 4 recites, in part:

> providing a feedback signal to the voltage regulator to reduce its output voltage below a specified output voltage (emphasis added).

Independent Claim 4 recites that a feedback signal is provided to the voltage regulator to reduce its output voltage below a specified output voltage. Applicants respectfully assert that neither Orton nor AAPA teach or suggest these claim limitations, alone or in combination.

The rejection concedes that Orton does not explicitly teach providing feedback to the voltage regulator. Applicants respectfully assert that Orton does not teach or suggest these limitations.

AAPA ("Maxim" specification, page 10) may teach how to raise the output voltage of the voltage regulator, but not to lower the output voltage, as claimed. Therefore, AAPA fails to teach or suggest the claim limitations.

For the foregoing reasons, Applicants assert that Independent Claim 4 is neither taught nor suggested by the combination of Orton and AAPA. Consequently, Applicants earnestly request that Claim 4 be allowed.

CLAIM 12

Independent Claim 12 recites, in part:

> means for reducing the selectable voltage below a level provided by the voltage regulator comprising:
>
> a voltage divider network joined between the output terminal and a voltage source furnishing a value higher than the selectable voltage, and
>
> the voltage regulator feedback circuit receiving a value from the voltage divider network (emphasis added).

Claim 12 recites that a voltage divider network is joined between the output terminal and a voltage source furnishing a value higher than the selectable voltage. The rejection concedes that Orton does not teach the voltage divider network. Therefore, Orton does not teach or suggest "a voltage divider network joined between the output terminal and a voltage source furnishing a value higher than the selectable voltage," as claimed.

Applicants respectfully assert that AAPA does not teach the claimed "voltage divider network joined between the output terminal and a voltage source furnishing a value *higher* than the selectable voltage."

For the foregoing reasons, Applicants assert that Independent Claim 12 is neither taught nor suggested by the combination of Orton and AAPA. Consequently, Applicants earnestly request that Claim 12 be allowed.

CLAIMS 14-18

Independent Claim 14 recites, in part:

> a voltage source furnishing a value higher than the selectable voltage; and
>
> a feedback circuit coupled to the voltage source, the output terminal, and the voltage regulator feedback circuit.

For reasons discussed in the response to Claim 12, Applicants assert that Independent Claim 14 is neither taught nor suggested by the combination of Orton and AAPA. Consequently, Applicants earnestly request that Claim 14 be allowed.

Claims 15-18 depend from Claims 4 and 14. By virtue of their dependency from a claim that is believed to be allowable, Applicants believe Claims 15-18 to be allowable.

35 U.S.C. §102

Claims 5-11 and 13 are rejected under 35 U.S.C. §102(a) or (e) as being anticipated by Orton. The rejection is respectfully traversed for the following reasons.

CLAIMS 5 and 6

Independent Claim 5 recites, in part:

> transferring operation of a voltage regulator furnishing core voltage in a mode in which power is dissipated during reductions in core voltage to a mode in which power is saved during a voltage transition when it is determined that a processor is transitioning from a computing mode to a mode is which system clock to the processor is disabled (emphasis added).

The underscored language refers to modes of operating the voltage regulator (power dissipation mode/power saving mode). The Applicants respectfully assert that Orton fails to teach or suggest the limitations of Claim 5. Orton may discuss reducing power consumption (see, e.g., col. 2, lines 18-20). Orton may achieve a reduction in power by, for example, reducing the operating frequency of the processor. However, power savings can be achieved in manners other than reducing frequency and/or reducing voltage. Applicants have specifically recited in this embodiment that saving power is performed by a choice of mode of operation of the voltage regulator. Orton is silent as to operating the voltage regulator in a mode in which power is dissipated to a mode in which power is saved, as claimed. Thus,

Orton fails to teach or suggest the claimed transferring the operation of a voltage regulator from a mode in which power is dissipated to a mode in which power is saved, during a voltage transition.

For the foregoing reasons, Orton fails to teach or suggest the limitations of Claim 5. Therefore, Applicants earnestly request allowance of Claim 5.

Claim 6 depends from Claim 5. By virtue of its dependency on a claim that is believed to be allowable, Applicants believe Claim 6 to be allowable.

CLAIMS 7-10

Independent Claim 7 recites, in part:

> means for providing signals at the input terminal of the voltage regulator for selecting a voltage for operating the processor in a computing mode and a voltage of a level less than that for operating the processor in a computing mode, wherein the level less than that for operating the processor in a computing mode is sufficient to maintain state of the processor (emphasis added).

For at least the reasons discussed in the response to Claim 1, Claim 7 is neither taught nor suggested by Orton. As such, Applicants earnestly request allowance of Claim 7.

Claims 8-10 depend from Claim 7. By virtue of their dependency from a claim that is believed to be allowable, Applicants believe Claims 8-10 to be allowable.

CLAIM 11

Currently Amended Independent Claim 11 recites, in part:

> a voltage regulator having:
>
> an output terminal providing a selectable voltage, and
>
> an input terminal for receiving signals indicating the selectable voltage level;
>
> ...
>
> means for reducing the selectable voltage below a lowest level the voltage regulator is specified to output (emphasis added).

Orton may describe causing the voltage regulator to output different voltages. However, Applicants respectfully assert that Orton is silent as to causing the voltage regulator to output a voltage below a lowest level the voltage regulator is specified to output, as claimed. Applicants respectfully assert that one of ordinary skill in the art would understand Orton to teach that the output voltage of the voltage regulator to be within a range specified by the voltage regulator, as Orton is silent as to causing the voltage regulator to output a voltage outside of that range.

For the foregoing reasons, Applicants respectfully assert that Orton fails to teach or suggest the limitations, "means for reducing the selectable

voltage below a lowest level the voltage regulator is specified to output." Therefore, Applicants earnestly request allowance of Claim 11.

CLAIM 13

Claim 13 recites, in part:

> a voltage regulator having:
>
> an output terminal providing a selectable voltage, and
>
> an input terminal for receiving signals indicating the selectable voltage level;
>
> ...
>
> circuitry for conserving charge stored by the voltage regulator when the selectable voltage decreases, and
>
> means for enabling the circuitry for conserving charge stored by the voltage regulator when the selectable voltage decreases (emphasis added).

Applicants respectfully assert that Orton fails to teach or suggest the limitations of Claim 13. The rejection asserts that Orton teaches a battery (60) as a charge storage unit. However, while a battery may be capable of storing charge, Applicants respectfully assert that Orton does not teach or suggest how charge from the voltage regulator is stored in the battery, as claimed. Moreover, Applicants respectfully assert that Orton fails to teach or suggest how charge from the voltage regulator is stored in the battery when the selectable voltage decreases, as claimed.

For the foregoing reasons, Orton fails to teach or suggest the limitations of Claim 13. Therefore, Applicants earnestly request allowance of Claim 13.

NEW CLAIMS

Claims 19-37 have been added. No new matter has been added as a result of these claim amendments.

New Independent Claim 19 recites, in part:

wherein said second transition time is within an allowed time for transitioning from a sleep state to an operating state; and

wherein said first transition time is greater than said allowed time

Applicants respectfully assert that the cited prior art fails to teach or suggest these limitations.

New Independent Claim 25 recites, in part:

> wherein a transition time for changing from said sleep voltage directly to said second operating voltage is greater than said allowed time for transitioning from said sleep state to said operating state.

Applicants respectfully assert that the cited prior art fails to teach or suggest these limitations.

New Independent Claim 29 recites, in part

> a first operating voltage that, based on a rate of transitioning from said sleep voltage to said first operating voltage, is not achievable from said sleep voltage within an allowed time for transitioning from a sleep state to an operating state.

Applicants respectfully assert that the cited prior art fails to teach or suggest these limitations.

New Independent Claim 33 recites, in part

> a first operating voltage when transitioning from said first sleep voltage; and
>
> a second operating voltage when transitioning from said second sleep voltage

Applicants respectfully assert that the cited prior art fails to teach or suggest these limitations.

Claims 20-24, 26-28, 30-32 and 34-37 depend from Claims 19, 25, 29, and 33, which are believed to be allowable for the foregoing reasons. Therefore, Claims 20-24, 26-28, 30-32 and 34-37 are believed to be allowable by virtue of this dependency.

CONCLUSION

In light of the above listed amendments and remarks, allowance of Claims 1-37 is requested.

Should the Examiner have a question regarding the instant amendment and response, the Applicants invite the Examiner to contact the Applicants' undersigned representative at the below listed telephone number.

Respectfully submitted,
WAGNER, MURABITO & HAO LLP

Dated: 3/22, 2005

Ronald M. Pomerenke
Registration No. 43,009

Address: WAGNER, MURABITO & HAO LLP
Two North Market Street
Third Floor
San Jose, California 95113

Telephone: (408) 938-9060 Voice
(408) 938-9069 FAX

Attorney Docket No.: TRAN-P059

$ 2185

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

I hereby certify that this transmittal of the below described document is being deposited with the United States Postal Service in an envelope bearing First Class Postage and addressed to the Commissioner for Patents P.O. Box 1450, Alexandria, VA 22313-1450, on the below date of deposit.					
Date of Deposit:	03/22/05	Name of Person Making the Deposit:	KATHERINE RINALDI	Signature of the Person Making the Deposit:	Katherine Rinaldi

In re Application of: Andrew Read, Sameer Halapete and Keith Klayman

Application No.: 09/694,433 Examiner: CAO, CHUN

Filed: 10/23/00 Art Unit: 2185

Confirmation No.: 3072

For: SAVING POWER WHEN IN OR TRANSITIONING TO A STATIC MODE OF A PROCESSOR (AS AMENDED)

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

AMENDMENT TRANSMITTAL

1. Transmitted herewith is an amendment for this application

X Transmitted herewith is a response to an office action for the above identified patent application. (29 sheets)

____ Transmitted herewith are ____ sheets of substitute formal drawings.

X IDS, Form 1449 and fee of $180.00

X References (5)

03/28/2005 MWOLDGE1 00000043 09694433

01 FC:1253 1020.00 OP
02 FC:1201 ~~360.00 OP~~
02 FC:1202 ~~850.00 OP~~

2. Applicant is other than a small entity

Extension of Term

3. The proceedings herein are for a patent application and the provisions of 37 C.F.R. 1.136 apply.

(a) [X] Applicant petitions for an extension of time under 37 C.F.R. 1.136 (fees: 37 C.F.R. 1.17(a)-(d) for the total number of months checked below:)

Extension	Fee
[ ] one month	$120.00
[ ] two months	$450.00
[X] three months	$1,020.00
[ ] four months	$1,590.00

Fee $ 1,020.00

If an additional extension of time is required, please consider this a petition therefor.

(b) [ ] Applicant believes that no extension of term is required. However, this conditional petition is being made to provide for the possibility that applicant has inadvertently overlooked the need for a petition for extension of time.

rev. 11/98 kgr

Fee Calculation

4. The fee for claims (37 C.F.R. 1.16(b)-(d)) has been calculated as shown below:

(for other than a small entity)					
Fee Items	Claims Remaining After Amendment	Highest Number of Claims Previously Paid For	Present Extra Claims	Fee Rate	Total
Total Claims	37	- 20 =	17	x $50.00	$850.00
Independent Claims	12	- 8 =	4	x $200.00	$800.00
Multiple Dependent Claim Fee (one or more, first added by this amendment)				$300.00	$0.00
Total Fees					$1,450.00

PAYMENT OF FEES

5. The full fee due in connection with this communication is provided as follows:

[x] The Commissioner is hereby authorized to charge any additional fees associated with this communication or credit any overpayment to Deposit Account No.: 23-0085. A duplicate copy of this authorization is enclosed.

[x] A check in the amount of $2,850.00

[ ] Charge any fees required or credit any overpayments associated with this filing to Deposit Account No.: 23-0085.

Please direct all correspondence concerning the above-identified application to the following address:

WAGNER, MURABITO & HAO LLP
Two North Market Street, Third Floor
San Jose, California 95113
(408) 938-9060
Confirmation No.: 45590

Respectfully submitted,

Date: 3/22/05

By: Ronald M. Pomerenke
Ronald M. Pomerenke
Reg. No. 43,009

rev. 11/98 kgr

Attorney Docket No.: TRAN-P059

$ 210

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

I hereby certify that this transmittal of the below described document is being deposited with the United States Postal Service in an envelope bearing First Class Postage and addressed to the Commissioner for Patents P.O. Box 1450, Alexandria, VA 22313-1450, on the below date of deposit.					
Date of Deposit:	03/22/05	Name of Person Making the Deposit:	KATHERINE RINALDI	Signature of the Person Making the Deposit:	Katherine Rinaldi

In re Application of: Andrew Read, Sameer Halapete and Keith Klayman

Application No.: 09/694,433 Examiner: CAO, CHUN

Filed: 10/23/00 Art Unit: 2185

Confirmation No.: 3072

For: SAVING POWER WHEN IN OR TRANSITIONING TO A STATIC MODE OF A PROCESSOR (AS AMENDED)

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

AMENDMENT TRANSMITTAL

1. Transmitted herewith is an amendment for this application

X Transmitted herewith is a response to an office action for the above identified patent application. (29 sheets)

____ Transmitted herewith are ____ sheets of substitute formal drawings.

X IDS, Form 1449 and fee of $180.00

X References (5)

03/28/2005 MWOLDGE1 00000043 09694433

01 FC:1253 1020.00 OP

02 FC:1201 ~~360.00 OP~~

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Extension	Fee
[ ] one month	$120.00
[ ] two months	$450.00
[X] three months	$1,020.00
[ ] four months	$1,590.00

Fee $ 1,020.00

If an additional extension of time is required, please consider this a petition therefor.

(b) [ ] Applicant believes that no extension of term is required. However, this conditional petition is being made to provide for the possibility that applicant has inadvertently overlooked the need for a petition for extension of time.

rev. 11/98 kgr

Fee Calculation

4. The fee for claims (37 C.F.R. 1.16(b)-(d)) has been calculated as shown below:

(for other than a small entity)					
Fee Items	Claims Remaining After Amendment	Highest Number of Claims Previously Paid For	Present Extra Claims	Fee Rate	Total
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Independent Claims	12	- 8 =	4	x $200.00	$800.00
Multiple Dependent Claim Fee (one or more, first added by this amendment)				$300.00	$0.00
Total Fees					$1,450.00

PAYMENT OF FEES

5. The full fee due in connection with this communication is provided as follows:

[x] The Commissioner is hereby authorized to charge any additional fees associated with this communication or credit any overpayment to Deposit Account No.: 23-0085. A duplicate copy of this authorization is enclosed.

[x] A check in the amount of $2,850.00

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Respectfully submitted,

Date: 3/22/05

By: Ronald M. Pomerenke
Ronald M. Pomerenke
Reg. No. 43,009

rev. 11/98 kgr

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Attorney Docket No.: TRAN-P059

Inventor(s): Andrew Read, Sameer Halapete, Keith Klayman

Application No.: 09/694,433 Group Art Unit: 2185

Filed: 10/23/00 Examiner: CAO, Chun

Title: SAVING POWER WHEN IN OR ON TRANSITIONING TO A STATIC MODE OF A PROCESSOR (AS AMENDED)

Commissioner of Patents
P. O. Box 1450
Alexandria, VA 22313-1450

Sir:

Information Disclosure Statement Submitted Pursuant to 37 C.F.R. 1.97(c)

The citations referenced herein, copies attached, may be material to the examination of the above-identified application and are, therefore, submitted in compliance with the duty of disclosure as defined in 37 C.F.R. 1.56. The Examiner is requested to make these citations of official record in the application.

This Information Disclosure Statement submitted in accordance with 37 C.F.R. 1.97(c) is not to be construed as a representation that a search has been made, that additional items material to the examination of this application do not exist, or that any one or more of these citations constitute prior art under 35 U.S.C. 102.

The Examiner's attention is respectfully directed to the following U.S. Patents:

Pat. No.	Pat. Title	Grant Date
6,704,880	REDUCING SLEEP MODE SUBTHRESHOLD LEAKAGE IN A BATTERY POWERED DEVICE BY MAKING LOW SUPPLY VOLTAGE LESS THAN TWICE THE THRESHOLD VOLTAGE OF ONE DEVICE TRANSISTOR	03/09/04
6,675,304	SYSTEM FOR TRANSITIONING A PROCESSOR FROM A HIGHER TO A LOWER ACTIVITY STATE BY SWITCHING IN AND OUT OF AN IMPEDANCE ON THE VOLTAGE REGULATOR	01/06/04
5,852,737	METHOD AND APPARATUS FOR OPERATING DIGITAL STATIC CMOS COMPONENTS IN A VERY LOW VOLTAGE MODE DURING POWER-DOWN	12/22/98
6,425,086	METHOD AND APPARATUS FOR DYNAMIC POWER CCONTROL OF A LOW POWER PROCESSOR	07/23/02
5,440,520	INTEGRATED CIRCUIT DEVICE THAT SELECTS ITS OWN SUPPLY VOLTAGE BY CONTROLLING A POWER SUPPLY	08/08/95
5,727,208	METHOD AND APPARATUS FOR CONFIGURATION OF A PROCESSOR OPERATING PARAMETERS	03/10/98
6,484,265	SOFTWARE CONTROL OF TRANSISTOR BODY BIAS IN CONTROLLING CHIP PARAMETERS	11/19/02
5,787,294	SYSTEM FOR REDUCING THE POWER CONSUMPTION OF A COMPUTER SYSTEM AND METHOD THEREFOR	07/28/98
5,142,684	POWER CONSERVATION IN MICROPORCESSOR CONTROLLED DEVICES	08/25/92

Foreign Patent or Published Foreign Patent Application

Document No.	Publication Date	Country or Patent Office	Class	Sub-class	Translation Yes	Translation No
EP0978781	02/09/00	EPO	G06F	1/32	X	
EP0632360	01/04/95	EPO	G06F	1/32	X	

03/28/2005 MWOLDGE1 00000043 09694433

04 FC:1806 180.00 OP

rev. 6/97 jpw

US. Published Patent Applications

Pub. No.	Date	Applicant	Class	Sub-class	Publication Date
2002/0087896	07/04/02	Cline et al.	713	300	12/29/00

The Examiner's attention is respectfully directed to the following Documents:

"AMD ATHLON- PROCESSOR MODEL 4 DATA SHEET", No. 23792, Rev. K, November 2001, Advanced Micro Devices, Inc.

"MANUAL FOR KINETIZ 7T", 2000, QDI Computer, Inc. (USA)

"VT82C686A 'SUPER SOUTH' SOUTH BRIDGE", 02/25/00, Rev. 1.54, VIA Technologies, Inc.

Please direct all correspondence concerning the above-identified application to the following address:

WAGNER, MURABITO & HAO LLP
Two North Market Street, Third Floor
San Jose, California 95113
(408) 938-9060
Customer No: 000041066

Respectfully submitted,

Date: 3/22/05

By: Ronald M Pomerenke
Ronald M. Pomerenke
Reg. No. 43,009

rev. 6/97 jpw

Attorney Docket No.: TRAN-P059

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Patent Application

Inventor(s): Andrew Read, Sameer Halapete, Keith Klayman

Application No.: 09/694,433 Group Art Unit: 2185

Filed: 10/23/00 Examiner: CAO, Chun

Title: SAVING POWER WHEN IN OR ON TRANSITIONING TO A STATIC MODE OF A PROCESSOR (AS AMENDED)

Form 1449

U.S. Patent Documents

Examiner Initial	No.	Patent No.	Date	Patentee	Class	Sub-class	Filing Date
	A	6,704,880	03/09/04	Dai et al.	713	323	10/18/01
	B	6,675,304	01/06/04	Pole, II et al.	713	322	11/29/99
	C	5,852,737	12/22/98	Bikowsky	395	750.05	12/31/96
	D	6,425,086	07/23/02	Clark et al.	713	322	04/30/99
	E	5,440,520	08/08/95	Schutz et al.	365	226	09/16/94
	F	5,727,208	03/10/98	Brown	395	653	07/03/95
	G	6,484,265	11/19/02	Borkar et al.	713	324	12/30/98
	H	5,787,294	07/28/98	Evoy	395	750.03	10/13/95
	I	5,142,684	08/25/92	Perry et al.	395	750	06/23/89

Foreign Patent or Published Foreign Patent Application

Examiner Initial	No.	Document No.	Publication Date	Country or Patent Office	Class	Sub-class	Translation Yes	Translation No
	J	EPO978781	02/09/00	EPO	G06F	1/32	X	
	K	EPO632360	01/04/95	EPO	G06F	1/32	X	

US. Published Patent Applications

Examiner Initial	No.	Pub. No.	Date	Applicant	Class	Sub-class	Publication Date
	L	2002/0087896	07/04/02	Cline et al.	713	300	12/29/00

Other Documents

Examiner Initial	No.	Author, Title, Date, Place (e.g. Journal) of Publication
	M	AMD ATHLON- PROCESSOR MODEL 4 DATA SHEET", No. 23792, Rev. K, November 2001, Advanced Micro Devices, Inc.
	N	"MANUAL FOR KINETIZ 7T", 2000, QDI Computer, Inc. (USA)
	O	"VT82C686A 'SUPER SOUTH' SOUTH BRIDGE", 02/25/00, Rev. 1.54, VIA Technologies, Inc.

Examiner	Date Considered

Examiner: Initial citation considered. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

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(84) Designated Contracting States:
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(71) Applicant: **XEROX CORPORATION**
Xerox Square
Rochester
New York 14644 (US)

(72) Inventor: **Weiser, Mark D.**
1144 Greenwood Avenue
Palo Alto,
California 94301 (US)
Inventor: **Wood, David A.**
2115 Bascom Street
Madison,
Wisconsin 53705 (US)
Inventor: **Demers, Alan J.**
720 Hopkins Gulch
Boulder Creek,
California 95006 (US)
Inventor: **Atkinson, Russell R.**
3223 Redwood Drive
Aptos,
California 95003 (US)

(74) Representative: **Reynolds, Julian David et al**
Rank Xerox Ltd
Patent Department
Parkway
Marlow
Buckinghamshire SL7 1YL (GB)

(54) Reducing computer power consumption by dynamic voltage and frequency variation.

(57) A method for dynamically varying the power consumption of computer circuits (20) under program control. A power control subsystem (22) determines the minimum required level of power (52;Fig. 2) based on a number of factors (Fig. 3) including the particular operation and the recent amount of idle time of the circuit. Voltage (42) and clock speed (38) are determined for the circuit (20) to provide the minimum level of power. The system (22) for controlling the power consumption of the computer circuit (20) comprises a power control subsystem (22) for determining the power level (24), a sequencer (26) for controlling the change in voltage and clock speed, a variable voltage source (40), and a variable clock source (36).

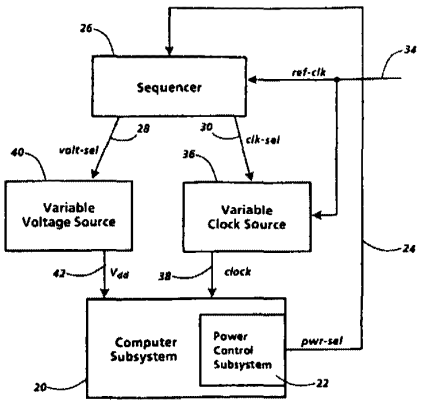

Fig. 1

EP 0 632 360 A1

The present invention relates to the reduction of power consumption in computers. More specifically, the invention relates to techniques for reducing the power consumption in computers by dynamically varying the voltage and frequency of computer systems under program control.

In computer systems, and especially in portable computer systems, power consumption is an important consideration. Conservation of power extends the period of time that portable computing devices are able to operate effectively from an internal battery when the computer is disconnected from an external power source. Among users of the portable computers there is a need for the same or more computational capability as found in desktop machines placed in a low-power environment.

Power dissipation in "well-designed" CMOS circuits is dominated by the switching component, which may be approximated by the formula

$$P = fC{*}V_{dd}^2,$$

where f is the clock frequency, C is the average effective capacitance being switched at each clock cycle, and V_{dd} is the supply voltage. Thus, the task of reducing power needs becomes that of minimizing f , C, and V_{dd}, while retaining the required functionality. Since the maximum frequency decreases in roughly linear proportion to V_{dd}, it can be approximated it by the formula

$$f = k{*}V_{dd},$$

where k is a constant factor. Thus, lowering the voltage from 5 volts to 2 volts, by a factor of 2.5, offers a possible fifteen fold reduction in power ($2.5{*}5^2/2^2$) while similarly slowing the maximum operating frequency of the computer by only a factor of about two and a half. Many integrated circuit (IC) manufacturers sell chips that operate over a range of supply voltages. In some cases, chips have simply been recharacterized, and work unchanged for different voltage modes. Some systems achieve a reduction in power consumption by running at a constant lower voltage However, running at a continuously lowered voltage can result in poorer performance, which may be unacceptable to the user.

Other low power computer systems vary their clock rate to conserve power. Varying the clock rate alone gives a linear decrease in power usage. For static ICs that can actually stop their clock altogether when they are not busy, however, there is little advantage in slowing the clock over simply running the clock as fast as possible when there is work, and stopping it completely when there is no work.

US-A-5,167,024 describes a power management method for a portable computer which controls various units within the computer through transistor switches which control the distribution of power by deactivating clock signals to the various units within the computer when they are not in use, removing the supply voltage from a device until usage is requested, or decreasing the frequency of clock signals for a "slow mode", providing a 25-30% power saving.

Some applications require real-time operation. Radio modem, speech and video compression, and speech recognition operations may require computation at near-peak rates. However, once the real-time requirements of the applications are met, there may be no real advantage in increasing the computational throughput.

It is an object of the invention to reduce the power consumption in a computer system by dynamically reducing both voltage and clock speed without significantly affecting the user's perception of performance.

It is a further object of the Invention to reduce power consumption by dynamically reducing voltage and clock speed to a computer system or portions of a computer system under program control.

The present invention describes a method for reducing the power consumption of an electrical circuit by determining a task to be performed, determining the lowest level of power needed to perform the task, and determining the voltage and clock speed necessary to run at that power level. The clock speed and supply voltage are set to the determined levels and the task is performed.

The method may further be performed by determining the lowest acceptable voltage for the task to be performed and the clock speed necessary to run at that voltage, or by determining the minimum clock speed needed to complete the task and the voltage needed to support that clock speed. The clock speed and supply voltage are set to the determined levels and the task is performed.

The invention further provides a method for dynamically adjusting the power consumption of an electrical circuit for performing a second task, the circuit comprising a supply voltage source and a clock source and set at a first power level for performing a first task, the method comprising: determining the second task to be performed by the electrical circuit; determining a second power level necessary to perform the second task; determining a change in voltage to provide the determined second power level; determining a change in clock speed to provide the determined second power level; changing the supply voltage to the electrical circuit according to said determined change in voltage; changing the clock source according to said determined change in clock speed; and performing the second task.

In another aspect of the invention, a method for determining the power level is performed by determining the amount of recent idle time in the circuit. The power level is chosen based on the amount of recent idle time, and voltage and clock speed are adjusted to provide that power level to perform the task.

In the present system, power consumption is reduced by dynamically varying the voltage under program control. An IC or computer subsystem running at a lower voltage also requires a lower clock rate, since it cannot switch as quickly The operating system software of the computer determines the appropriate power level for the task being run at a given time, lowering the voltage and clock speed for tasks that can take longer to run.

Running the whole computer at a low voltage or speed all the time has the problem that it may not be fast enough for some tasks. Dynamically varying the voltage and speed under operating system control means the CPU can be fast when needed and power conservative at other times, depending on the task to be performed.

Embodiments of the invention will now be described, by way of example, with reference to the accompanying drawings, in which:

Fig. 1 shows a block diagram of the system of the invention;

Fig. 2 describes a general method for performing power level selection for the system of Fig. 1;

Fig 3 describes a method for determining necessary power requirements;

Fig. 4 describes the timing implemented in the sequencer;

Fig. 5 shows a block diagram of the sequencer of Fig. 1;

Fig. 6 shows a more detailed block diagram of the delay circuit for the sequencer of Fig. 5;

Fig. 7 shows a block diagram of the variable clock source of the system of Fig. 1; and

Fig. 8 shows a block diagram of the variable voltage source of the system of Fig. 1.

Fig. 1 shows a block diagram for general system 10. The system is based on a general computer system 20. For the purposes of the description here, computer system 20 may be an integrated circuit (IC), a computer board, some subsystem, or a computer itself. Further, in a computer there may be several of these systems, each controlling different parts of a system

A portion of computer system 20 comprises a power control subsystem 22, which performs calculations to determine the power level needed to run an operation of computer system 20 This desired power level is provided to sequencer 26 by a power select signal *pwr−sel* 24. Although for illustrative purposes *pwr−sel* 24 is shown and described in this figure in terms of a single signal, it will be obvious that *pwr−sel* could be a number of lines *n* describing a desired power level.

Sequencer 26 selects the clock speeds and voltage values that achieve the desired power level. The voltage is required at all times to be greater than or equal to the minimum voltage for the current clock speed. Thus, if the clock speed is being reduced, the voltage must be lowered later than the clock, but if the clock speed is being increased, the voltage needs to be raised in advance of the clock.

Variable clock source 36 is provided with a reference frequency *ref−clk* signal 34. This clock may come from the computer or a dedicated or external source. *clk−sel* signal 30 provides the desired clock speed to variable clock source 36. Although for illustrative purposes *clk−sel* signal 30 is shown and described in this figure in terms of a single signal, it will be obvious that *clk−sel* could be a number of signals *m* describing a desired clock speed. The output of variable clock source 36, *clock* signal 38, is provided to computer system 20 to perform the desired operation.

Variable voltage source 40 is provided a voltage select *volt−sel* signal 28 Although for illustrative purposes *volt−sel* signal 30 is shown and described in this figure in terms of a single signal, it will be obvious that *volt−sel* could be a number of signals *p* describing a desired voltage level. The selected voltage V_{dd} 42 is provided to computer system 20 to perform the desired operation.

Fig. 2 describes a general overview of the present method for performing power level selection for system 10. These steps may be performed by a combination of the subsystems of system 10.

The step in box 50 finds the operation or task to be performed. The step in box 52 determines the minimum power requirements to perform the operation at an acceptable performance level. There are many ways by which a lower power consumption rate might be chosen. Some tasks may be labeled "background" or not time critical. A mail delivery process, for example, must eventually complete, but it can afford to take longer without significantly affecting the user's perception of the performance of the machine. Some tasks have a scheduled time to complete, and have a very predictable performance. Such a task might have the clock slowed so that the task completes exactly on time, within its margin of performance prediction, and no sooner. The appropriate voltage would be derived from the calculated clock value. Tasks may be relabeled with different priorities, with the voltage and clock rate determined based on their priority User interactive tasks might have a high priority, work that requires less interaction a medium priority, and work that is permitted to go slowly a background priority.

Voltage could also be lowered in a portable computer when the battery life is low, thus permitting a user to continue useful work but at a reduced speed. This might be an acceptable tradeoff for a user who could otherwise do nothing at all Or the user might be given control over the tasks, for instance, by having a "speed bar" on each window which could be varied by the user to control the speed of activities of the tasks in that window, so that activities that are allowed to run more slowly will consume less power.

For each chip or subsystem, the minimum and maximum voltages at which the chip will run must be characterized, and an appropriate clock level for each voltage chosen. Some chips which have already been characterized by their manufacturer from 3.3V to 5V, for example, may have a clock speed specified for each of 3.3V and 5V, but not for voltages in between. These values could be determined experimentally, or experimentation may be reduced by choosing a conservative clock speed.

The step in box 54 determines if the new power requirement is a decreased level from the previous power level If so, the step in box 56 initiates a reduction in the clock speed, and the step in box 58, after a delay period, initiates a decrease in the voltage. Note that this delay can be omitted for some circuits. Then the step in box 66 initiates the operation. In the figure, the reduction in clock speed and voltage are initiated, but may not complete before the operation itself is initiated. The operation may also be initiated before both steps 56 and 58 have been performed. Thus the clock and voltage adjustment may be performed in parallel with the operation. The operation may run slower later in its process than at the beginning due to this slowdown. In systems or operations where this may cause timing problems, the operation may not be initiated until a sufficient time has passed for the clock and voltage to reach the desired level.

If the new power requirement is not a decrease from the previous level, the step in box 60 checks for an increase in power required. If no increase is required, the operation simply begins in the step in box 66. If an increase in power is necessary, the step in box 62 initiates an increase in the voltage. After a delay period sufficient for the voltage increase to have taken effect throughout the computer system, the step in box 64 initiates an increase in the clock speed. The operation is initiated in the step in box 66. Again, the increase in voltage and clock speed are initiated, but may not complete before the operation itself is initiated, and the operation may be performed in parallel with the voltage and clock speed increase. In systems or operations where increasing the speed of the operation during its performance may cause timing problems, the operation may not be initiated until a sufficient time has passed for the clock and voltage to reach the desired level.

The flowchart of Fig 3 describes an example method that could be used to determine the necessary power requirements as described in step 52. It is essentially a test for a number of conditions. Other conditions could easily be added. This code may be simply added to an operating system since it does not interfere with the task scheduling activity and it can be executed quickly. In the step in box 70, the operating system scheduler chooses the next job or task to run. The step in box 72 determines the priority of the task. If it is a low priority task, the minimum clock speed may be chosen by the step in box 88.

If the current task is not low priority, the step in box 74 determines if there has been a large proportion of idle time recently For example, if the system is running so fast that it completes all it operations and still has a great deal of idle time, then perhaps the system might be run slower and at a lower voltage, in order to optimize the power consumption. This proportion may be set by the user or the system designer, and may vary according to the perceived speed and/or operational needs of the system.

If there has been a lot of recent idle time, the step in box 80 determines if screen or keyboard I/O operations are necessary for this task. To perform screen or keyboard I/O operations, the step in box 86 may set the clock to the maximum clock speed, and correspondingly set the voltage level to the maximum voltage. If there are no screen or keyboard I/O operations in the current task, however, the step in box 84 will reduce the clock speed and the voltage. This should reduce the amount of idle time while reducing the power consumption.

In most instances, the voltage and clock speed should be lowered if there is too much idle time. Checking for a screen or I/O operation is shown in the method above to be an exception to lowering the clock speed, since these operations generally require a faster or maximum speed. However, in some systems it may be necessary to always increase the clock speed to the maximum for screen or keyboard or other I/O operations, rather than just when there has been recent idle time, to prevent effects on the performance of the system. This would require the test in box 80 to be performed earlier, perhaps before the steps in boxes 74 or 72.

If there has not been a great deal of recent idle time, the step in box 76 determines if there has been no recent idle time For example, if the system is running at such a slow speed that it is

running constantly, the performance of the system may suffer. If there has been no recent idle time, the step in box 82 increases the clock to a faster clock speed, with a corresponding increase in voltage If there has been some recent idle time, the step in box 78 determines that no change is needed in the clock speed and it remains at the current settings. The scheduler in the operating system is returned control in the step in box 90.

The average desired amount of idle time to provide the optimum power consumption and performance may be tuned to the particular system to allow the system to run as slowly as possible without significantly detrimentally affecting the user's perception of system performance. The steps in Fig. 3 may further be repeated during the operation of the task, adjusting the voltage and clock speed iteratively throughout the operation based on the amount of idle time during operation. This works particularly for tasks in which the parameters of the task are fairly stationary throughout operation.

Fig. 4 describes the timing implemented in system 10 by sequencer 26. For example, when the *pwr−sel* line indicates an increase in power, the *volt−sel* line goes up t_1 later. The clock speed should not be raised until the voltage has reached a suitable level to support that clock speed, so *clk−sel* is delayed t_2. When power is reduced, *clk−sel* is reduced at t_3 after *pwr−sel* is reduced. Since the voltage should not be reduced until the clock is slow enough to support a lower voltage, *volt−sel* is delayed to t_4 later. Note that t_2 is likely to be much longer than t_1, t_3, and t_4. The delay values may be derived by experimentation, since manufacturers do not currently anticipate dynamically varying the voltage supply or specify such delays for chips. However, experimentation may be reduced by choosing a conservative value, say one millisecond, for the delay

Figs. 5-8 describe block diagrams of circuits that may be used to create system 10 as shown in Fig. 1. For clarity, the circuitry is described herein in terms of two selectable clock speeds and two selectable voltage levels. However, it will be clear to one skilled in the art that the circuitry may be expanded to provide a greater number of both clock speeds and voltage levels.

A block diagram of sequencer 26 is shown in Fig 5. The signal *pwr−sel* is input to a delay circuit 100 which is clocked by the *ref−clk* line 34 The delayed output is input to a multiplexer 104. *ref−clk* 34 is inverted and input to a D-flipflop 108 which is triggered by the *pwr−sel* line 24. The output of the flipflop is a delayed *pwr−sel−delay*, which is input to the multiplexer This delayed power signal is triggered on the opposite clock edge from the delay units, so that the *clk−sel* line does not cause a glitch on the *clock* output line.

pwr−sel signal 24 is inverted and input into a second delay 102, the inverted output of which is input to a second multiplexer 106. The output of multiplexer 104 provides the clk-sel signal 30, and the output of multiplexer 106 provides the volt-sel signal 28.

Fig. 6 describes delay circuit 100 or 102 of Fig. 5. The input (In) is coupled with the reference clock input (clk) at AND gate 118 A positive output from gate 118 begins a counter 120. The output of counter 120 is compared by comparator 122 with a fixed delay 128. When the counter has reached the delay value, the comparator output signal is ORed (at gate 124) with the output of flipflop 126, and the result is input to flipflop 126. Both the counter 120 and the flipflop 126 may be cleared by the reset line (Reset).

For more than one *pwr−sel* line, delay circuit 100 may further have a decoder before gate 118.

Fig. 7 shows a block diagram of a circuit that may be used for variable clock source 36. The signal *ref−clk*, which runs at the maximum clock speed of the system, is provided to a programmable frequency divider In this case, the frequency divider comprises a flipflop 140, which divides the clock source ref-clk, and a multiplexer 142 which isolates the frequency selected by *clk−sel*. There may be more than one *clk−sel* line 30 and a plurality of clock frequencies, and it will be obvious that the clock source must be designed so as to avoid introducing glitches on the clock output.

Fig. 8 shows a block diagram of a circuit that may be used for variable voltage source 40. *volt−sel* line 28 is input to the voltage source circuitry. *volt−sel* may comprise several signals for indicating a desired voltage level, and may be input to a decoder. The appropriate lines of transistors in the feedback amplifier 147 are energized by *volt−sel* to produce output V_{dd}. The voltage source 40 may also require a low-pass filter so that the voltage changes gradually across the subsystem This filter value may be determined experimentally for a system Experimentation may be reduced by adding a relatively large filter, which will cause the voltage to take longer to change.

Varying the clock to subsystems or ICs in a computer may mean that the CPU will either need to buffer its data for delivery for a different external clock rate, or entire systems will need to change the clock rate to match the CPU Multiple different clock rates within a computer system are not uncommon, and there are standard methods of moving data among parts of the system using different clocks. In this case the problem may be simplified, since the slowed CPU clock could still be synchronized with other clocks, running at an integral multiple or traction of the base rate. Performance en-

hancements, such as parallel processing circuitry or pipelining circuitry, may increase the performance of the system, and may be used in conjunction with the present invention.

Claims

1. A method for dynamically adjusting the power consumption of an electrical circuit (20), the circuit comprising a supply voltage source (40) and a clock source (36), the method comprising:
   determining (50) a task to be performed by the electrical circuit (20);
   determining (52) the required level of power to perform the task;
   determining a change in voltage to provide the determined level of power;
   determining a change in clock speed to provide the determined level of power;
   changing (62,58) the supply voltage to the electrical circuit according to said determined change in voltage;
   changing (64,56) the clock source according to said determined change in clock speed.

2. The method of claim 1, wherein (1) said step of determining a change in voltage (62) is performed before said step of determining a change in clock speed (64), or (2) said step of determining a change in clock speed (56) is performed before said step of determining a change in voltage (58).

3. The method of claim 1, further including the step of commencing performance of said task before completion of said supply voltage changing and said clock source changing steps.

4. A method for reducing the power consumption of an electrical circuit (20), comprising:
   determining (50) a task to be performed;
   determining (52) a lowest acceptable voltage for the task to be performed;
   determining (78-88) a clock speed of the circuit at said determined voltage;
   setting (56) the clock of said electrical circuit to said determined clock speed;
   setting (58) the supply voltage of said electrical circuit to said determined voltage.

5. The method of claim 5, wherein (1) if said determined voltage is less than an immediately previous voltage, said step of setting the clock is done before said step of setting the supply voltage, and (2)
   if said determined voltage is greater that an immediately previous voltage, said step of setting the supply voltage is done before said step of setting the clock.

6. A method for reducing the power consumption of an electrical circuit, comprising:
   determining (50) a task to be performed;
   determining (52) a lowest acceptable clock speed for the task to be performed;
   determining a voltage of the circuit for said determined clock speed;
   setting (56) the clock of said electrical circuit to said determined clock speed;
   setting (58) the supply voltage of said electrical circuit to said determined voltage.

7. A method for dynamically adjusting the power consumption of an electrical circuit (20) for performing a second task, the circuit comprising a supply voltage source (40) and a clock source (36) and set at a first power level for performing a first task, the method comprising:
   determining (50) the second task to be performed by the electrical circuit;
   determining (52) a second power level necessary to perform the second task;
   determining a change in voltage to provide the determined second power level;
   determining a change in clock speed to provide the determined second power level;
   changing (62) the supply voltage to the electrical circuit according to said determined change in voltage;
   changing (64) the clock source according to said determined change in clock speed.

8. The method of claim 9, wherein (1) if said determined change in voltage is negative, said step of changing the clock source is performed before said step of changing the supply voltage, and (2) if said determined change in voltage is positive, said step of changing the supply voltage is done before said step of changing the clock source.

9. A method for dynamically adjusting the power consumption of an electrical circuit (20), the circuit comprising a supply voltage source (40) and a clock source (36), the method comprising:
   determining a task to be performed by the electrical circuit;
   determining the amount of recent idle time of said circuit;
   determining a level of power for said task based on said amount of recent idle time;
   determining a change in voltage to provide said determined level of power;

determining a change in clock speed to provide said determined level of power;

changing the supply voltage to the electrical circuit according to said determined change in voltage;

changing the clock source according to said determined change in clock speed.

10. The method of claim 9, wherein the step of determining a level of power for said task is further based upon the priority of said task, and/or wherein the steps of determining the amount of recent idle time of said circuit, determining a level of power, determining a change in voltage, determining a change in clock speed, changing the supply voltage, and changing the clock source are performed repeatedly during operation of said task.

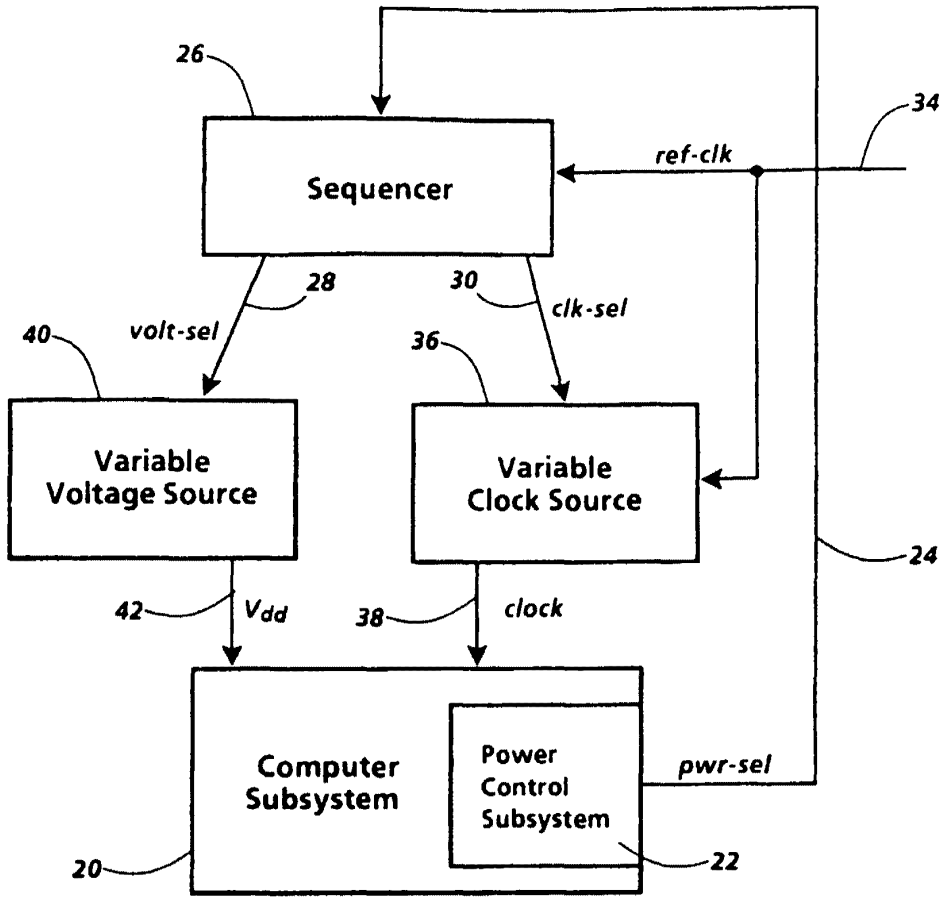

Fig. 1

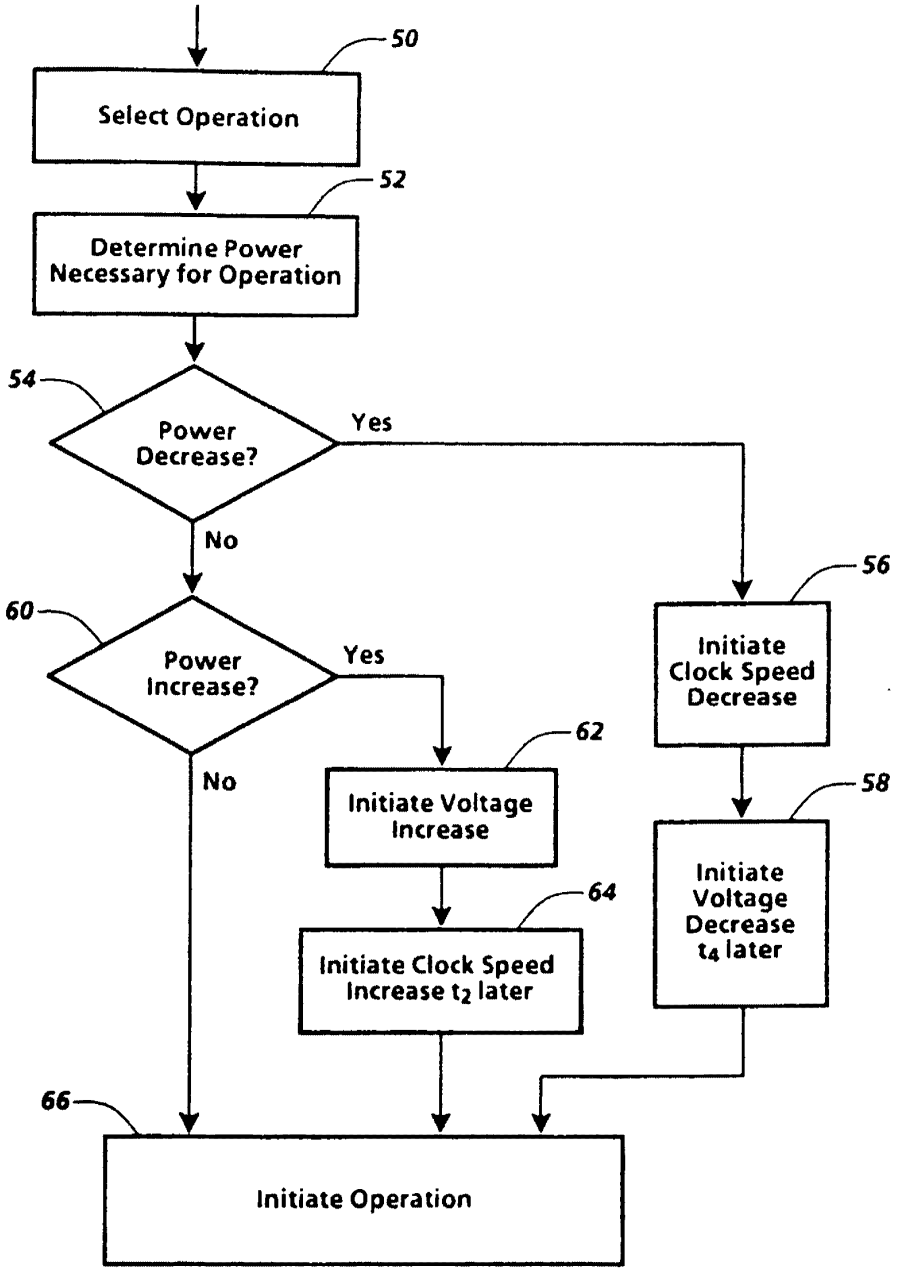

Fig. 2

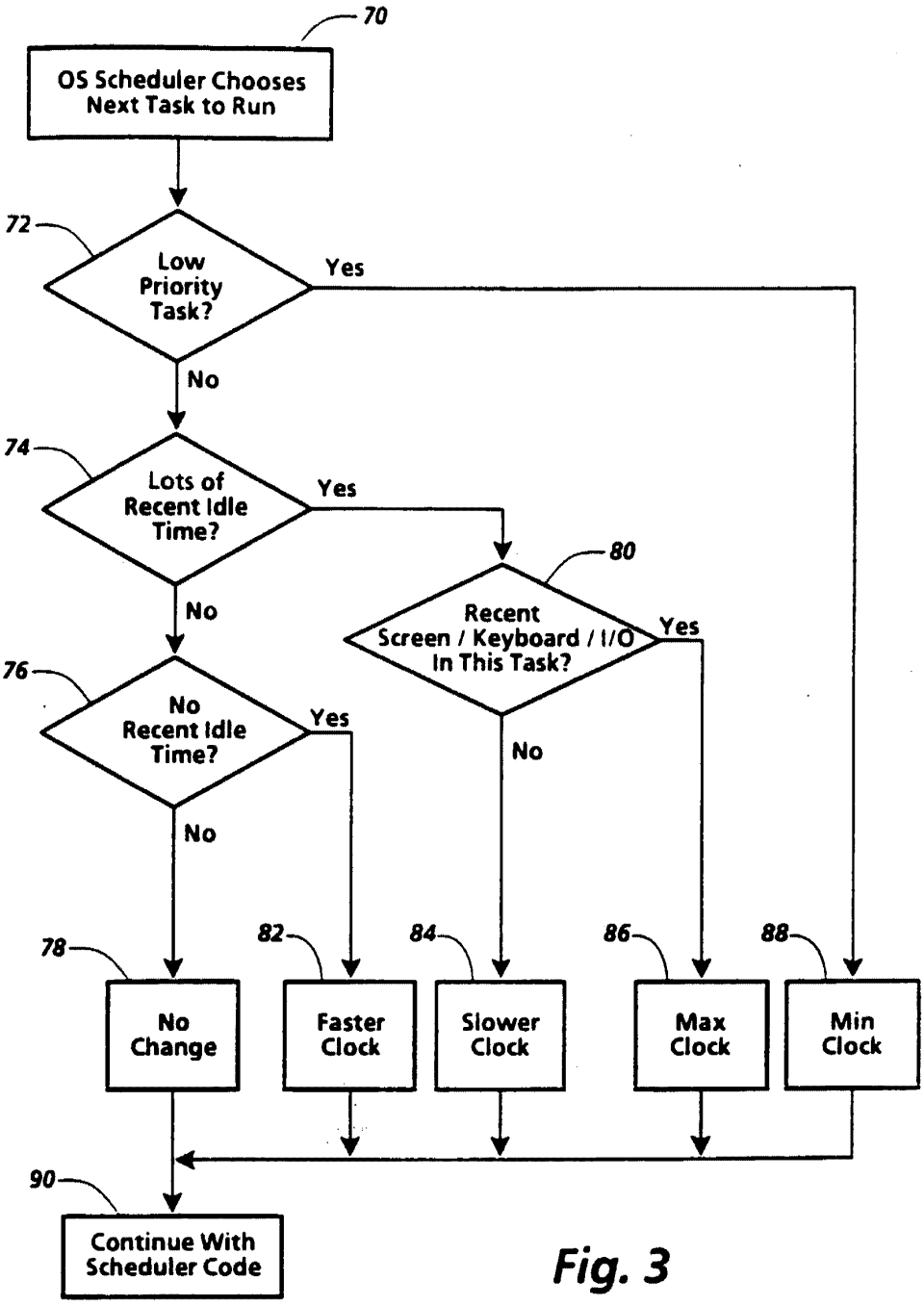

Fig. 3

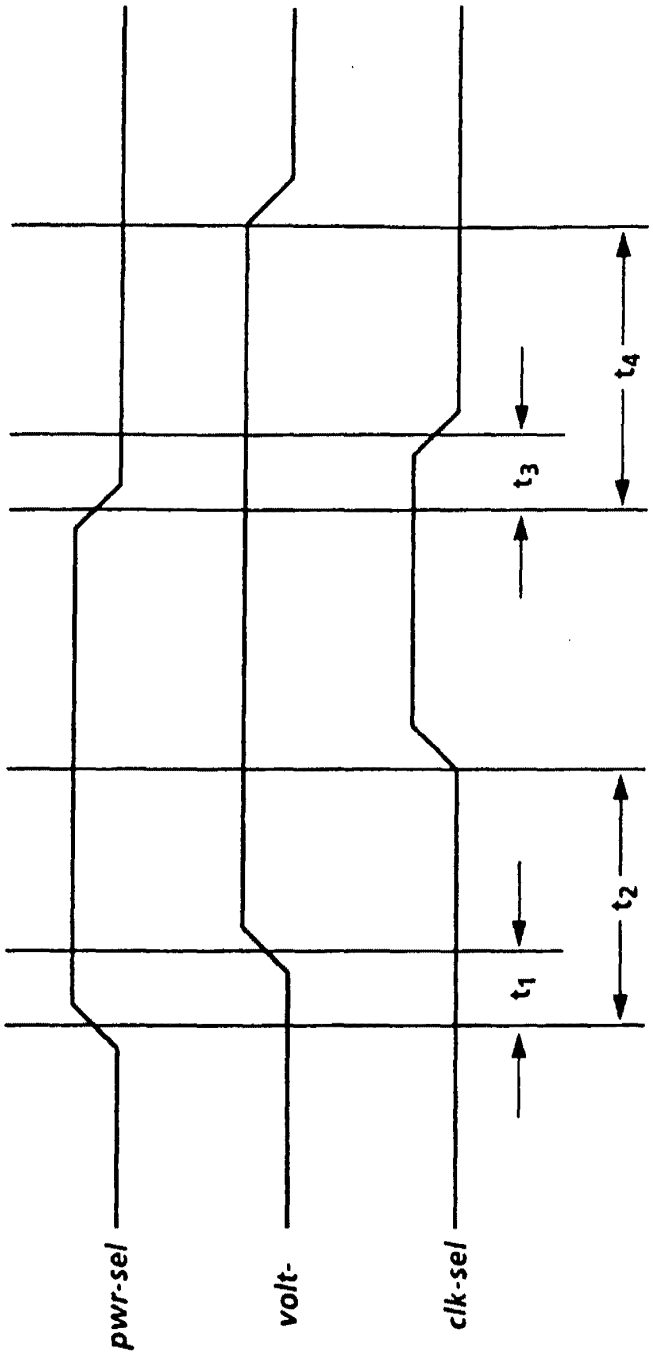

Fig. 4

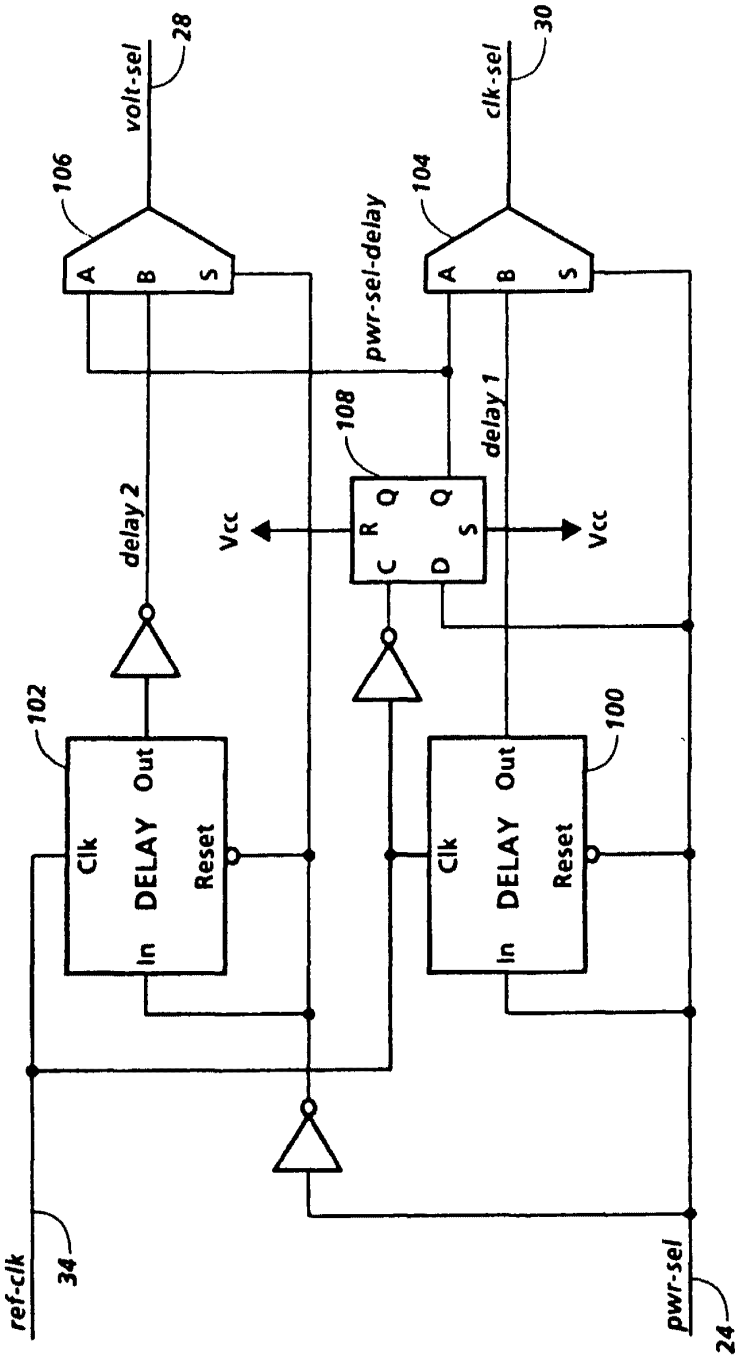

Fig. 5

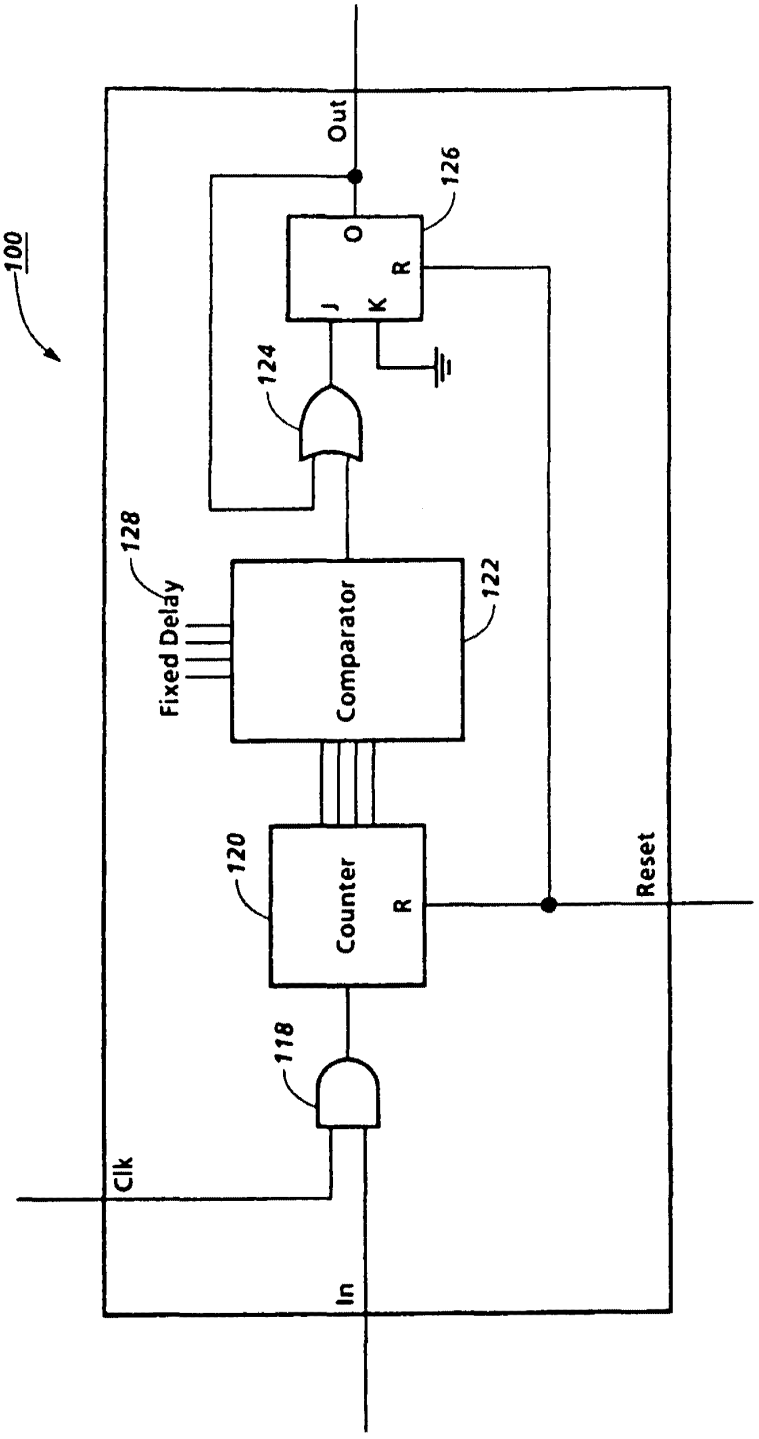

Fig. 6

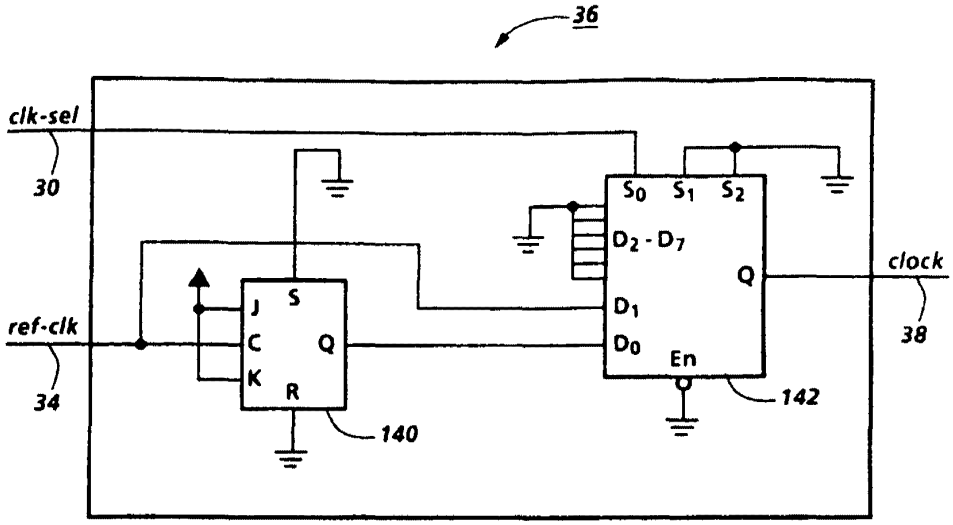

Fig. 7

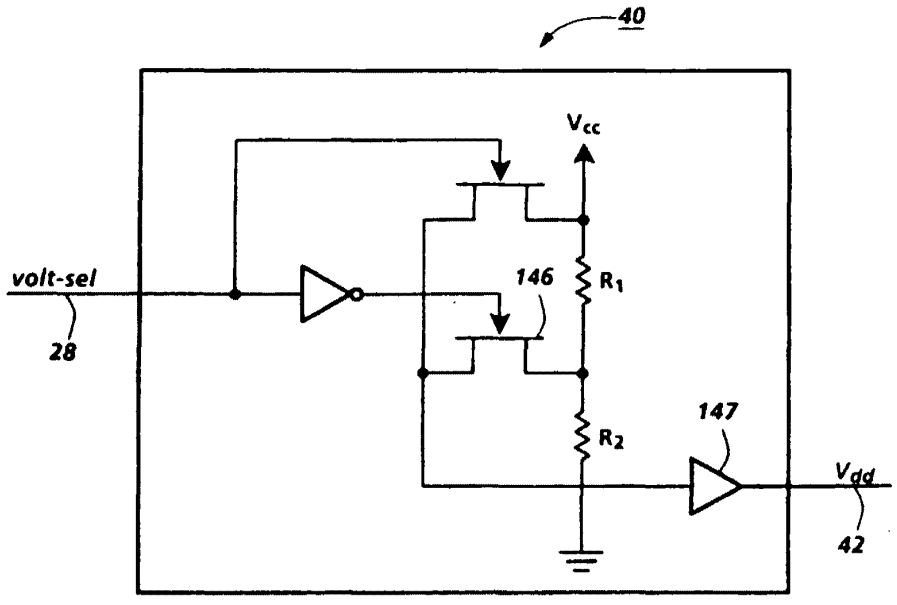

Fig. 8

European Patent Office

EUROPEAN SEARCH REPORT

Application Number
EP 94 30 4457

DOCUMENTS CONSIDERED TO BE RELEVANT

Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (Int.Cl.6)
X	EP-A-0 539 884 (TOSHIBA) * column 1, line 33 - column 3, line 29 * * column 4, line 1 - column 5, line 12 *	1,2,7	G06F1/32
Y		4-6,8-10	
X	WO-A-91 00564 (POQET COMPUTER) * page 2, line 8 - page 5, line 2 *	1,2,4-6	
X	PATENT ABSTRACTS OF JAPAN vol. 9, no. 127 (P-360)31 May 1985 & JP-A-60 010 318 (SANYO) 19 January 1985 * abstract *	1,7	
A		4,6,7	
Y	ELECTRONIC COMPONENTS AND APPLICATIONS vol. 7, no. 3 , 1986 , EINDHOVEN NL pages 179 - 186 CROES R. 'Battery backup of HCMOS logic ICs' * page 181, left column, line 15 - line 21 *	4-6	
			TECHNICAL FIELDS SEARCHED (Int.Cl.6)
Y	MOTOROLA TECHNICAL DEVELOPMENTS vol. 14 , December 1991 , SCHAUMBURG, ILLINOIS US pages 53 - 54 XP276157 SCHULTZ C. P. 'DYNAMIC CLOCK CONTROL FOR MICROPROCESSOR SYSTEM ENERGY MANAGEMENT' * page 53, left column, line 1 - line 20 *	8-10	G06F
A	MOTOROLA TECHNICAL DEVELOPMENTS vol. 15 , May 1992 , SCHAUMBURG, ILLINOIS US pages 43 - 44 XP306138 YOUNG R. ET AL 'ADDPTIVE CLOCK SPEED CONTROL FOR VARIABLE PROCESSOR LOADING' * the whole document *	1,4,7,9	

The present search report has been drawn up for all claims

Place of search	Date of completion of the search	Examiner
THE HAGUE	12 October 1994	Bailas, A

CATEGORY OF CITED DOCUMENTS

X : particularly relevant if taken alone
Y : particularly relevant if combined with another document of the same category
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E : earlier patent document, but published on, or after the filing date
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(71) Applicant: **LUCENT TECHNOLOGIES INC.**
Murray Hill, New Jersey 07974-0636 (US)

(72) Inventors:
- **Nicol, Christopher John**
  Springwood, N.S.W. (AU)
- **Singh, Kanwar Jit**
  Hazlet, New Jersey 07730 (US)

(74) Representative:
Buckley, Christopher Simon Thirsk et al
Lucent Technologies (UK) Ltd,
5 Mornington Road
Woodford Green, Essex IG8 0TU (GB)

(54) Power reduction in a multiprocessor digital signal processor

(57) Improved operation of multi-processor chips is achieved by dynamically controlling processing load of chips and controlling, significantly greater than on/off granularity, the operating voltages of those chips so as to minimize overall power consumption. A controller in a multi-processor chip allocates tasks to the individual processors to equalize processing load among the chips, then the controller lowers the clock frequency on the chip to as low a level as possible while assuring proper operation, and finally reduces the supply voltage. Further improvement is possible by controlling the supply voltage of individual processing elements within the multi-processor chip, as well as controlling the supply voltage of other elements in the system within which the multi-processor chip operates.

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Description

Background

[0001] This invention relates to electronic circuits and, more particularly to power consumption within electronic circuits.

[0002] Integrated circuits are designed to meet speed requirements under worst-case operating conditions. In Lucent Technology's 0.35µm 3.3V CMOS technology, the "worst-case-slow" condition is specified for a temperature of 125C and a chip supply voltage, V_{dd}, of 2.7V. The worst-case power consumption of the chip is quoted at the maximum supply voltage of 3.6V. The difference in chip performance at the "worst-case slow", nominal, and "worst-case-fast" conditions is shown in FIG. 1, where the frequency of a 25-stage ring oscillator is shown at different supply voltages and process corners. At the nominal operating voltage of 3.3V, the speed difference between "worst case slow" (WCS) and "worst case fast" (WCF) is a factor of 2.2. From the graph it can be seen that if a chip is designed to operate at 140MHz and at 2.1V supply even when it is "worst-case-slow", a manufactured chip whose characteristics happen to be nominal will continue to operate at 140MHz even when the chip supply is reduced to 2.1V.

[0003] The power consumption of a CMOS circuit increases linearly with operating frequency and quadratically with supply voltage. Therefore, a reduction in supply voltage can significantly reduce power consumption. For example, by reducing the nominal operating voltage from 3.3V to 2.1 V, the nominal power consumption of a 140MHz chip is reduced by 60% without altering the circuit. This, of course, presumes an ability to identify and measure a chip's variation from nominal characteristics, and an ability to modify the supply voltage based on this measurement.

[0004] To achieve variable power supply voltage scaling, a programmable dc-dc converter may be used. Probably, the most efficient approach in use today is the buck converter circuit. These are well known in the art.

[0005] Voltage scaling as a function of temperature has been incorporated into the Intel Pentium product family as a technique to achieve high performance at varying operating temperatures and process corners. It is described in US Patent No. 5,440,520. The approach uses an on-chip temperature sensor and associated processing circuitry which issues a code to the off-chip power supply to provide a particular supply voltage. The process variation information is hard-coded into each device as a final step of manufacturing. This approach has the disadvantage of costly testing of each chip to determine its variance from nominal processing. Several manufacturers make Pentium-compatible dc-dc converter circuits, which are highlighted in "Powering the Big Microprocessors", by B. Travis, *EDN*, August 15, pp. 31-44, 1997.

[0006] Recently, there has been considerable interest in integrating much of the buck controller circuit onto the chip. The only off-chip components are the inductor (typically about 10µH) and capacitor (typically about 30µF) used in the buck converter. Efficiencies in excess of 80% are typical for a range of voltages and load currents. See, for example, "A High-Efficiency Variable Voltage CMOS Dynamic dc-dc Switching Regulator," by W. Namgoong, M. Yu, and T. Meng, Proceedings ISSCC97 pp. 380-381, February, 1997. Researchers have been also experimenting with on-chip voltage scaling techniques to counter process and temperature variations. See "Variable Supply-Voltage Scheme for Low Power High-Speed COMS Digital Design," by T. Kuroda et al, *CICC97 Conference Proceedings, and JSSC Issue of CISS97*, May, 1998. The Kuroda et al paper demonstrates that the speed of the circuit can be maintained (or at least the speed degradation can be minimized) by tuning the threshold voltages even as the supply voltage is lowered. The tuning is achieved on-chip by varying the substrate-bias voltage. These techniques are needed to ensure that the leakage current, which increasing as the threshold voltage is reduced, does not become too large.

[0007] Thus, it is known that varying supply voltage to a chip can improve performance by eliminating unexpected variability in the supply voltage, and by accounting for process and operating temperature variations.

Summary of the Invention

[0008] Improved performance of multi-processor chips is achieved by dynamically controlling the processing load of chips and controlling, which significantly greater than on/off granularity, the operating voltages of those chips so as to minimize overall power consumption. A controller in a multi-processor chip allocates tasks to the individual processors to equalize processing load among the chips, then the controller lowers the clock frequency on the chip to as low a level as possible while assuring proper operation, and finally reduces the supply voltage. Further improvement is possible by controlling the supply voltage of individual processing elements within the multi-processor chip, as well as controlling the supply voltage of other elements in the system within which the multi-processor chip operates.

Brief Description of the Drawings

[0009]

FIG. 1 illustrates the maximum operating frequency that is achievable with a 0.35µm technology CMOS chip as a function of supply voltage;

FIG. 2 presents a block diagram of a multi-processor chip with supply voltage control in accordance with the principles disclosed herein;

FIG. 3 shows the relationship between the voltage control clock, Clk, of FIG. 2, the clock applied to the processing elements of FIG. 2, Clk-L, and the supply voltage applied to the processing elements, V_{dd}-local; and

FIG. 4 depicts the block diagram of a multi-processor chip with supply voltage control that is individual to each of the processing elements.

Detailed Description

[0010] FIG. 2 depicts a block diagram of a multi-processor chip. It contains processing elements (PEs) 100, 101, 102, 103, ... 104, and each PE contains a central processing unit (CPU) and a local cache memory (not shown). A real-time operating system resides in PE 100 and allocates tasks to the other PEs from a mix of many digital signal processing applications. The load ofthe FIG. 2 system is time varying and is dependent on the applications that are being executed at any given time. For example, a set-top-box for a multimedia broadband access system might need to receive an HDTV signal. It could also be transmitting data from a computer, to the Internet, and responding to button requests from a remote control handset. Over time, this dynamic mix of applications places different load requirements on the system.

[0011] For a maximally utilized system, all of the available processors ought to be operating at full speed when satisfying the maximum load encountered by the system. At such a time, the power consumption of the multiprocessor chip is at its maximum level. However, as the load requirements are lowered, the system should, advantageously, reduce its power consumption. It may be noted that, typically, computers spend 99% of their time waiting for a user to press a key. This presents a great opportunity to drastically reduce the average power consumption. The specific approach by which the system "scales back" its performance can greatly impact the realizable power savings.

[0012] In the FIG. 2 arrangement, in accordance with the principles disclosed herein, the applications that need to be processed are mapped to the N PEs under control of real time operating system (RTOS) executed on PE 100. If the number of instructions that need to be executed for each task is known and made available to the operating system, a scheduler within the operating system can use this information to determine the best way to allocate the tasks to the available processors in order to balance the computation. The intermediate goal, of course, is to maximize the parallelism and to evenly distribute the load presented to the FIG. 2 system among all of the PE's.

[0013] When an application that is running on the FIG. 2 system is subdivided into N concurrent task streams, as suggested above, each of the PEs become lightly loaded. This allows the clock frequency of the PEs to be reduced, and if the task division can be carried out perfectly, then the clock frequency of the FIG. 2 system can be reduced by a factor of N. Reducing the frequency, as indicated above, allows reducing the necessary supply voltage, and reducing the supply voltage reduces the system's power consumption (quadratically). To illustrate, if a given application that is executed on 1 PE requires operating the PE at 140MHz, it is known from FIG. 1 that the PE can be operated at approximately a 2.7V supply. When the application is divided into two concurrent tasks and assigned to two PEs that are designed to operate at 140MHz from a 2.7V supply, then the PEs can be operated at 70 MHz and at a supply voltage of 1.8V. This reduction in operating voltage represents a power saving of 55%. Of course, it is unlikely that an application can be perfectly divided into two equal load task streams and, therefore, the 55% power saving is the maximum achievable power saving for two PEs.

[0014] It should be understood that in the above example, when two PEs are employed and their operating frequency can be reduced to 70 MHz, the indicated reduction presumes that it is desired to perform the given tasks as if there was a single PE that operates at 140MHz. That is, the presumption is that there is a certain time when the tasks assigned to the chip must be finished. In fact, there might not be any particular requirement for when the tasks are to be finished. Alternatively, a requirement for when the tasks are to be finished might not be related to the highest operating frequency of the chip.

[0015] For example, the above-illustrated chip (where each of the PEs is designed to operate at 140 MHz) might be employed in a system whose basic frequency is related to 160 MHz. In such an arrangement, dividing tasks between the two PEs of the chip and operating each of the PEs at 80MHz would be preferable because it would be easier to synchronize the chip's input and output functions to the other elements in the system. Thus, in a sense it is the expected completion time for the collection of assigned tasks that is controlling, and the reduction of frequency from the maximum that the chip can support may be controlled by the division of tasks that may be accomplished.

[0016] Hence, the operating system of PE 100 needs to ascertain the required completion time, divide the collection of tasks as evenly as possible (in terms of needed processing time), consider the PE with the tasks that require the most time to carry out, and adjust the clock frequency to insure that the most heavily loaded PE carries out its assigned tasks within the required completion time. Once the frequency is thus determined, a minimum supply voltage can be determined. The supply voltage determination can be made by reference to a plot like the one shown in FIG. 1 or, advantageously, by evaluating the actual performance of the multiprocessor at hand.

[0017] As indicated above, the operating system can

reduce the supply voltage even further by tracking temperature and process variations. For example, when the chip is nominal in its characteristics, then it can be operated along line 20 of FIG. 1, which calls for only 1.5V supply when operating at 70MHz.

[0018] Returning the discussion to FIG. 2, the programmable-frequency clock is generated using an appropriately multiplied input reference clock (line 101) via a phase lock loop frequency synthesizer circuit 110 which has a high resolution, e.g., can be altered in increments of 5MHz. Advantageously, two clocks are generated by PLL 110 (requiring two synthesizer circuits), a Clk clock, and a Clk-L which is 1 frequency step lower than Clk when Clk is being increased. For example, in a PLL 110 unit that provides 5MHz resolution, when Clk is being increased from 75 MHz to 80MHz, the value of Clk-L is set to 75MHz.

[0019] Clk-L is applied to the PEs, while Clk is applied to calibration circuit 120, which generates a supply voltage command. The supply voltage command is applied to dc-dc converter 130 followed by L-C circuit 140 to cause the combination of converter 130 and L-C circuit 140 to create the supply voltage V_{dd}-local, which is fed back to calibration circuit 120 via line 102. The V_{dd}-local supply voltage is also applied to all of the PEs (excluding perhaps the operating system PE 100).

[0020] The reason for having the frequency Clk-L lag behind the frequency Clk is that the clock frequency applied to the PEs should not be increased prior to the supply voltage being increased to accommodate the higher frequency. Otherwise, the PEs might fail to perform properly. Circuit 120 observes the level on line 102 to determine whether it corresponds to the voltage necessary to make PEs 100-104 operate properly (described below), and it also waits till the signal on line 102 is stable (following whatever ringing occurs at the output of L-C circuit 140. The signal on line 121 provides information to PE 100 (yes/no) to inform the operating system of when the supply voltage is stable. When the voltage is stable and Clk has reached the required frequency, the operating system sets Clk-L to Clk and then changes the task allocation on the PEs to correspond to that which the PEs were set up to accommodate.

[0021] FIG. 3 demonstrates the timing associated with increasing Clk, Clk-L and V_{dd}-local when a new task is created and the load on the multiprocessor is thus increased, and the timing associated with decreasing Clk, Clk-L and V_{dd}-local when the load on the multiprocessor is decreased. Specifically, it shows the system operating at 70MHz from a 1.8V supply when the load is increased in three steps to 140MHz. When the 2.7V supply is stable, as shown by the supply voltage plot, the new task is enabled for execution. Some time thereafter according to FIG. 3, a task completes, which reduces the load on the multiprocessor. The reduced load permits lowering the clock frequency to 100MHz and lowering the supply voltage to 2.1V. This, too, is accommodated in steps (two steps, this time), with Clk-L preceding Clk to insure, again, that the PEs continue to operate properly while the supply voltage is decreased.

[0022] Calibration block 120 can use one of several techniques to determine the voltage required to operate the circuit at a given clock frequency. One technique is given in Koruda et al article. Recognizing that each of the PEs (101-104) has a critical path which controls the ultimate speed of the PE, block 120 uses two copies of that portion of the PE circuit that contains the critical path of the PE circuit, with one of the copies being purposely designed to be just slightly slower. Both of the copies are operated from clock signal Clk and from the V_{dd}-local supply voltage of line 102, and that voltage is adjusted within block 120 so that, while operating at frequency Clk, the slightly slower PE fails to operate properly while the other PE does operate properly. This guarantees that the PE's are operating from a supply voltage that is "just above" the point at which they are likely to fail. Since the two critical path copies within element 120 experience the same variations in temperature as do PEs 101-104, the V_{dd}-local supply voltage appropriately tracks the temperature variations as well as the different operating frequency specifications.

[0023] The FIG. 2 system uses the operating system to react to variations in the system load. As more tasks are entered into the "to-do" list, the operating system of PE 100 computes the correct way to balance the additional computational requirements and allocates the tasks to the processors. It then computes the required operating frequency.

[0024] It is noted that the frequency is gradually programmed into the system (as shown by the stepped changes in FIG. 3). This prevents excessive noise on the V_{dd}-local supply voltage and possible circuit failure. For example, if the system is operating at 50MHz and it needs to operate at 75MHz, the clock frequency is increased slowly, perhaps even as slowly as in 5MHz increments. In addition, as indicated above, the V_{dd}-local supply voltage is increased ahead of increasing the frequency of the clock the operates the PEs, when increased processing capability is desired, and the clock is reduced ahead of reducing the supply voltage when reduced processing capability will suffice.

[0025] Of course, V_{dd}-local can only be reduced so far before the circuits start to fail, at which point the operating system employs gated clocking techniques to "shut down" PEs that are not needed. Of course, the fact that supply voltage V_{dd}-local varies as a function of load should be accounted for in the interface between the PEs 101-104 and PE 100 (as well as in the interface between the multiprocessor chip and the "outside world". This is accomplished with level converter 150, which is quite conventional. It basically converts between the voltage level of PEs 101-104 and the voltage level of PE 100.

[0026] The notion of adjusting operating frequency to load and adjusting supply voltage to track the operating frequency can be extended to allow each PE to have its

own supply voltage. The benefit of this approach for some applications becomes apparent when it is realized that the chip-wise voltage scaling is most effective when the load of the computation can be evenly distributed across all of the PEs. In some applications, however, one may encounter tasks that cannot be partitioned into concurrent evenly-loaded threads and, therefore, some PE within the multiprocessor would require a higher operating frequency and a higher operating voltage. This would require raising the frequency and voltage of the entire multiprocessor chip.

[0027] A separate power supply for each PE in a chip overcomes this limitation by allowing the operating system to independently program the lowest operating frequency and corresponding lowest supply voltage for each PE. The architecture of such an arrangement is shown in FIG. 4. Each PE in FIG. 4 needs an independent controller that performs the functions of PE 100 (except it does not divide tasks among PEs). As shown in FIG. 4, all of the controllers are embodied in a single controller 200, which may be just another processing element of the integrated circuit that contains the other processing elements. Each processing element also requires a calibration circuit like circuit 120, and a voltage converter circuit like circuits 130 and 140. It also has a PE 200 that assigns the tasks given to the multi-processor chip of FIG. 4 among the PEs.

[0028] It may be noted that if the frequencies at which the individual PEs operate differ from one another and from other elements within the system where the multiprocessor chip is employed, there is an issue of synchronization that must be addressed. That is, a synchronization schema must be implemented when there is a need to communicate data between PEs (or with other system elements) that operate at different frequencies. It is possible to arrange the frequencies so that the collection of tasks that are assigned to the multiprocessor is completed at a predetermined time. In such a case, the synchronization problem of the multiprocessor vis-a-vis other elements within the system where the multiprocessor is employed is minimized. However, that leaves the issue of synchronizing the exchange of data among the PEs of a multiprocessor chip.

[0029] To effect such synchronization, each PE within the FIG. 4 arrangement is connection to an arrangement comprising elements 150 and 160. Level converter 150 converts the variable voltage swings of the PEs to a fixed level swing, and network 160 resolves the issue of different clock domains.

[0030] The principles disclosed above for a multiprocessor is extendible to other system arrangements. This includes systems with a plurality of separate processor elements that operate at different frequencies and operating voltages, as well as components that are not typically thought of as processor elements. For example, there is a current often-used practice to maintain program code and data for different applications of a personal computer in a fast memory. As each new application is called, more information is stored in the fast memory, until that memory is filled. Thereafter, when a new application is called, some of the information in the fast memory is discarded, some other information is placed in the slower hard drive, and the released memory is populated with the new application. It is possible to anticipate that memory stored in the fast memory is so old as to be unlikely to be accessed before a new application is called. When so anticipated, some of the fast memory can be released (storing some of the data that needed to be remembered) at a leisurely pace. That is, lower clock frequency can be employed in connection with the fast memory and the hard drive, with a corresponding lower supply voltage, resulting in an overall power saving in both the memory's operation and in the operation of the hard drive.

[0031] The above description illustrated the principles of this invention, but it should be realized that a skilled artisan may easily make various modifications and improvements that are within the scope of this invention as defined by the appended claims. For example, in one of the embodiment disclosed above all of the PEs in a multi-processor chip are subjected to a single controlled supply voltage. In another embodiment disclosed above each of the PEs in a multi-processor chip is subjected to its own, individually controlled, supply voltage. It should be realized, however, that a middle ground is also possible; i.e., the PEs of a multi-processor chip can be divided into groups, and each group of PEs can be arranged to operate from its own controlled supply voltage. To cite another example, the FIG. 2 embodiment employs two almost identical critical path circuits to establish the minimum supply voltage. Alternatively, the voltage may be set in accordance with a preset frequency-voltage relationship that is not unlike the one depicted in FIG. 1.

[0032] It should also be noted that level converter 150 is interposed in FIG. 2 between PE 100 and the other PEs because PE 100 is operating off V_{dd}. PE 100 can also be operated off V_{dd}-local, in which case the level converter is interposed between PE 100 and the input/output port of the FIG. 2 circuits that interacts with PE 100.

[0033] It should further be noted that the power supply circuit need not have any elements outside the circuit itself (as depicted in FIG. 2). A skilled artisan would be aware that circuit design exists that can be manufactured wholly within an integrated circuit.

[0034] Yet another modification may be implemented by discarding the two-step application of voltages and frequencies of FIG. 3 when appropriate timing conditions are met.

Claims

1. A method for controlling power consumption of a system sub-circuit comprising the steps of:

ascertaining time allotted for carrying out an assigned task;
determining a lowest frequency at which or above which the sub-circuit must operate in order to complete execution of the assigned task within the allotted time; and
based on characteristics of the sub-circuit, setting a supply voltage that is applied to the sub-circuit to a lowest level that insures proper operation of the sub-circuit at the determined frequency.

2. The method of claim **1**, carried out in a multiprocessor sub-circuit, wherein said assigned task comprises a plurality of sub-tasks, the method further comprising the step of

apportioning said sub-tasks among processors of said multiprocessor sub-circuit, resulting in one of said processors carrying the largest load of sub-tasks processing, compared to the sub-tasks processing load of others of said processors, where
said step of apportioning is executed prior to said step of determining, and
said step of determining ascertains the lowest frequency at which the processor carrying the largest load of sub-tasks processing may operate in order to complete its assigned sub-tasks processing within the allotted time.

3. The method of claim **2** further comprising the steps of:

determining a new lowest frequency, when a new task is assigned, at which or above which the sub-circuit must operate in order to complete execution of the assigned task within the allotted time;
comparing the lowest frequency to the new lowest frequency to determine whether a new operating frequency should be set for said sub-circuit;
when said step of comparing determines that the new lowest frequency may be lower than said lowest frequency, reducing the frequency at which said sub-circuit is set to operate and, thereafter, reducing the supply voltage that is applied to the sub-circuit; and
when said step of comparing determines that the new lowest frequency must be higher than said lowest frequency, increasing the supply voltage that is applied to the sub-circuit and, thereafter, increasing the frequency at which said sub-circuit is set to operate to said new lowest frequency.

4. A circuit that includes a processor, comprising:

a controller, responsive to an applied task and to a specification for a time interval that may be devoted to executing said task, for developing a frequency of operation for said processor that is the lowest frequency of operation that allows completion of said applied task within said time interval;
a calibration circuit responsive to said controller for directing creation of a supply voltage for said processor, and
a power supply responsive to said calibration circuit, for developing said supply voltage for said processor and applying said supply voltage to said processor;

wherein said controller directs said processor to execute said task after said supply voltage is applied to said processor and the frequency of a clock applied to said processor is set to said lowest frequency of operation that allows completion of said applied task within said time interval.

5. The circuit of claim **4** further comprising a level converter circuit interposed between input/output ports of said circuit and said processor, to convert voltages levels passing between said input/output ports and said processor.

6. The circuit of claim **4** wherein said controller includes a generator of clock signals that develops a first clock signal having a first frequency and applied to said calibration circuits, and a second clock signal having a second frequency applied to said processor, wherein the second frequency can be set to said first frequency or to a lower frequency.

7. The circuit of claim **4** wherein said task includes a plurality of sub-tasks, said processor comprises a plurality of processing elements, said controller partitions said sub-tasks among said processing element and develops said frequency of operation for said processor based on said partitioning.

8. The circuit of claim **7** wherein said controller develops said frequency of operation for said processor by evaluating the lowest frequency of operation for a most-burdened processing element that would still complete execution within said time interval, wherein the most-burdened processing element is a processing element to which sub-tasks are allocated that require, in the aggregate, the most processing time.

9. The circuit of claim **4** wherein said processor comprises N processing elements, said controller comprises N controller sub-modules, said calibration circuit comprises N calibration circuit sub-modules, and said power supply comprises N power supply

modules, and wherein

the i-th calibration circuit sub-module is responsive to the i-th controller sub-module and directs the i-th power supply module, the i-th power supply module provides power to the i-th processing element and the i-th processing element is responsive to the i-th controller sub-module.

10. The apparatus of claim **9** further comprising a processing element for accepting said task and, when Said task comprises a plurality of sub-tasks, for partitioning said sub-tasks among the N processing elements.

11. The apparatus of claim **9** further comprising a level converter associated with each of said processing elements and coupled to input/output ports of said associated processing elements.

12. A circuit comprising:

a controller processing element;
a plurality of task-handling processing elements;
a calibration circuit responsive to said controller processing element for directing creation of a supply voltage for said processor; and
a power supply circuit, responsive to said calibration circuit, for developing a supply voltage for said task-handling processing elements;
wherein said controller processing element directs said task-handling processing elements to execute tasks at a selected processing frequency.

13. A method for operating a processor comprising the step of applying a supply voltage to said processor as a function of frequency necessary to operate said processor to complete an assigned task within an assigned time interval.

14. The method of claim **13** wherein said function substantially minimizes power consumption in said processor.

FIG. 1

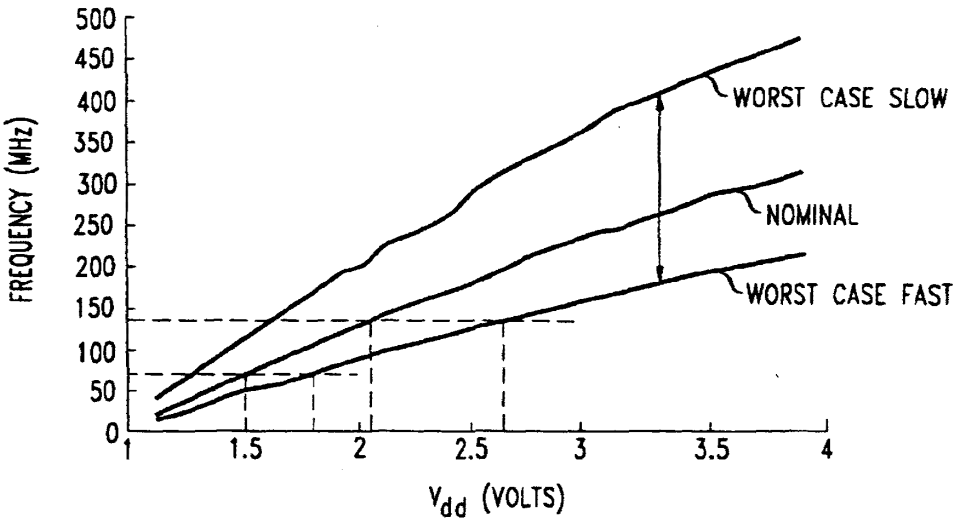


FIG. 2

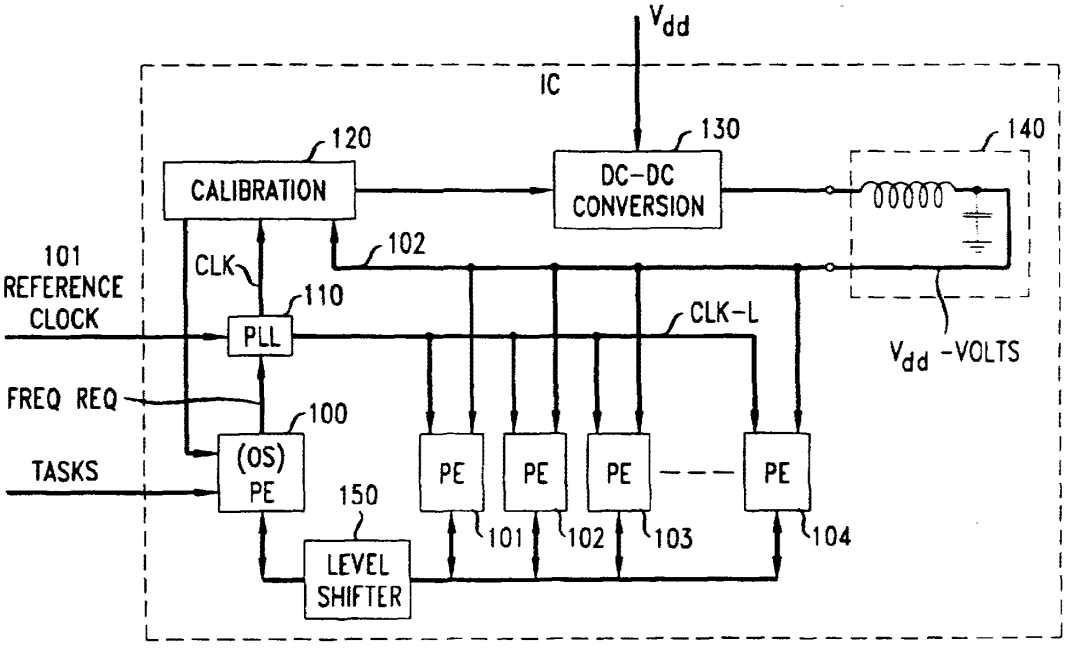


FIG. 3

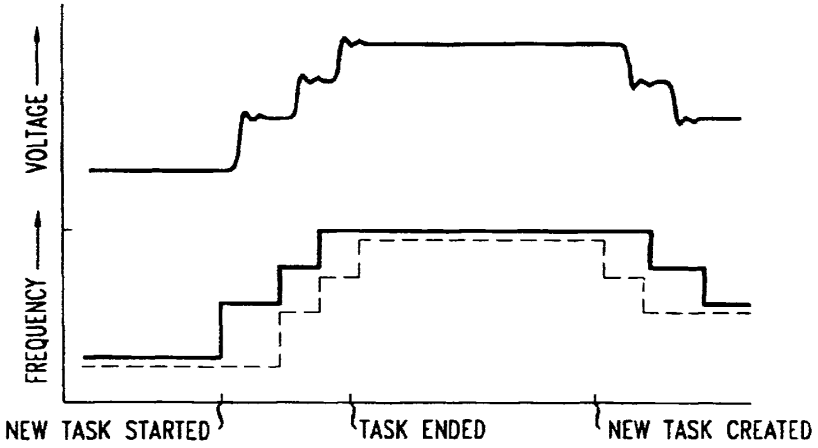
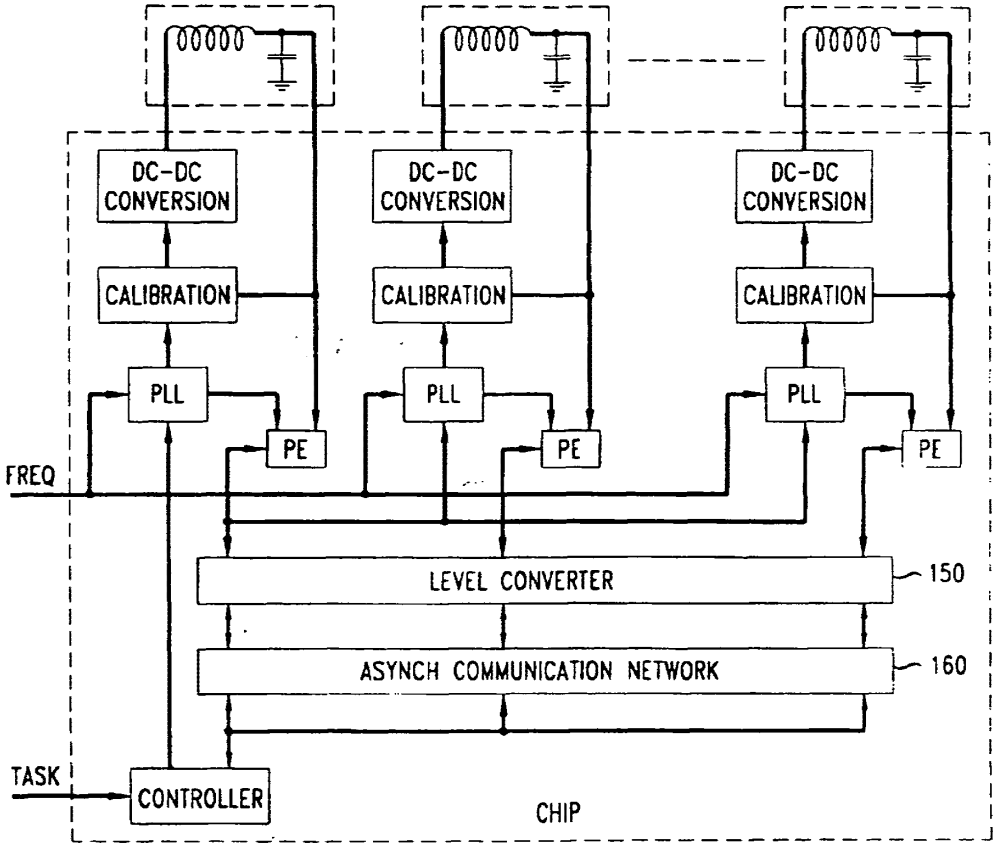


FIG. 4



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(71) Applicant: **LUCENT TECHNOLOGIES INC.**
Murray Hill, New Jersey 07974-0636 (US)

(72) Inventors:
- **Nicol, Christopher John**
  Springwood, N.S.W. (AU)
- **Singh, Kanwar Jit**
  Hazlet, New Jersey 07730 (US)

(74) Representative: **Williams, David John et al**
Page White & Farrer,
54 Doughty Street
London WC1N 2LS (GB)

(54) Power reduction in a multiprocessor digital signal processor

(57) Operation of multi-processor chips is achieved by dynamically controlling processing load of chips and controlling, significantly greater than on/off granularity, the operating voltages of those chips so as to minimize overall power consumption. A controller in a multi-processor chip allocates tasks to the individual processors to equalize processing load among the chips, then the controller lowers the clock frequency on the chip to as low a level as possible while assuring proper operation, and finally reduces the supply voltage. Further reduction is possible by controlling the supply voltage of individual processing elements within the multi-processor chip, as well as controlling the supply voltage of other elements in the system within which the multi-processor chip operates.

EP 0 978 781 A3

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EPNSDOCID: <EP_____0978781A3_I_>

European Patent Office

EUROPEAN SEARCH REPORT

Application Number
EP 99 30 5916

DOCUMENTS CONSIDERED TO BE RELEVANT

Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (Int.Cl.7)
X	EP 0 632 360 A (XEROX CORP) 4 January 1995 (1995-01-04)	1,4	G06F1/32
Y	* column 2, line 34 - line 54 * * column 4, line 4 - line 11 *	12-14	
A	* column 5, line 12 - line 42 * * column 8, line 21 - line 46 * * column 10, line 5 - line 15 * * figure 1 *	3	
Y	EP 0 340 900 A (DU PONT PIXEL SYSTEMS) 8 November 1989 (1989-11-08)	12-14	
A	* page 3, paragraph 1 *	7,8	
X	US 5 778 237 A (YAMAMOTO MITSUYOSHI ET AL) 7 July 1998 (1998-07-07) * column 1, line 50 - column 2, line 2 *	12-14	
A	* column 2, line 40 - line 65 * * column 3, line 31 - line 35 *	3,7,9,10	
Y	US 5 787 294 A (EVOY DAVID R) 28 July 1998 (1998-07-28) * column 1, line 48 - line 62 * * column 2, line 38 - line 45 * * column 3, line 7 - line 21 * * column 5, line 25 - line 58; figure 6 *	1-4, 7-10, 12-14	TECHNICAL FIELDS SEARCHED (Int.Cl.7) G06F
Y	US 5 142 684 A (PERRY RICHARD A ET AL) 25 August 1992 (1992-08-25) * column 2, line 25 - line 64 * * column 5, line 14 - line 20 * * column 4, line 40 - line 46 *	1-4, 7-10, 12-14	
A	US 5 727 193 A (TAKEUCHI KESATOSHI) 10 March 1998 (1998-03-10) * column 2, line 1 - line 27; figure 9 *	6,11	

The present search report has been drawn up for all claims

Place of search	Date of completion of the search	Examiner
BERLIN	28 January 2003	de la Torre, D

CATEGORY OF CITED DOCUMENTS

X : particularly relevant if taken alone
Y : particularly relevant if combined with another document of the same category
A : technological background
O : non-written disclosure
P : intermediate document

T : theory or principle underlying the invention
E : earlier patent document, but published on, or after the filing date
D : document cited in the application
L : document cited for other reasons

& : member of the same patent family, corresponding document

EPO FORM 1503 03.82 (P04C01)

ANNEX TO THE EUROPEAN SEARCH REPORT ON EUROPEAN PATENT APPLICATION NO. EP 99 30 5916

This annex lists the patent family members relating to the patent documents cited in the above-mentioned European search report. The members are as contained in the European Patent Office EDP file on
The European Patent Office is in no way liable for these particulars which are merely given for the purpose of information

28-01-2003

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
EP 0632360 A	04-01-1995	EP 0632360 A1	04-01-1995
		JP 7020968 A	24-01-1995
EP 0340900 A	08-11-1989	GB 2217062 A	18-10-1989
		GB 2215881 A	27-09-1989
		CA 1304509 A1	30-06-1992
		EP 0340900 A2	08-11-1989
		JP 2146668 A	05-06-1990
		US 5428754 A	27-06-1995
US 5778237 A	07-07-1998	JP 7287699 A	31-10-1995
US 5787294 A	28-07-1998	JP 9204242 A	05-08-1997
US 5142684 A	25-08-1992	WO 9100565 A2	10-01-1991
US 5727193 A	10-03-1998	JP 8044465 A	16-02-1996

For more details about this annex : see Official Journal of the European Patent Office, No. 12/82

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PATENT APPLICATION FEE DETERMINATION RECORD
Effective October 1, 2000

Application or Docket Number: 09 644 433

CLAIMS AS FILED - PART I

	(Column 1)	(Column 2)
TOTAL CLAIMS	13	
FOR	NUMBER FILED	NUMBER EXTRA
TOTAL CHARGEABLE CLAIMS	13 minus 20=	* 0
INDEPENDENT CLAIMS	2 minus 3 =	* 0
MULTIPLE DEPENDENT CLAIM PRESENT		☐

* If the difference in column 1 is less than zero, enter "0" in column 2

SMALL ENTITY TYPE ☐		OR	OTHER THAN SMALL ENTITY	
RATE	FEE		RATE	FEE
BASIC FEE ~~355.00~~		OR	BASIC FEE ~~710.00~~ 770	
X$ 9=		OR	X$18=	
X40=		OR	X80=	
+135=		OR	+270=	
TOTAL	355	OR	TOTAL	770

2/3/04

CLAIMS AS AMENDED - PART II

AMENDMENT A

	(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA
Total	* 13	Minus	** 20	= 0
Independent	* 6	Minus	*** 3	= 3
FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM				☐

SMALL ENTITY		OR	OTHER THAN SMALL ENTITY	
RATE	ADDITIONAL FEE		RATE	ADDITIONAL FEE
X$ 9=		OR	X$18=	
X40=		OR	X80=	258
+135=		OR	+270=	
TOTAL ADDIT. FEE		OR	TOTAL ADDIT. FEE	258

8/3/04

AMENDMENT B

	(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA
Total	* 18	Minus	** 20	= 0
Independent	* 8	Minus	*** 6	= 2
FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM				☐

RATE	ADDITIONAL FEE		RATE	ADDITIONAL FEE
X$ 9=		OR	X$18=	0
X40=		OR	[redacted]	172
+135=		OR	+270=	
TOTAL ADDIT. FEE		OR	TOTAL ADDIT. FEE	172

3/25/05

AMENDMENT C

	(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA
Total	* 37	Minus	** 20	= 17
Independent	* 12	Minus	*** 8	= 4
FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM				☐

RATE	ADDITIONAL FEE		RATE	ADDITIONAL FEE
X$ 9=		OR	[redacted]	850
X40=		OR	[redacted]	800
+135=		OR	+270=	
TOTAL ADDIT. FEE		OR	TOTAL ADDIT. FEE	1650

* If the entry in column 1 is less than the entry in column 2, write "0" in column 3.
** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20."
*** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3."
The "Highest Number Previously Paid For" (Total or Independent) is the highest number found in the appropriate box in column 1.

FORM PTO-875
(Rev. 8/00)

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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/694,433	10/23/2000	Andrew Read	TRANS59	3072

7590 06/09/2005

WAGNER, MURABITO & HAO LLP
TWO NORTH MARKET STREET
THIRD FLOOR
SAN JOSE, CA 95113

EXAMINER	
CAO, CHUN	
ART UNIT	**PAPER NUMBER**
2115	

DATE MAILED: 06/09/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

PTO-90C (Rev. 10/03)

Office Action Summary	Application No.	Applicant(s)	
	09/694,433	READ ET AL.	
	Examiner	Art Unit	
	Chun Cao	2115	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *25 March 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-37* is/are pending in the application.

4a) Of the above claim(s) *19-37* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-18* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *3/25/05*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAIL ACTION

1. Claims 1-37 are presented for examination. Claims 19-37 are newly added claims and presented for examination.

2. The text of those applicable section of Title 35, U.S. Code not included in this action can be found in the prior Office Action.

Election/Restrictions

3. Newly submitted claims 19-37 are directed to an invention that is independent or distinct from the invention originally claimed for the following reasons:

Original claims 1-18, drawn to: reducing power utilized by a processor, and reducing core voltage to the processor to a value sufficient to maintain state during the mode in which system clock is disable, classified in class 713, subclass 322.

Newly added claims 19-37, drawn to: a computer system has a first transition time and second transition for transitioning from sleep voltage to an operating voltage, wherein the first transition time is greater than an allowed time, classified in class 713, subclass 310.

a. These inventions have acquired a separate status in the art as shown by their different classification;

b. The search required for one Group is not required for the other Groups for the reasons above restriction for examination purpose as indicated is proper.

Since applicant has received an action on the merits for the originally presented invention, this invention has been constructively elected by original presentation for prosecution on the merits. Accordingly, claims 19-37 are withdrawn from consideration

as being directed to a non-elected invention. See 37 CFR 1.142(b) and MPEP § 821.03.

4. The rejections are respectfully maintained and reproduced infra for applicant's convenience.

5. Claims 1-3 are rejected under 35 U.S.C. 103(a) as being unpatentable over Orton et al. (Orton), US patent no. 6,118,306, in view of "Re: AX64Pro or AK72?", NewsReader, June 15, 2000, pages 1-2; (hereinafter, "Newsreader").

Orton is a prior art reference cited by applicant in IDS paper no. 6.

As per claim 1, Orton teaches a method for reducing power utilized by a processor comprising the steps of:

determining that a processor is transitioning from a computing mode to a mode in which system clock to the processor is disabled [col. 2, lines 44-60]; and

reducing core voltage to the processor to a value sufficient to maintain state during the mode of which system clock is disable [col. 3, lines 10-20].

Orton does not explicitly teach that the value of the core voltage is not sufficient to maintain processing activity in said processor. In other words, Orton does not teach reducing the core voltage to one Volt or less during deep sleep mode.

Newsreader teaches of reducing the core voltage to one Volt or less during deep sleep mode [page 2, paragraph 3]. Therefore, Newsreader teaches that the value of the core voltage is not sufficient to maintain processing activity in said processor.

It would have been obvious to one of ordinary skill in the art at time the invention to combine the teachings of Orton and Newsreader because they are both directed to the problem of reducing the power consumption of a processor core, and the specify teachings of Newsreader stated above would improve power consumption by further reducing the core voltage to a minimum supported voltage.

As per claim 2, Orton teaches of determining the processor is transitioning from a computing mode to a mode in which system clock to the processor is disabled comprises monitoring a stop clock signal [col. 2, lines 44-60; col. 5, lines 4-11; col. 7, lines 38-43].

As per claim 3, Orton teaches of reducing an output voltage providing by a voltage regulator furnishing core voltage to the processor and providing a feedback signal to the voltage regulator to reduce its output voltage below a specified output voltage [col. 2, lines 24-27; col. 3, lines 10-19; col. 7, lines 14-19, 44-58].

6. Claims 4, 12 and 14-18 are rejected under 35 U.S.C. 103 (a) as being unpatentable over Orton et al. (Orton), US patent no. 6,118,306 in view of Applicant Admitted Prior Art (AAPA).

7. As per claim 4, Orton teaches that a method for reducing power utilized by a processor comprising the steps of:

determining that a processor is transitioning from a computing mode to a mode is which system clock to the processor is disabled [col. 2, lines 44-60];

reducing core voltage to the processor to a value sufficient to maintain state during the mode of which system clock is disable by [col. 3, lines 10-20]:

furnishing an input to reduce an output voltage provided by a voltage regulator furnishing core voltage to the processor [col. 2, lines 24-27; col. 3, lines 10-19; col. 7, lines 14-19, 44-58]; and

providing a control signal to the voltage regulator to reduce its output voltage below a specified output voltage [col. 2, lines 24-27; col. 3, lines 10-19; col. 7, lines 14-19, 44-58].

Orton does not explicitly teach of providing a feedback to the voltage regulator.

AAPA teaches of providing a feedback to the voltage regulator [page 5, lines 6-9].

It would have been obvious to one of ordinary skill in the art at time the invention to combine the teachings of Orton and AAPA because the specify teachings of AAPA stated above would allow the processor to run stable and reliable by adjusting the core voltage accordingly.

As per claim 18, Orton teaches that the output voltage to which said voltage regulator is reduced depends upon output voltage of said voltage regulator prior to furnishing the input to reduce the output voltage provided by the voltage regulator [col. 7, lines 14-58].

8. As per claim 12, Orton discloses a circuit [fig. 5] for providing a regulated voltage to a processor comprising:

a voltage regulator [52, fig. 1, fig. 5] having: an output terminal [col. 7, lines 50-51; " the output from the voltage regulator 52", inherently, there is an output terminal in the voltage regulator 52] providing a selectable voltage [col. 3, lines 10-12; col. 7, lines 28-31, 46-47, "...adjust the voltage level supplied by the voltage regulator 52 up or down" and "to indicate that the voltage level from the voltage regulator 52 is changing"];

input terminal [fig. 5; col. 7, lines 52-55; "the voltage interface provided the control logic portion 400 allows the voltage regulator 52 to change settings", inherently, there is an input terminal in the voltage regulator 52] for receiving signals indicating the selectable voltage level;

means for providing signal at the input terminal of the voltage regulator for selecting a voltage for operating the processor in a computing mode and a voltage of a level less than that for operating the processor in computing mode [col. 7, lines 50-65],

means for reducing the selectable voltage below a level provided by the voltage regulator [col. 7, lines 50-65].

Orton does not explicitly disclose a voltage regulator feedback circuit and a voltage divider network.

AAPA discloses a voltage regulator including a voltage regulator feedback circuit and a voltage divider network [page 5, lines 6-9].

It would have been obvious to one of ordinary skill in the art at time the invention to combine the teachings of Orton and AAPA because the specify teachings of AAPA stated above would allow the processor to run stable and reliable by adjusting the core voltage accordingly.

9. As per claim 14, is contained same limitations as set forth in claim 12. Therefore, same rejection is applied.

As per claim 15, Orton teaches that the first voltage is for operating the processor in a computing mode and the second voltage is a level less than that for operating the processor in the computing mode [col. 7, lines 50-65].

As to claims 16 and 17, AAPA discloses that the feedback circuit comprises a voltage divider [page 5, lines 6-9].

10. Claims 5-11 and 13 are rejected under 35 U.S.C. 102 (a) or 102(e) as being anticipated by Orton et al. (Orton), US patent no. 6,118,306.

As per claim 5, Orton teaches a method for reducing power utilized by a processor comprising the steps of:

determining that a processor is transitioning from a computing mode to a mode is which system clock to the processor is disabled [col. 2, lines 44-60];

reducing core voltage to the processor to a value sufficient to maintain state during the mode of which system clock is disable; [col. 3, lines 10-20]; and

transferring operation of a voltage regulator furnishing core voltage in a mode in which power is dissipated during reductions in core voltage to a mode in which power is saved during a voltage transition when it is determined at a processor is transitioning from a computing mode to a mode is which system clock to the processor is disabled [col. 2, lines 11-27, 44-65; col. 7, line 59-col. 8, line 5].

As per claim 6, Orton teaches of returning the voltage regulator to its original mode of operation [col. 3, lines 10-14; col. 7, lines 51-58; col. 8, lines 54-65].

11. As per claim 7, Orton discloses a circuit [fig. 5] for providing a regulated voltage to a processor comprising:

a voltage regulator [52, fig. 1, fig. 5] having: an output terminal [col. 7, lines 50-51; " the output from the voltage regulator 52", inherently, there is an output terminal in the voltage regulator 52] providing a selectable voltage [col. 3, lines 10-12; col. 7, lines 28-31, 46-47, "...adjust the voltage level supplied by the voltage regulator 52 up or down" and "to indicate that the voltage level from the voltage regulator 52 is changing"];

input terminal [fig. 5; col. 7, lines 52-55; "the voltage interface provided the control logic portion 400 allows the voltage regulator 52 to change settings" , inherently, there is an input terminal in the voltage regulator 52] for receiving signals indicating the selectable voltage level;

means for providing signal at the input terminal of the voltage regulator for selecting a voltage for operating the processor in a computing mode and a voltage of a level less than that for operating the processor in computing mode [col. 7, lines 50-65], wherein the level less than that for operating the processor in a computing mode is sufficient to maintain state of the processor [col. 2, lines 44-65; col. 3, lines 10-20; col. 7, line 59-col. 8, line 5].

As per claim 8, Orton discloses that the voltage regulator comprises means for accepting binary signals [LO/HI signals] indicating different voltage level [fig. 5; col. 7, lines 20-37, 63-65; "A signal **VR_LO/HI#**...adjust the voltage level supplied by the voltage regulator 52 up or down"].

As per claim 9, Orton discloses that the voltage regulator comprises:

Selection circuitry; means for furnishing a plurality of signals at the input to the selection circuitry and means for controlling the selection by the selection circuitry [fig. 3A] [col. 5, lines 38-55].

As per claim 10, Orton discloses a multiplexor [col. 5, lines 44-45; fig. 3A] and means for controlling the selection by the selection circuitry including a control terminal for receiving signals indicating a system clock to the processor is being terminated [col. 5, lines 38-65].

12. As per claim 11, Orton discloses a circuit [fig. 5] for providing a regulated voltage to a processor comprising:

a voltage regulator [52, fig. 1, fig. 5] having: an output terminal [col. 7, lines 50-51; " the output from the voltage regulator 52", inherently, there is an output terminal in the voltage regulator 52] providing a selectable voltage [col. 3, lines 10-12; col. 7, lines 28-31, 46-47, "...adjust the voltage level supplied by the voltage regulator 52 up or down" and "to indicate that the voltage level from the voltage regulator 52 is changing"];

input terminal [fig. 5; col. 7, lines 52-55; "the voltage interface provided the control logic portion 400 allows the voltage regulator 52 to change settings" , inherently, there is an input terminal in the voltage regulator 52] for receiving signals indicating the selectable voltage level;

means for providing signal at the input terminal of the voltage regulator for selecting a voltage for operating the processor in a computing mode and a voltage of a level less than that for operating the processor in computing mode [col. 7, lines 50-65],

means for reducing the selectable voltage below a lowest level the voltage regulator is specified to output [col. 7, lines 50-65].

13. As per claim 13, Orton discloses a circuit [fig. 5] for providing a regulated voltage to a processor comprising:

a voltage regulator [52, fig. 1, fig. 5] having: an output terminal [col. 7, lines 50-51; " the output from the voltage regulator 52", inherently, there is an output terminal in the voltage regulator 52] providing a selectable voltage [col. 3, lines 10-12; col. 7, lines 28-31, 46-47, "...adjust the voltage level supplied by the voltage regulator 52 up or down" and "to indicate that the voltage level from the voltage regulator 52 is changing"];

input terminal [fig. 5; col. 7, lines 52-55; "the voltage interface provided the control logic portion 400 allows the voltage regulator 52 to change settings" , inherently, there is an input terminal in the voltage regulator 52] for receiving signals indicating the selectable voltage level;

means for providing signal at the input terminal of the voltage regulator for selecting a voltage for operating the processor in a computing mode and a voltage of a level less than that for operating the processor in computing mode [col. 7, lines 50-65],

circuitry for conserving charge [battery 60] stored by the voltage regulator when the selectable voltage decreases; and means for enabling the circuitry for conserving charge stored by the voltage regulator when the selectable voltage decreases [col. 7, lines 28-58].

Response to Arguments

14. Applicant's arguments filed on 3/25/05, which have been fully considered but they are not persuasive.

15. In the remarks, Applicants argued that 1) Orton fails to teach, disclose or suggest as to whether or not, in this mode, a processor would be capable of processing activity based on the mode's processor voltage; and Newsreader is silent as to whether or not the processor is clocked in deep-sleep mode. 2) Orton is silent as to operate the voltage regulator in a mode in which power is dissipated to a mode in which power is saved. 3) Orton is silent as to cause the voltage regulator to output a voltage below a lowest level the voltage regulator is specified to output.

16. The examiner respectfully traverses the argument for the following reasons:

As to point 1): Orton does not explicitly teach the limitation. However, there is no claim language directed to the above limitation. Orton teaches the limitation as set forth in claim 1 of reducing core voltage to the processor to a value sufficient to maintain state during the mode [C3 state] of which system clock is disable ["the external clock is stopping"; col. 3, lines 10-20]. Also, Orton teaches that in a deep-sleep state (C3 state), an external clock to the processor is stopped [col. 2, lines 55-57]. Newsreader discloses that a processor is operating a deep-sleep state. It would have been obvious to one of ordinary skill in the art at time the invention based on Orton's teachings as state above, the clock of the processor is stopped in deep-sleep mode in Newreader's system. Furthermore, Newsreader teaches that the value [1.0 volt] of the core voltage is not sufficient to maintain processing activity in said processor [page 2, paragraph 3].

As to point 2): Orton teaches of operating the voltage regulator in a mode in which power is dissipated to a mode in which power is saved ["the processor's core voltage level may be reduced since power consumption is proportional to the square of the supply voltage level"; col. 2, lines 11-27, 44-65; col. 7, line 59-col. 8, line 5].

As to point 3): Orton teaches of causing the voltage regulator to output a voltage below a lowest level the voltage regulator is specified to output [col. 7, lines 50-65].

Also see detailed rejection indicated above.

17. **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Chun Cao whose telephone number is 571-272-3664. The examiner can normally be reached on Monday-Friday from 7:30 am-4:00 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Thomas C. Lee can be reached on 571-272-3667. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Any inquiry of a general nature or relating to the status of this application should be directed to the Group receptionist whose telephone number is 571-272-2100.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Chun Cao

June 7, 2005

Attorney Docket No.: TRAN-P059

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Patent Application

Inventor(s): Andrew Read, Sameer Halapete, Keith Klayman

Application No.: 09/694,433 Group Art Unit: 2185

Filed: 10/23/00 Examiner: CAO, Chun

Title: SAVING POWER WHEN IN OR ON TRANSITIONING TO A STATIC MODE OF A PROCESSOR (AS AMENDED)

Form 1449

U.S. Patent Documents

Examiner Initial	No.	Patent No.	Date	Patentee	Class	Sub-class	Filing Date
~~—~~	~~A~~	~~6,704,880~~	~~03/09/04~~	~~Dai et al.~~	~~713~~	~~323~~	~~10/18/01~~
~~—~~	~~B~~	~~6,675,304~~	~~01/06/04~~	~~Pole, II et al.~~	~~713~~	~~322~~	~~11/29/99~~
~~—~~	~~C~~	~~5,852,737~~	~~12/22/98~~	~~Bikowsky~~	~~395~~	~~750.05~~	~~12/31/96~~
C	D	6,425,086	07/23/02	Clark et al.	713	322	04/30/99
|	E	5,440,520	08/08/95	Schutz et al.	365	226	09/16/94
|	F	5,727,208	03/10/98	Brown	395	653	07/03/95
|	G	6,484,265	11/19/02	Borkar et al.	713	324	12/30/98
|	H	5,787,294	07/28/98	Evoy	395	750.03	10/13/95
C	I	5,142,684	08/25/92	Perry et al.	395	750	06/23/89

Duplicate in paper NO. 20040917

Foreign Patent or Published Foreign Patent Application

Examiner Initial	No.	Document No.	Publication Date	Country or Patent Office	Class	Sub-class	Translation Yes	Translation No
C	J	EP0978781	02/09/00	EPO	G06F	1/32	X	
C	K	EP0632360	01/04/95	EPO	G06F	1/32	X	

US. Published Patent Applications

Examiner Initial	No.	Pub. No.	Date	Applicant	Class	Sub-class	Publication Date
C	L	2002/0087896	07/04/02	Cline et al.	713	300	12/29/00

Other Documents

Examiner Initial	No.	Author, Title, Date, Place (e.g. Journal) of Publication
C	M	AMD ATHLON- PROCESSOR MODEL 4 DATA SHEET™, No. 23792, Rev. K, November 2001, Advanced Micro Devices, Inc.
C	N	"MANUAL FOR KINETIZ 7T", 2000, QDI Computer, Inc. (USA)
C	O	"VT82C686A 'SUPER SOUTH' SOUTH BRIDGE", 02/25/00, Rev. 1.54, VIA Technologies, Inc.

Examiner	CAO	Date Considered	6/7/05

Examiner: Initial citation considered. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

Index of Claims

Application/Control No.	Applicant(s)/Patent under Reexamination
09/694,433	READ ET AL.
Examiner	**Art Unit**
Chun Cao	2115

√	Rejected	–	(Through numeral) Cancelled	N	Non-Elected	A	Appeal
=	Allowed	÷	Restricted	I	Interference	O	Objected

Claim		Date
Final	Original	6/7/05
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UNITED STATES PATENT AND TRADEMARK OFFICE

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www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/694,433	10/23/2000	Andrew Read	TRANS59	3072

7590 11/10/2005

WAGNER, MURABITO & HAO LLP
TWO NORTH MARKET STREET
THIRD FLOOR
SAN JOSE, CA 95113

EXAMINER	
CAO, CHUN	

ART UNIT	PAPER NUMBER
2115	

DATE MAILED: 11/10/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

PTO-90C (Rev. 10/03)

Interview Summary	Application No.	Applicant(s)	
	09/694,433	READ ET AL.	
	Examiner	Art Unit	
	Chun Cao	2115	

All participants (applicant, applicant's representative, PTO personnel):

(1) *Chun Cao*. (3)_____.

(2) *Neal Osborn*. (4)_____.

Date of Interview: *07 November 2005*.

Type: a)☒ Telephonic b)☐ Video Conference
c)☐ Personal [copy given to: 1)☐ applicant 2)☐ applicant's representative]

Exhibit shown or demonstration conducted: d)☐ Yes e)☒ No.
If Yes, brief description: _____.

Claim(s) discussed: *1,4,5 and 7*.

Identification of prior art discussed: *US patent 6,118,306; "Re: AX64Pro or AK72?", NewsReader; AMD Athlon Processor Module Data Sheet*.

Agreement with respect to the claims f)☐ was reached. g)☐ was not reached. h)☒ N/A.

Substance of Interview including description of the general nature of what was agreed to if an agreement was reached, or any other comments: *Final rejection was discussed. Applicant argued that the cited references do not teach the claimed limitations in claims 1, 4, 5 and 7. Examiner agreed to further review the cited references in light of today's discussion, and then further discuss the claims in the next interview*.

(A fuller description, if necessary, and a copy of the amendments which the examiner agreed would render the claims allowable, if available, must be attached. Also, where no copy of the amendments that would render the claims allowable is available, a summary thereof must be attached.)

THE FORMAL WRITTEN REPLY TO THE LAST OFFICE ACTION MUST INCLUDE THE SUBSTANCE OF THE INTERVIEW. (See MPEP Section 713.04). If a reply to the last Office action has already been filed, APPLICANT IS GIVEN A NON-EXTENDABLE PERIOD OF THE LONGER OF ONE MONTH OR THIRTY DAYS FROM THIS INTERVIEW DATE, OR THE MAILING DATE OF THIS INTERVIEW SUMMARY FORM, WHICHEVER IS LATER, TO FILE A STATEMENT OF THE SUBSTANCE OF THE INTERVIEW. See Summary of Record of Interview requirements on reverse side or on attached sheet.

Examiner Note: You must sign this form unless it is an Attachment to a signed Office action.

Examiner's signature, if required

Summary of Record of Interview Requirements

Manual of Patent Examining Procedure (MPEP), Section 713.04, Substance of Interview Must be Made of Record
A complete written statement as to the substance of any face-to-face, video conference, or telephone interview with regard to an application must be made of record in the application whether or not an agreement with the examiner was reached at the interview.

Title 37 Code of Federal Regulations (CFR) § 1.133 Interviews
Paragraph (b)
In every instance where reconsideration is requested in view of an interview with an examiner, a complete written statement of the reasons presented at the interview as warranting favorable action must be filed by the applicant. An interview does not remove the necessity for reply to Office action as specified in §§ 1.111, 1.135. (35 U.S.C. 132)

37 CFR §1.2 Business to be transacted in writing.
All business with the Patent or Trademark Office should be transacted in writing. The personal attendance of applicants or their attorneys or agents at the Patent and Trademark Office is unnecessary. The action of the Patent and Trademark Office will be based exclusively on the written record in the Office. No attention will be paid to any alleged oral promise, stipulation, or understanding in relation to which there is disagreement or doubt.

The action of the Patent and Trademark Office cannot be based exclusively on the written record in the Office if that record is itself incomplete through the failure to record the substance of interviews.

It is the responsibility of the applicant or the attorney or agent to make the substance of an interview of record in the application file, unless the examiner indicates he or she will do so. It is the examiner's responsibility to see that such a record is made and to correct material inaccuracies which bear directly on the question of patentability.

Examiners must complete an Interview Summary Form for each interview held where a matter of substance has been discussed during the interview by checking the appropriate boxes and filling in the blanks. Discussions regarding only procedural matters, directed solely to restriction requirements for which interview recordation is otherwise provided for in Section 812.01 of the Manual of Patent Examining Procedure, or pointing out typographical errors or unreadable script in Office actions or the like, are excluded from the interview recordation procedures below. Where the substance of an interview is completely recorded in an Examiners Amendment, no separate Interview Summary Record is required.

The Interview Summary Form shall be given an appropriate Paper No., placed in the right hand portion of the file, and listed on the "Contents" section of the file wrapper. In a personal interview, a duplicate of the Form is given to the applicant (or attorney or agent) at the conclusion of the interview. In the case of a telephone or video-conference interview, the copy is mailed to the applicant's correspondence address either with or prior to the next official communication. If additional correspondence from the examiner is not likely before an allowance or if other circumstances dictate, the Form should be mailed promptly after the interview rather than with the next official communication.

The Form provides for recordation of the following information:
- Application Number (Series Code and Serial Number)
- Name of applicant
- Name of examiner
- Date of interview
- Type of interview (telephonic, video-conference, or personal)
- Name of participant(s) (applicant, attorney or agent, examiner, other PTO personnel, etc.)
- An indication whether or not an exhibit was shown or a demonstration conducted
- An identification of the specific prior art discussed
- An indication whether an agreement was reached and if so, a description of the general nature of the agreement (may be by attachment of a copy of amendments or claims agreed as being allowable). Note: Agreement as to allowability is tentative and does not restrict further action by the examiner to the contrary.
- The signature of the examiner who conducted the interview (if Form is not an attachment to a signed Office action)

It is desirable that the examiner orally remind the applicant of his or her obligation to record the substance of the interview of each case. It should be noted, however, that the Interview Summary Form will not normally be considered a complete and proper recordation of the interview unless it includes, or is supplemented by the applicant or the examiner to include, all of the applicable items required below concerning the substance of the interview.

A complete and proper recordation of the substance of any interview should include at least the following applicable items:
1) A brief description of the nature of any exhibit shown or any demonstration conducted,
2) an identification of the claims discussed,
3) an identification of the specific prior art discussed,
4) an identification of the principal proposed amendments of a substantive nature discussed, unless these are already described on the Interview Summary Form completed by the Examiner,
5) a brief identification of the general thrust of the principal arguments presented to the examiner,
   (The identification of arguments need not be lengthy or elaborate. A verbatim or highly detailed description of the arguments is not required. The identification of the arguments is sufficient if the general nature or thrust of the principal arguments made to the examiner can be understood in the context of the application file. Of course, the applicant may desire to emphasize and fully describe those arguments which he or she feels were or might be persuasive to the examiner.)
6) a general indication of any other pertinent matters discussed, and
7) if appropriate, the general results or outcome of the interview unless already described in the Interview Summary Form completed by the examiner.

Examiners are expected to carefully review the applicant's record of the substance of an interview. If the record is not complete and accurate, the examiner will give the applicant an extendable one month time period to correct the record.

Examiner to Check for Accuracy

If the claims are allowable for other reasons of record, the examiner should send a letter setting forth the examiner's version of the statement attributed to him or her. If the record is complete and accurate, the examiner should place the indication, "Interview Record OK" on the paper recording the substance of the interview along with the date and the examiner's initials.

AF

Attorney Docket No.: TRAN-P059

IFW 2185

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

I hereby certify that this transmittal of the below described document is being deposited with the United States Postal Service in an envelope bearing First Class Postage and addressed to the Commissioner for Patents P.O. Box 1450, Alexandria, VA 22313-1450, on the below date of deposit.					
Date of Deposit:	11/23/05	Name of Person Making the Deposit:	KATHERINE RINALDI	Signature of the Person Making the Deposit:	Katherine Rinaldi

In re Application of: Andrew Read, Sameer Halapete and Keith Klayman

Application No.: 09/694,433 Examiner: CAO, CHUN

Filed: 10/23/00 Art Unit: 2185

Confirmation No.: 3072

For: SAVING POWER WHEN IN OR TRANSITIONING TO A STATIC MODE OF A PROCESSOR (AS AMENDED)

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

AMENDMENT TRANSMITTAL

1. Transmitted herewith is an amendment for this application

X Transmitted herewith is a response to an office action for the above identified patent application. (4 sheets)

2. Applicant is other than a small entity

Extension of Term

3. The proceedings herein are for a patent application and the provisions of 37 C.F.R. 1.136 apply.

(a) [X] Applicant petitions for an extension of time under 37 C.F.R. 1.136 (fees: 37 C.F.R. 1.17(a)-(d) for the total number of months checked below:)

Extension	Fee
[ ] one month	$120.00
[ ] two months	$450.00
[X] three months	$1,020.00
[ ] four months	$1,590.00

Fee $ 1,020.00

If an additional extension of time is required, please consider this a petition therefor.

(b) [ ] Applicant believes that no extension of term is required. However, this conditional petition is being made to provide for the possibility that applicant has inadvertently overlooked the need for a petition for extension of time.

rev. 11/98 kgr

Fee Calculation

4. The fee for claims (37 C.F.R. 1.16(b)-(d)) has been calculated as shown below:

(for other than a small entity)					
Fee Items	Claims Remaining After Amendment	Highest Number of Claims Previously Paid For	Present Extra Claims	Fee Rate	Total
Total Claims	18	- 37 =	0	x $50.00	$0.00
Independent Claims	8	- 8 =	0	x $200.00	$0.00
Multiple Dependent Claim Fee (one or more, first added by this amendment)				$300.00	$0.00
Total Fees					$0.00

PAYMENT OF FEES

5. The full fee due in connection with this communication is provided as follows:

[x] The Commissioner is hereby authorized to charge any additional fees associated with this communication or credit any overpayment to Deposit Account No.: 23-0085. A duplicate copy of this authorization is enclosed.

[x] A check in the amount of $1,020.00

[ ] Charge any fees required or credit any overpayments associated with this filing to Deposit Account No.: 23-0085.

Please direct all correspondence concerning the above-identified application to the following address:

WAGNER, MURABITO & HAO LLP
Two North Market Street, Third Floor
San Jose, California 95113
(408) 938-9060
Confirmation No.: 45590

Respectfully submitted,

Date: 11/23/2005

By: _____
Anthony C. Murabito
Reg. No. 35,295

rev. 11/98 kgr

TRAN-P059 PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of: Read, et al.

Serial:	09/694,433	Group Art Unit: 2115
Filed:	October 23, 2000	Examiner: Cao, Chun
For:	STATIC POWER CONTROL (As Filed)	

Honorable Commissioner for Patents
PO Box 1450
Alexandria, VA 22313-1450

RESPONSE

Dear Sir:

In response to the Office Action mailed June 9, 2005 in the above captioned case, Applicants respectfully request the Examiner to consider the following remarks.

REMARKS

Claims remaining in the present application are 1-18. The Applicants respectfully request reconsideration of the above captioned patent application.

Examiner Interview Summary

On November 7, 2005, Applicants' representatives conducted an Examiner Interview with Examiner Cao via telephone. The cited prior art and the current rejection were discussed. Applicants agreed to submit the instant response.

Applicants thank Examiner Cao for the interview.

35 U.S.C. §102

Claims 5-11 and 13 are rejected under 35 U.S.C. §102(a) or (e) as being allegedly anticipated by Orton et al., U.S. 6,118,306 ("Orton"). Applicants have carefully reviewed the cited reference and respectfully assert that Orton does not anticipate or render obvious embodiments in accordance with the present invention as recited in Claims 5-11 and 13.

Applicants respectfully request reconsideration of this rejection.

35 U.S.C. § 103

Claims 1-3 are rejected under 35 U.S.C. §103(a) as being allegedly unpatentable over Orton et al., U.S. 6,118,306 ("Orton") in view of "AX64PRO OR AK72?," Newsreader, June 15, 2000 ("Newsreader"). Applicants have carefully reviewed the cited references and respectfully assert that Orton in view of Newsreader does not render obvious embodiments in accordance with the present invention as recited in Claims 1-3.

Applicants respectfully request reconsideration of this rejection.

Claims 4, 12 and 14-18 are rejected under 35 U.S.C. §103(a) as being allegedly unpatentable over Orton in view of Applicant Admitted Prior Art (APA). Applicants have carefully reviewed the cited references and respectfully assert that Orton in view of APA does not render obvious embodiments in accordance with the present invention as recited in Claims 4, 12 and 14-18.

Applicants respectfully request reconsideration of this rejection.

CONCLUSION

Claims remaining in the present application are 1-18. The Applicants respectfully request reconsideration of the above captioned patent application.

The Examiner is invited to contact Applicant's undersigned representative if the Examiner believes such action would expedite resolution of the present application.

Please charge any additional fees or apply any credits to our PTO deposit account number: 23-0085.

Respectfully submitted,
WAGNER, MURABITO & HAO LLP

Date: 11/23/2005

Anthony C. Murabito
Reg. No. 35,295

Two North Market Street
Third Floor
San Jose, California 95113
(408) 938-9060

	Type	Hits	Search Text	DBs
60	BRS	0	maxim near2 "1711"	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB
61	BRS	13516	maxim	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB
62	BRS	151	S61 near5 regulator$1	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB
63	BRS	6	S62 and g06f$.ipc.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB
64	BRS	11	S62 same feedback	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB
65	BRS	0	S55 and "713"/$.ccls.	USPAT
66	BRS	6	S55 same reduc$3	USPAT
67	BRS	1448	feedback with (voltage near3 regulator$1)	USPAT
68	BRS	206	S67 with (reduc$3 adjust$3 increas$3)	USPAT
69	BRS	6	S68 and "713"/$.ccls.	USPAT
70	BRS	50	feedback with (voltage near3 regulator$1) with (reduc$3 increas$3 decreas$3)	EPO; JPO; DERWENT

	Type	Hits	Search Text	DBs
71	BRS	0	S70 and g06f$.ipc.	EPO; JPO; DERWENT
72	BRS	1	"6920571"	USPAT
73	BRS	11	("5528127" | "5632039" | "5764529" | "5925133" | "6035358" | "6100673" | "6106565" | "6223297" | "6457135" | "6459175" | "6538419").PN. OR ("6920571").URPN.	US-PGPUB; USPAT; USOCR
74	BRS	115	(loop) with (voltage near3 regulator$1) with (reduc$3 increas$3 decreas$3)	US-PGPUB; USPAT; USOCR; IBM_TDB
75	BRS	21	(loop) with (voltage near3 regulator$1) with (reduc$3 increas$3 decreas$3)	EPO; JPO; DERWENT
76	BRS	0	S74 same close$1	EPO; JPO; DERWENT
77	BRS	18	S75 with close$1	US-PGPUB; USPAT; USOCR; IBM_TDB
78	BRS	15	S77 and resistor$1	US-PGPUB; USPAT; USOCR; IBM_TDB
79	BRS	1	maxim.as. and ((voltage adj1 regulator$1) same (close$1 near1 loop))	US-PGPUB; USPAT; USOCR; IBM_TDB
80	BRS	8	("4893228" | "5905370" | "5969515").PN. OR ("6208127").URPN.	US-PGPUB; USPAT; USOCR
81	BRS	2	maxim.as. and ((voltage adj1 regulator$1) same (step-down))	US-PGPUB; USPAT; USOCR; IBM_TDB
82	BRS	495	((voltage adj1 regulator$1) same (step-down))	US-PGPUB; USPAT; USOCR; IBM_TDB

	Type	Hits	Search Text	DBs
83	BRS	9	S82 same (close$1 near1 loop)	US-PGPUB; USPAT; USOCR; IBM_TDB

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
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www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/694,433	10/23/2000	Andrew Read	TRANS59	3072

7590 12/14/2005

WAGNER, MURABITO & HAO LLP
TWO NORTH MARKET STREET
THIRD FLOOR
SAN JOSE, CA 95113

EXAMINER	
CAO, CHUN	
ART UNIT	**PAPER NUMBER**
2115	

DATE MAILED: 12/14/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

PTO-90C (Rev. 10/03)

Office Action Summary	Application No.	Applicant(s)	
	09/694,433	READ ET AL.	
	Examiner	Art Unit	
	Chun Cao	2115	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *28 November 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-37* is/are pending in the application.

4a) Of the above claim(s) *19-37* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-18* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAIL ACTION

1. Claims 1-37 are presented for examination. Claims 19-37 are newly added claims and presented for examination.

2. The text of those applicable section of Title 35, U.S. Code not included in this action can be found in the prior Office Action.

3. Applicant's response for the finality of rejection of the last office action is persuasive, therefore the finality of that action is hereby withdrawn, and the prosecution on the merit is hereby reopened.

Election/Restrictions

4. Newly submitted claims 19-37 are directed to an invention that is independent or distinct from the invention originally claimed for the following reasons:

Original claims 1-18, drawn to: reducing power utilized by a processor, and reducing core voltage to the processor to a value sufficient to maintain state during the mode in which system clock is disable, classified in class 713, subclass 322.

Newly added claims 19-37, drawn to: a computer system has a first transition time and second transition for transitioning from sleep voltage to an operating voltage, wherein the first transition time is greater than an allowed time, classified in class 713, subclass 310.

a. These inventions have acquired a separate status in the art as shown by their different classification;

b. The search required for one Group is not required for the other Groups for the reasons above restriction for examination purpose as indicated is proper.

Since applicant has received an action on the merits for the originally presented invention, this invention has been constructively elected by original presentation for prosecution on the merits. Accordingly, claims 19-37 are withdrawn from consideration as being directed to a non-elected invention. See 37 CFR 1.142(b) and MPEP § 821.03.

5. Claims 1-3, 5-11 and 13 are rejected under 35 U.S.C. 102(e) as being anticipated by Pole, II et al. (Pole), US patent no. 6,675,304.

Pole is a prior art reference cited in prior office action in IDS paper no. 20040917.

As per claim 1, Pole teaches a method for reducing power utilized by a processor [fig. 5] comprising the steps of:

determining that a processor is transitioning from a computing mode to a mode in which system clock to the processor is disabled [col. 1, lines 30-34; col. 4, lines 15-32; col. 5, lines 10-16]; and

reducing core voltage to the processor to a value sufficient to maintain state during the mode in which system clock is disable [col. 4, lines 15-40], wherein said value of the core voltage is not sufficient to maintain processing activity in said processor [deep sleep state, col. 1, line 30-34].

As per claim 2, Pole teaches of determining the processor is transitioning from a computing mode to a mode in which system clock to the processor is disabled comprises monitoring a stop clock signal [col. 4, lines 15-40; col. 5, lines 10-16].

As per claim 3, Pole teaches of reducing core voltage to the processor to a value sufficient to maintain state during the state in which system clock is disabled [col. 1, lines 30-34] comprises: furnishing an input to reduce an output voltage provided by a voltage regulator furnishing core voltage to the processor [col. 3, lines 31-67].

As per claim 5, Pole teaches a method for reducing power utilized by a processor [fig. 5] comprising the steps of:

determining that a processor is transitioning from a computing mode to a mode is which system clock to the processor is disabled [col. 1, lines 30-34; col. 4, lines 15-32; col. 5, lines 10-16];

reducing core voltage to the processor to a value sufficient to maintain state during the mode of which system clock is disable [col. 4, lines 15-40]; and

transferring operation of a voltage regulator furnishing core voltage in a mode in which power is dissipated during reductions in core voltage to a mode in which power is saved during a voltage transition when it is determined at a processor is transitioning from a computing mode to a mode is which system clock to the processor is disabled [col. 1, lines 30-34; col. 4, lines 15-40; col. 5, lines 10-16].

As per claim 6, Pole teaches of returning the voltage regulator to its original mode of operation when the value of the core voltage sufficient to maintain state during the mode in which system clock is disabled is reached [col. 1, lines 30-34; col. 4, lines 15-40; col. 5, lines 10-16].

6. As per claim 7, Pole discloses a circuit [fig. 2] for providing a regulated voltage to a processor comprising:

a voltage regulator [52, figures 1, 2] having: an output terminal [col. 3, lines 31-55; " the output from the voltage regulator 52", inherently, there is an output terminal in the voltage regulator 52] providing a selectable voltage [col. 3, lines 43-50, "...adjust the voltage level supplied by the voltage regulator 52 up or down" and "to indicate that the voltage level from the voltage regulator 52 is changing"];

input terminal [fig. 2] for receiving signals indicating the selectable voltage level [col. 3, lines 31-55];

means for providing signal at the input terminal of the voltage regulator for selecting a voltage for operating the processor in a computing mode and a voltage of a level less than that for operating the processor in computing mode [col. 4, lines 2-11], wherein the level less than that for operating the processor in a computing mode is sufficient to maintain state of the processor [col. 1, lines 30-34; col. 4, lines 15-40; col. 5, lines 10-16].

As per claim 8, Pole discloses that the voltage regulator comprises means for accepting binary signals [LO/HI signals] indicating different voltage level [fig. 2; col. 3, lines 43-61; "A signal VR_LO/HI#...adjust the voltage level supplied by the voltage regulator 52 up or down"].

As per claim 9, Pole discloses that the voltage regulator comprises:

Selection circuitry, means for furnishing a plurality of signals at the input to the selection circuitry and means for controlling the selection by the selection circuitry [fig. 2; col. 3, lines 31-67].

As per claim 10, Pole discloses a multiplexor and means for controlling the selection by the selection circuitry including a control terminal for receiving signals indicating a system clock to the processor is being terminated [fig. 2; col. 3, lines 31-67].

7. As per claim 11, Pole discloses a circuit [fig. 2] for providing a regulated voltage to a processor comprising:

a voltage regulator [52, figures 1, 2] having: an output terminal [col. 3, lines 31-55; " the output from the voltage regulator 52", inherently, there is an output terminal in the voltage regulator 52] providing a selectable voltage [col. 3, lines 43-50, "...adjust the voltage level supplied by the voltage regulator 52 up or down" and "to indicate that the voltage level from the voltage regulator 52 is changing"];

input terminal [fig. 2] for receiving signals indicating the selectable voltage level [col. 3, lines 31-55];

means for providing signal at the input terminal of the voltage regulator for selecting a voltage for operating the processor in a computing mode and a voltage of a level less than that for operating the processor in computing mode [col. 4, lines 2-11], means for reducing the selectable voltage below a lowest level the voltage regulator is specified to output [col. 1, lines 30-34; col. 4, lines 15-40; col. 5, lines 10-16].

8. As per claim 13, Pole discloses a circuit [fig. 2] for providing a regulated voltage to a processor comprising:

a voltage regulator [52, figures 1, 2] having: an output terminal [col. 3, lines 31-55; " the output from the voltage regulator 52", inherently, there is an output terminal in the voltage regulator 52] providing a selectable voltage [col. 3, lines 43-50, "...adjust the voltage level supplied by the voltage regulator 52 up or down" and "to indicate that the voltage level from the voltage regulator 52 is changing"];

input terminal [fig. 2] for receiving signals indicating the selectable voltage level [col. 3, lines 31-55];

means for providing signal at the input terminal of the voltage regulator for selecting a voltage for operating the processor in a computing mode and a voltage of a level less than that for operating the processor in computing mode [col. 4, lines 2-11],

circuitry for conserving charge [battery 60] stored by the voltage regulator when the selectable voltage decreases; and means for enabling the circuitry for conserving charge stored by the voltage regulator when the selectable voltage decreases [col. 3, lines 43-67; col. 4, lines 15-40; col. 5, lines 10-16].

9. Claims 4, 12 and 14-18 are rejected under 35 U.S.C. 103 (a) as being unpatentable over Pole, II et al. (Pole), US patent no. 6,675,304 in view of Applicant Admitted Prior Art (AAPA) and "High-speed, Digitally adjusted step-down controllers for notebook CPUs" Maxim, July 2000, pages 1-28 (hereinafter "Maxim).

As per claim 4, Pole teaches a method for reducing power utilized by a processor [fig. 5] comprising the steps of:

determining that a processor is transitioning from a computing mode to a mode in which system clock to the processor is disabled [col. 1, lines 30-34; col. 4, lines 15-32; col. 5, lines 10-16]; and

reducing core voltage to the processor to a value sufficient to maintain state during the mode in which system clock is disable [col. 4, lines 15-40] by:

furnishing an input to reduce an output voltage provided by a voltage regulator furnishing core voltage to the processor [col. 3, lines 31-67]; and

providing a control signal to the voltage regulator to reduce its output voltage below a specified output voltage [col. 4, lines 5-7].

Pole does not explicitly teach of providing a feedback to the voltage regulator.

AAPA teaches of providing a feedback to the voltage regulator [Maxim 1711, page 10, lines 6-9].

Furthermore, Maxim teaches a Maxim 1711 is a step-down controller, wherein Maxim 1711 is implemented in a computer system to reduce voltage level to a CPU core [see page 1].

It would have been obvious to one of ordinary skill in the art at time the invention to combine the teachings of Pole and AAPA because the specify teachings of AAPA stated above would allow the processor to run stable and reliable by adjusting the core voltage accordingly.

As per claim 18, Pole teaches that the output voltage to which said voltage regulator is reduced depends upon output voltage of said voltage regulator prior to

furnishing the input to reduce the output voltage provided by the voltage regulator [col. 3, lines 43-67].

10. As per claim 12, Pole discloses a circuit [fig. 2] for providing a regulated voltage to a processor comprising:

a voltage regulator [52, figures 1, 2] having: an output terminal [col. 3, lines 31-55; " the output from the voltage regulator 52", inherently, there is an output terminal in the voltage regulator 52] providing a selectable voltage [col. 3, lines 43-50, "...adjust the voltage level supplied by the voltage regulator 52 up or down" and "to indicate that the voltage level from the voltage regulator 52 is changing"];

input terminal [fig. 2] for receiving signals indicating the selectable voltage level [col. 3, lines 31-55];

means for providing signal at the input terminal of the voltage regulator for selecting a voltage for operating the processor in a computing mode and a voltage of a level less than that for operating the processor in computing mode [col. 4, lines 2-11],

means for reducing the selectable voltage below a level provided by the voltage regulator [col. 4, lines 2-11].

Pole does not explicitly disclose a voltage regulator feedback circuit and a voltage divider network.

AAPA discloses a voltage regulator including a voltage regulator feedback circuit and a voltage divider network [page 10, lines 6-9].

Furthermore, Maxim teaches a Maxim 1711 is a step-down controller with a voltage divider network [see page 1], wherein Maxim 1711 is implemented in a computer system to reduce voltage level to a CPU core [see page 1].

It would have been obvious to one of ordinary skill in the art at time the invention to combine the teachings of Orton and AAPA because the specify teachings of AAPA stated above would allow the processor to run stable and reliable by adjusting the core voltage accordingly.

As per claim 14 is contained same limitations as set forth in claim 12. Therefore, same rejection is applied.

As per claim 15, Pole teaches that the first voltage is for operating the processor in a computing mode and the second voltage is a level less than that for operating the processor in the computing mode [col. 4, lines 2-7].

As to claims 16 and 17, Maxim discloses that the feedback circuit comprises a voltage divider [see page 1].

Response to Arguments

11. Applicant's arguments filed on 11/28/05 have been fully considered but are moot in view of new ground(s) of rejection.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Chun Cao whose telephone number is 571-272-3664. The examiner can normally be reached on Monday-Friday from 7:30 am-4:00 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Thomas C. Lee can be reached on 571-272-3667. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Any inquiry of a general nature or relating to the status of this application should be directed to the Group receptionist whose telephone number is 571-272-2100.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

CHUN CAO
PRIMARY EXAMINER

Dec 9, 2005

Notice of References Cited	Application/Control No. 09/694,433	Applicant(s)/Patent Under Reexamination READ ET AL.	
	Examiner Chun Cao	Art Unit 2115	Page 1 of 1

U.S. PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Name	Classification
*	A	US-5,528,127 A	06-1996	Streit, Lawrence C.	323/269
*	B	US-6,208,127 B1	03-2001	Doluca, Tun.cedilla.	323/349
*	C	US-6,047,248	04-2000	Georgiou et al.	702/132
*	D	US-6,457,135	09-2002	Cooper, Barnes	713/323
	E	US-			
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	J	US-			
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	L	US-			
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FOREIGN PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Country	Name	Classification
	N					
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	P					
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	S					
	T					

NON-PATENT DOCUMENTS

*		Include as applicable: Author, Title Date, Publisher, Edition or Volume, Pertinent Pages)
	U	"high-speed step-doen controller with synchronous rectification for CPU power", Maxim, pages 1-16.
	V	"High-speed, Digitally Adjusted step-down controllers for notebook CPUs", Maxim, July 2000, pages 1-28.
	W	
	X	

*A copy of this reference is not being furnished with this Office action. (See MPEP § 707.05(a).)
Dates in MM-YYYY format are publication dates. Classifications may be US or foreign.

Index of Claims

Application/Control No.	Applicant(s)/Patent under Reexamination
09/694,433	READ ET AL.
Examiner	**Art Unit**
Chun Cao	2115

√	Rejected	–	(Through numeral) Cancelled	N	Non-Elected	A	Appeal
=	Allowed	÷	Restricted	I	Interference	O	Objected

Claim		Date
Final	Original	12/9/05
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Search Notes	Application/Control No.	Applicant(s)/Patent under Reexamination	
	09/694,433	READ ET AL.	
	Examiner	Art Unit	
	Chun Cao	2115	

SEARCHED			
Class	Subclass	Date	Examiner

INTERFERENCE SEARCHED			
Class	Subclass	Date	Examiner

SEARCH NOTES (INCLUDING SEARCH STRATEGY)		
	DATE	EXMR
east search	12/9/2005	CC

Attorney Docket No.: TRAN-P059

2115
IFW

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

I hereby certify that this transmittal of the below described document is being deposited with the United States Postal Service in an envelope bearing First Class Postage and addressed to the Commissioner for Patents P.O. Box 1450, Alexandria, VA 22313-1450, on the below date of deposit.					
Date of Deposit:	3/2/06	Name of Person Making the Deposit:	Mina Oliveri	Signature of the Person Making the Deposit:	Mina Oliveri

In re Application of: Andrew Read, Sameer Halapete and Keith Klayman

Application No.: 09/694,433 Examiner: Cao, Chun

Filed: October 23, 2000 Art Unit: 2115

Confirmation No.: 3072

For: STATIC POWER CONTROL (As Filed)

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

AMENDMENT TRANSMITTAL

1. Transmitted herewith is an amendment for this application

X Transmitted herewith is a response to an office action for the above identified patent application. (22 sheets)
____ Transmitted herewith are _____ sheets of substitute formal drawings.
____ Other:

2. Applicant is other than a small entity

Extension of Term

3. The proceedings herein are for a patent application and the provisions of 37 C.F.R. 1.136 apply.

(a) [ ] Applicant petitions for an extension of time under 37 C.F.R. 1.136 (fees: 37 C.F.R. 1.17(a)-(d) for the total number of months checked below:)

Extension	Fee
[ ] one month	$120.00
[ ] two months	$450.00
[ ] three months	$1,020.00
[ ] four months	$1,590.00
[ ] five months	$2,160.00
	Fee $ _____

If an additional extension of time is required, please consider this a petition therefor.

rev. 10/04 kgr

(b) [x] Applicant believes that no extension of term is required. However, this conditional petition is being made to provide for the possibility that applicant has inadvertently overlooked the need for a petition for extension of time.

Fee Calculation

4. The fee for claims (37 C.F.R. 1.16(b)-(d)) has been calculated as shown below:

(for other than a small entity)					
Fee Items	Claims Remaining After Amendment	Highest Number of Claims Previously Paid For	Present Extra Claims	Fee Rate	Total
Total Claims	18	- 37 =	0	x $50.00	$0.00
Independent Claims	8	- 8 =	0	x $200.00	$0.00
Multiple Dependent Claim Fee (one or more, first added by this amendment)				$360.00	
Total Fees					$0.00

PAYMENT OF FEES

5. The full fee due in connection with this communication is provided as follows:

[x] The Commissioner is hereby authorized to charge any additional fees associated with this communication or credit any overpayment to Deposit Account No.: 23-0085.
A duplicate copy of this authorization is enclosed.

[ ] A check in the amount of $

[ ] Charge any fees required or credit any overpayments associated with this filing to Deposit Account No.: 23-0085.

Please direct all correspondence concerning the above-identified application to the following address:

WAGNER, MURABITO & HAO LLP
Two North Market Street, Third Floor
San Jose, California 95113
(408) 938-9060
Customer No:45590

Respectfully submitted,

Date: March 8, 2006

By: _____
Anthony C. Murabito
Reg. No. 35,295

rev. 10/04 kgr

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of: Read, et al.

Serial:	09/694,433	Group Art Unit: 2115
Filed:	October 23, 2000	Examiner: Cao, Chun
For:	STATIC POWER CONTROL (As Filed)	

Honorable Commissioner for Patents
PO Box 1450
Alexandria, VA 22313-1450

RESPONSE

Dear Sir:

In response to the Office Action mailed December 14, 2005 in the above captioned case, Applicants respectfully request the Examiner to consider the following remarks.

IN THE CLAIMS:

1. (Previously Presented) A method for reducing power utilized by a processor comprising the steps of:

determining that a processor is transitioning from a computing mode to a mode in which system clock to the processor is disabled, and

reducing core voltage to the processor to a value sufficient to maintain state during the mode in which system clock is disabled, wherein said value of the core voltage is not sufficient to maintain processing activity in said processor.

Claim 2. (Previously Presented) A method as claimed in Claim 1 in which the step of determining that a processor is transitioning from a computing mode to a mode in which system clock to the processor is disabled comprises monitoring a stop clock signal.

Claim 3. (Original) A method as claimed in Claim 1 in which the step of reducing core voltage to the processor to a value sufficient to maintain state during the state in which system clock is disabled comprises furnishing an input to reduce an output voltage provided by a voltage regulator furnishing core voltage to the processor.

Claim 4. (Previously Presented) A method for reducing power utilized by a processor comprising the steps of:

determining that a processor is transitioning from a computing mode to a mode in which system clock to the processor is disabled, and

reducing core voltage to the processor to a value sufficient to maintain state during the mode in which system clock is disabled by:

furnishing an input to reduce an output voltage provided by a voltage regulator furnishing core voltage to the processor, and

providing a feedback signal to the voltage regulator to reduce its output voltage below a specified output voltage.

Claim 5. (Previously Presented) A method for reducing power utilized by a processor comprising the steps of:

determining that a processor is transitioning from a computing mode to a mode in which system clock to the processor is disabled,

reducing core voltage to the processor to a value sufficient to maintain state during the mode in which system clock is disabled, and

transferring operation of a voltage regulator furnishing core voltage in a mode in which power is dissipated during reductions in core voltage to a mode in which power is saved during a voltage transition when it is determined that a processor is transitioning from a computing mode to a mode is which system

clock to the processor is disabled.

Claim 6. (Previously Presented) A method as claimed in Claim 5 further comprising the steps of returning the voltage regulator to its original mode of operation when the value of the core voltage sufficient to maintain state during the mode in which system clock is disabled is reached.

Claim 7. (Previously Presented) A circuit for providing a regulated voltage to a processor comprising:

a voltage regulator having:

an output terminal providing a selectable voltage, and

an input terminal for receiving signals indicating the selectable voltage level;

means for providing signals at the input terminal of the voltage regulator for selecting a voltage for operating the processor in a computing mode and a voltage of a level less than that for operating the processor in a computing mode, wherein the level less than that for operating the processor in a computing mode is sufficient to maintain state of the processor.

Claim 8. (Original) A circuit as claimed in Claim 7 in which the means for providing signals at the input terminal of the voltage regulator comprises means for accepting binary signals indicating different levels of voltage.

Claim 9. (Original) A circuit as claimed in Claim 7 in which the means for providing signals at the input terminal of the voltage regulator comprises:

selection circuitry,

means for furnishing a plurality of signals at the input to the selection circuitry, and

means for controlling the selection by the selection circuitry.

Claim 10. (Original) A circuit as claimed in Claim 9 in which:

the selection circuitry is a multiplexor, and

the means for controlling the selection by the selection circuitry includes a control terminal for receiving signals indicating a system clock to the processor is being terminated.

Claim 11. (currently amended) A circuit for providing a regulated voltage to a processor comprising:

a voltage regulator having:

an output terminal providing a selectable voltage, and

an input terminal for receiving signals indicating the selectable voltage level;

means for providing signals at the input terminal of the voltage regulator for selecting a voltage for operating the processor in a computing mode and a voltage of a level less than that for operating the processor in a computing mode; and

means for reducing the selectable voltage below a level ~~provided~~ specified by the voltage regulator.

Claim 12. (Previously Presented) A circuit for providing a regulated voltage to a processor comprising:

a voltage regulator having:

an output terminal providing a selectable voltage;

an input terminal for receiving signals indicating the selectable voltage level; and

a voltage regulator feedback circuit;

means for providing signals at the input terminal of the voltage regulator for selecting a voltage for operating the processor in a

computing mode and a voltage of a level less than that for operating the processor in a computing mode; and

means for reducing the selectable voltage below a level provided by the voltage regulator comprising:

a voltage divider network joined between the output terminal and a voltage source furnishing a value higher than the selectable voltage, and

the voltage regulator feedback circuit receiving a value from the voltage divider network.

Claim 13. (Previously Presented) A circuit for providing a regulated voltage to a processor comprising:

a voltage regulator having:

an output terminal providing a selectable voltage, and

an input terminal for receiving signals indicating the selectable voltage level;

means for providing signals at the input terminal of the voltage regulator for selecting a voltage for operating the processor in a computing mode and a

voltage of a level less than that for operating the processor in a computing mode;

circuitry for conserving charge stored by the voltage regulator when the selectable voltage decreases, and

means for enabling the circuitry for conserving charge stored by the voltage regulator when the selectable voltage decreases.

Claim 14. (Previously Presented) A circuit for providing a regulated voltage to a processor comprising:

a voltage regulator having:

an output terminal providing a selectable voltage, and

an input terminal for receiving signals indicating the selectable voltage level; and

a voltage regulator feedback circuit;

circuitry coupled to said input terminal and configured to provide signals to the input terminal for selecting a first voltage for operating the processor in a first mode and a second voltage for operating the processor in a second mode;

a voltage source furnishing a value higher than the selectable voltage; and

a feedback circuit coupled to the voltage source, the output terminal, and the voltage regulator feedback circuit.

15. (Previously Presented) The circuit of Claim 14, wherein the first voltage is for operating the processor in a computing mode and the second voltage is a level less than that for operating the processor in the computing mode.

16. (Previously Presented) The circuit of Claim 15, wherein the feedback circuit comprises a voltage divider.

17. (Previously Presented) The circuit of Claim 14, wherein the feedback circuit comprises a voltage divider.

18. (Previously Presented) The method of Claim 4, wherein the output voltage to which said voltage regulator is reduced depends upon output voltage of said voltage regulator prior to furnishing the input to reduce the output voltage provided by the voltage regulator.

19-37 (canceled) (election)

REMARKS

Claims remaining in the present application are 1-18. Claim 11 is amended herein. Claims 19-37 were canceled per the election referred to in a previous Official Action. The Applicants thank the Examiner for withdrawing the finality of the prior rejection. The Applicants respectfully request reconsideration of the above captioned patent application in view of the remarks presented herein.

35 U.S.C. §102

Claims 1-3, 5-11 and 13 are rejected under 35 U.S.C. §102(e) as being allegedly anticipated by Pole, II et al., U.S. 6,675,304 ("Pole"). Applicants have carefully reviewed the cited reference and respectfully assert that embodiments in accordance with the present invention as recited in Claims 1-3, 5-11 and 13 are patentable over Pole.

With respect to Claim 1, Applicants respectfully assert that Pole does not teach or fairly suggest the limitation "reducing core voltage to the processor to a value sufficient to maintain state during the mode in which system clock is disabled" as recited by Claim 1.

The referenced portion of Pole alleged to teach this claimed element, column 4 lines 15-40, may describe lowering an output voltage level, but Pole fails to teach that such lowered level is sufficient to maintain a processor's state, as recited by Claim 1.

For this reason, Applicants respectfully assert that Claim 1 overcomes the rejections of record, and respectfully solicit allowance of this Claim.

In addition, with respect to Claim 1, Pole teaches a deep sleep state in which only data stored in the processor's internal caches is maintained (column 1, lines 30-34). As is well known to those of ordinary skill in the art, a processor's state is not represented in the processor's internal caches, and includes, for example, the contents of internal registers which are not represented in the caches. Thus, Pole actually teaches away from the claimed embodiments in accordance with the present invention that recite maintaining processor state, as recited by Claim 1.

For this additional reason, Applicants respectfully assert that Claim 1 overcomes the rejections of record, and respectfully solicit allowance of this Claim.

Further with respect to Claim 1, Applicants respectfully assert that Pole does not teach or fairly suggest the limitation "wherein said value of the core

voltage is not sufficient to maintain processing activity in said processor" as recited by Claim 1.

While Pole may teach, "chang(ing) the voltage regulator setting from a higher to a lower output level" (column 4 lines 36-38), Applicants respectfully assert that Pole fails to teach or fairly suggest that such a "lower output level" is "not sufficient to maintain processing activity in said processor" as recited by Claim 1.

In addition, the rejection's citations to Pole column 5, lines 10-16 and column 1 lines 30-34 refer to clock activity, e.g., "the external clock to the processor is disabled," but are devoid of teachings related to "core voltage is not sufficient to maintain processing activity in said processor" as recited by Claim 1.

For these further reasons, Applicants respectfully assert that Claim 1 overcomes the rejections of record, and respectfully solicit allowance of this Claim.

Claims 2-3 depend from Claim 1. Applicants respectfully assert that Claims 2-3 overcome the rejections of record as they depend from an allowable claim, and respectfully solicit allowance of these Claims.

With respect to independent Claim 5, Applicants respectfully assert that Pole does not teach or fairly suggest the limitation "reducing core voltage to the processor to a value sufficient to maintain state during the mode in which system clock is disabled" as recited by Claim 5. As described previously with respect to Claim 1, the referenced portion of Pole may teach lowering an output voltage level, but does not teach that such lowered level is sufficient to maintain a processor's state, as recited by Claim 1.

For this reason, Applicants respectfully assert that Claim 5 overcomes the rejections of record, and respectfully solicit allowance of this Claim.

In addition, with respect to Claim 5, Pole teaches a deep sleep state in which only data stored in the processor's internal caches is maintained (column 1, lines 30-34). As is well known to those of ordinary skill in the art, a processor's state is not represented in the processor's internal caches, and includes, for example, the contents of internal registers which are not represented in the caches. Thus, Pole actually teaches away from the claimed embodiments in accordance with the present invention that recite maintaining processor state, as recited by Claim 5.

For this additional reason, Applicants respectfully assert that Claim 5 overcomes the rejections of record, and respectfully solicit allowance of this Claim.

Further, with respect to Claim 5, Applicants respectfully assert that Pole fails to teach or suggest the limitation:

> transferring operation of a voltage regulator furnishing core voltage in a mode in which power is dissipated during reductions in core voltage to a mode in which power is saved during a voltage transition when it is determined that a processor is transitioning from a computing mode to a mode is which system clock to the processor is disabled

as recited by Claim 5.

The underscored language refers to modes of operating a voltage regulator (power dissipation mode/power saving mode). Applicants respectfully assert that Pole fails to teach or suggest the limitations of Claim 5. Pole may discuss lowering a voltage level supplied to a processor. However, power savings can be achieved in manners other than reducing frequency and/or reducing voltage of a processor. Applicants have specifically recited in this embodiment that saving power is performed by a choice of mode of operation of the voltage regulator. Pole is silent as to any mode of operation of a voltage regulator, aside from outputting a plurality of voltages. Consequently, Pole is silent as to operating the voltage regulator in a mode in which power is dissipated to a mode in which power is saved, as claimed. Thus, Pole fails to teach or fairly suggest the claimed transferring the operation of

a voltage regulator from a mode in which power is dissipated to a mode in which power is saved, during a voltage transition.

For this further reason, Applicants respectfully assert that Claim 5 overcomes the rejections of record, and respectfully solicit allowance of this Claim.

Claim 6 depends from Claim 5. Applicants respectfully assert that Claim 6 overcomes the rejections of record as this claim depends from an allowable base claim, and respectfully solicit allowance of this Claim.

With respect to Claim 7, Applicants respectfully assert that Pole does not teach or fairly suggest the limitation "wherein the level less than that for operating the processor in a computing mode is sufficient to maintain state of the processor" as recited by Claim 7. As described previously with respect to Claim 1, the referenced portion of Pole may teach lowering an output voltage level, but does not teach that such lowered level is sufficient to maintain a processor's state, as recited by Claim 7.

For this reason, Applicants respectfully assert that Claim 7 overcomes the rejections of record, and respectfully solicit allowance of this Claim.

Claims 8-10 depend from Claim 7. Applicants respectfully assert that these Claims overcome the rejections of record as they depend from an allowable claim, and respectfully solicit allowance of these Claims.

With respect to Claim 11, Applicants respectfully assert that Pole fails to teach or fairly suggest the limitation "means for reducing the selectable voltage below a level specified by the voltage regulator" as recited by amended Claim 11.

Pole may describe causing the voltage regulator to output different voltages. However, Applicants respectfully assert that Pole is silent as to causing the voltage regulator to output a "voltage below a level specified by the voltage regulator," as claimed. Applicants respectfully assert that one of ordinary skill in the art would understand Pole to teach that the output voltage of the voltage regulator to be within, e.g., neither above nor below, a range specified by the voltage regulator, as Pole is silent as to causing the voltage regulator to output a voltage outside of that range.

For this reason, Applicants respectfully assert that Claim 11 overcomes the rejections of record, and respectfully solicit allowance of this Claim.

With respect to Claim 13, Applicants respectfully assert that Pole fails to teach or fairly suggest the limitation:

circuitry for conserving charge stored by the voltage regulator when the selectable voltage decreases, and means for enabling the circuitry for conserving charge stored by the voltage regulator when the selectable voltage decreases

as recited by Claim 13.

Applicants respectfully assert that Pole fails to teach or fairly suggest the limitations of Claim 13. The rejection asserts that Pole teaches a battery (60) as a charge storage unit. However, while a battery may be capable of storing charge, Applicants respectfully assert that Pole does not teach or fairly suggest how charge from the voltage regulator is stored in the battery, as claimed. Moreover, Applicants respectfully assert that Pole fails to teach or fairly suggest how charge from the voltage regulator is stored in the battery when the selectable voltage decreases, as claimed.

Applicants respectfully note that Pole fails to teach any coupling of the battery 60 to the voltage regulator, and thus cannot teach the claimed limitations. Further, Pole fails to teach any means for "enabling" the battery "for conserving charge stored by the voltage regulator" as recited by Claim 13.

For these many reasons, Applicants respectfully assert that Claim 13 overcomes the rejections of record, and respectfully solicit allowance of this Claim.

35 U.S.C. § 103

Claims 4, 12 and 14-18 are rejected under 35 U.S.C. §103(a) as being allegedly unpatentable over Pole in view of Applicants' admitted prior art ("APA") and further in view of "High-speed, Digitally adjusted step-down controllers for notebook CPUs," Maxim, July 2000, pages 1-28 ("Maxim"). Applicants have carefully reviewed the cited references and respectfully assert that embodiments in accordance with the present invention as recited in Claims 4, 12 and 14-18 are patentable over Pole in view of APA and further in view of Maxim.

With respect to Claim 4, Applicants respectfully assert that Pole in view of APA and further in view of Maxim fails to teach the limitation, "providing a feedback signal to the voltage regulator to reduce its output voltage below a specified output voltage" as recited by Claim 4.

APA teaches, "prior art regulators such as the Maxim 1711 provide a feedback terminal and describe how that terminal may be utilized with a

resistor-voltage-divider network... to raise the output voltage level" (page 10 lines 6-9, emphasis added). Pole and Maxim fail to remedy this short coming.

In this manner, APA actually teaches away from embodiments in accordance with the present invention that recite using feedback to reduce an output voltage as recited by Claim 4.

For this reason, Applicants respectfully assert that Claim 4 overcomes the rejections of record, and respectfully solicit allowance of this Claim.

Claim 18 depends from Claim 4. Applicants respectfully assert that Claim 18 overcomes the rejections of record as this Claim depends from an allowable claim, and respectfully solicit allowance of the Claim.

With respect to Claim 12, Applicants respectfully assert that Pole in view of APA and further in view of Maxim fails to teach or fairly suggest the limitation, "means for reducing the selectable voltage below a level provided by the voltage regulator" as recited by Claim 12.

Pole teaches throughout, "a voltage regulator 52 that regulates the supply voltage of the processor" (column 2, lines 38-40, *inter alia*). Applicants respectfully assert that a voltage supplied by a voltage regulator is inherently

supplied at, e.g., neither above or below, a level provided by the voltage regulator. Consequently, Pole teaches away from embodiments in accordance with the present invention that recite reducing a voltage to a processor below a level provided by the voltage regulator as recited by Claim 12. Maxim and APA doe not remedy this defect.

For this reason, Applicants respectfully assert that Claim 12 overcomes the rejections of record, and respectfully solicit allowance of this Claim.

Furthermore, Pole teaches operating a voltage regulator "within specifications" (column 4, line 8). Applicants respectfully assert that one of ordinary skill in the art would be taught away from embodiments in accordance with the present invention that recite reducing a voltage to a processor below a level provided by the voltage regulator as recited by Claim 4 by this teaching of Pole.

For this additional reason, Applicants respectfully assert that Claim 12 overcomes the rejections of record, and respectfully solicit allowance of this Claim.

With respect to Claim 14, the rejection alleges that this claim contains the "same limitation as set forth in claim 12." Applicants respectfully traverse.

Applicants respectfully assert that Claims 12 and 14 set forth different embodiments in accordance with the present invention.

The rejection applies the "same rejection" to Claim 14 as was applied to Claim 12. Applicants respectfully assert that Claim 14 overcomes the rejections of record for at least the rationale previously presented with respect to Claim 12, and respectfully solicit allowance of this Claim.

Claims 15-17 depend from Claim 14. Applicants respectfully assert that these Claims overcome the rejections of record as they depend from an allowable claim, and respectfully solicit allowance of these Claims.

CONCLUSION

Claims remaining in the present application are 1-18. Claims 19-37 were canceled per the election referred to in a previous Official Action. The Applicants respectfully request reconsideration of the above captioned patent application in view of the remarks presented herein.

Applicants have reviewed the following references that were cited but not relied upon and do not find these references to teach or fairly suggest the present claimed invention: US 5,5258,127, US 6,208,127, US 6,047,248, US 6,457,135, "High speed step-down controller with synchronous rectification for CPU power," Maxim, 2005, pp 1-16.

The Examiner is invited to contact Applicant's undersigned representative if the Examiner believes such action would expedite resolution of the present Application.

Please charge any additional fees or apply any credits to our PTO deposit account number: 23-0085.

Respectfully submitted,

WAGNER, MURABITO & HAO LLP

Date: March 8, 2006

Anthony C. Murabito
Reg. No. 35,295

Two North Market Street
Third Floor
San Jose, California 95113
(408) 938-9060

carg

PATENT APPLICATION FEE DETERMINATION RECORD
Effective December 8, 2004

09/694433

CLAIMS AS FILED - PART I

	(Column 1)	(Column 2)
TOTAL CLAIMS		
FOR	NUMBER FILED	NUMBER EXTRA
TOTAL CHARGEABLE CLAIMS	minus 20=	*
INDEPENDENT CLAIMS	minus 3 =	*
MULTIPLE DEPENDENT CLAIM PRESENT		☐

* If the difference in column 1 is less than zero, enter "0" in column 2

SMALL ENTITY TYPE ☐		OR	OTHER THAN SMALL ENTITY	
RATE	FEE		RATE	FEE
BASIC FEE		OR	BASIC FEE	
X$ 25=		OR	X$50=	
X100=		OR	X200=	
+180=		OR	+360=	
TOTAL		OR	TOTAL	

CLAIMS AS AMENDED - PART II

AMENDMENT A — 3-13-06

	(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA
Total	* 18	Minus	** 37	= 0
Independent	* 8	Minus	*** 12	= 0
FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM				☐

SMALL ENTITY		OR	OTHER THAN SMALL ENTITY	
RATE	ADDITIONAL FEE		RATE	ADDITIONAL FEE
X$ 25=		OR	X$50=	
X100=		OR	X200=	
+180=		OR	+360=	
TOTAL ADDIT. FEE		OR	TOTAL ADDIT. FEE	

AMENDMENT B

	(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA
Total	*	Minus	**	=
Independent	*	Minus	***	=
FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM				☐

RATE	ADDITIONAL FEE		RATE	ADDITIONAL FEE
X$ 25=		OR	X$50=	
X100=		OR	X200=	
+180=		OR	+360=	
TOTAL ADDIT. FEE		OR	TOTAL ADDIT. FEE	

AMENDMENT C

	(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA
Total	*	Minus	**	=
Independent	*	Minus	***	=
FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM				☐

RATE	ADDITIONAL FEE		RATE	ADDITIONAL FEE
X$ 25=		OR	X$50=	
X100=		OR	X200=	
+180=		OR	+360=	

UNITED STATES PATENT AND TRADEMARK OFFICE

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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/694,433	10/23/2000	Andrew Read	TRANS59	3072

7590 05/23/2006

WAGNER, MURABITO & HAO LLP
TWO NORTH MARKET STREET
THIRD FLOOR
SAN JOSE, CA 95113

EXAMINER	
CAO, CHUN	
ART UNIT	**PAPER NUMBER**
2115	

DATE MAILED: 05/23/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

PTO-90C (Rev. 10/03)

Notice of Non-Compliant Amendment (37 CFR 1.121)	Application No. 09/694,433	Applicant(s) READ ET AL.
	Examiner Chun Cao	Art Unit 2115

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

The amendment document filed on *25 March 2006* is considered non-compliant because it has failed to meet the requirements of 37 CFR 1.121 or 1.4. In order for the amendment document to be compliant, correction of the following item(s) is required.

THE FOLLOWING MARKED (X) ITEM(S) CAUSE THE AMENDMENT DOCUMENT TO BE NON-COMPLIANT:

- ☐ 1. Amendments to the specification:
  - ☐ A. Amended paragraph(s) do not include markings.
  - ☐ B. New paragraph(s) should not be underlined.
  - ☐ C. Other _____.
- ☐ 2. Abstract:
  - ☐ A. Not presented on a separate sheet. 37 CFR 1.72.
  - ☐ B. Other _____.
- ☐ 3. Amendments to the drawings:
  - ☐ A. The drawings are not properly identified in the top margin as "Replacement Sheet," "New Sheet," or "Annotated Sheet" as required by 37 CFR 1.121(d).
  - ☐ B. The practice of submitting proposed drawing correction has been eliminated. Replacement drawings showing amended figures, without markings, in compliance with 37 CFR 1.84 are required.
  - ☐ C. Other _____.
- ☒ 4. Amendments to the claims:
  - ☐ A. A complete listing of all of the claims is not present.
  - ☐ B. The listing of claims does not include the text of all pending claims (including withdrawn claims)
  - ☐ C. Each claim has not been provided with the proper status identifier, and as such, the individual status of each claim cannot be identified. Note: the status of every claim must be indicated after its claim number by using one of the following status identifiers: (Original), (Currently amended), (Canceled), (Previously presented), (New), (Not entered), (Withdrawn) and (Withdrawn-currently amended).
  - ☐ D. The claims of this amendment paper have not been presented in ascending numerical order.
  - ☒ E. Other: *See Continuation Sheet*.
- ☐ 5. Other (e.g., the amendment is unsigned or not signed in accordance with 37 CFR 1.4):

_____

For further explanation of the amendment format required by 37 CFR 1.121, see MPEP § 714.

TIME PERIODS FOR FILING A REPLY TO THIS NOTICE:

1. Applicant is given **no new time period** if the non-compliant amendment is an after-final amendment or an amendment filed after allowance. If applicant wishes to resubmit the non-compliant after-final amendment with corrections, the **entire corrected amendment** must be resubmitted.
2. Applicant is given **one month**, or thirty (30) days, whichever is longer, from the mail date of this notice to supply the correction, if the non-compliant amendment is one of the following: a preliminary amendment, a non-final amendment (including a submission for a request for continued examination (RCE) under 37 CFR 1.114), a supplemental amendment filed within a suspension period under 37 CFR 1.103(a) or (c), and an amendment filed in response to a *Quayle* action. If any of above boxes 1. to 4. are checked, the correction required is only the **corrected section** of the non-compliant amendment in compliance with 37 CFR 1.121.

   Extensions of time are available under 37 CFR 1.136(a) only if the non-compliant amendment is a non-final amendment or an amendment filed in response to a *Quayle* action.

   Failure to timely respond to this notice will result in:
   Abandonment of the application if the non-compliant amendment is a non-final amendment or an amendment filed in response to a *Quayle* action; or
   Non-entry of the amendment if the non-compliant amendment is a preliminary amendment or supplemental amendment.

CHUN CAO
PRIMARY EXAMINER

Legal Instruments Examiner (LIE), if applicable Telephone No.

Continuation of 4(e) Other: the limitations previously presented in Claim 11 are not shown in currently amended claim 11 .

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of: Read, et al.

Serial:	09/694,433	Group Art Unit: 2115
Filed:	October 23, 2000	Examiner: Cao, Chun
For:	STATIC POWER CONTROL (As Filed)	

Honorable Commissioner for Patents
PO Box 1450
Alexandria, VA 22313-1450

RESPONSE

Dear Sir:

In response to the Notice of Non-Compliant Amendment mailed May 23, 2006 in the above captioned case, Applicants respectfully submit the following corrected response and respectfully request the Examiner to consider the following remarks.

IN THE CLAIMS:

1. (Previously Presented) A method for reducing power utilized by a processor comprising the steps of:

determining that a processor is transitioning from a computing mode to a mode in which system clock to the processor is disabled, and

reducing core voltage to the processor to a value sufficient to maintain state during the mode in which system clock is disabled, wherein said value of the core voltage is not sufficient to maintain processing activity in said processor.

Claim 2. (Previously Presented) A method as claimed in Claim 1 in which the step of determining that a processor is transitioning from a computing mode to a mode in which system clock to the processor is disabled comprises monitoring a stop clock signal.

Claim 3. (Original) A method as claimed in Claim 1 in which the step of reducing core voltage to the processor to a value sufficient to maintain state during the state in which system clock is disabled comprises furnishing an input to reduce an output voltage provided by a voltage regulator furnishing core voltage to the processor.

Claim 4. (Previously Presented) A method for reducing power utilized by a processor comprising the steps of:

determining that a processor is transitioning from a computing mode to a mode in which system clock to the processor is disabled, and

reducing core voltage to the processor to a value sufficient to maintain state during the mode in which system clock is disabled by:

furnishing an input to reduce an output voltage provided by a voltage regulator furnishing core voltage to the processor, and

providing a feedback signal to the voltage regulator to reduce its output voltage below a specified output voltage.

Claim 5. (Previously Presented) A method for reducing power utilized by a processor comprising the steps of:

determining that a processor is transitioning from a computing mode to a mode in which system clock to the processor is disabled,

reducing core voltage to the processor to a value sufficient to maintain state during the mode in which system clock is disabled, and

transferring operation of a voltage regulator furnishing core voltage in a mode in which power is dissipated during reductions in core voltage to a mode in which power is saved during a voltage transition when it is determined that a processor is transitioning from a computing mode to a mode is which system

clock to the processor is disabled.

Claim 6. (Previously Presented) A method as claimed in Claim 5 further comprising the steps of returning the voltage regulator to its original mode of operation when the value of the core voltage sufficient to maintain state during the mode in which system clock is disabled is reached.

Claim 7. (Previously Presented) A circuit for providing a regulated voltage to a processor comprising:

a voltage regulator having:

an output terminal providing a selectable voltage, and

an input terminal for receiving signals indicating the selectable voltage level;

means for providing signals at the input terminal of the voltage regulator for selecting a voltage for operating the processor in a computing mode and a voltage of a level less than that for operating the processor in a computing mode, wherein the level less than that for operating the processor in a computing mode is sufficient to maintain state of the processor.

Claim 8. (Original) A circuit as claimed in Claim 7 in which the means for providing signals at the input terminal of the voltage regulator comprises means for accepting binary signals indicating different levels of voltage.

Claim 9. (Original) A circuit as claimed in Claim 7 in which the means for providing signals at the input terminal of the voltage regulator comprises:

selection circuitry,

means for furnishing a plurality of signals at the input to the selection circuitry, and

means for controlling the selection by the selection circuitry.

Claim 10. (Original) A circuit as claimed in Claim 9 in which:

the selection circuitry is a multiplexor, and

the means for controlling the selection by the selection circuitry includes a control terminal for receiving signals indicating a system clock to the processor is being terminated.

Claim 11. (previously presented) A circuit for providing a regulated voltage to a processor comprising:

a voltage regulator having:

an output terminal providing a selectable voltage, and

an input terminal for receiving signals indicating the selectable voltage level;

means for providing signals at the input terminal of the voltage regulator for selecting a voltage for operating the processor in a computing mode and a voltage of a level less than that for operating the processor in a computing mode; and

means for reducing the selectable voltage below a lowest level the voltage regulator is specified to output.

Claim 12. (Previously Presented) A circuit for providing a regulated voltage to a processor comprising:

a voltage regulator having:

an output terminal providing a selectable voltage;

an input terminal for receiving signals indicating the selectable voltage level; and

a voltage regulator feedback circuit;

means for providing signals at the input terminal of the voltage regulator for selecting a voltage for operating the processor in a

computing mode and a voltage of a level less than that for operating the processor in a computing mode; and

means for reducing the selectable voltage below a level provided by the voltage regulator comprising:

a voltage divider network joined between the output terminal and a voltage source furnishing a value higher than the selectable voltage, and

the voltage regulator feedback circuit receiving a value from the voltage divider network.

Claim 13. (Previously Presented) A circuit for providing a regulated voltage to a processor comprising:

a voltage regulator having:

an output terminal providing a selectable voltage, and

an input terminal for receiving signals indicating the selectable voltage level;

means for providing signals at the input terminal of the voltage regulator for selecting a voltage for operating the processor in a computing mode and a

voltage of a level less than that for operating the processor in a computing mode;

circuitry for conserving charge stored by the voltage regulator when the selectable voltage decreases, and

means for enabling the circuitry for conserving charge stored by the voltage regulator when the selectable voltage decreases.

Claim 14. (Previously Presented) A circuit for providing a regulated voltage to a processor comprising:

a voltage regulator having:

an output terminal providing a selectable voltage, and

an input terminal for receiving signals indicating the selectable voltage level; and

a voltage regulator feedback circuit;

circuitry coupled to said input terminal and configured to provide signals to the input terminal for selecting a first voltage for operating the processor in a first mode and a second voltage for operating the processor in a second mode;

a voltage source furnishing a value higher than the selectable voltage; and

a feedback circuit coupled to the voltage source, the output terminal, and the voltage regulator feedback circuit.

15. (Previously Presented) The circuit of Claim 14, wherein the first voltage is for operating the processor in a computing mode and the second voltage is a level less than that for operating the processor in the computing mode.

16. (Previously Presented) The circuit of Claim 15, wherein the feedback circuit comprises a voltage divider.

17. (Previously Presented) The circuit of Claim 14, wherein the feedback circuit comprises a voltage divider.

18. (Previously Presented) The method of Claim 4, wherein the output voltage to which said voltage regulator is reduced depends upon output voltage of said voltage regulator prior to furnishing the input to reduce the output voltage provided by the voltage regulator.

19-37 (canceled) (election)

REMARKS

Claims remaining in the present application are 1-18. Claims 19-37 were canceled per the election referred to in a previous Official Action. The Applicants thank the Examiner for withdrawing the finality of the prior rejection. The Applicants respectfully request reconsideration of the above captioned patent application in view of the remarks presented herein.

35 U.S.C. §102

Claims 1-3, 5-11 and 13 are rejected under 35 U.S.C. §102(e) as being allegedly anticipated by Pole, II et al., U.S. 6,675,304 ("Pole"). Applicants have carefully reviewed the cited reference and respectfully assert that embodiments in accordance with the present invention as recited in Claims 1-3, 5-11 and 13 are patentable over Pole.

With respect to Claim 1, Applicants respectfully assert that Pole does not teach or fairly suggest the limitation "reducing core voltage to the processor to a value sufficient to maintain state during the mode in which system clock is disabled" as recited by Claim 1.

The referenced portion of Pole alleged to teach this claimed element, column 4 lines 15-40, may describe lowering an output voltage level, but Pole fails to teach

that such lowered level is sufficient to maintain a processor's state, as recited by Claim 1.

For this reason, Applicants respectfully assert that Claim 1 overcomes the rejections of record, and respectfully solicit allowance of this Claim.

In addition, with respect to Claim 1, Pole teaches a deep sleep state in which only data stored in the processor's internal caches is maintained (column 1, lines 30-34). As is well known to those of ordinary skill in the art, a processor's state is not represented in the processor's internal caches, and includes, for example, the contents of internal registers that are not represented in the caches. Thus, Pole actually teaches away from the claimed embodiments in accordance with the present invention that recite maintaining processor state, as recited by Claim 1.

For this additional reason, Applicants respectfully assert that Claim 1 overcomes the rejections of record, and respectfully solicit allowance of this Claim.

Further with respect to Claim 1, Applicants respectfully assert that Pole does not teach or fairly suggest the limitation "wherein said value of the core voltage is not sufficient to maintain processing activity in said processor" as recited by Claim 1.

While Pole may teach, "chang(ing) the voltage regulator setting from a higher to a lower output level" (column 4 lines 36-38), Applicants respectfully assert that Pole fails to teach or fairly suggest that such a "lower output level" is "not sufficient to maintain processing activity in said processor" as recited by Claim 1.

In addition, the rejection's citations to Pole column 5, lines 10-16 and column 1 lines 30-34 refer to clock activity, e.g., "the external clock to the processor is disabled," but are devoid of teachings related to "core voltage is not sufficient to maintain processing activity in said processor" as recited by Claim 1.

For these further reasons, Applicants respectfully assert that Claim 1 overcomes the rejections of record, and respectfully solicit allowance of this Claim.

Claims 2-3 depend from Claim 1. Applicants respectfully assert that Claims 2-3 overcome the rejections of record as they depend from an allowable claim, and respectfully solicit allowance of these Claims.

With respect to independent Claim 5, Applicants respectfully assert that Pole does not teach or fairly suggest the limitation "reducing core voltage to the processor to a value sufficient to maintain state during the mode in which system

clock is disabled" as recited by Claim 5. As described previously with respect to Claim 1, the referenced portion of Pole may teach lowering an output voltage level, but does not teach that such lowered level is sufficient to maintain a processor's state, as recited by Claim 1.

For this reason, Applicants respectfully assert that Claim 5 overcomes the rejections of record, and respectfully solicit allowance of this Claim.

In addition, with respect to Claim 5, Pole teaches a deep sleep state in which only data stored in the processor's internal caches is maintained (column 1, lines 30-34). As is well known to those of ordinary skill in the art, a processor's state is not represented in the processor's internal caches, and includes, for example, the contents of internal registers which are not represented in the caches. Thus, Pole actually teaches away from the claimed embodiments in accordance with the present invention that recite maintaining processor state, as recited by Claim 5.

For this additional reason, Applicants respectfully assert that Claim 5 overcomes the rejections of record, and respectfully solicit allowance of this Claim.

Further, with respect to Claim 5, Applicants respectfully assert that Pole fails to teach or suggest the limitation:

transferring operation of a voltage regulator furnishing core voltage in a mode in which power is dissipated during reductions in core voltage to a mode in which power is saved during a voltage transition when it is determined that a processor is transitioning from a computing mode to a mode is which system clock to the processor is disabled

as recited by Claim 5.

The underscored language refers to modes of operating a voltage regulator (power dissipation mode/power saving mode). Applicants respectfully assert that Pole fails to teach or suggest the limitations of Claim 5. Pole may discuss lowering a voltage level supplied to a processor. However, power savings can be achieved in manners other than reducing frequency and/or reducing voltage of a processor. Applicants have specifically recited in this embodiment that saving power is performed by a choice of mode of operation of the voltage regulator. Pole is silent as to any mode of operation of a voltage regulator, aside from outputting a plurality of voltages. Consequently, Pole is silent as to operating the voltage regulator in a mode in which power is dissipated to a mode in which power is saved, as claimed. Thus, Pole fails to teach or fairly suggest the claimed transferring the operation of a voltage regulator from a mode in which power is dissipated to a mode in which power is saved, during a voltage transition.

For this further reason, Applicants respectfully assert that Claim 5 overcomes the rejections of record, and respectfully solicit allowance of this Claim.

Claim 6 depends from Claim 5. Applicants respectfully assert that Claim 6 overcomes the rejections of record as this claim depends from an allowable base claim, and respectfully solicit allowance of this Claim.

With respect to Claim 7, Applicants respectfully assert that Pole does not teach or fairly suggest the limitation "wherein the level less than that for operating the processor in a computing mode is sufficient to maintain state of the processor" as recited by Claim 7. As described previously with respect to Claim 1, the referenced portion of Pole may teach lowering an output voltage level, but does not teach that such lowered level is sufficient to maintain a processor's state, as recited by Claim 7.

For this reason, Applicants respectfully assert that Claim 7 overcomes the rejections of record, and respectfully solicit allowance of this Claim.

Claims 8-10 depend from Claim 7. Applicants respectfully assert that these Claims overcome the rejections of record as they depend from an allowable claim, and respectfully solicit allowance of these Claims.

With respect to Claim 11, Applicants respectfully assert that Pole fails to teach or fairly suggest the limitation "means for reducing the selectable voltage below a lowest level the voltage regulator is specified to output" as recited by Claim 11.

Pole may describe causing the voltage regulator to output different voltages. However, Applicants respectfully assert that Pole is silent as to causing the voltage regulator to output a "voltage below a lowest level the voltage regulator is specified to output," as claimed. Applicants respectfully assert that one of ordinary skill in the art would understand Pole to teach that the output voltage of the voltage regulator to be within, e.g., neither above nor below, a range specified by the voltage regulator, as Pole is silent as to causing the voltage regulator to output a voltage outside of that range.

For this reason, Applicants respectfully assert that Claim 11 overcomes the rejections of record, and respectfully solicit allowance of this Claim.

With respect to Claim 13, Applicants respectfully assert that Pole fails to teach or fairly suggest the limitation:

> circuitry for conserving charge stored by the voltage regulator when the selectable voltage decreases, and means for enabling the circuitry for conserving charge stored by the voltage regulator when the selectable

voltage decreases

as recited by Claim 13.

Applicants respectfully assert that Pole fails to teach or fairly suggest the limitations of Claim 13. The rejection asserts that Pole teaches a battery (60) as a charge storage unit. However, while a battery may be capable of storing charge, Applicants respectfully assert that Pole does not teach or fairly suggest how charge from the voltage regulator is stored in the battery, as claimed. Moreover, Applicants respectfully assert that Pole fails to teach or fairly suggest how charge from the voltage regulator is stored in the battery when the selectable voltage decreases, as claimed.

Applicants respectfully note that Pole fails to teach any coupling of the battery 60 to the voltage regulator, and thus cannot teach the claimed limitations. Further, Pole fails to teach any means for "enabling" the battery "for conserving charge stored by the voltage regulator" as recited by Claim 13.

For these many reasons, Applicants respectfully assert that Claim 13 overcomes the rejections of record, and respectfully solicit allowance of this Claim.

35 U.S.C. § 103

Claims 4, 12 and 14-18 are rejected under 35 U.S.C. §103(a) as being allegedly unpatentable over Pole in view of Applicants' admitted prior art ("APA") and further in view of "High-speed, Digitally adjusted step-down controllers for notebook CPUs," Maxim, July 2000, pages 1-28 ("Maxim"). Applicants have carefully reviewed the cited references and respectfully assert that embodiments in accordance with the present invention as recited in Claims 4, 12 and 14-18 are patentable over Pole in view of APA and further in view of Maxim.

With respect to Claim 4, Applicants respectfully assert that Pole in view of APA and further in view of Maxim fails to teach the limitation, "providing a feedback signal to the voltage regulator to reduce its output voltage below a specified output voltage" as recited by Claim 4.

APA teaches, "prior art regulators such as the Maxim 1711 provide a feedback terminal and describe how that terminal may be utilized with a resistor-voltage-divider network... to raise the output voltage level" (page 10 lines 6-9, emphasis added). Pole and Maxim fail to remedy this shortcoming.

In this manner, APA actually teaches away from embodiments in accordance with the present invention that recite using feedback to reduce an output voltage as recited by Claim 4.

For this reason, Applicants respectfully assert that Claim 4 overcomes the rejections of record, and respectfully solicit allowance of this Claim.

Claim 18 depends from Claim 4. Applicants respectfully assert that Claim 18 overcomes the rejections of record as this Claim depends from an allowable claim, and respectfully solicit allowance of the Claim.

With respect to Claim 12, Applicants respectfully assert that Pole in view of APA and further in view of Maxim fails to teach or fairly suggest the limitation, "means for reducing the selectable voltage below a level provided by the voltage regulator" as recited by Claim 12.

Pole teaches throughout, "a voltage regulator 52 that regulates the supply voltage of the processor" (column 2, lines 38-40, *inter alia*). Applicants respectfully assert that a voltage supplied by a voltage regulator is inherently supplied at, e.g., neither above or below, a level provided by the voltage regulator. Consequently, Pole teaches away from embodiments in accordance with the present invention that recite reducing a voltage to a processor below a level provided by the voltage regulator as recited by Claim 12. Maxim and APA doe not remedy this defect.

For this reason, Applicants respectfully assert that Claim 12 overcomes the rejections of record, and respectfully solicit allowance of this Claim.

Furthermore, Pole teaches operating a voltage regulator "within specifications" (column 4, line 8). Applicants respectfully assert that one of ordinary skill in the art would be taught away from embodiments in accordance with the present invention that recite reducing a voltage to a processor below a level provided by the voltage regulator as recited by Claim 4 by this teaching of Pole.

For this additional reason, Applicants respectfully assert that Claim 12 overcomes the rejections of record, and respectfully solicit allowance of this Claim.

With respect to Claim 14, the rejection alleges that this claim contains the "same limitation as set forth in claim 12." Applicants respectfully traverse. Applicants respectfully assert that Claims 12 and 14 set forth different embodiments in accordance with the present invention.

The rejection applies the "same rejection" to Claim 14 as was applied to Claim 12. Applicants respectfully assert that Claim 14 overcomes the rejections

of record for at least the rationale previously presented with respect to Claim 12, and respectfully solicit allowance of this Claim.

Claims 15-17 depend from Claim 14. Applicants respectfully assert that these Claims overcome the rejections of record as they depend from an allowable claim, and respectfully solicit allowance of these Claims.

CONCLUSION

Claims remaining in the present application are 1-18. Claims 19-37 were canceled per the election referred to in a previous Official Action. The Applicants respectfully request reconsideration of the above captioned patent application in view of the remarks presented herein.

Applicants have reviewed the following references that were cited but not relied upon and do not find these references to teach or fairly suggest the present claimed invention: US 5,5258,127, US 6,208,127, US 6,047,248, US 6,457,135, "High speed step-down controller with synchronous rectification for CPU power," Maxim, 2005, pp 1-16.

The Examiner is invited to contact Applicant's undersigned representative if the Examiner believes such action would expedite resolution of the present Application.

Please charge any additional fees or apply any credits to our PTO deposit account number: 23-0085.

Respectfully submitted,

WAGNER, MURABITO & HAO LLP

Date: July 19, 2006

Anthony C. Murabito
Reg. No. 35,295

Two North Market Street
Third Floor
San Jose, California 95113
(408) 938-9060

Attorney Docket No.: TRAN-P059

FF 2115 $

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

I hereby certify that this transmittal of the below described document is being deposited with the United States Postal Service in an envelope bearing First Class Postage and addressed to the Commissioner for Patents P.O. Box 1450, Alexandria, VA 22313-1450, on the below date of deposit.

Date of Deposit:	7/19/06	Name of Person Making the Deposit:	Mina Oliveri	Signature of the Person Making the Deposit:	Mina Oliveri

In re Application of: Andrew Read, Sameer Halapete and Keith Klayman

Application No.: 09/694,433 Examiner: Cao, Chun

Filed: October 23, 2000 Art Unit: 2115

Confirmation No.: 3072

07/25/2006 STEUHEL1 00000036 230085 09694433
01 FC:1251 120.00 DA

For: STATIC POWER CONTROL (As Filed)

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

NON-COMPLIANT AMENDMENT RESPONSE TRANSMITTAL

1. Transmitted herewith is an amendment for this application

X Transmitted herewith is a response to an office action for the above identified patent application. (22 sheets)
___ Transmitted herewith are ___ sheets of substitute formal drawings.
___ Other:

2. Applicant is other than a small entity

Extension of Term

3. The proceedings herein are for a patent application and the provisions of 37 C.F.R. 1.136 apply.

(a) [X] Applicant petitions for an extension of time under 37 C.F.R. 1.136 (fees: 37 C.F.R. 1.17(a)-(d) for the total number of months checked below:)

Extension	Fee
[X] one month	$120.00
[ ] two months	$450.00
[ ] three months	$1,020.00
[ ] four months	$1,590.00
[ ] five months	$2,160.00
	Fee $120.00

If an additional extension of time is required, please consider this a petition therefor.

(b) [ ] Applicant believes that no extension of term is required. However, this conditional petition is being made to provide for the possibility that applicant has inadvertently overlooked the need for a petition for extension of time.

rev. 10/04 kgr

Fee Calculation

4. The fee for claims (37 C.F.R. 1.16(b)-(d)) has been calculated as shown below:

(for other than a small entity)					
Fee Items	Claims Remaining After Amendment	Highest Number of Claims Previously Paid For	Present Extra Claims	Fee Rate	Total
Total Claims	18	- 37 =	0	x $50.00	$0.00
Independent Claims	8	- 8 =	0	x $200.00	$0.00
Multiple Dependent Claim Fee (one or more, first added by this amendment)				$360.00	
Total Fees					$0.00

PAYMENT OF FEES

5. The full fee due in connection with this communication is provided as follows:

[X] The Commissioner is hereby authorized to charge any additional fees associated with this communication or credit any overpayment to Deposit Account No.: 23-0085 .
A duplicate copy of this authorization is enclosed.

[ ] A check in the amount of $

[X] Charge any fees required or credit any overpayments associated with this filing to Deposit Account No.: 23-0085.

Please direct all correspondence concerning the above-identified application to the following address:

WAGNER, MURABITO & HAO LLP
Two North Market Street, Third Floor
San Jose, California 95113
(408) 938-9060
Customer No: 45590

Respectfully submitted,

Date: July 19, 2006

By: _____
Anthony C. Murabito
Reg. No. 35,295

rev. 10/04 kgr

Large

PATENT APPLICATION FEE DETERMINATION RECORD
Effective December 8, 2004

09/694433

CLAIMS AS FILED - PART I

	(Column 1)	(Column 2)
TOTAL CLAIMS		
FOR	NUMBER FILED	NUMBER EXTRA
TOTAL CHARGEABLE CLAIMS	minus 20=	*
INDEPENDENT CLAIMS	minus 3 =	*
MULTIPLE DEPENDENT CLAIM PRESENT		☐

* If the difference in column 1 is less than zero, enter "0" in column 2

SMALL ENTITY TYPE ☐			OR	OTHER THAN SMALL ENTITY	
RATE	FEE			RATE	FEE
BASIC FEE			OR	BASIC FEE	
X$ 25=			OR	X$50=	
X100=			OR	X200=	
+180=			OR	+360=	
TOTAL			OR	TOTAL	

CLAIMS AS AMENDED - PART II

AMENDMENT A — 3-13-06

	(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA
Total	* 18	Minus	** 37	= 0
Independent	* 8	Minus	*** 12	= 0
FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM				☐

SMALL ENTITY			OR	OTHER THAN SMALL ENTITY	
RATE	ADDITIONAL FEE			RATE	ADDITIONAL FEE
X$ 25=			OR	X$50=	
X100=			OR	X200=	
+180=			OR	+360=	
TOTAL ADDIT. FEE			OR	TOTAL ADDIT. FEE	

AMENDMENT B — 1-24-06

	(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA
Total	* 18	Minus	** 37	= 0
Independent	* 8	Minus	*** 12	= 0
FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM				☐

RATE	ADDITIONAL FEE		OR	RATE	ADDITIONAL FEE
X$ 25=			OR	X$50=	
X100=			OR	X200=	
+180=			OR	+360=	
TOTAL ADDIT. FEE			OR	TOTAL ADDIT. FEE	

AMENDMENT C

	(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA
Total	*	Minus	**	=
Independent	*	Minus	***	=
FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM				☐

RATE	ADDITIONAL FEE		OR	RATE	ADDITIONAL FEE
X$ 25=			OR	X$50=	
X100=			OR	X200=	
+180=			OR	+360=	

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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/694,433	10/23/2000	Andrew Read	TRANS59	3072

7590 09/29/2006

WAGNER, MURABITO & HAO LLP
TWO NORTH MARKET STREET
THIRD FLOOR
SAN JOSE, CA 95113

EXAMINER	
CAO, CHUN	

ART UNIT	PAPER NUMBER
2115	

DATE MAILED: 09/29/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/694,433	READ ET AL.	
	Examiner	Art Unit	
	Chun Cao	2115	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *24 July 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-18* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-18* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

Final Rejection

1. Claims 1-18 are presented for examination. Claims 19-37 are canceled.

2. The text of those applicable section of Title 35, U.S. Code not included in this action can be found in the prior Office Action.

3. The rejections are respectfully maintained and reproduced infra for applicant's convenience.

4. Claims 1-3, 5-11 and 13 are rejected under 35 U.S.C. 102(e) as being anticipated by Pole, II et al. (Pole), US patent no. 6,675,304.

Pole is a prior art reference cited in prior office action in IDS paper no. 20040917.

As per claim 1, Pole teaches a method for reducing power utilized by a processor [fig. 5] comprising the steps of:

determining that a processor is transitioning from a computing mode to a mode in which system clock to the processor is disabled [col. 1, lines 30-34; col. 4, lines 15-32; col. 5, lines 10-16]; and

reducing core voltage to the processor to a value sufficient to maintain state during the mode in which system clock is disable [col. 4, lines 15-40], wherein said value of the core voltage is not sufficient to maintain processing activity in said processor [deep sleep state, col. 1, line 30-34].

As per claim 2, Pole teaches of determining the processor is transitioning from a computing mode to a mode in which system clock to the processor is

disabled comprises monitoring a stop clock signal [col. 4, lines 15-40; col. 5, lines 10-16].

As per claim 3, Pole teaches of reducing core voltage to the processor to a value sufficient to maintain state during the state in which system clock is disabled [col. 1, lines 30-34] comprises: furnishing an input to reduce an output voltage provided by a voltage regulator furnishing core voltage to the processor [col. 3, lines 31-67].

As per claim 5, Pole teaches a method for reducing power utilized by a processor [fig. 5] comprising the steps of:

determining that a processor is transitioning from a computing mode to a mode is which system clock to the processor is disabled [col. 1, lines 30-34; col. 4, lines 15-32; col. 5, lines 10-16];

reducing core voltage to the processor to a value sufficient to maintain state during the mode of which system clock is disable [col. 4, lines 15-40]; and

transferring operation of a voltage regulator furnishing core voltage in a mode in which power is dissipated during reductions in core voltage to a mode in which power is saved during a voltage transition when it is determined at a processor is transitioning from a computing mode to a mode is which system clock to the processor is disabled [col. 1, lines 30-34; col. 4, lines 5-40; col. 5, lines 10-16].

As per claim 6, Pole teaches of returning the voltage regulator to its original mode of operation when the value of the core voltage sufficient to

maintain state during the mode in which system clock is disabled is reached [col. 1, lines 30-34; col. 4, lines 15-40; col. 5, lines 10-16].

5. As per claim 7, Pole discloses a circuit [fig. 2] for providing a regulated voltage to a processor comprising:

a voltage regulator [52, figures 1, 2] having: an output terminal [col. 3, lines 31-55; " the output from the voltage regulator 52", inherently, there is an output terminal in the voltage regulator 52] providing a selectable voltage [col. 3, lines 43-50, "...adjust the voltage level supplied by the voltage regulator 52 up or down" and "to indicate that the voltage level from the voltage regulator 52 is changing"];

input terminal [fig. 2] for receiving signals indicating the selectable voltage level [col. 3, lines 31-55];

means for providing signal at the input terminal of the voltage regulator for selecting a voltage for operating the processor in a computing mode and a voltage of a level less than that for operating the processor in computing mode [col. 4, lines 2-11], wherein the level less than that for operating the processor in a computing mode is sufficient to maintain state of the processor [col. 1, lines 30-34; col. 4, lines 15-40; col. 5, lines 10-16].

As per claim 8, Pole discloses that the voltage regulator comprises means for accepting binary signals [LO/HI signals] indicating different voltage level [fig. 2; col. 3, lines 43-61; "A signal VR_LO/HI#...adjust the voltage level supplied by the voltage regulator 52 up or down"].

As per claim 9, Pole discloses that the voltage regulator comprises:

Selection circuitry, means for furnishing a plurality of signals at the input to the selection circuitry and means for controlling the selection by the selection circuitry [fig. 2; col. 3, lines 31-67].

As per claim 10, Pole discloses a multiplexor and means for controlling the selection by the selection circuitry including a control terminal for receiving signals indicating a system clock to the processor is being terminated [fig. 2; col. 3, lines 31-67].

6. As per claim 11, Pole discloses a circuit [fig. 2] for providing a regulated voltage to a processor comprising:

a voltage regulator [52, figures 1, 2] having: an output terminal [col. 3, lines 31-55; " the output from the voltage regulator 52", inherently, there is an output terminal in the voltage regulator 52] providing a selectable voltage [col. 3, lines 43-50, "...adjust the voltage level supplied by the voltage regulator 52 up or down" and "to indicate that the voltage level from the voltage regulator 52 is changing"];

input terminal [fig. 2] for receiving signals indicating the selectable voltage level [col. 3, lines 31-55];

means for providing signal at the input terminal of the voltage regulator for selecting a voltage for operating the processor in a computing mode and a voltage of a level less than that for operating the processor in computing mode [col. 4, lines 2-11],

means for reducing the selectable voltage below a lowest level the voltage regulator is specified to output [col. 1, lines 30-34; col. 4, lines 15-40; col. 5, lines 10-16].

7. As per claim 13, Pole discloses a circuit [fig. 2] for providing a regulated voltage to a processor comprising:

a voltage regulator [52, figures 1, 2] having: an output terminal [col. 3, lines 31-55; " the output from the voltage regulator 52", inherently, there is an output terminal in the voltage regulator 52] providing a selectable voltage [col. 3, lines 43-50, "...adjust the voltage level supplied by the voltage regulator 52 up or down" and "to indicate that the voltage level from the voltage regulator 52 is changing"];

input terminal [fig. 2] for receiving signals indicating the selectable voltage level [col. 3, lines 31-55];

means for providing signal at the input terminal of the voltage regulator for selecting a voltage for operating the processor in a computing mode and a voltage of a level less than that for operating the processor in computing mode [col. 4, lines 2-11],

circuitry for conserving charge [battery 60] stored by the voltage regulator when the selectable voltage decreases; and means for enabling the circuitry for conserving charge stored by the voltage regulator when the selectable voltage decreases [col. 3, lines 43-67; col. 4, lines 15-40; col. 5, lines 10-16].

8. Claims 4, 12 and 14-18 are rejected under 35 U.S.C. 103 (a) as being unpatentable over Pole, II et al. (Pole), US patent no. 6,675,304 in view of Applicant Admitted Prior Art (AAPA) and "High-speed, Digitally adjusted step-down controllers for notebook CPUs" Maxim, July 2000, pages 1-28 (hereinafter "Maxim).

As per claim 4, Pole teaches a method for reducing power utilized by a processor [fig. 5] comprising the steps of:

determining that a processor is transitioning from a computing mode to a mode in which system clock to the processor is disabled [col. 1, lines 30-34; col. 4, lines 15-32; col. 5, lines 10-16]; and

reducing core voltage to the processor to a value sufficient to maintain state during the mode in which system clock is disable [col. 4, lines 15-40] by:

furnishing an input to reduce an output voltage provided by a voltage regulator furnishing core voltage to the processor [col. 3, lines 31-67]; and

providing a control signal to the voltage regulator to reduce its output voltage below a specified output voltage [col. 4, lines 5-7].

Pole does not explicitly teach of providing a feedback to the voltage regulator.

AAPA teaches of providing a feedback to the voltage regulator [Maxim 1711, page 10, lines 6-9].

Furthermore, Maxim teaches a Maxim 1711 is a step-down controller, wherein Maxim 1711 is implemented in a computer system to reduce voltage level to a CPU core [see page 1].

It would have been obvious to one of ordinary skill in the art at time the invention to combine the teachings of Pole and AAPA because the specify teachings of AAPA stated above would allow the processor to run stable and reliable by adjusting the core voltage accordingly.

As per claim 18, Pole teaches that the output voltage to which said voltage regulator is reduced depends upon output voltage of said voltage regulator prior to furnishing the input to reduce the output voltage provided by the voltage regulator [col. 3, lines 43-67].

9. As per claim 12, Pole discloses a circuit [fig. 2] for providing a regulated voltage to a processor comprising:

a voltage regulator [52, figures 1, 2] having: an output terminal [col. 3, lines 31-55; " the output from the voltage regulator 52", inherently, there is an output terminal in the voltage regulator 52] providing a selectable voltage [col. 3, lines 43-50, "...adjust the voltage level supplied by the voltage regulator 52 up or down" and "to indicate that the voltage level from the voltage regulator 52 is changing"];

input terminal [fig. 2] for receiving signals indicating the selectable voltage level [col. 3, lines 31-55];

means for providing signal at the input terminal of the voltage regulator for selecting a voltage for operating the processor in a computing mode and a voltage of a level less than that for operating the processor in computing mode [col. 4, lines 2-11],

means for reducing the selectable voltage below a level provided by the voltage regulator [col. 4, lines 2-11].

Pole does not explicitly disclose a voltage regulator feedback circuit and a voltage divider network.

AAPA discloses a voltage regulator including a voltage regulator feedback circuit and a voltage divider network [page 10, lines 6-9].

Furthermore, Maxim teaches a Maxim 1711 is a step-down controller with a voltage divider network [see page 1], wherein Maxim 1711 is implemented in a computer system to reduce voltage level to a CPU core [see page 1].

It would have been obvious to one of ordinary skill in the art at time the invention to combine the teachings of Orton and AAPA because the specify teachings of AAPA stated above would allow the processor to run stable and reliable by adjusting the core voltage accordingly.

As per claim 14 is contained same limitations as set forth in claim 12. Therefore, same rejection is applied.

As per claim 15, Pole teaches that the first voltage is for operating the processor in a computing mode and the second voltage is a level less than that for operating the processor in the computing mode [col. 4, lines 2-7].

As to claims 16 and 17, Maxim discloses that the feedback circuit comprises a voltage divider [see page 1].

Response to Arguments

10. Applicant's arguments filed 7/24/2006 have been fully considered but are not persuasive.

11. In the remarks, applicants argued in substance that 1) Pole does not disclose the limitation "reducing core voltage to the processor to a value sufficient to maintain state during the mode in which system clock is disable, wherein said value of the core voltage is not sufficient to maintain processing activity in said processor" as recited in claim 1. 2) Pole fails to teach of transferring operation of a voltage regulator furnishing core voltage in a mode in which power is dissipated during reductions in core voltage to a mode in which power is saved during a voltage transition [col. 1, lines 30-34; col. 4, lines 5-40; col. 5, lines 10-16]. 3) Pole fails to teach the limitation "mean for reducing the selectable voltage below a lowest level the voltage regulator is specified to output". 4) Pole fails to teach the limitation "circuitry for conserving charge stored by the voltage regulator when the selectable voltage decreases; and means for enabling the circuitry for conserving charge stored by the voltage regulator when the selectable voltage decrease". 5) Pole and AAPA and Maxim fail to teach the limitation "providing a feedback signal to the voltage regulator to reduce its output voltage below a specified output voltage".

12. The examiner respectfully traverses. As to 1), Pole teaches of reducing core voltage to the processor to a value sufficient [a low voltage level of 1.3 volts] to maintain state [maintain a deep sleep state] during the mode in which system

clock is disable [col. 4, lines 15-40, emphasis added, "stopping the processor bus clock"], wherein said value of the core voltage is not sufficient to maintain processing activity in said processor [emphasis added "there is no activities are performed by the processor while it is in a deep sleep state", see col. 1, line 30-34]. As to 2) Pole teaches of transferring operation of a voltage regulator furnishing core voltage in a mode in which power is dissipated during reductions in core voltage to a mode in which power is saved during a voltage transition [col. 1, lines 30-34; col. 4, lines 5-40; col. 5, lines 10-16; emphasis added, "power is saved from high performance state (normal mode) to low performance state (deep sleep state)"]. As to 3) Pole teaches that means for reducing the selectable voltage below a lowest level the voltage regulator is specified to output [col. 1, lines 30-34; col. 4, lines 15-40; col. 5, lines 10-16]. As to 4) Pole teaches that circuitry for conserving charge [battery 60] stored by the voltage regulator when the selectable voltage decreases; and means for enabling the circuitry for conserving charge stored by the voltage regulator when the selectable voltage decreases [col. 3, lines 43-67; col. 4, lines 15-40; col. 5, lines 10-16; also, the battery is connected to the voltage regulator show in figure 1]. As to 5) AAPA teaches of providing a feedback to the voltage regulator [Maxim 1711, page 10, lines 6-9]; however, Maxim teaches a Maxim 1711(as cited in AAPA) is a step-down controller, wherein Maxim 1711 is implemented in a computer system to allow of adjusting and reducing voltage level to a CPU core [see page 1].

Also see rejection above.

13. **THIS ACTION IS MADE FINAL.** See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Chun Cao whose telephone number is 703-308-6106. The examiner can normally be reached on Monday-Friday from 7:30 am-4:00 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Thomas C. Lee can be reached on 703-305-9717. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Any inquiry of a general nature or relating to the status of this application should be directed to the Group receptionist whose telephone number is (703) 306-5631.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Sep. 26, 2006

CHUN CAO
PRIMARY EXAMINER

Notice of References Cited	Application/Control No. 09/694,433	Applicant(s)/Patent Under Reexamination READ ET AL.	
	Examiner Chun Cao	Art Unit 2115	Page 1 of 1

U.S. PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Name	Classification
*	A	US-6,457,082 B1	09-2002	Zhang et al.	710/260
*	B	US-6,111,806 A	08-2000	Shirley et al.	365/226
*	C	US-5,760,636 A	06-1998	Noble et al.	327/513
	D	US-			
	E	US-			
	F	US-			
	G	US-			
	H	US-			
	I	US-			
	J	US-			
	K	US-			
	L	US-			
	M	US-			

FOREIGN PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Country	Name	Classification
	N					
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	S					
	T					

NON-PATENT DOCUMENTS

*		Include as applicable: Author, Title Date, Publisher, Edition or Volume, Pertinent Pages)
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	V	
	W	
	X	

*A copy of this reference is not being furnished with this Office action. (See MPEP § 707.05(a).)
Dates in MM-YYYY format are publication dates. Classifications may be US or foreign.

Index of Claims

Application/Control No.	Applicant(s)/Patent under Reexamination
09/694,433	READ ET AL.
Examiner	**Art Unit**
Chun Cao	2115

√	Rejected	–	(Through numeral) Cancelled	N	Non-Elected	A	Appeal
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Claim		Date
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Doc Code: AP.PRE.REQ

PTO/SB/33 (07-05)
Approved for use through xx/xx/200x. OMB 0651-00xx
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE

PRE-APPEAL BRIEF REQUEST FOR REVIEW

Docket Number (Optional): TRAN-P059

I hereby certify that this correspondence is being deposited with the United States Postal Service with sufficient postage as first class mail in an envelope addressed to "Mail Stop AF, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450" [37 CFR 1.8(a)]

on 12/28/06

Signature _____

Typed or printed name Julie Williams

Application Number	Filed
09/694,433	10/23/00

First Named Inventor: Read, etal.

Art Unit	Examiner
2115	Cao, Chun

Applicant requests review of the final rejection in the above-identified application. No amendments are being filed with this request.

This request is being filed with a notice of appeal.

The review is requested for the reason(s) stated on the attached sheet(s).
Note: No more than five (5) pages may be provided.

I am the

- [ ] applicant/inventor.
- [ ] assignee of record of the entire interest. See 37 CFR 3.71. Statement under 37 CFR 3.73(b) is enclosed. (Form PTO/SB/96)
- [X] attorney or agent of record. Registration number 35,295
- [ ] attorney or agent acting under 37 CFR 1.34. Registration number if acting under 37 CFR 1.34 _____

Signature

Anthony C. Murabito
Typed or printed name

(408) 938-9060
Telephone number

12/28/06
Date

NOTE: Signatures of all the inventors or assignees of record of the entire interest or their representative(s) are required. Submit multiple forms if more than one signature is required, see below*.

[X] *Total of 4 forms are submitted.

TRAN-P059 PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of: Read, et al.

Serial:	09/694,433	Group Art Unit: 2115
Filed:	October 23, 2000	Examiner: Cao, Chun
For:	STATIC POWER CONTROL (As Filed)	

PRE-APPEAL BRIEF REQUEST FOR REVIEW

Honorable Commissioner for Patents
PO Box 1450
Alexandria, VA 22313-1450

Dear Sir:

In response to the final Office Action dated September 29, 2006 Applicants respectfully request review of the final rejection in the above-identified application. Applicants respectfully submit that the Examiner's rejections of the Claims are improper as an essential element needed for a proper prima facie rejection under 35 U.S.C. §102 and 35 U.S.C. §10 is missing (e.g., the teaching of all of the recited claim limitations).

Claims 1-3, 5-11 and 13 are rejected under 35 U.S.C. §102(e) as being allegedly anticipated by Pole, II et al., U.S. 6,675,304 ("Pole"). Claims 4, 12 and 14-18 are rejected under 35 U.S.C. §103(a) as being allegedly unpatentable over Pole in view of Applicants' admitted prior art ("APA") and further in view of "High-speed, Digitally adjusted step-down controllers for notebook CPUs," Maxim, July 2000, pages 1-28 ("Maxim").

CLAIM LIMITATIONS THAT ARE NOT MET BY THE CITED REFERENCES

With respect to independent Claim 1, Pole fails to teach or fairly suggest the limitations "reducing core voltage to the processor to a value sufficient to maintain state during the mode in which system clock is disabled, wherein said value of the core voltage is not sufficient to maintain processing activity in said processor" as recited by Claim 1. While Pole may describe a "a reduction in voltage," Pole is completely silent as to supplying a voltage "not sufficient to maintain processing activity in said processor" as recited by Claim 1.

In the rejection, the Examiner cites Pole column 1, lines 30-34 as suggesting this limitation. Applicants strongly traverse. The cited passage refers to an external clock signal but fails to suggest changing voltage. The use of hindsight reasoning is not proper and this particular citation indicates that the rejection is guided by the recited claims to establish teachings not present in the cited art.

Elsewhere, Pole may suggest that a voltage may be changed. However, Pole's voltage teachings are limited to "adjusting" (column 1 line 39), high/low (column 4 lines 18-29), higher/lower (column 4 lines 38-39) and the like. Pole does not teach any functional requirement of a voltage. Importantly, Pole's relative terms describing voltage fail to teach or fairly suggest the limitation of a voltage "sufficient to maintain state (but) not sufficient to maintain processing activity in said processor" as recited by Claim 1. Applicants assert that a voltage that maintains state and is sufficient to maintain processing activity is consistent with Pole. In contrast, the description of the claimed limitation is not taught or fairly suggested by the cited art.

With respect to independent Claim 5, Pole fails to teach or fairly suggest the limitations "reducing core voltage to the processor to a value sufficient to maintain state during the mode in which system clock is disabled, and transferring operation of a voltage regulator furnishing core voltage in a mode in which power is dissipated during reductions in core voltage to a mode in which power is saved during a voltage transition when it is determined that a processor is transitioning from a computing mode to a mode is which system clock to the processor is disabled" as recited by Claim 5. The limitations are not taught or fairly suggested by the cited art.

Pole is completely silent as to a mode of operation of a voltage regulator. While Pole may teach increasing or reducing voltage, Pole fails to teach or fairly suggest changing modes of operation of the voltage regulator. For example, operating a voltage regulator in the same mode, e.g., linear regulation mode at both "high" and "low" voltages, is completely consistent with the teachings of Pole. Consequently, Pole fails to teach or fairly suggest changing modes of operating the voltage regulator, as recited by Claim 5. The limitation is not taught or fairly suggested by the cited art.

In addition with respect to Claim 5, power savings can be achieved in manners other than reducing frequency and/or reducing voltage of a processor. Applicants have specifically recited in this embodiment that saving power is performed by a choice of mode of operation of the voltage regulator. Pole is silent as to any mode of operation of a voltage regulator. Consequently, Pole is silent as to changing the mode of operation of the voltage regulator in a mode in which power is dissipated to a mode in which power is saved, as claimed. Thus, Pole fails to teach or fairly suggest the claimed transferring the operation of a voltage regulator from a mode in which power is dissipated to a mode in which power is saved, during a voltage transition. These limitations are not taught or fairly suggested by the cited art.

Further with respect to Claim 5, Pole is directed to adding ("switching in") an impedance when a voltage regulator is at a lower output voltage level (Abstract, column 5 lines 4-18, *inter alia*). In this manner, the load on the regulator is increased, increasing power consumption. Thus Pole trades increased power consumption in exchange for decreased latency in increasing voltage. This teaching leads away from power saving, as recited in Claim 5. These limitations are not taught or fairly suggested by the cited art.

With respect to independent Claim 11, Pole fails to teach or fairly suggest the limitations "means for reducing the selectable voltage below a lowest level the voltage regulator is specified to output" as recited by Claim 11. Pole is completely silent as to operation of a voltage regulator outside of its specified output range. In fact, the teachings of Pole are specifically limited to operation when the outputs of the voltage regulator are "within specifications" (column 4 line 8), which actually teaches away from the cited limitation. Applicants respectfully assert that the whole of Pole is directed to operation of a voltage regulator within its specifications, in contrast to the recited limitations of Claim 11. These limitations are not taught or fairly suggested by the cited art.

With respect to independent Claim 13, Pole fails to teach or fairly suggest the limitations "means for enabling the circuitry for conserving charge stored by the voltage regulator when the selectable voltage decreases" as recited by Claim 13. Pole teaches adding ("switching in") an impedance when a voltage regulator is at a lower output voltage level (Abstract, column 5 lines 4-18, *inter alia*). In adding such an impedance, charge stored by the voltage regulator is actually dissipated in Pole, in contrast to the recited limitation of conserving charge as recited by Claim 13. In this manner, Pole actually teaches away from embodiments of Claim 13. These limitations are not taught or fairly suggested by the cited art.

With respect to dependent Claim 4, Pole in view of APA and Maxim fail to teach or fairy suggest the limitations "providing a feedback signal to the voltage regulator to reduce its output voltage below a specified output voltage" as recited by Claim 4. The rejection concedes that Pole does not teach providing the recited feedback. While APA may teach "feedback... to raise the output voltage level" (page 10 lines 6-9, emphasis added), APA fails to suggest "reduc(ing)" a voltage level, as recited by Claim 4. Maxim fails to teach feedback or changing an output level to a processor. The rejection confuses the mode of operation of Maxim ("step down" conversion) to allegedly teach changing an output voltage. However, "step down" as used in Maxim refers to accessing a higher input (to the regulator) voltage, e.g., from a 28 volt battery (Maxim page 1), to produce a lower regulator output, e.g., 2 volts.

Applicants respectfully assert that Pole ("no feedback") in view of APA ("feedback to raise voltage") actually teaches feedback to raise voltage, thereby teaching away from the recited element. Thus, neither Pole, nor APA nor Maxim, alone or in combination, teach or fairly suggest feedback to reduce regulator output voltage, as recited by Claim 4. These limitations are not taught or fairly suggested by the cited art.

Further with respect to Claim 4, Pole in view of APA and Maxim fail to teach or fairy suggest the limitations "providing a feedback signal to the voltage regulator to reduce its output voltage below a specified output voltage" as recited by Claim 4. As previously presented, Pole is silent as to operation outside of specifications, and actually teaches away from this limitation. APA is silent as to these limitations. Maxim teaches operation within specification, which actually teaches away from these limitations.

Thus, neither Pole, nor APA nor Maxim, alone or in combination, teach or fairly suggest operation below specification, as recited by Claim 4. In fact, two of the references actually teach away from these limitations. These limitations are not taught or fairly suggested by the cited art.

In summary, Applicants respectfully submit that the Examiner's rejections of the Claims are improper as key limitations needed for proper prima facie rejections of Applicants' Claims are not met by the cited reference as outlined above.

Moreover, because key limitations of independent Claims 1, 5, 7, 11, 13, (from which Claims 2-3, 6, and 8-10 depend) are not taught or fairly suggested by Pole, and key limitations of Claims 4, 12 and 14-18 are not taught or fairly suggested by Pole in view of APA and further in view of Maxim, Applicants respectfully submit that the rejection of Claims 1-18 are improper and should be reversed.

The Commissioner is hereby authorized to charge any additional fees, which may be required for this request, or credit any overpayment, to Deposit Account 23-0085. In the event that an extension of time is required, or may be required in addition to that requested in a petition for an extension of time, the Commissioner is requested to grant a petition for that extension of time which is required to make this response timely and is hereby authorized to charge any fee for such an extension of time or credit any overpayment for an extension of time to Deposit Account 23-0085.

Respectfully submitted,

WAGNER, MURABITO & HAO LLP

Date: 12/28/2006

Anthony C. Murabito
Reg. No. 35,295
Two North Market Street
Third Floor
San Jose, California 95113
(408) 938-9060

Patent
Docket No.: TRAN-P059

Notice of Appeal

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Inventor(s): Read, et al.

Application No.: 09/694,433 Group Art Unit: 2115

Filed: 10/23/00 Examiner: Cao, Chun

Confirmation No: 3072

Title: STATIC POWER CONTROL (AS FILED)

Mail Stop AF
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

NOTICE OF APPEAL FROM THE PRIMARY EXAMINER
TO THE BOARD OF PATENT APPEALS AND INTERFERENCES

Applicant hereby appeals to the Board from the decision of the Primary Examiner, mailed, finally rejecting claims 04/18/06.

The item(s) checked below are appropriate:

1. STATUS OF APPLICANT
   This application is on behalf of
   - [X] other than a small entity.
   - [ ] a small entity.
   - [ ] A verified statement
     - [ ] is attached.
     - [ ] was already filed on _____.

CERTIFICATE OF MAILING/TRANSMISSION (37 C.F.R. 1.8a)

I hereby certify that this correspondence is, on the date shown below, being:

MAILING	FACSIMILE
X deposited with the United States Postal Service, with sufficient postage, as first class mail in an envelope addressed to Mail Stop AF Commissioner for Patents P.O. Box 1450 Alexandria, VA 22313-1450.	☐ transmitted by facsimile to the Patent and Trademark Office.

Date: 12/28/06

Julie Williams
Signature

Julie Williams
(type or print name of person certifying)

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2. FEE FOR FILING NOTICE OF APPEAL
   Pursuant to 37 C.F.R. 1.17(e), the fee for filing the Notice of Appeal is:
   - [ ] small entity $250.00
   - [X] other than a small entity $500.00

   Notice of Appeal fee due $ 500.00

01/05/2007 WASFAW1 00000015 09694433

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3. EXTENSION OF TERM

The proceedings herein are for a patent application and the provisions of 37 C.F.R. 1.136 apply.

(a) [ ] Applicant petitions for an extension of time under 37 C.F.R. 1.136 (fees: 37 C.F.R. 1.17(a)-(d)) for the total number of months checked below:

	Extension (months)	Fee for other than small entity	Fee for small entity
[ ]	one month	$120.00	$60.00
[ ]	two months	$450.00	$225.00
[ ]	three months	$1,020.00	$510.00
[ ]	four months	$1,530.00	$795.00
[ ]	five months	$2,160.00	$1,080.00

Fee $ _____

If an additional extension of time is required, please consider this a petition therefor.

[ ] An extension for _____ months has already been secured. The fee paid therefor of $_____ is deducted from the total fee due for the total months of extension now requested.

Extension fee due with this request $_____

or

(b) [X] Applicant believes that no extension of term is required. However, this conditional petition is being made to provide for the possibility that applicant has inadvertently overlooked the need for a petition and fee for extension of time.

4. TOTAL FEE DUE

The total fee due is:

Notice of Appeal fee $ 500.00

Extension fee (if any) $ _

TOTAL FEE DUE $ 500.00

5. **FEE PAYMENT**

[X] Attached is a check in the sum of $ 500.00.

[ ] Change Account No. 23-0085 the sum of $_____. A duplicate of this transmittal is attached.

6. **FEE DEFICIENCY**

If any additional fee is required, charge Account No. 23-0085.

12/28/2006

SIGNATURE OF ATTORNEY

Anthony C. Murabito
Reg. No.: 35,295

WAGNER, MURABITO & HAO LLP
Two North Market Street
Third Floor
San Jose, CA 95113
Tel. No.: (408) 938-9060

AF / JFW

Attorney Docket No.: TRAN-P059

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of: Read, et al.

Application No.: 09/694,433 Group No.: 2115

Filed: 10/23/00 Examiner: Cao, Chun

For: STATIC POWER CONTROL (AS FILED)

Mail Stop AF
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

TRANSMITTAL OF NOTICE OF APPEAL

1. Transmitted Herewith, In Triplicate, Is A Notice Of Appeal

2. STATUS OF APPLICANT
This application is on behalf of
[X] other than a small entity
[ ] a small entity
A verified statement:
[ ] is attached
[ ] was already filed

3. FEE FOR FILING NOTICE OF APPEAL
Pursuant to 37 C.F.R 1.17(f), the fee for filing the Notice of Appeal is:
[ ] small entity $250.00
[X] other than small entity $500.00

Notice of Appeal fee due $500.00

CERTIFICATE OF MAILING/TRANSMISSION (37 CFR 1.8A)

I hereby certify that this correspondence is, on the date shown below, being:

MAILING

☑ deposited with the United States Postal Service with sufficient postage as first class mail in an envelope addressed to Mail Stop AF
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450.

Date: 12/28/06

FACSIMILE

☐ transmitted by facsimile to the Patent Trademark Office.

Julie Williams
Signature

Julie Williams
Type or print name of person certifying

SIGNATURE OF ATTORNEY
Anthony C. Murabito
Reg. No.: 35,295
WAGNER, MURABITO & HAO LLP
Two North Market Street, Third Floor
San Jose, CA 95113
Tel. No.: (408) 938-9060

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/694,433	10/23/2000	Andrew Read	TRANS59	3072

7590 02/21/2007

WAGNER, MURABITO & HAO LLP
TWO NORTH MARKET STREET
THIRD FLOOR
SAN JOSE, CA 95113

EXAMINER	
CAO, CHUN	
ART UNIT	**PAPER NUMBER**
2115	

MAIL DATE	DELIVERY MODE
02/21/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

Application Number	Application/Control No.	Applicant(s)/Patent under Reexamination	
	09/694,433	READ ET AL.	
	Thomas Lee	Art Unit 2115	
Document Code - AP.PRE.DEC			

Notice of Panel Decision from Pre-Appeal Brief Review

This is in response to the Pre-Appeal Brief Request for Review filed 1/4/2007.

1. ☐ **Improper Request** – The Request is improper and a conference will not be held for the following reason(s):

☐ The Notice of Appeal has not been filed concurrent with the Pre-Appeal Brief Request.
☐ The request does not include reasons why a review is appropriate.
☐ A proposed amendment is included with the Pre-Appeal Brief request.
☐ Other:

The time period for filing a response continues to run from the receipt date of the Notice of Appeal or from the mail date of the last Office communication, if no Notice of Appeal has been received.

2. ☐ **Proceed to Board of Patent Appeals and Interferences** – A Pre-Appeal Brief conference has been held. The application remains under appeal because there is at least one actual issue for appeal. Applicant is required to submit an appeal brief in accordance with 37 CFR 41.37. The time period for filing an appeal brief will be reset to be one month from mailing this decision, or the balance of the two-month time period running from the receipt of the notice of appeal, whichever is greater. Further, the time period for filing of the appeal brief is extendible under 37 CFR 1.136 based upon the mail date of this decision or the receipt date of the notice of appeal, as applicable.

☐ The panel has determined the status of the claim(s) is as follows:
Claim(s) allowed: _____.
Claim(s) objected to: _____.
Claim(s) rejected: _____.
Claim(s) withdrawn from consideration: _____.

3. ☐ **Allowable application** – A conference has been held. The rejection is withdrawn and a Notice of Allowance will be mailed. Prosecution on the merits remains closed. No further action is required by applicant at this time.

4. ☒ **Reopen Prosecution** – A conference has been held. The rejection is withdrawn and a new Office action will be mailed. No further action is required by applicant at this time.

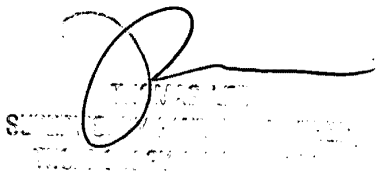
All participants:

(1) *Thomas Lee*.

(2) *Chun Cao*.

(3) *Lynne Browne*.

(4)_____.



UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
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P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/694,433	10/23/2000	Andrew Read	TRANS59	3072

7590 02/21/2007

WAGNER, MURABITO & HAO LLP
TWO NORTH MARKET STREET
THIRD FLOOR
SAN JOSE, CA 95113

EXAMINER	
CAO, CHUN	
ART UNIT	**PAPER NUMBER**
2115	

MAIL DATE	DELIVERY MODE
02/21/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

Interview Summary	Application No.	Applicant(s)	
	09/694,433	READ ET AL.	
	Examiner	Art Unit	
	Chun Cao	2115	

All participants (applicant, applicant's representative, PTO personnel):

(1) *Chun Cao*. (3) *Anthony C. Murabito*.

(2) *Thomas Lee*. (4)_____.

Date of Interview: *1/23/07, 2/8/07*.

Type: a)☒ Telephonic b)☐ Video Conference
c)☐ Personal [copy given to: 1)☐ applicant 2)☐ applicant's representative]

Exhibit shown or demonstration conducted: d)☐ Yes e)☒ No.
If Yes, brief description: _____.

Claim(s) discussed: *1-3,5,7-10 and 13*.

Identification of prior art discussed: *US patent no. 5,852,737*.

Agreement with respect to the claims f)☒ was reached. g)☐ was not reached. h)☐ N/A.

Substance of Interview including description of the general nature of what was agreed to if an agreement was reached, or any other comments: *112 2nd paragraph rejection pertaining to claims 5 and 13 were discussed. The teachings of the prior art reference (5,852,737) and the limitations as set forth in claims 1 and 7 were also discussed. Understanding had been reached to amend claims 1 and 7 to distinguish over the prior art reference and to amend claims 5 and 13 to overcome the 112 2nd paragraph rejection. Applicant agreed to file an amendment in due course*.

(A fuller description, if necessary, and a copy of the amendments which the examiner agreed would render the claims allowable, if available, must be attached. Also, where no copy of the amendments that would render the claims allowable is available, a summary thereof must be attached.)

THE FORMAL WRITTEN REPLY TO THE LAST OFFICE ACTION MUST INCLUDE THE SUBSTANCE OF THE INTERVIEW. (See MPEP Section 713.04). If a reply to the last Office action has already been filed, APPLICANT IS GIVEN A NON-EXTENDABLE PERIOD OF THE LONGER OF ONE MONTH OR THIRTY DAYS FROM THIS INTERVIEW DATE, OR THE MAILING DATE OF THIS INTERVIEW SUMMARY FORM, WHICHEVER IS LATER, TO FILE A STATEMENT OF THE SUBSTANCE OF THE INTERVIEW. See Summary of Record of Interview requirements on reverse side or on attached sheet.

Examiner Note: You must sign this form unless it is an Attachment to a signed Office action.

Examiner's signature, if required

Summary of Record of Interview Requirements

Manual of Patent Examining Procedure (MPEP), Section 713.04, Substance of Interview Must be Made of Record
A complete written statement as to the substance of any face-to-face, video conference, or telephone interview with regard to an application must be made of record in the application whether or not an agreement with the examiner was reached at the interview.

Title 37 Code of Federal Regulations (CFR) § 1.133 Interviews
Paragraph (b)
In every instance where reconsideration is requested in view of an interview with an examiner, a complete written statement of the reasons presented at the interview as warranting favorable action must be filed by the applicant. An interview does not remove the necessity for reply to Office action as specified in §§ 1.111, 1.135. (35 U.S.C. 132)

37 CFR §1.2 Business to be transacted in writing.
All business with the Patent or Trademark Office should be transacted in writing. The personal attendance of applicants or their attorneys or agents at the Patent and Trademark Office is unnecessary. The action of the Patent and Trademark Office will be based exclusively on the written record in the Office. No attention will be paid to any alleged oral promise, stipulation, or understanding in relation to which there is disagreement or doubt.

The action of the Patent and Trademark Office cannot be based exclusively on the written record in the Office if that record is itself incomplete through the failure to record the substance of interviews.

It is the responsibility of the applicant or the attorney or agent to make the substance of an interview of record in the application file, unless the examiner indicates he or she will do so. It is the examiner's responsibility to see that such a record is made and to correct material inaccuracies which bear directly on the question of patentability.

Examiners must complete an Interview Summary Form for each interview held where a matter of substance has been discussed during the interview by checking the appropriate boxes and filling in the blanks. Discussions regarding only procedural matters, directed solely to restriction requirements for which interview recordation is otherwise provided for in Section 812.01 of the Manual of Patent Examining Procedure, or pointing out typographical errors or unreadable script in Office actions or the like, are excluded from the interview recordation procedures below. Where the substance of an interview is completely recorded in an Examiners Amendment, no separate Interview Summary Record is required.

The Interview Summary Form shall be given an appropriate Paper No., placed in the right hand portion of the file, and listed on the "Contents" section of the file wrapper. In a personal interview, a duplicate of the Form is given to the applicant (or attorney or agent) at the conclusion of the interview. In the case of a telephone or video-conference interview, the copy is mailed to the applicant's correspondence address either with or prior to the next official communication. If additional correspondence from the examiner is not likely before an allowance or if other circumstances dictate, the Form should be mailed promptly after the interview rather than with the next official communication.

The Form provides for recordation of the following information:
- Application Number (Series Code and Serial Number)
- Name of applicant
- Name of examiner
- Date of interview
- Type of interview (telephonic, video-conference, or personal)
- Name of participant(s) (applicant, attorney or agent, examiner, other PTO personnel, etc.)
- An indication whether or not an exhibit was shown or a demonstration conducted
- An identification of the specific prior art discussed
- An indication whether an agreement was reached and if so, a description of the general nature of the agreement (may be by attachment of a copy of amendments or claims agreed as being allowable). Note: Agreement as to allowability is tentative and does not restrict further action by the examiner to the contrary.
- The signature of the examiner who conducted the interview (if Form is not an attachment to a signed Office action)

It is desirable that the examiner orally remind the applicant of his or her obligation to record the substance of the interview of each case. It should be noted, however, that the Interview Summary Form will not normally be considered a complete and proper recordation of the interview unless it includes, or is supplemented by the applicant or the examiner to include, all of the applicable items required below concerning the substance of the interview.

A complete and proper recordation of the substance of any interview should include at least the following applicable items:
1) A brief description of the nature of any exhibit shown or any demonstration conducted,
2) an identification of the claims discussed,
3) an identification of the specific prior art discussed,
4) an identification of the principal proposed amendments of a substantive nature discussed, unless these are already described on the Interview Summary Form completed by the Examiner,
5) a brief identification of the general thrust of the principal arguments presented to the examiner,
   (The identification of arguments need not be lengthy or elaborate. A verbatim or highly detailed description of the arguments is not required. The identification of the arguments is sufficient if the general nature or thrust of the principal arguments made to the examiner can be understood in the context of the application file. Of course, the applicant may desire to emphasize and fully describe those arguments which he or she feels were or might be persuasive to the examiner.)
6) a general indication of any other pertinent matters discussed, and
7) if appropriate, the general results or outcome of the interview unless already described in the Interview Summary Form completed by the examiner.

Examiners are expected to carefully review the applicant's record of the substance of an interview. If the record is not complete and accurate, the examiner will give the applicant an extendable one month time period to correct the record.

Examiner to Check for Accuracy

If the claims are allowable for other reasons of record, the examiner should send a letter setting forth the examiner's version of the statement attributed to him or her. If the record is complete and accurate, the examiner should place the indication, "Interview Record OK" on the paper recording the substance of the interview along with the date and the examiner's initials.

Attorney Docket No.: TRAN-P059

2115

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

I hereby certify that this transmittal of the below described document is being deposited with the United States Postal Service in an envelope bearing First Class Postage and addressed to the Commissioner for Patents P.O. Box 1450, Alexandria, VA 22313-1450, on the below date of deposit.

Date of Deposit:	03/19/07	Name of Person Making the Deposit:	Julie Giaramita	Signature of the Person Making the Deposit:	Julie Giaramita

In re Application of: Read, et al.

Application No.: 09/694,433 Examiner: Cao, Chun

Filed: 10/23/00 Art Unit: 2115

Confirmation No.: 3072

For: STATIC POWER CONTROL (AS FILED)

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

SUPPLEMENTAL AMENDMENT TRANSMITTAL

1. Transmitted herewith is an amendment for this application

X Transmitted herewith is a response to an office action for the above identified patent application.
(12 sheets)
____ Transmitted herewith are _____ sheets of substitute formal drawings.
____ Other:

2. Applicant is other than a small entity

Extension of Term

3. The proceedings herein are for a patent application and the provisions of 37 C.F.R. 1.136 apply.

(a) [ ] Applicant petitions for an extension of time under 37 C.F.R. 1.136 (fees: 37 C.F.R. 1.17(a)-(d) for the total number of months checked below:)

Extension	Fee
[ ] one month	$120.00
[ ] two months	$450.00
[ ] three months	$1,020.00
[ ] four months	$1,590.00
[ ] five months	$2,160.00
	Fee $ _____

If an additional extension of time is required, please consider this a petition therefor.

(b) [X] Applicant believes that no extension of term is required. However, this conditional petition is being made to provide for the possibility that applicant has inadvertently overlooked the need for a petition for extension of time.

rev. 10/04 kgr

Fee Calculation

4. The fee for claims (37 C.F.R. 1.16(b)-(d)) has been calculated as shown below:

(for other than a small entity)					
Fee Items	Claims Remaining After Amendment	Highest Number of Claims Previously Paid For	Present Extra Claims	Fee Rate	Total
Total Claims	18	- 37 =	0	x $50.00	$0.00
Independent Claims	8	- 8 =	0	x $200.00	$0.00
Multiple Dependent Claim Fee (one or more, first added by this amendment)				$360.00	$0.00
Total Fees					$0.00

PAYMENT OF FEES

5. The full fee due in connection with this communication is provided as follows:

[X] The Commissioner is hereby authorized to charge any additional fees associated with this communication or credit any overpayment to Deposit Account No.: 23-0085 . A duplicate copy of this authorization is enclosed.

[ ] A check in the amount of $

[ ] Charge any fees required or credit any overpayments associated with this filing to Deposit Account No.: 23-0085.

Please direct all correspondence concerning the above-identified application to the following address:

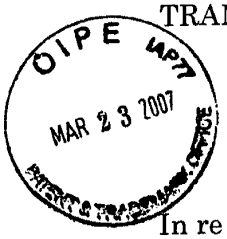
WAGNER, MURABITO & HAO LLP
Two North Market Street, Third Floor
San Jose, California 95113
(408) 938-9060
Customer No: 45590

Respectfully submitted,

Date: 3/19/2007

By: _____
Anthony C. Murabito
Reg. No. 35,295

rev. 10/04 kgr



IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of: Read, et al.

Serial:	09/694,433	Group Art Unit: 2115
Filed:	October 23, 2000	Examiner: Cao, Chun
For:	STATIC POWER CONTROL (As Filed)	

Honorable Commissioner for Patents
PO Box 1450
Alexandria, VA 22313-1450

SUPPLEMENTAL AMENDMENT

Dear Sir:

Applicants respectfully submit the following Supplemental Amendment for filing in the above captioned case.

In the Claims:

1. (currently amended) A method for reducing power utilized by a processor comprising the steps of:

determining that a processor is transitioning from a computing mode to a mode in which a system clock to the processor is disabled, and

reducing core voltage to the processor to a value sufficient to maintain state during the mode in which said system clock is disabled, wherein said value of the core voltage is not sufficient to maintain processing activity in said processor,

responsive to said determining, at a voltage regulator supplying said core voltage, transitioning from a first regulation mode to a second regulation mode,

wherein power is dissipated during a voltage transition that reduces said selectable voltage in said first regulation mode and power is saved during said voltage transition in said second regulation mode.

2. (currently amended) The [[A]] method as claimed in Claim 1 in which the step of determining that a processor is transitioning from a computing mode to a mode in which system clock to the processor is disabled comprises monitoring a stop clock signal.

3. (currently amended) The [[A]] method as claimed in Claim 1 in which the step of reducing core voltage to the processor to a value sufficient to maintain state during the state in which system clock is disabled comprises furnishing an input to reduce an output voltage provided by a voltage regulator furnishing core voltage to the processor.

4. (Previously Presented) A method for reducing power utilized by a processor comprising the steps of:

determining that a processor is transitioning from a computing mode to a mode in which system clock to the processor is disabled, and

reducing core voltage to the processor to a value sufficient to maintain state during the mode in which system clock is disabled by:

furnishing an input to reduce an output voltage provided by a voltage regulator furnishing core voltage to the processor, and

providing a feedback signal to the voltage regulator to reduce its output voltage below a specified output voltage.

5. (currently amended) A method for reducing power utilized by a <u>system having a least a</u> processor, comprising the steps of:

determining that [[a]] <u>the</u> processor is transitioning from a computing mode to a mode in which <u>a</u> system clock to the processor is disabled,

reducing core voltage being furnished by a voltage regulator to the processor to a value sufficient to maintain state during the mode in which the system clock is disabled, and

transferring operation of [[a]] the voltage regulator ~~furnishing core voltage~~ in a mode in which power is dissipated during a voltage transition in reduction[[s]] in core voltage to a mode in which power is saved during [[a]] said voltage transition in the reduction in core voltage when it is determined that [[a]] the processor is transitioning from [[a]] the computing mode to [[a]] the mode [[is]] in which the system clock to the processor is disabled.

6. (currently amended) The [[A]] method as claimed in Claim 5 further comprising the steps of returning the voltage regulator to its original mode of operation when the value of the core voltage sufficient to maintain state during the mode in which system clock is disabled is reached.

7. (currently amended) A circuit for providing a regulated voltage to a processor comprising:

a voltage regulator having:

an output terminal providing a selectable voltage, and

an input terminal for receiving signals indicating the selectable voltage level;

means for providing signals at the input terminal of the voltage regulator for selecting a voltage for operating the processor in a computing mode and a voltage of a level less than that for operating the processor in a computing mode, wherein the level less than that for operating the processor in a computing mode is sufficient to maintain state of the processor; and

means for changing the voltage regulator from a mode in which power is dissipated during a voltage transition that reduces said selectable voltage to a mode in which power is saved during said voltage transition.

8. (Original) A circuit as claimed in Claim 7 in which the means for providing signals at the input terminal of the voltage regulator comprises means for accepting binary signals indicating different levels of voltage.

9. (currently amended) The [[A]] circuit as claimed in Claim 7 in which the means for providing signals at the input terminal of the voltage regulator comprises:

selection circuitry,

means for furnishing a plurality of signals at the input to the selection circuitry, and

means for controlling the selection by the selection circuitry.

10. (currently amended) The [[A]] circuit as claimed in Claim 9 in which:

the selection circuitry is a multiplexor, and

the means for controlling the selection by the selection circuitry includes a control terminal for receiving signals indicating a system clock to the processor is being terminated.

11. (previously presented) A circuit for providing a regulated voltage to a processor comprising:

a voltage regulator having:

an output terminal providing a selectable voltage, and

an input terminal for receiving signals indicating the selectable voltage level;

means for providing signals at the input terminal of the voltage regulator for selecting a voltage for operating the processor in a computing mode and a voltage of a level less than that for operating the processor in a computing mode; and

means for reducing the selectable voltage below a lowest level the voltage regulator is specified to output.

12. (Previously Presented) A circuit for providing a regulated voltage to a processor comprising:

a voltage regulator having:

an output terminal providing a selectable voltage;

an input terminal for receiving signals indicating the selectable voltage level; and

a voltage regulator feedback circuit;

means for providing signals at the input terminal of the voltage regulator for selecting a voltage for operating the processor in a computing mode and a voltage of a level less than that for operating the processor in a computing mode; and

means for reducing the selectable voltage below a level provided by the voltage regulator comprising:

a voltage divider network joined between the output terminal and a voltage source furnishing a value higher than the selectable voltage, and

the voltage regulator feedback circuit receiving a value from the voltage divider network.

13. (currently amended) A circuit for providing a regulated voltage to a processor comprising:

a voltage regulator having:

an output terminal providing a selectable voltage, and

an input terminal for receiving signals indicating the selectable voltage level;

means for providing signals at the input terminal of the voltage regulator for selecting a voltage for operating the processor in a computing mode and a voltage of a level less than that for operating the processor in a computing mode;

circuitry for ~~conserving charge stored by the voltage regulator when the selectable voltage decreases~~ changing the voltage regulator from a mode in which power is dissipated during a voltage transition in reduction of the selectable voltage to a mode in which system power is saved during said voltage transition in reduction of the selectable voltage, and

means for enabling the circuitry for conserving charge stored by the voltage regulator when the selectable voltage decreases.

14. (Previously Presented) A circuit for providing a regulated voltage to a processor comprising:

a voltage regulator having:

an output terminal providing a selectable voltage, and

an input terminal for receiving signals indicating the selectable voltage level; and

a voltage regulator feedback circuit;

circuitry coupled to said input terminal and configured to provide signals to the input terminal for selecting a first voltage for operating the processor in a first mode and a second voltage for operating the processor in a second mode;

a voltage source furnishing a value higher than the selectable voltage; and

a feedback circuit coupled to the voltage source, the output terminal, and the voltage regulator feedback circuit.

15. (Previously Presented) The circuit of Claim 14, wherein the first voltage is for operating the processor in a computing mode and the second voltage is a level less than that for operating the processor in the computing mode.

16. (Previously Presented) The circuit of Claim 15, wherein the feedback circuit comprises a voltage divider.

17. (Previously Presented) The circuit of Claim 14, wherein the feedback circuit comprises a voltage divider.

18. (Previously Presented) The method of Claim 4, wherein the output voltage to which said voltage regulator is reduced depends upon output voltage of said voltage regulator prior to furnishing the input to reduce the output voltage provided by the voltage regulator.

19-37 (canceled) (election)

REMARKS

Claims remaining in the present application are 1-18. Claims 19-37 were previously canceled. Claims 1-3, 5-7, 9, 10 and 13 are amended herein. The Applicants respectfully request reconsideration of the above captioned patent application in view of the amendments presented herein.

Applicants' intent and belief is that the claims are amended per the agreement reached during the Examiner Interview described below.

Examiner Interview Summary

On January 23, 2007 and February 8, 2007, Examiner Cao and Supervisory Examiner Lee conducted an Examiner Interview with Applicants' representatives. Claims 1, 5, 7 and 13, and prior art citation US 5,852,737 were discussed. Agreement on Claims 1-18 was reached.

Applicants thank the Examiners for the Interview.

Conclusion

Claims remaining in the present application are 1 – 18. Applicants respectfully assert that the above captioned application is in condition for allowance, and respectfully solicit such allowance.

The Examiner is invited to contact Applicants' undersigned representative if the Examiner believes such action would expedite resolution of the present Application.

Please charge any additional fees or apply any credits to our PTO deposit account number: 23-0085.

Respectfully submitted,

WAGNER, MURABITO & HAO LLP

Date: 3/19/2007

Anthony C. Murabito
Reg. No. 35,295

Two North Market Street
Third Floor
San Jose, California 95113
(408) 938-9060

PTO/SB/06 (07-06)
Approved for use through 1/31/2007. OMB 0651-0032
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

PATENT APPLICATION FEE DETERMINATION RECORD Substitute for Form PTO-875	Application or Docket Number 09/694,433	Filing Date 10/23/2000	☐ To be Mailed

APPLICATION AS FILED – PART I

	(Column 1)	(Column 2)	SMALL ENTITY ☐		OR	OTHER THAN SMALL ENTITY	
FOR	NUMBER FILED	NUMBER EXTRA	RATE ($)	FEE ($)		RATE ($)	FEE ($)
☐ BASIC FEE (37 CFR 1.16(a), (b), or (c))	N/A	N/A	N/A			N/A	
☐ SEARCH FEE (37 CFR 1.16(k), (i), or (m))	N/A	N/A	N/A			N/A	
☐ EXAMINATION FEE (37 CFR 1.16(o), (p), or (q))	N/A	N/A	N/A			N/A	
TOTAL CLAIMS (37 CFR 1.16(i))	minus 20 =	*	X $ =		OR	X $ =	
INDEPENDENT CLAIMS (37 CFR 1.16(h))	minus 3 =	*	X $ =			X $ =	
☐ APPLICATION SIZE FEE (37 CFR 1.16(s))	If the specification and drawings exceed 100 sheets of paper, the application size fee due is $250 ($125 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).						
☐ MULTIPLE DEPENDENT CLAIM PRESENT (37 CFR 1.16(j))							
* If the difference in column 1 is less than zero, enter "0" in column 2.			TOTAL			TOTAL	

APPLICATION AS AMENDED – PART II

AMENDMENT	03/23/2007	(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA	SMALL ENTITY RATE ($)	ADDITIONAL FEE ($)	OR	OTHER THAN SMALL ENTITY RATE ($)	ADDITIONAL FEE ($)
	Total (37 CFR 1.16(i))	* 18	Minus	** 37	= 0	X $ =		OR	X $50=	0
	Independent (37 CFR 1.16(h))	* 8	Minus	***12	= 0	X $ =		OR	X $200=	0
	☐ Application Size Fee (37 CFR 1.16(s))									
	☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))							OR		
						TOTAL ADD'L FEE		OR	TOTAL ADD'L FEE	0

AMENDMENT		(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA	RATE ($)	ADDITIONAL FEE ($)		RATE ($)	ADDITIONAL FEE ($)
	Total (37 CFR 1.16(i))	*	Minus	**	=	X $ =		OR	X $ =	
	Independent (37 CFR 1.16(h))	*	Minus	***	=	X $ =		OR	X $ =	
	☐ Application Size Fee (37 CFR 1.16(s))									
	☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))							OR		
						TOTAL ADD'L FEE		OR	TOTAL ADD'L FEE	

* If the entry in column 1 is less than the entry in column 2, write "0" in column 3.
** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20".
*** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3".
The "Highest Number Previously Paid For" (Total or Independent) is the highest number found in the appropriate box in column 1.

Legal Instrument Examiner:
Rozenia Harmon

This collection of information is required by 37 CFR 1.16. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

EAST Search History

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L1	64	(core near3 (voltage power)) with ((enough sufficient) near6 (operat$3 activ$5 execut$3))	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2007/04/03 13:43
L2	13	1.clm.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2007/04/03 13:46
L3	1500	713/320.ccls.	US-PGPUB; USPAT; USOCR	OR	OFF	2007/04/03 14:41
L4	934	(voltage adj1 regulator$1) with (mode near8 (chang$3 switch$3))	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2007/04/03 14:01
L5	0	("core voltage" near5 (low$2 reduc$3)) same 4	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2007/04/03 14:38
L6	5	("core voltage" near5 (low$2 reduc$3)) and 4	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2007/04/03 14:38
L7	2744	713/300.ccls.	US-PGPUB; USPAT; USOCR	OR	OFF	2007/04/03 14:41
L8	79	(stop$3 or disable$1) near4 clock same ((reduc$3 or lower$3) near8 core)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2007/04/03 14:53
L9	5	8.clm.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2007/04/03 14:53

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

NOTICE OF ALLOWANCE AND FEE(S) DUE

7590 04/11/2007

WAGNER, MURABITO & HAO LLP
TWO NORTH MARKET STREET
THIRD FLOOR
SAN JOSE, CA 95113

EXAMINER	
CAO, CHUN	
ART UNIT	PAPER NUMBER
2115	

DATE MAILED: 04/11/2007

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/694,433	10/23/2000	Andrew Read	TRANS59	3072

TITLE OF INVENTION: SAVING POWER WHEN IN OR TRANSITIONING TO A STATIC MODE OF A PROCESSOR

APPLN. TYPE	SMALL ENTITY	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	NO	$1400	$0	$0	$1400	07/11/2007

THE APPLICATION IDENTIFIED ABOVE HAS BEEN EXAMINED AND IS ALLOWED FOR ISSUANCE AS A PATENT. PROSECUTION ON THE MERITS IS CLOSED. THIS NOTICE OF ALLOWANCE IS NOT A GRANT OF PATENT RIGHTS. THIS APPLICATION IS SUBJECT TO WITHDRAWAL FROM ISSUE AT THE INITIATIVE OF THE OFFICE OR UPON PETITION BY THE APPLICANT. SEE 37 CFR 1.313 AND MPEP 1308.

THE ISSUE FEE AND PUBLICATION FEE (IF REQUIRED) MUST BE PAID WITHIN THREE MONTHS FROM THE MAILING DATE OF THIS NOTICE OR THIS APPLICATION SHALL BE REGARDED AS ABANDONED. THIS STATUTORY PERIOD CANNOT BE EXTENDED. SEE 35 U.S.C. 151. THE ISSUE FEE DUE INDICATED ABOVE DOES NOT REFLECT A CREDIT FOR ANY PREVIOUSLY PAID ISSUE FEE IN THIS APPLICATION. IF AN ISSUE FEE HAS PREVIOUSLY BEEN PAID IN THIS APPLICATION (AS SHOWN ABOVE), THE RETURN OF PART B OF THIS FORM WILL BE CONSIDERED A REQUEST TO REAPPLY THE PREVIOUSLY PAID ISSUE FEE TOWARD THE ISSUE FEE NOW DUE.

HOW TO REPLY TO THIS NOTICE:

I. Review the SMALL ENTITY status shown above.

If the SMALL ENTITY is shown as YES, verify your current SMALL ENTITY status:

A. If the status is the same, pay the TOTAL FEE(S) DUE shown above.

B. If the status above is to be removed, check box 5b on Part B - Fee(s) Transmittal and pay the PUBLICATION FEE (if required) and twice the amount of the ISSUE FEE shown above, or

If the SMALL ENTITY is shown as NO:

A. Pay TOTAL FEE(S) DUE shown above, or

B. If applicant claimed SMALL ENTITY status before, or is now claiming SMALL ENTITY status, check box 5a on Part B - Fee(s) Transmittal and pay the PUBLICATION FEE (if required) and 1/2 the ISSUE FEE shown above.

II. PART B - FEE(S) TRANSMITTAL, or its equivalent, must be completed and returned to the United States Patent and Trademark Office (USPTO) with your ISSUE FEE and PUBLICATION FEE (if required). If you are charging the fee(s) to your deposit account, section "4b" of Part B - Fee(s) Transmittal should be completed and an extra copy of the form should be submitted. If an equivalent of Part B is filed, a request to reapply a previously paid issue fee must be clearly made, and delays in processing may occur due to the difficulty in recognizing the paper as an equivalent of Part B.

III. All communications regarding this application must give the application number. Please direct all communications prior to issuance to Mail Stop ISSUE FEE unless advised to the contrary.

IMPORTANT REMINDER: Utility patents issuing on applications filed on or after Dec. 12, 1980 may require payment of maintenance fees. It is patentee's responsibility to ensure timely payment of maintenance fees when due.

PTOL-85 (Rev. 07/06) Approved for use through 04/30/2007.

PART B - FEE(S) TRANSMITTAL

Complete and send this form, together with applicable fee(s), to: Mail **Mail Stop ISSUE FEE**
Commissioner for Patents
P.O. Box 1450
Alexandria, Virginia 22313-1450
or Fax (571)-273-2885

INSTRUCTIONS: This form should be used for transmitting the ISSUE FEE and PUBLICATION FEE (if required). Blocks 1 through 5 should be completed where appropriate. All further correspondence including the Patent, advance orders and notification of maintenance fees will be mailed to the current correspondence address as indicated unless corrected below or directed otherwise in Block 1, by (a) specifying a new correspondence address; and/or (b) indicating a separate "FEE ADDRESS" for maintenance fee notifications.

CURRENT CORRESPONDENCE ADDRESS (Note: Use Block 1 for any change of address)

7590 04/11/2007

WAGNER, MURABITO & HAO LLP
TWO NORTH MARKET STREET
THIRD FLOOR
SAN JOSE, CA 95113

Note: A certificate of mailing can only be used for domestic mailings of the Fee(s) Transmittal. This certificate cannot be used for any other accompanying papers. Each additional paper, such as an assignment or formal drawing, must have its own certificate of mailing or transmission.

Certificate of Mailing or Transmission
I hereby certify that this Fee(s) Transmittal is being deposited with the United States Postal Service with sufficient postage for first class mail in an envelope addressed to the Mail Stop ISSUE FEE address above, or being facsimile transmitted to the USPTO (571) 273-2885, on the date indicated below.

(Depositor's name)
(Signature)
(Date)

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/694,433	10/23/2000	Andrew Read	TRANS59	3072

TITLE OF INVENTION: SAVING POWER WHEN IN OR TRANSITIONING TO A STATIC MODE OF A PROCESSOR

APPLN. TYPE	SMALL ENTITY	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	NO	$1400	$0	$0	$1400	07/11/2007

EXAMINER	ART UNIT	CLASS-SUBCLASS
CAO, CHUN	2115	713-001000

1. Change of correspondence address or indication of "Fee Address" (37 CFR 1.363).

☐ Change of correspondence address (or Change of Correspondence Address form PTO/SB/122) attached.

☐ "Fee Address" indication (or "Fee Address" Indication form PTO/SB/47; Rev 03-02 or more recent) attached. **Use of a Customer Number is required.**

2. For printing on the patent front page, list

(1) the names of up to 3 registered patent attorneys or agents OR, alternatively,

(2) the name of a single firm (having as a member a registered attorney or agent) and the names of up to 2 registered patent attorneys or agents. If no name is listed, no name will be printed.

1 _____

2 _____

3 _____

3. ASSIGNEE NAME AND RESIDENCE DATA TO BE PRINTED ON THE PATENT (print or type)

PLEASE NOTE: Unless an assignee is identified below, no assignee data will appear on the patent. If an assignee is identified below, the document has been filed for recordation as set forth in 37 CFR 3.11. Completion of this form is NOT a substitute for filing an assignment.

(A) NAME OF ASSIGNEE (B) RESIDENCE: (CITY and STATE OR COUNTRY)

Please check the appropriate assignee category or categories (will not be printed on the patent) : ☐ Individual ☐ Corporation or other private group entity ☐ Government

4a. The following fee(s) are submitted:

☐ Issue Fee

☐ Publication Fee (No small entity discount permitted)

☐ Advance Order - # of Copies _____

4b. Payment of Fee(s): **(Please first reapply any previously paid issue fee shown above)**

☐ A check is enclosed.

☐ Payment by credit card. Form PTO-2038 is attached.

☐ The Director is hereby authorized to charge the required fee(s), any deficiency, or credit any overpayment, to Deposit Account Number _____ (enclose an extra copy of this form).

5. **Change in Entity Status** (from status indicated above)

☐ a. Applicant claims SMALL ENTITY status. See 37 CFR 1.27.

☐ b. Applicant is no longer claiming SMALL ENTITY status. See 37 CFR 1.27(g)(2).

NOTE: The Issue Fee and Publication Fee (if required) will not be accepted from anyone other than the applicant; a registered attorney or agent; or the assignee or other party in interest as shown by the records of the United States Patent and Trademark Office.

Authorized Signature _____ Date _____

Typed or printed name _____ Registration No. _____

This collection of information is required by 37 CFR 1.311. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, Virginia 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, Virginia 22313-1450.

Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/694,433	10/23/2000	Andrew Read	TRANS59	3072

7590 04/11/2007

WAGNER, MURABITO & HAO LLP
TWO NORTH MARKET STREET
THIRD FLOOR
SAN JOSE, CA 95113

EXAMINER	
CAO, CHUN	
ART UNIT	PAPER NUMBER
2115	

DATE MAILED: 04/11/2007

Determination of Patent Term Adjustment under 35 U.S.C. 154 (b)
(application filed on or after May 29, 2000)

The Patent Term Adjustment to date is 35 day(s). If the issue fee is paid on the date that is three months after the mailing date of this notice and the patent issues on the Tuesday before the date that is 28 weeks (six and a half months) after the mailing date of this notice, the Patent Term Adjustment will be 35 day(s).

If a Continued Prosecution Application (CPA) was filed in the above-identified application, the filing date that determines Patent Term Adjustment is the filing date of the most recent CPA.

Applicant will be able to obtain more detailed information by accessing the Patent Application Information Retrieval (PAIR) WEB site (http://pair.uspto.gov).

Any questions regarding the Patent Term Extension or Adjustment determination should be directed to the Office of Patent Legal Administration at (571)-272-7702. Questions relating to issue and publication fee payments should be directed to the Customer Service Center of the Office of Patent Publication at 1-(888)-786-0101 or (571)-272-4200.

PTOL-85 (Rev. 07/06) Approved for use through 04/30/2007.

Notice of Allowability	Application No.	Applicant(s)	
	09/694,433	READ ET AL.	
	Examiner	Art Unit	
	Chun Cao	2115	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to *amendment filed on 3/23/07*.

2. ☒ The allowed claim(s) is/are *1-18*.

3. ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
   a) ☐ All b) ☐ Some* c) ☐ None of the:
      1. ☐ Certified copies of the priority documents have been received.
      2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
      3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

   * Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

4. ☐ A SUBSTITUTE OATH OR DECLARATION must be submitted. Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL PATENT APPLICATION (PTO-152) which gives reason(s) why the oath or declaration is deficient.

5. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
   (a) ☐ including changes required by the Notice of Draftsperson's Patent Drawing Review (PTO-948) attached
      1) ☐ hereto or 2) ☐ to Paper No./Mail Date _____.
   (b) ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.

   Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).

6. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☐ Notice of References Cited (PTO-892)
2. ☐ Notice of Draftperson's Patent Drawing Review (PTO-948)
3. ☐ Information Disclosure Statements (PTO/SB/08), Paper No./Mail Date _____
4. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material
5. ☐ Notice of Informal Patent Application
6. ☐ Interview Summary (PTO-413), Paper No./Mail Date _____ .
7. ☐ Examiner's Amendment/Comment
8. ☐ Examiner's Statement of Reasons for Allowance
9. ☐ Other _____.

CHUN CAO
PRIMARY EXAMINER

Issue Classification	Application/Control No. 09/694,433	Applicant(s)/Patent under Reexamination READ ET AL.
	Examiner Chun Cao	Art Unit 2115

ISSUE CLASSIFICATION

ORIGINAL		INTERNATIONAL CLASSIFICATION									
CLASS	SUBCLASS	CLAIMED					NON-CLAIMED				
713	320	G	06	F	1	132					
CROSS REFERENCES											
CLASS	SUBCLASS (ONE SUBCLASS PER BLOCK)										
713	300										

(Assistant Examiner) (Date)

(Legal Instruments Examiner) (Date)

CHUN CAO
PRIMARY EXAMINER
4/4/07
(Primary Examiner) (Date)

Total Claims Allowed: 18

O.G. Print Claim(s)	O.G. Print Fig.
1	5

☐ Claims renumbered in the same order as presented by applicant ☐ CPA ☐ T.D. ☐ R.1.47

Final	Original	Final	Original	Final	Original	Final	Original	Final	Original	Final	Original	Final	Original
1	1		31		61		91		121		151		181
2	2		32		62		92		122		152		182
3	3		33		63		93		123		153		183
4	4		34		64		94		124		154		184
6	5		35		65		95		125		155		185
7	6		36		66		96		126		156		186
8	7		37		67		97		127		157		187
9	8		38		68		98		128		158		188
10	9		39		69		99		129		159		189
11	10		40		70		100		130		160		190
12	11		41		71		101		131		161		191
13	12		42		72		102		132		162		192
14	13		43		73		103		133		163		193
15	14		44		74		104		134		164		194
16	15		45		75		105		135		165		195
17	16		46		76		106		136		166		196
18	17		47		77		107		137		167		197
5	18		48		78		108		138		168		198
	19		49		79		109		139		169		199
	20		50		80		110		140		170		200
	21		51		81		111		141		171		201
	22		52		82		112		142		172		202
	23		53		83		113		143		173		203
	24		54		84		114		144		174		204
	25		55		85		115		145		175		205
	26		56		86		116		146		176		206
	27		57		87		117		147		177		207
	28		58		88		118		148		178		208
	29		59		89		119		149		179		209
	30		60		90		120		150		180		210

Search Notes	Application/Control No.	Applicant(s)/Patent under Reexamination
	09/694,433	READ ET AL.
	Examiner	Art Unit
	Chun Cao	2115

SEARCHED			
Class	Subclass	Date	Examiner

INTERFERENCE SEARCHED			
Class	Subclass	Date	Examiner
713	300,320	4/3/2007	CC
PGPUB text search		4/3/2007	CC

SEARCH NOTES (INCLUDING SEARCH STRATEGY)		
	DATE	EXMR
East updated search	4/3/2007	CC

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United States Patent and Trademark Office
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Bib Data Sheet

CONFIRMATION NO. 3072

SERIAL NUMBER	FILING OR 371(c) DATE	CLASS	GROUP ART UNIT	ATTORNEY DOCKET NO.
09/694,433	10/23/2000 RULE	713	2115	TRANS59

APPLICANTS

Andrew Read, Sunnyvale, CA;
Sameer Halepete, San Jose, CA;
Keith Klayman, Sunnyvale, CA;

** CONTINUING DATA **********

** FOREIGN APPLICATIONS **********

IF REQUIRED, FOREIGN FILING LICENSE GRANTED
** 12/15/2000

Foreign Priority claimed	STATE OR COUNTRY	SHEETS DRAWING	TOTAL CLAIMS	INDEPENDENT CLAIMS
☐ yes ☑ no	CA	2	~~13~~ 18	2 8
35 USC 119 (a-d) conditions met ☐ yes ☑ no ☐ Met after Allowance				
Verified and Acknowledged MAO Examiner's Signature — Initials				

ADDRESS
WAGNER, MURABITO & HAO LLP
TWO NORTH MARKET STREET
THIRD FLOOR
SAN JOSE, CA95113

TITLE

SAVING POWER WHEN IN OR TRANSITIONING TO A STATIC MODE OF A PROCESSOR

FILING FEE RECEIVED		
2980	FEES: Authority has been given in Paper No. _____ to charge/credit DEPOSIT ACCOUNT No. _____ for following:	☐ All Fees ☐ 1.16 Fees (Filing) ☐ 1.17 Fees (Processing Ext. of time) ☐ 1.18 Fees (Issue) ☐ Other _____ ☐ Credit

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Docket No.: TRAN-P059

I hereby certify that this transmittal of the below described document is being deposited with the United States Postal Service in an envelope bearing First Class Postage and addressed to the Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450, on the below date of deposit.

Date of Deposit:	7/11/07	Name of Person Making the Deposit:	Mina Oliveri	Signature of the Person Making the Deposit:	Mina Oliveri

Inventor(s): Read et al.

Serial No.: 09/694,433 Group Art Unit: 2115

Filed: 10/23/2000 Examiner: Cao, Chun

Confirmation No: 3072

Title: SAVING POWER WHEN IN OR TRANSITIONING TO A STATIC MODE OF A PROCESSOR

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450
ATTENTION: Mail Stop Issue Fee
Sir:

TRANSMITTAL OF PAYMENT OF ISSUE FEE (37 CFR 1.311)

1. Applicant hereby pays the issue fee for the attached Issue Fee Transmittal PTOL-85

2. [X] Applicant is other than a small entity

Fee Calculation

(for other than a small entity)				
Application Status is:		Regular	Design	Total
Fee (CFR 1.18(a) and (b)):	X	$1,400.00	$800.00	1,400.00
Additional Copies (10 @ $3.00)				30.00
Total Fees				1,430.00

PAYMENT OF FEES

1. The full fee due in connection with this communication is provided as follows:

[X] The Commissioner is hereby authorized to charge any additional fees associated with this communication or credit any overpayment to Deposit Account No.:50-4160.
A duplicate copy of this authorization is enclosed.

[X] A check in the amount of $1,430.00

[ ] Charge any fees required or credit any overpayments associated with this filing to Deposit Account No.: 50-4160.

rev. 12/04 dbp

Please direct all correspondence concerning the above-identified application to the following address:

MURABITO, HAO & BARNES LLP
Two North Market Street, Third Floor
San Jose, California 95113
(408) 938-9060

Respectfully submitted,

Date: 7/11/2007

By: _____
Anthony C. Murabito
Reg. No.: 35,295

rev. 12/04 dbp

PART B - FEE(S) TRANSMITTAL

Complete and send this form, together with applicable fee(s), to: Mail Mail Stop ISSUE FEE
Commissioner for Patents
P.O. Box 1450
Alexandria, Virginia 22313-1450
or Fax (571)-273-2885

INSTRUCTIONS: This form should be used for transmitting the ISSUE FEE and PUBLICATION FEE (if required). Blocks 1 through 5 should be completed where appropriate. All further correspondence including the Patent, advance orders and notification of maintenance fees will be mailed to the current correspondence address as indicated unless corrected below or directed otherwise in Block 1, by (a) specifying a new correspondence address; and/or (b) indicating a separate "FEE ADDRESS" for maintenance fee notifications.

CURRENT CORRESPONDENCE ADDRESS (Note: Use Block 1 for any change of address)

7590 04/11/2007

WAGNER, MURABITO & HAO LLP
TWO NORTH MARKET STREET
THIRD FLOOR
SAN JOSE, CA 95113

07/17/2007 FMETEKI2 00000038 09694433

01 FC:1501 1400.00 OP
02 FC:8001 30.00 OP

Note: A certificate of mailing can only be used for domestic mailings of the Fee(s) Transmittal. This certificate cannot be used for any other accompanying papers. Each additional paper, such as an assignment or formal drawing, must have its own certificate of mailing or transmission.

Certificate of Mailing or Transmission

I hereby certify that this Fee(s) Transmittal is being deposited with the United States Postal Service with sufficient postage for first class mail in an envelope addressed to the Mail Stop ISSUE FEE address above, or being facsimile transmitted to the USPTO (571) 273-2885, on the date indicated below.

Mina Oliveri	(Depositor's name)
Mina Oliveri	(Signature)
7/11/07	(Date)

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/694,433	10/23/2000	Andrew Read	TRANS59	3072

TITLE OF INVENTION: SAVING POWER WHEN IN OR TRANSITIONING TO A STATIC MODE OF A PROCESSOR

APPLN. TYPE	SMALL ENTITY	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	NO	$1400	$0	$0	$1400	07/11/2007

EXAMINER	ART UNIT	CLASS-SUBCLASS
CAO, CHUN	2115	713-001000

1. Change of correspondence address or indication of "Fee Address" (37 CFR 1.363).

☐ Change of correspondence address (or Change of Correspondence Address form PTO/SB/122) attached.

☐ "Fee Address" indication (or "Fee Address" Indication form PTO/SB/47; Rev 03-02 or more recent) attached. **Use of a Customer Number is required.**

2. For printing on the patent front page, list

(1) the names of up to 3 registered patent attorneys or agents OR, alternatively,

(2) the name of a single firm (having as a member a registered attorney or agent) and the names of up to 2 registered patent attorneys or agents. If no name is listed, no name will be printed.

1 _____
2 _____
3 _____

3. ASSIGNEE NAME AND RESIDENCE DATA TO BE PRINTED ON THE PATENT (print or type)

PLEASE NOTE: Unless an assignee is identified below, no assignee data will appear on the patent. If an assignee is identified below, the document has been filed for recordation as set forth in 37 CFR 3.11. Completion of this form is NOT a substitute for filing an assignment.

(A) NAME OF ASSIGNEE: Transmeta Corporation

(B) RESIDENCE: (CITY and STATE OR COUNTRY): Santa Clara, CA

Please check the appropriate assignee category or categories (will not be printed on the patent) : ☐ Individual ☒ Corporation or other private group entity ☐ Government

4a. The following fee(s) are submitted:

☒ Issue Fee

☐ Publication Fee (No small entity discount permitted)

☒ Advance Order - # of Copies 10

4b. Payment of Fee(s): **(Please first reapply any previously paid issue fee shown above)**

☒ A check is enclosed.

☐ Payment by credit card. Form PTO-2038 is attached.

☒ The Director is hereby authorized to charge the required fee(s), any deficiency, or credit any overpayment, to Deposit Account Number 50-4160 (enclose an extra copy of this form).

5. **Change in Entity Status** (from status indicated above)

☐ a. Applicant claims SMALL ENTITY status. See 37 CFR 1.27.

☐ b. Applicant is no longer claiming SMALL ENTITY status. See 37 CFR 1.27(g)(2).

NOTE: The Issue Fee and Publication Fee (if required) will not be accepted from anyone other than the applicant; a registered attorney or agent; or the assignee or other party in interest as shown by the records of the United States Patent and Trademark Office.

Authorized Signature _____ Date 7/11/2007

Typed or printed name Anthony C. Murabito Registration No. 35,295

This collection of information is required by 37 CFR 1.311. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, Virginia 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, Virginia 22313-1450.

Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	ISSUE DATE	PATENT NO.	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/694,433	08/21/2007	7260731	TRANS59	3072

7590 08/01/2007

WAGNER, MURABITO & HAO LLP
TWO NORTH MARKET STREET
THIRD FLOOR
SAN JOSE, CA 95113

ISSUE NOTIFICATION

The projected patent number and issue date are specified above.

Determination of Patent Term Adjustment under 35 U.S.C. 154 (b)
(application filed on or after May 29, 2000)

The Patent Term Adjustment is 30 day(s). Any patent to issue from the above-identified application will include an indication of the adjustment on the front page.

If a Continued Prosecution Application (CPA) was filed in the above-identified application, the filing date that determines Patent Term Adjustment is the filing date of the most recent CPA.

Applicant will be able to obtain more detailed information by accessing the Patent Application Information Retrieval (PAIR) WEB site (http://pair.uspto.gov).

Any questions regarding the Patent Term Extension or Adjustment determination should be directed to the Office of Patent Legal Administration at (571)-272-7702. Questions relating to issue and publication fee payments should be directed to the Customer Service Center of the Office of Patent Publication at (571)-272-4200.

APPLICANT(s) (Please see PAIR WEB site http://pair.uspto.gov for additional applicants):

Andrew Read, Sunnyvale, CA;
Sameer Halepete, San Jose, CA;
Keith Klayman, Sunnyvale, CA;

IR103 (Rev. 11/05)

Attorney Docket No.: TRAN-P059

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

I hereby certify that this transmittal of the below described document is being deposited with the United States Postal Service in an envelope bearing First Class Postage and addressed to the Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450 on the below date of deposit.					
Date of Deposit:	8/21/2007	Name of Person Making the Deposit:	Mina Oliveri	Signature of the Person Making the Deposit:	Mina Oliveri

In re Application of:

Inventor(s): Andrew Read, Sameer Halapete, and Keith Klayman

Application No.: 09/694,433

Filed: 10/23/2000

Title: SAVING POWER WHEN IN OR TRANSITIONING TO A STATIC MODE OF A PROCESSOR

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

CONDITIONAL PETITION FOR EXTENSION OF TIME

This conditional petition is being filed along with the accompanying DIVISIONAL and provides for the possibility that applicant has inadvertently overlooked the need for a petition and fee for extension of time.

Conditional petition for extension of time

If any extension of time for the accompanying response is required, applicant requests that this be considered a petition therefor.

Status

This application is on behalf of

[X] other than a small entity
[ ] a small entity
A verified statement:
[ ] is attached
[ ] is already filed

[ ] The Commissioner is hereby authorized to charge any additional fees associated with this communication or credit any overpayment to Deposit Account No.: 50-4160.
A duplicate copy of this authorization is enclosed.

rev. 6/97 jpw

Please direct all correspondence concerning the above-identified application to the following address:

MURABITO, HAO & BARNES LLP
Two North Market Street, Third Floor
San Jose, California 95113
(408) 938-9060
Customer No: 45590

Respectfully submitted,

Date: August 21, 2007

By: _____
Anthony C. Murabito
Reg. No. 35,295

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NUMBER	PATENT NUMBER	GROUP ART UNIT	FILE WRAPPER LOCATION
09/694,433	7260731	2115	9200

OC000000031805142

Correspondence Address/Fee Address Change

The following fields have been set to Customer Number 45590 on 08/27/2008

- **Correspondence Address**
- **Maintenance Fee Address**
- **Power of Attorney Address**

The address of record for Customer Number 45590 is:

45590
TRANSMETA C/O MURABITO, HAO & BARNES LLP
TWO NORTH MARKET STREET
THIRD FLOOR
SAN JOSE, CA 95113

PATENT ASSIGNMENT COVER SHEET

Electronic Version v1.1
Stylesheet Version v1.2

EPAS ID: PAT6027515

SUBMISSION TYPE:	NEW ASSIGNMENT
NATURE OF CONVEYANCE:	NUNC PRO TUNC ASSIGNMENT
EFFECTIVE DATE:	01/10/2020
SEQUENCE:	2

CONVEYING PARTY DATA

Name	Execution Date
INTELLECTUAL VENTURES ASSETS 156 LLC	01/10/2020

RECEIVING PARTY DATA

Name:	INNOVATIVE SILICON SOLUTIONS, LLC
Street Address:	2382 ROCKFIELD BLVD.
Internal Address:	SUITE 170
City:	LAKE FOREST
State/Country:	CALIFORNIA
Postal Code:	92630

PROPERTY NUMBERS Total: 10

Property Type	Number
Patent Number:	7260731
Patent Number:	7870404
Patent Number:	9436264
Patent Number:	9690366
Patent Number:	7302619
Patent Number:	7600166
Patent Number:	7334173
Patent Number:	7634701
Patent Number:	7810002
Patent Number:	6774033

CORRESPONDENCE DATA

Fax Number:

Correspondence will be sent to the e-mail address first; if that is unsuccessful, it will be sent using a fax number, if provided; if that is unsuccessful, it will be sent via US Mail.

Phone: 949-791-9366
Email: fahim@hongdungroup.com
Correspondent Name: FAHIM AFTAB
Address Line 1: 2382 ROCKFIELD BLVD.

Address Line 2:	SUITE 170
Address Line 4:	LAKE FOREST, CALIFORNIA 92630
ATTORNEY DOCKET NUMBER:	JG032320-2
NAME OF SUBMITTER:	FAHIM AFTAB
SIGNATURE:	/Fahim Aftab/
DATE SIGNED:	03/23/2020
	This document serves as an Oath/Declaration (37 CFR 1.63).

Total Attachments: 3
source=IV Assignment A-2#page1.tif
source=IV Assignment A-2#page2.tif
source=IV Assignment A-2#page3.tif

Exhibit A-2

ASSIGNMENT OF PATENT RIGHTS

For good and valuable consideration, the receipt of which is hereby acknowledged, Intellectual Ventures Assets 156 LLC, a Delaware limited liability company, with an address at 251 Little Falls Drive, Wilmington, DE 19808 ("***Assignor***"), does hereby sell, assign, transfer, and convey unto Innovative Silicon Solutions, LLC, a Texas limited liability company having an address at 5900 Balcones Drive, STE 100, Austin, TX 78731 ("***Assignee***"), all of Assignor's right, title, and interest in and to the following (collectively, the "***Assigned Patent Rights***"):

(a) the patents and patent applications listed in the table below (the "***Patents***");

Active Patent(s) – (Filed; Granted)

Patent/Application Number	Country	Issue Date/ Filing Date	Title of Patent and First Named Inventor
7260731 (09/694433)	US	2007-08-21 (2000-10-23)	Saving Power When In Or Transitioning To A Static Mode Of A Processor Andrew Read
7870404 (11/894991)	US	2011-01-11 (2007-08-21)	Transitioning To And From A Sleep State Of A Processor Andrew Read
9436264 (12/987423)	US	2016-09-06 (2011-01-10)	Saving Power When In Or Transitioning To A Static Mode Of A Processor Andrew Read
9690366 (15/241690)	US	2017-06-27 (2016-08-19)	Saving Power When In Or Transitioning To A Static Mode Of A Processor By Using Feedback-Configured Voltage Regulator Andrew Read
7302619 (10/885356)	US	2007-11-27 (2004-07-06)	Error Correction In A Cache Memory Joseph Tompkins
7600166 (11/169403)	US	2009-10-06 (2005-06-28)	Method And System For Providing Trusted Access To A JTAG Scan Interface In A Microprocessor David Dunn
7334173 (11/241104)	US	2008-02-19 (2005-09-29)	Method And System For Protecting Processors From Unauthorized Debug Access

Patent/Application Number	Country	Issue Date/ Filing Date	Title of Patent and First Named Inventor
			Morgan, Andrew
TWI325534 (TW095136358)	TW	2010-06-01 (2006-09-29)	Securing Scan Test Architecture Morgan, Andrew
7634701 (12/033864)	US	2009-12-15 (2008-02-19)	Method And System For Protecting Processors From Unauthorized Debug Access Morgan, Andrew
7810002 (12/544145)	US	2010-10-05 (2009-08-19)	Providing Trusted Access To A Jtag Scan Interface In A Microprocessor David Dunn
6774033 (10/287258)	US	2004-08-10 (2002-11-04)	Metal Stack For Local Interconnect Layer Ben-Tzur, Mira

(b) any future reissues, reexaminations, extensions, continuations, continuing prosecution application, requests for continuing examinations, divisions, and registrations of any of the Patents;

(c) rights to apply in any or all countries of the world for future patents, certificates of invention, utility models, industrial design protections, design patent protections, or other future governmental grants or issuances of any type related to the Patents; and

(d) causes of action and enforcement rights of any kind under, or on account of, any of the Patents and/or any of the items described in either of the foregoing categories (b) or (c), including, without limitation, all causes of action, enforcement rights and all other rights to seek and obtain any other remedies of any kind for past, current and future infringement.

Assignor hereby authorizes the respective patent office or governmental agency in each jurisdiction to issue any and all future patents, certificates of invention, utility models or other governmental grants or issuances that may be granted upon any of the Assigned Patent Rights in the name of Assignee, as the assignee to the entire interest therein. This Assignment of Patent Rights will inure for the benefit of any permitted successors or assigns of Assignee.

Assignor will, at the reasonable request of Assignee, take all reasonable steps necessary and proper, to confirm the assignment to Assignee of the Assigned Patent Rights pursuant to this Assignment of Patent Rights, including without limitation, the execution, acknowledgment, and recordation of specific assignments, oaths, declarations, and other documents on a country-by-country basis, to assist Assignee in obtaining and perfecting the Assigned Patent Rights.

IN WITNESS WHEREOF this Assignment of Patent Rights is executed on January 10, 2020 to be effective as of January 10, 2020.

ASSIGNOR:

INTELLECTUAL VENTURES ASSETS 156 LLC
By: _____
Name: Jim Weisfield
Title: Authorized Person

PATENT ASSIGNMENT COVER SHEET

Electronic Version v1.1
Stylesheet Version v1.2

EPAS ID: PAT6036476

SUBMISSION TYPE:	CORRECTIVE ASSIGNMENT
NATURE OF CONVEYANCE:	Corrective Assignment to correct the RE-RECORD ASSIGNMENT PREVIOUSLY RECORDED UNDER 052199/0838 TO CORRECT ADDRESS OF RECEIVING PARTY. previously recorded on Reel 052199 Frame 0838. Assignor(s) hereby confirms the NUNC PRO TUNC ASSIGNMENT.
SEQUENCE:	2

CONVEYING PARTY DATA

Name	Execution Date
INTELLECTUAL VENTURES ASSETS 156 LLC	01/10/2020

RECEIVING PARTY DATA

Name:	INNOVATIVE SILICON SOLUTIONS, LLC
Street Address:	5900 BALCONES DRIVE
City:	AUSTIN
State/Country:	TEXAS
Postal Code:	78731

PROPERTY NUMBERS Total: 10

Property Type	Number
Patent Number:	7260731
Patent Number:	7870404
Patent Number:	9436264
Patent Number:	9690366
Patent Number:	7302619
Patent Number:	7600166
Patent Number:	7334173
Patent Number:	7634701
Patent Number:	7810002
Patent Number:	6774033

CORRESPONDENCE DATA

Fax Number:

Correspondence will be sent to the e-mail address first; if that is unsuccessful, it will be sent using a fax number, if provided; if that is unsuccessful, it will be sent via US Mail.

Phone: 9497919366
Email: fahim@hongdungroup.com
Correspondent Name: FAHIM AFTAB

Address Line 1:	23832 ROCKFIELD BLVD.
Address Line 2:	SUITE 170
Address Line 4:	LAKE FOREST, CALIFORNIA 92630

ATTORNEY DOCKET NUMBER:	JG032320-2 CORRECTED
NAME OF SUBMITTER:	FAHIM AFTAB
SIGNATURE:	/Fahim Aftab/
DATE SIGNED:	03/28/2020
	This document serves as an Oath/Declaration (37 CFR 1.63).

Total Attachments: 6
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source=IV156 Assignment to ISS#page6.tif

Electronic Patent Assignment System

Confirmation Receipt

Your assignment has been received by the USPTO.
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PATENT ASSIGNMENT COVER SHEET

Electronic Version v1.1
Stylesheet Version v1.2

SUBMISSION TYPE:	NEW ASSIGNMENT
NATURE OF CONVEYANCE:	NUNC PRO TUNC ASSIGNMENT
EFFECTIVE DATE:	01/10/2020
SEQUENCE:	2

CONVEYING PARTY DATA

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INTELLECTUAL VENTURES ASSETS 156 LLC	01/10/2020

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Internal Address:	SUITE 170
City:	LAKE FOREST
State/Country:	CALIFORNIA
Postal Code:	92630

PROPERTY NUMBERS Total: 10

Property Type	Number (Issue Date)
Patent Number:	7260731 8/21/2007 09/694,433

Fees Paid

Patent Number:	7870404	01/11/2011	11/894,991	expires	01/11/22
Patent Number:	9436264	9/6/2016	12/987,423	Fees Due	9/6/23
Patent Number:	9690366	6/27/2017	15/241,690	Fees Due	6/27/2020
Patent Number:	7302619	11/27/2007	10/885,356	Fees Paid	3.5yr
Patent Number:	7600166	10/06/2009	11/169,403	Fees due	10/06/2020
Patent Number:	7334173	02/19/2008	11/241,104	Fees Paid	
Patent Number:	7634701	12/15/2009	12/033,864	Fees Due	12/15/2020
Patent Number:	7810002	10/05/2010	12/544,145	Fees Due	10/05/2021
Patent Number:	6774033	08/10/2004	10/287,255	Fees Paid	

11.5yr window

CORRESPONDENCE DATA

Fax Number:
Phone: 949-791-9366
Email: fahim@hongdangroup.com

Correspondence will be sent to the e-mail address first; if that is unsuccessful, it will be sent using a fax number, if provided; if that is unsuccessful, it will be sent via US Mail.

Correspondent Name: FAHIM AFTAB
Address Line 1: 2382 ROCKFIELD BLVD
Address Line 2: SUITE 170
Address Line 4: LAKE FOREST, CALIFORNIA 92630

ATTORNEY DOCKET NUMBER:	JG032320-2
NAME OF SUBMITTER:	FAHIM AFTAB
Signature:	/Fahim Aftab/
Date:	03/23/2020
	This document serves as an Oath/Declaration (37 CFR 1.63).

Total Attachments: 3
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source=IV Assignment A-2#page3.tif

RECEIPT INFORMATION

EPAS ID: PAT6037515
Receipt Date: 03/23/2020

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Exhibit A-2

ASSIGNMENT OF PATENT RIGHTS

For good and valuable consideration, the receipt of which is hereby acknowledged, Intellectual Ventures Assets 156 LLC, a Delaware limited liability company, with an address at 251 Little Falls Drive, Wilmington, DE 19808 ("***Assignor***"), does hereby sell, assign, transfer, and convey unto Innovative Silicon Solutions, LLC, a Texas limited liability company having an address at 5900 Balcones Drive, STE 100, Austin, TX 78731 ("***Assignee***"), all of Assignor's right, title, and interest in and to the following (collectively, the "***Assigned Patent Rights***"):

(a) the patents and patent applications listed in the table below (the "***Patents***");

Active Patent(s) – (Filed; Granted)

Patent/Application Number	Country	Issue Date/ Filing Date	Title of Patent and First Named Inventor
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7870404 (11/894991)	US	2011-01-11 (2007-08-21)	Transitioning To And From A Sleep State Of A Processor Andrew Read
9436264 (12/987423)	US	2016-09-06 (2011-01-10)	Saving Power When In Or Transitioning To A Static Mode Of A Processor Andrew Read
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7634701 (12/033864)	US	2009-12-15 (2008-02-19)	Method And System For Protecting Processors From Unauthorized Debug Access Morgan, Andrew
7810002 (12/544145)	US	2010-10-05 (2009-08-19)	Providing Trusted Access To A Jtag Scan Interface In A Microprocessor David Dunn
6774033 (10/287258)	US	2004-08-10 (2002-11-04)	Metal Stack For Local Interconnect Layer Ben-Tzur, Mira

(b) any future reissues, reexaminations, extensions, continuations, continuing prosecution application, requests for continuing examinations, divisions, and registrations of any of the Patents;

(c) rights to apply in any or all countries of the world for future patents, certificates of invention, utility models, industrial design protections, design patent protections, or other future governmental grants or issuances of any type related to the Patents; and

(d) causes of action and enforcement rights of any kind under, or on account of, any of the Patents and/or any of the items described in either of the foregoing categories (b) or (c), including, without limitation, all causes of action, enforcement rights and all other rights to seek and obtain any other remedies of any kind for past, current and future infringement.

Assignor hereby authorizes the respective patent office or governmental agency in each jurisdiction to issue any and all future patents, certificates of invention, utility models or other governmental grants or issuances that may be granted upon any of the Assigned Patent Rights in the name of Assignee, as the assignee to the entire interest therein. This Assignment of Patent Rights will inure for the benefit of any permitted successors or assigns of Assignee.

Assignor will, at the reasonable request of Assignee, take all reasonable steps necessary and proper, to confirm the assignment to Assignee of the Assigned Patent Rights pursuant to this Assignment of Patent Rights, including without limitation, the execution, acknowledgment, and recordation of specific assignments, oaths, declarations, and other documents on a country-by-country basis, to assist Assignee in obtaining and perfecting the Assigned Patent Rights.

IN WITNESS WHEREOF this Assignment of Patent Rights is executed on January 10, 2020 to be effective as of January 10, 2020.

ASSIGNOR:

INTELLECTUAL VENTURES ASSETS 156 LLC
By: _____
Name: Jim Weisfield
Title: Authorized Person

Exhibit B-2

ASSIGNMENT OF RIGHTS IN CERTAIN ASSETS

For good and valuable consideration, the receipt of which is hereby acknowledged, Intellectual Ventures Assets 156 LLC, a Delaware limited liability company, with an address at 251 Little Falls Drive, Wilmington, DE 19808 ("***Assignor***"), does hereby sell, assign, transfer, and convey unto Innovative Silicon Solutions, LLC, a Texas limited liability company having an address at 5900 Balcones Drive, STE 100, Austin, TX 78731 ("***Assignee***"), its right, title, and interest in and to any and all of the following provisional patent applications, patent applications, patents, and other governmental grants or issuances of any kind (the "***Certain Assets***"):

Inactive Patent(s) – (Abandoned; Lapsed; Expired)

Patent/Application Number	Country	Issue Date/ Filing Date	Title of Patent and First Named Inventor
(PCT/US2001/050801)	WO	(2001-10-18)	Method And Apparatus For Reducing Static Power Loss Andrew Read
(PCT/US2006/038168)	WO	(2006-09-28)	Securing Scan Test Architecture Morgan, Andrew

Assignor assigns to Assignee all of its rights to the inventions, invention disclosures, and discoveries in the assets listed above, together, with its rights, if any, to revive prosecution of claims under such assets and to sue or otherwise enforce any claims under such assets for past, present or future infringement.

Assignor hereby authorizes the respective patent office or governmental agency in each jurisdiction to make available to Assignee all records regarding the Certain Assets.

The terms and conditions of this Assignment of Rights in Certain Assets will inure to the benefit of Assignee, its successors, assigns, and other legal representatives and will be binding upon Assignor, its successors, assigns, and other legal representatives.

EXECUTED this 10th day of January 2020, to be effective as of January 10, 2020.

ASSIGNOR:

INTELLECTUAL VENTURES ASSETS 156 LLC
By: _____
Name: Jim Weisfield
Title: Authorized Person

PATENT ASSIGNMENT COVER SHEET

Electronic Version v1.1
Stylesheet Version v1.2

EPAS ID: PAT6398647

SUBMISSION TYPE:	NEW ASSIGNMENT
NATURE OF CONVEYANCE:	CHANGE OF NAME

CONVEYING PARTY DATA

Name	Execution Date
INNOVATIVE SILICON SOLUTIONS LLC	11/12/2020

RECEIVING PARTY DATA

Name:	HD SILICON SOLUTIONS LLC
Street Address:	5900 BALCONES DR STE 100
City:	AUSTIN
State/Country:	TEXAS
Postal Code:	78731

PROPERTY NUMBERS Total: 12

Property Type	Number
Patent Number:	7302619
Patent Number:	6774033
Patent Number:	7154299
Patent Number:	6748577
Patent Number:	7260731
Patent Number:	9436264
Patent Number:	9690366
Patent Number:	7870404
Patent Number:	7600166
Patent Number:	7810002
Patent Number:	7634701
Patent Number:	7334173

CORRESPONDENCE DATA

Fax Number:

Correspondence will be sent to the e-mail address first; if that is unsuccessful, it will be sent using a fax number, if provided; if that is unsuccessful, it will be sent via US Mail.

Phone: 9494390365
Email: fahim@hongdungroup.com
Correspondent Name: FAHIM AFTAB
Address Line 1: 5900 BALCONES DR STE 100
Address Line 4: AUSTIN, TEXAS 78731

NAME OF SUBMITTER:	FAHIM AFTAB
SIGNATURE:	/fa/
DATE SIGNED:	11/12/2020
	This document serves as an Oath/Declaration (37 CFR 1.63).
Total Attachments: 1 source=Certificate of Filing of HD Silicon#page1.tif	

Corporations Section
P.O.Box 13697
Austin, Texas 78711-3697

Ruth R. Hughs
Secretary of State

Office of the Secretary of State

CERTIFICATE OF FILING
OF

HD Silicon Solutions LLC
803500718

[formerly: Innovative Silicon Solutions, LLC]

The undersigned, as Secretary of State of Texas, hereby certifies that a Certificate of Amendment for the above named entity has been received in this office and has been found to conform to the applicable provisions of law.

ACCORDINGLY, the undersigned, as Secretary of State, and by virtue of the authority vested in the secretary by law, hereby issues this certificate evidencing filing effective on the date shown below.

Dated: 11/10/2020

Effective: 11/10/2020

Ruth R. Hughs
Secretary of State