Declaration of Donald Alpert, Ph.D. in Support of
Petition for *Inter Partes* Review of
U.S. Patent No. 7,260,731

UNITED STATES PATENT AND TRADEMARK OFFICE

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BEFORE THE PATENT TRIAL AND APPEAL BOARD

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MICROCHIP TECHNOLOGY INC.,
Petitioner,

v.

HD SILICON SOLUTIONS LLC
Patent Owner

_____

Case No. IPR2021-01420
Case No. IPR2021-01421
U.S. Patent No. 7,260,731
Issue Date: August 21, 2007

Title: SAVING POWER WHEN IN OR TRANSITIONING TO
A STATIC MODE OF A PROCESSOR

**DECLARATION OF DONALD ALPERT, PH.D. IN SUPPORT OF
PETITION FOR *INTER PARTES* REVIEW OF U.S. PATENT NO. 7,260,731**

Mail Stop PATENT BOARD
Patent Trial and Appeal Board
United States Patent and Trademark Office
P.O. Box 1450
Alexandria, VA 22313-1450

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I, Donald Alpert, Ph.D., declare as follows:

## I. INTRODUCTION AND QUALIFICATIONS

### A. Introduction

1. I am an independent consultant with Camelback Computer Architecture, LLC. My residence and place of business is at 2020 21st Street, Sacramento, CA 95818. I am over the age of eighteen, and I am a citizen of the United States.

2. I have been retained by Microchip Technology, Inc. ("Microchip" or "Petitioner") as a technical expert witness in connection with the petition for *inter partes* review of U.S. Patent No. 7,260,731 ("'731 patent") ("Ex.1001.") I understand that the '731 patent claims priority to October 23, 2000. For purposes of my analysis herein, I have used this date as the relevant time period.

3. I have been asked by Petitioner to offer opinions regarding the '731 patent, including the interpretation of certain claim terms and the patentability of the claims in view of certain prior art references and the knowledge of a person of ordinary skill in the art ("POSITA"). This declaration sets forth the opinions I have reached to date regarding these matters.

4. In preparing this Declaration, I have reviewed the '731 patent, its prosecution history, and each of the documents I reference herein. In reaching my

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opinions, I have relied upon my experience in the field and have also considered

the viewpoint of a POSITA at the time of the '731 patent's priority date. As

explained below, I am familiar with the level of skill of a POSITA regarding the

technology at issue as of that time frame.

5.      Camelback Computer Architecture is being compensated for my time

working on this matter at my standard hourly rate of $600 per hour, plus expenses.

Neither Camelback Computer Architecture nor I have any personal or financial

stake or interest in the outcome of the present proceeding, and the compensation is

not dependent on the outcome of this IPR and in no way affects the substance of

my statements in this declaration.

## B.      Qualifications and Experience

6.      My qualifications for forming the opinions set forth in this

Declaration are summarized here and explained in more detail in my curriculum

vitae, which is attached as Exhibit 1003.

7.      I have 45 years of academic and industrial experience in applying,

designing, studying, teaching, and writing about microprocessors and computer

systems. I received an Electrical Engineering Ph.D. degree in 1984 from Stanford

University. I earlier received an Electrical Engineering B.S. degree from MIT in

1973 and an Electrical Engineering M.S. degree from Stanford University in 1978.

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I have taught classes in computer architecture at Stanford, Tel Aviv, and Arizona State Universities.

8.     From 1976 to 1977, I worked at Burroughs Corporation, where I designed peripheral interface controllers, including those for serial data communications based on Intel 8080 microprocessor components.  From 1980 to 1989, I was the lead architect for the design of three high-performance microprocessors at Zilog and National Semiconductor. Later, at Intel, I was the lead architect of the Pentium® Processor from 1989 to 1992 and of the 815 chipset from 1999 to 2000, both of which became the most widely used PC components of their time.  The 815 chipset comprised two components: (1) a memory controller hub (MCH) that included a graphics controller and memory controller with interfaces to the CPU, 133 MHz SDRAM system memory modules, an optional, external graphics controller and (2) an I/O controller hub (ICH) that included various I/O controllers (*e.g.*, network, hard drive, USB) for system peripheral devices and power management control registers. Additionally, I served as co-manager for the Itanium processor design from 1993-1997.

9.     I am a Senior Member of the Institute of Electrical and Electronics Engineers (IEEE), and served as the chair of the IEEE Technical Committee on Microprocessors and Microcomputers from 1999 to 2000.  I was the keynote

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speaker at the first Cool Chips conference, dedicated to the study of low-power microprocessors and systems. I have given invited lectures at several universities, and published ten papers in various professional journals and conference proceedings. My paper entitled "Architecture of the Pentium Processor," was selected as best paper in IEEE Micro for 1993. I am a named inventor on over 30 U.S. patents that pertain to microprocessors, computer systems, and related technology.

10. I have reviewed the '731 Patent, and I am familiar with the patent's subject matter, which is within the scope of my education and professional experience. Based at least on my background in academia, industry, and consulting, I am familiar with the issues and technology relating to processors, chipsets, memory, peripheral devices, and power management for computer systems. I have personally analyzed, developed, and tested such computer components and systems. More specifically, the Pentium® Processor and 815 chipset for which I was the lead architect at Intel implemented various features for supporting power management, including those related to Advanced Power Management (APM) and Advanced Configuration and Power Interface Specification (ACPI) industry standards.

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### C.      Materials Considered

11.      The analysis that I provide in this Declaration is based on my

education and experience in the field of computer systems, as well as the

documents I have considered, including the '731 patent (Ex.1001) and its

prosecution history (Ex.1004).  The '731 patent states on its face that it issued from

Application No. 09/694,433, filed on October 23, 2000.  For the purposes of this

Declaration, I have been instructed to assume October 23, 2000 as the effective

filing date for the '731 patent.  I have cited to the following documents in my

analysis below:

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## LIST OF EXHIBITS

| EXHIBIT NO. | DESCRIPTION |
|---|---|
| 1001 | U.S. Patent No. 7,260,731 issued to Andrew Read, et al., (filed Oct. 23, 2000, issued Aug. 21, 2007) |
| 1003 | Curriculum Vitae of Donald Alpert, Ph.D. |
| 1004 | Prosecution History for U.S. Patent Application No. 09/694,433, which issued as U.S. Patent No. 7,260,731 |
| 1005 | Excerpts from *Single-Chip Microcomputer Databook,* NEC Electronics Inc. (May 1990) |
| 1006 | Thomas Burd et al., "A Dynamic Voltage Scaled Microprocessor System," in Digest of Technical Papers, 2000 IEEE Int. Solid-State Circuits Conf. (Feb. 2000) ("Burd") |
| 1007 | U.S. Patent No. 5,955,871 to Nguyen ("Nguyen") |
| 1008 | TPS5210 Programmable Synchronous-Buck Regulator Controller (as evidenced by Texas Instruments, Inc., "TPS5210 Programmable Synchronous-Buck Regulator Controller," (May 1999) ("TI-TPS5210-Datasheet")) |
| 1009 | U.S. Patent No. 5,919,262 to Kikinis et al. ("Kikinis") |
| 1010 | U.S. Patent No. 6,748,545 to Helms et al. ("Helms") |
| 1011 | Maxim MAX1652–MAX1655 High-Efficiency, PWM, Step-Down DC-DC Controllers (as evidenced by Maxim |

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| 1001 | U.S. Patent No. 7,260,731 issued to Andrew Read, et al., (filed Oct. 23, 2000, issued Aug. 21, 2007) |
| 1003 | Curriculum Vitae of Donald Alpert, Ph.D. |
| 1004 | Prosecution History for U.S. Patent Application No. 09/694,433, which issued as U.S. Patent No. 7,260,731 |
| 1005 | Excerpts from *Single-Chip Microcomputer Databook,* NEC Electronics Inc. (May 1990) |
| 1006 | Thomas Burd et al., "A Dynamic Voltage Scaled Microprocessor System," in Digest of Technical Papers, 2000 IEEE Int. Solid-State Circuits Conf. (Feb. 2000) ("Burd") |
| 1007 | U.S. Patent No. 5,955,871 to Nguyen ("Nguyen") |
| 1008 | TPS5210 Programmable Synchronous-Buck Regulator Controller (as evidenced by Texas Instruments, Inc., "TPS5210 Programmable Synchronous-Buck Regulator Controller," (May 1999) ("TI-TPS5210-Datasheet")) |
| 1009 | U.S. Patent No. 5,919,262 to Kikinis et al. ("Kikinis") |
| 1010 | U.S. Patent No. 6,748,545 to Helms et al. ("Helms") |
| 1011 | Maxim MAX1652–MAX1655 High-Efficiency, PWM, Step-Down DC-DC Controllers (as evidenced by Maxim |

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| EXHIBIT NO. | DESCRIPTION |
|---|---|
| | Integrated Inc., "High-Efficiency, PWM, Step-Down DC-DC Controllers in 16-Pin QSOP, MAX1652–MAX1655," Rev. 1 (July 1998) ("Maxim-165X-Datasheet")) |
| 1012 | Maxim Integrated, Inc., "MAX1711 Voltage Positioning Evaluation Kit," Rev. 1 (June 2000) ("MAX1711-Kit")) |
| 1013 | James W. Nilsson, "Electronic Circuits," (Addison Wesley, 4th ed.) (1993) ("Nilsson") |
| 1014 | *Not Used* |
| 1015 | U.S. Patent No. 3,941,989 |
| 1016 | U.S. Patent No. 4,293,927 |
| 1017 | CMOS, the Ideal Logic Family |
| 1018 | Inki Hong, *et al.*, "Synthesis Techniques for Low-Power Hard Real-Time Systems on Variable Voltage Processors," in Proceedings of the 19th IEEE Real-Time Systems Symposium (Dec. 1998) |
| 1019 | U.S. Patent No. 5,021,679 |
| 1020 | "Terms, Definitions, and Letter Symbols for Microcomputers, Microprocessors, and Memory Integrated Circuits," JEDEC Standard JESD-100A (Aug. 1993) |
| 1021 | U.S. Patent No. 5,898,235 |
| 1022 | U.S. Patent No. 6,347,379 |

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| EXHIBIT NO. | DESCRIPTION |
|---|---|
| 1023 | L. L. Vadasz, *et al.*, "Silicon-Gate Technology," IEEE Spectrum, vol. 6 no. 10 at 35 (October 1969) |
| 1024 | *Not Used* |
| 1025 | *Not Used* |
| 1026 | U.S. Patent No. 5,677,558 |
| 1027 | Bang S. Lee, *"Technical Review of Low Dropout Voltage Regulator Operation and Performance,"* Texas Instruments Application Report SLVA072 (Aug. 1999) |
| 1028 | Bob Wolbert, "Micrel's Guide to Designing With Low-Dropout Voltage Regulators," (Dec. 1998) |
| 1029 | Jim Williams, "Step-Down Switching Regulators," Linear Technology Application Note 35 (Aug. 1989) |
| 1030 | U.S. Patent No. 5,731,731 |
| 1031 | *Not Used* |
| 1032 | Mobile Power Guidelines '99, Rev. 1.00, Intel Corporation (December 1, 1997 |
| 1033 | U.S. Patent No. 6,212,094 |
| 1034 | U.S. Patent No. 5,568,044 to Bittner ("Bittner") |
| 1035 | Maxim Integrated, Inc., "High-Speed, Digitally Adjusted Step-Down Controllers for Notebook CPUs, |

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| EXHIBIT NO. | DESCRIPTION |
|---|---|
| | MAX1710/MAX1711," Rev. 0 (Nov. 1998) ("MAX171X-1998-Datasheet") |
| 1036 | Advanced Micro Devices, Inc., "AMD Athlon Processor Datasheet," Rev. G (1999) ("Athlon-99-Datasheet") |
| 1037 | Advanced Micro Devices, Inc., "AMD Athlon Processor Module Datasheet, Rev. M (June 2000) ("Athlon-00-Datasheet") |
| 1038 | Advanced Micro Devices, Inc., "AMD 756 Peripheral Bus Control Datasheet," Rev. B (August 1999) ("AMD-756-Datasheet") |
| 1039 | Advanced Configuration and Power Interface Specification, Rev. 1.0 (Dec. 22, 1996) (the "ACPI standard" or the "ACPI") |
| 1040 | Bang Sup Lee, "Extended output voltage adjustment (0 V to 3.5 V) using the TI TPS5210 (SLYT195)," Analog Applications (Aug. 1999) |
| 1041 | U.S. Patent No. 5,457,421 to Tanabe ("Tanabe") |
| 1042 | High Speed Synchronous Power MOSFET Smart Driver SC1405 ("SC1405") |
| 1043 | U.S. Patent No. 5,565,761 to Hwang |
| 1044 | U.S. Patent No. 5,627,460 to Bazinet *et al.* |

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| EXHIBIT NO. | DESCRIPTION |
|---|---|
| 1045 | Maxim Integrated, Inc., "High-Speed, Digitally Adjusted Step-Down Controllers for Notebook CPUs, MAX1710/MAX1711," Rev. 1 (Jul. 2000) ("MAX171X-2000-Datasheet") |

## II. LEGAL PRINCIPLES

12. I am not an attorney. For purposes of this declaration, I have been informed about certain aspects of the law that are relevant to my analysis and opinions, as set forth below.

### A. Prior Art

13. I understand that the prior art to the '731 patent includes patents and printed publications in the relevant art that predate the '731 patent's priority date. As I explained previously, I have been instructed to assume for purposes of my analysis that October 23, 2000 is the relevant date for determining what is "prior art." In other words, I should consider as "prior art" anything publicly available prior to October 23, 2000. I further understand that, for purposes of this proceeding in the United States Patent Trial and Appeal Board, only patents and documents that have the legal status of a "printed publication" may be relied on as prior art.

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## B.    Claim Construction

14.    I understand that under the legal principles, claim terms are generally given their ordinary and customary meaning, which is the meaning that the term in question would have to a POSITA at the time of the invention, *i.e.*, as of the effective filing date of the patent application.  I further understand that a POSITA is deemed to read the claim term not only in the context of the particular claim in which a claim term appears, but in the context of the entire patent, including the specification.

15.    I am informed by counsel that the patent specification, under the legal principles, has been described as the single best guide to the meaning of a claim term, and is thus highly relevant to the interpretation of claim terms.  I understand for terms that do not have a customary meaning within the art, the specification usually supplies the best context of understanding the meaning of those terms.

16.    I am further informed by counsel that other claims of the patent in question, both asserted and unasserted, can be valuable sources of information as to the meaning of a claim term.  Because the claim terms are normally used consistently throughout the patent, the usage of a term in one claim can often illuminate the meaning of the same term in other claims.  Differences among claims can also be a useful guide in understanding the meaning of particular claim

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terms.

17.     I understand that the prosecution history can further inform the meaning of the claim language by demonstrating how the inventors understood the invention and whether the inventors limited the invention in the course of prosecution, making the claim scope narrower than it otherwise would be. Extrinsic evidence may also be consulted in construing the claim terms, such as my expert testimony.

18.     I have been informed by counsel that, in IPR proceedings, a claim of a patent shall be construed using the same claim construction standard that would be used to construe the claim in a civil action filed in a U.S. district court (which I understand is called the "*Phillips*" claim construction standard), including construing the claim in accordance with the ordinary and customary meaning of such claim as understood by one of ordinary skill in the art and the prosecution history pertaining to the patent.

19.     I have been instructed by counsel to apply the "*Phillips*" claim construction standard for purposes of interpreting the claims in this proceeding, to the extent they require an explicit construction. The description of the legal principles set forth above thus provides my understanding of the "*Phillips*" standard as provided to me by counsel.

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20.    I understand that some claims are independent, and that these claims
are complete by themselves.  Other claims refer to these independent claims and
are "dependent" from those independent claims.  The dependent claims include all
the limitations of the claims on which they depend.

21.    I am further informed and understand that certain claim elements
recite "*means for*" or "*means to*," and may therefore be understood as reciting
means-plus-function limitations.  I am also informed and understand that,
accordingly, the analysis of each of these claim elements may require the
identification of a respective function recited in each of these claim elements, and
the identification of a respective structure that is disclosed in the specification or
file history of the '731 patent, where the respective identified structure is linked to
and performs the respective recited function.

22.    I am additionally informed and understand that to show that the prior
art teaches any particular one of these claim elements, the prior art should disclose
a structure that performs the function recited in the particular claim element, where
the structure disclosed in the prior art is the same as or equivalent to the structure
disclosed in the '731 patent that performs the recited function.

23.    I am also informed and understand that the determination of
equivalence under 35 U.S.C. §112 does not involve the function-way-result test

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that is generally applied under the doctrine of equivalents in determining infringement of a claim. Rather, I am informed and understand, that equivalence is determined by comparing the prior art structure that performs the claimed function with the structure disclosed in the specification.

## C. Anticipation

24. I understand that to anticipate a patent claim under 35 U.S.C. § 102, a single asserted prior art reference must disclose each and every element of the claimed invention, either explicitly, implicitly, or inherently, to a POSITA. There must be no difference between the claimed invention and the disclosure of the alleged prior art reference as viewed from the perspective of a POSITA. Also, I understand that in order for a reference to be an anticipating reference, it must describe the claimed subject matter with sufficient clarity to establish that the subject matter existed and that its existence was recognized by persons of ordinary skill in the field of the invention. In addition, I understand that in order to establish that an element of a claim is "inherent" in the disclosure of an asserted prior art reference, extrinsic evidence (or the evidence outside the four corners of the asserted prior art reference) must make clear that the missing element is necessarily found in the prior art, and that it would be recognized as necessarily present by persons of ordinary skill in the relevant field.

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25. In my opinions below, when I say that a POSITA would have understood, readily understood, or recognized that an element or aspect of a claim is disclosed by a reference, I mean that the element or aspect of the claim is disclosed to a POSITA.

### D. Obviousness

26. I understand that obviousness is a determination of law based on various underlying determinations of fact. In particular, these underlying factual determinations include (1) the scope and content of the prior art; (2) the level of ordinary skill in the art at the time the claimed invention was made; (3) the differences between the claimed invention and the prior art; and (4) the extent of any proffered objective indicia of nonobviousness. I understand that the objective indicia which may be considered in such an analysis include commercial success of the patented invention (including evidence of industry recognition or awards), whether the invention fills a long-felt but unsolved need in the field, the failure of others to arrive at the invention, industry acquiescence and recognition, initial skepticism of others in the field, whether the inventors proceeded in a direction contrary to the accepted wisdom of those of ordinary skill in the art, and the taking of licenses under the patent by others, among other factors.

27. To ascertain the scope and content of the prior art, it is necessary to

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first examine the field of the inventor's endeavor and the particular problem for which the invention was made. The relevant prior art includes prior art in the field of the invention, and also prior art from other fields that a POSITA would look to when attempting to solve the problem.

28.     I understand that a determination of obviousness cannot be based on the hindsight combination of components selectively culled from the prior art to fit the parameters of the patented invention. Instead, it is my understanding that in order to render a patent claim invalid as being obvious from a combination of references, there must be some evidence within the prior art as a whole to suggest the desirability, and thus the obviousness, of making the combination in a way that would produce the patented invention.

29.     I further understand that in an obviousness analysis, neither the motivation nor the purpose of the patentee dictates. What is important is whether there existed at the time of the invention a known problem for which there was an obvious solution encompassed by the patent's claims.

30.     I also understand that the combination of familiar elements according to known methods is likely to be obvious when it yields predictable results. I also understand that an example of a solution in one field of endeavor may make that solution obvious in another related field, as well. I am informed that market

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demands or design considerations may prompt variations of a prior art system or

process, in the same field or a different one, where such variations may ordinarily

be considered obvious, straightforward changes to what has been explicitly

disclosed in the prior art.

31.     I also understand that if a POSITA could have implemented a

predictable variation without excessive experimentation, that variation would have

been considered obvious.  I understand that for similar reasons, if a technique has

been used to improve one device or processor, and a POSITA would have

recognized that that technique can improve a similar devices or process in the same

way, implementing such an improvement would have been obvious, unless the

implementation yields unexpected results or challenges in implementation.

32.     I understand that the obviousness analysis need not seek out precise

teachings directed to the specific subject matter of the challenged claim.  Rather, I

understand, that the analysis can take into account ordinary innovation and

experimentation, *e.g.*, inferences and creative steps that a POSITA would employ,

that yields predictable, benefits.  In this regard, I understand that a POSITA is also

a person of ordinary creativity.

33.     I understand that sometimes it will be necessary to consider

interrelated teachings of several prior art references, the demands or current

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problems known in the design community or present in the marketplace, and/or the

background knowledge of a POSITA. I understand that any of these factors may

be considered to assess whether there was a reason to combine the teachings of the

prior art references, where the combination would reveal the system or process

claimed in the challenged patent.

34. I understand that the obviousness analysis is not limited to a

formalistic conception of "teaching, suggestion, and motivation." I understand that

in 2007, the Supreme Court issued its decision in *KSR Int'l Co. v. Teleflex Inc.,*

550 U.S. 398, 418 (2007), where the Court rejected the previous requirement of a

"teaching, suggestion, or motivation to combine" known elements of prior art as a

precondition for concluding that a combination of those elements would be

obvious. It is my understanding that *KSR* confirms that any rational reason or

motivation that would have been known to a POSITA, including common sense,

one derived from the nature of the problem to be solved, *etc*., can be sufficient to

explain why such known prior art elements from one or more prior art references

would have been combined.

35. I understand that a POSITA attempting to solve a particular problem

will not be led only to those elements that the prior art explicitly discloses and/or

are described as a solution to that particular problem. Rather, I understand that

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under the *KSR* standard, steps suggested by common sense are important and should be considered. Common sense informs that disclosed elements or solutions may have obvious uses beyond the particular problem or application described in a reference. Common sense also suggests that if something can be done once it may be obvious to repeat it multiple times.

36.     I understand that in many cases a POSITA will be able to fit the teachings of several prior art references together, like pieces of a puzzle. As such, any need or problem known in the same or related fields that the prior art considered can provide a reason for combining the teachings of the prior art with those of another prior art. In other words, the prior art references need not be directed towards solving the particular problem addressed in the challenged patent. I also understand that the individual prior art references themselves need not all be directed towards solving a single problem.

37.     I understand that obviousness does not require that the elements not explicitly disclosed in one prior art reference (sometimes referred to as a primary reference) but disclosed in another prior art reference (sometimes referred to as a secondary reference) need not be shown to be bodily or actually incorporated into the structure of the primary reference. Rather, the test is what the combined teachings of those references would have informed a POSITA. Thus, I understand

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that the disclosures of the prior art references need not be physically combinable,

and that combining the teachings of references should be the focus of the analysis.

38.     I understand that an invention that might otherwise be considered an

obvious variation or modification of the prior art may nevertheless be considered

unobvious if any of the prior art references discourages or leads away from such a

modification.  I further understand, however, that a reference does not "teach

away" from a feature or its modification simply because the reference suggests that

an alternative, such as another embodiment of an invention disclosed in a prior art

patent, is better or preferred.  I understand that the doctrine of teaching away

requires a clear indication that the combination would not work or explicit

disclosure that the combination would be undesirable.

39.     I further understand that in many fields, especially in complex, well

evolved technologies, often there is little explicit discussion of obvious techniques,

variations, or combinations.  In some cases, market demands, rather than scientific

inquiry, drive design trends.  There may be a design need or market pressure to

solve a particular problem, and only a finite number of solutions may be known,

neither of which may be the most suited or optimized to meet the design need or to

solve the particular problem.

40.     I understand that in such cases, a POSITA has good reason to pursue

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the known solutions that are the available options within the POSITA's technical grasp. Should this lead to an anticipated success or a predictable beneficial result, it is likely the product not of innovation but of ordinary skill and common sense. In that instance, the combination and/or modification of the prior art technique(s) may be obvious because it was obvious to try.

41.     Thus I understand, that the fact that a particular combination of prior art elements was "obvious to try," regardless of whether it was actually tried, may indicate that the combination of references disclosing those elements was also obvious, even if no one previously attempted the combination.

### III.     LEVEL OF ORDINARY SKILL IN THE ART

42.     I understand that an assessment of claims of the '731 patent should be undertaken from the perspective of a POSITA as of the earliest claimed priority date, which I understand is October 23, 2000. I have also been advised that to determine the appropriate level of a person having ordinary skill in the art, the following factors may be considered: (1) the types of problems encountered by those working in the field and prior art solutions thereto; (2) the sophistication of the technology in question, and the rapidity with which innovations occur in the field; (3) the educational level of active workers in the field; and (4) the educational level of the inventor.

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43.     In my opinion, a POSITA at the time of the alleged invention of the

'731 patent would have possessed at least a bachelor's degree in electrical

engineering, computer engineering, or computer science, with at least two years of

experience in computer system development, including experience in developing

power/voltage regulation systems for portable devices.  A person could also have

qualified as a POSITA with some combination of (1) more formal education (such

as a master's of science degree) and less technical experience or (2) less formal

education and more technical or professional experience in the fields listed above.

44.     My opinions regarding the level of ordinary skill in the art are based

on, among other things, my more than 40 years of experience in electrical and

computer engineering, my understanding of the basic qualifications that would be

relevant to an engineer or scientist tasked with investigating methods and systems

in the relevant area, and my familiarity with the backgrounds of students,

colleagues, co-workers, and employees, both past and present.  Although my

qualifications and experience exceed those of the hypothetical person having

ordinary skill in the art defined above, my analysis and opinions regarding the '731

patent have been based on the perspective of a POSITA as of October 23, 2000.

## IV.     TECHNOLOGY BACKGROUND

45.     This section provides general technical background for computer

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systems, physical principles of power consumption, and methods for reducing

power and energy consumption by computer systems while maintaining

requirements for performance and responsiveness. Managing the power of

computer systems involves technologies related to microelectronics, logic and

memory circuits, power supplies, and operating systems.

46.     A computer system's hardware generally comprises three types of

components, as described below and shown in the demonstrative figure:

**Processors**: A processor is a device that fetches and executes the

instructions of a program.

**Memory**: Memory stores instructions executed by a processor and data

manipulated by a processor

**Input/Output (I/O) Devices**: I/O devices provide auxiliary storage,

communication between systems, and human interface.

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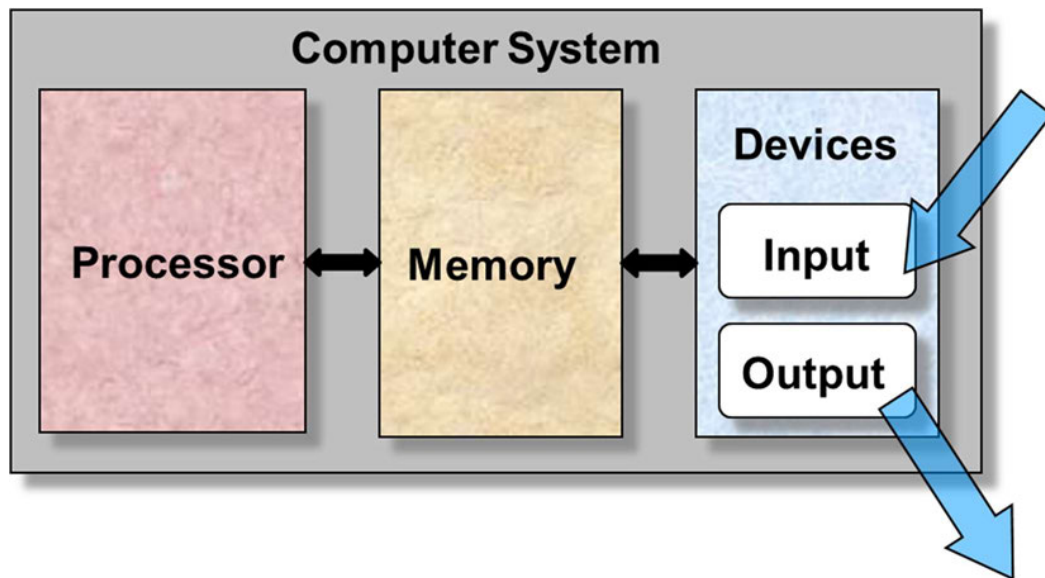


## A.    Power and Energy Consumption of Computer Systems

### 1.    CMOS and Power

47.    For more than 35 years, silicon CMOS (Complementary Metal-Oxide

Semiconductor) has been the most widely used technology for microelectronic

devices.  CMOS technology uses two types of transistors, "complementary" n-type

and p-type, to fabricate logic and memory circuits.  The complementary nature of

these transistors means that under conditions where one type of transistor switches

on, the other type switches off.  Thus, devices fabricated in CMOS have commonly

been designed to operate statically; that is, when the inputs to the device are stable,

no transistors are switching and the device consumes no "dynamic" power.  In

contrast, when inputs to the device are changing, transistors switch as a result, and

the device consumes dynamic power.

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48.     CMOS technology has continually improved during this period from a feature size of about 1.5 μm in 1985 to 5 nm in 2020, thus reducing linear feature size by a factor of about 300 over 35 years.  This reduction in size results in microelectronic structures that are generally much smaller, much faster, and require much less power.  However, "leakage" current (e.g., a small current that leaks through the channel of a transistor when the transistor is turned off) has become an increasingly important factor as semiconductor feature size has decreased.  As a result of leakage current, a device consumes power even when it is not performing useful work.

49.     Combining the dynamic and leakage types of power above, the power consumed by a CMOS device can be represented by the relationship reproduced below:

$$\text{Power} \propto (\text{Capacitance} * \text{Frequency} * (\text{Voltage})^2) + (\text{Voltage} * (\text{DC Current} + \text{Leakage Current}))$$

(Ex.1032, Mobile Power Guidelines '99, Rev. 1.00, Intel Corporation, at 9 (December 1, 1997).)  In this equation, the symbol "∝" means "proportional to." "Capacitance" is related to the "active area" of the device, which represents the total amount of circuitry.  The term "DC Current" generally relates to analog circuits that draw current even when they are not active, such as sense amplifiers.

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50. Thus, for an electronic device produced in CMOS technology, power consumption can be reduced by (i) slowing or stopping the clock or (ii) lowering or turning off the voltage supplied.

### 2. Slowing the Clock

51. One technique for reducing power consumed by a computer system is to reduce its clock frequency. For example, in 1974, it was known that one could reduce power consumption of a battery-powered, handheld calculator by slowing the calculator's clock frequency, as disclosed in U.S. Patent No. 3,941,989:

> An object of the invention is to reduce the power consumption of calculators, and particularly of hand-held calculators which are battery powered, by supplying to the calculator only as much power as actually needed for each different mode of operation and by clocking the calculator at a rate which is only as high as actually needed for each different mode of operation.

(Ex.1015, U.S. Patent No. 3,941,989, 1:45-52.)

52. In such a system, the dynamic power is reduced in direct proportion to the reduction in frequency. Although power (energy/time) is reduced, the computer's performance is also reduced proportionally with frequency. Therefore, the system requires proportionally longer time to complete its computation, and the energy consumption remains unchanged.

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### 3. Stopping the Clock

53. Another technique used in the 1970's to reduce power consumption of battery-powered, handheld calculators was to stop the clock when no calculation was occurring, such as after a period of time during which the user did not press any keys. Reducing the clock frequency to 0, *i.e.*, stopping the clock, eliminates all dynamic power. During this idle time, data can be retained, allowing calculation to resume when the user next presses a key. For example, U.S. Patent No. 4,293,927 discloses:

> With such a construction, when no keying in operation is performed for a given period of time while the power source is turned on, the oscillation of the oscillating circuit is stopped to stop generation of the clock signal and to thereby stop all the circuit operations. However, the operation results in the memory continue to be held or stored. Therefore, the wasteful power consumption when an operator fails to turn off the power source switch may be prevented. Additionally, the data obtained before the oscillation of the oscillating circuit stops is held and therefore the data is held even in the course of the operation execution. Accordingly, there is no need to reenter the identical data at the restart of the operation, thereby to allow the calculator to smoothly enter the execution of the operation. In this respect, the key in operation is remarkably improved.

(Ex.1016, U.S. Patent No. 4,293,927, 2:53-68.)

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54.     A processor that is idle with its clock stopped is said to be in sleep (or

deep sleep or deeper sleep), doze, or nap state.  Alternatively, other terms are used,

such as halt, stop, or standby state.  The transition from such an idle state to an

active state is said to be waking, resuming, or releasing.

### 4.      Dynamic Voltage-Frequency Scaling (DVFS)

55.     Another characteristic of CMOS technology is that the maximum

frequency at which a circuit can operate varies directly with the voltage.  That is,

operating the circuit at higher frequency requires higher voltage than operating the

circuit at lower frequency.  Thus, when the operating frequency is reduced, the

voltage can also be reduced, effectively reducing dynamic power consumption

linearly with frequency and quadratically with voltage.  Hence, the energy

consumed to perform a computation is also reduced.

56.     It was therefore understood that a system's power consumption and

energy could be minimized by operating the system at the minimum frequency

required to perform its function, and by setting the power supply voltage to the

minimum required for that frequency.  For example, CMOS, the Ideal Logic

Family states:

> So, we can see that for a given design, and therefore fixed capacitive
> load[,] increasing the power supply voltage will increase the speed of
> the system. Increasing $V_{CC}$ increases speed but it also increases power

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dissipation. This is true for two reasons. First, $CV^2f$ power increases.
This is the power dissipated in a CMOS circuit, or any other circuit
for that matter, when driving a capacitive load.

(Ex.1017, CMOS, the Ideal Logic Family at 2.)

57.     CMOS, the Ideal Logic Family also states:

**Minimizing system power dissipation**: To minimize power
consumption in a given system, it should be run at the minimum speed
to do the job with the lowest possible power supply voltage. AC and
DC transient power consumption both increase with frequency and
power supply voltage. The AC power is described as $CV^2f$ power.
This is the power dissipated in a driver driving a capacitive load.
Obviously, AC power consumption increases directly with frequency
and as the square of the power supply.

(*Id.* at 5.)

58.     Consequently, by 2000 it was known that a computer processor could
be designed to control power consumption by dynamically varying its voltage and
frequency, a technique known **as dynamic voltage-frequency scaling (DVFS)**.
Operating a processor in this manner requires a power supply that varies voltage.
For example, Hong states:

The problem outlined above really arises because conventional
systems are designed with a fixed supply voltage. However, there is
no fundamental reason that the supply voltage has to be fixed. Instead,

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it can in principle be varied dynamically at run time. Indeed, advances

in power supply technology makes it possible to vary the generated

supply voltage dynamically under external control. While many

CMOS circuits have always been capable of operating over a range of

supply voltages, it is the recent progress in power supply circuits that

has made feasible systems with dynamically variable supply voltages.

Since both the power consumed and the speed (maximal clock

frequency) are a function of the supply voltage, such *variable voltage*

systems can be made to operate at different points along their power

*vs.* speed curves in a controlled fashion.

(Ex.1018, Inki Hong, *et al*., "Synthesis Techniques for Low-Power Hard Real-

Time Systems on Variable Voltage Processors," in Proceedings of the 19th IEEE

Real-Time Systems Symposium at 1 (Dec. 1998) (citations omitted) (emphasis in

original).)

59.     For example, a handheld, battery-powered personal computer

developed by Poqet Computer Corporation during the late-1980s included a

processor that operated in a high-performance mode at 5 V and 6.6 MHz or in a

low-power mode at 3 V and 2.3 MHz.  The high-performance mode could be used

for numerical data computation, and the low-power mode could be used for word

processing applications.  Additionally, the clock frequency and supply voltage

could be further reduced below that required to operate the processor while the

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processor's data is retained. (*See, e.g.*, Ex.1019, U.S. Patent No. 5,021,679, 1:8-3:57.)

## B. Registers and Static Random Access Memory (SRAM)

60. The technique described above of stopping the clock will eliminate dynamic power, but leakage power remains because the device continues to be connected to the voltage of the power supply. A processor's power consumption due to leakage can be completely eliminated by shutting off its supply voltage. Nevertheless, when the supply voltage is removed, the state required for the processor to execute instructions, such as data stored in registers and integrated memory, is lost. Hence, the time and energy consumed by the processor to save is state when turning off its supply voltage and then restoring its state when resuming its supply voltage can result in poor performance and wasted energy. Consequently, it is beneficial for many computer applications that the processor retains its state while the clock is stopped so that computation can be resumed quickly and efficiently.

61. Within a processor, data can be stored by a register or memory when the clock is stopped by using a circuit with two cross-coupled inverters. Feedback through the coupling provides for two stable states with one inverter having its output low while the other inverter has its output high, thereby allowing one bit of

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information to be stored. For example, FIG. 1 from U.S. Patent No. 6,212,094 to

Rimondi, issued on April 3, 2001 and filed on November 25, 2998 (Ex.1033),

annotated and reproduced below shows a circuit for such a bit-cell, where one

inverter (output $\overline{Q}$) comprises nMOS transistor $M_1$ and pMOS transistor $M_2$, and

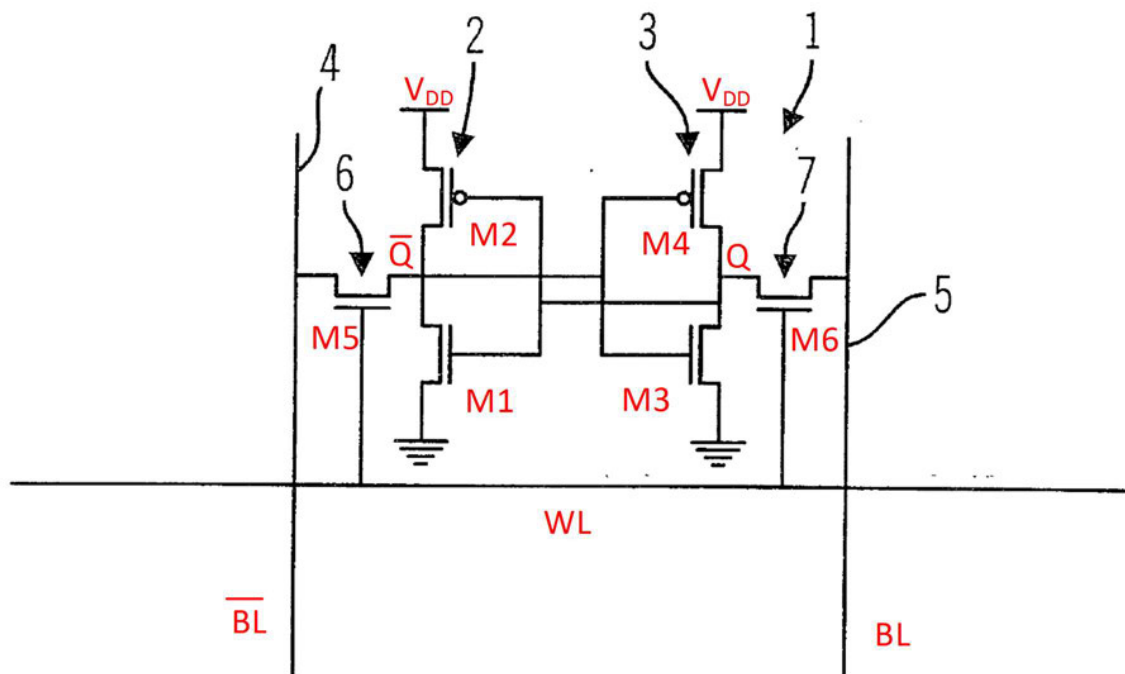the other inverter (output $Q$) comprises $M_3$ and $M_4$.



FIG. 1
PRIOR ART

(Ex.1033, FIG. 1 (annotated).)

62.    A stored bit is accessed by driving the wordline (WL) signal High,

which switches on nMOS transistors $M_5$ and $M_6$.  For read access, the true and

complement bitlines (*BL* and $\overline{BL}$) are precharged High, then WL is driven High,

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and depending on the state of the bit, either $BL$ or $\overline{BL}$ is pulled Low by $M_3$ or $M_1$.

For write access, the bitlines (BL and $\overline{BL}$) are strongly driven to the written value

and its complement, then WL is driven High, and the stored bit ($Q$ and $\overline{Q}$) is driven

to the written value.

63.     During periods when the data is not being accessed, a condition

known as *standby*, the data can be retained indefinitely.  Furthermore, it was

known before 2000 that the data could be retained even when the supply voltage

was lowered to a value below that required to access the data.  Industry standards

refer to this usage as **data-retention mode**.

> **data retention mode**
>
> A standby or battery mode of operation in which the integrity of
> stored data is maintained although the supply voltage is below that
> specified for reading or writing.

(Ex.1020, "Terms, Definitions, and Letter Symbols for Microcomputers,

Microprocessors, and Memory Integrated Circuits," JEDEC Standard JESD-100A,

at 4 (Aug. 1993.)

64.     Lowering the supply voltage during data-retention mode reduces

leakage power consumption by decreasing both supply voltage and transistor

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leakage current.[1]  The minimum data retention voltage can be a few tenths of a volt

above the threshold voltage[2] of typical transistors for the bit cell.  (*See* Ex.1021,

U.S. Patent No. 5,898,235, 2:52-62; *see also*, Ex.1022, U.S. Patent No. 6,347,379,

6:13-15.)

65.     For example, an early 256-bit SRAM product developed by Intel in

1969 reduced power consumption by a factor of 20 (from 1 mW per bit to 50 $\mu$W)

for standby mode by reducing the supply voltage to the memory cells, when

compared with normal operation.

---

[1] During operation and standby it is possible for data errors to occur as a result of

noise and high-energy events, such as alpha particles from packaging material and

cosmic rays from deep space.  As supply voltage is lowered, less charge is stored

in the bit circuit, so the rate of errors generally rises.  Consequently, it is necessary

to design and evaluate the storage circuitry and its supply voltage to ensure an

acceptable error rate according to application requirements.

[2] The threshold voltage of an MOSFET (Metal-Oxide-Silicon Field-Effect

Transistor) is the minimum gate-to-source voltage that is needed to turn on the

transistor, i.e., to form a conducting channel between the source and drain

terminals.

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Power dissipation is typically less than 2 mW per bit for normal operation. This, however, can be lowered to below 50 µW. In standby mode-when the chip will only store information, but does not need to be accessed-- the peripheral power supply can be completely shut down. This "idle" cuts the total power drain by a factor of 2. Furthermore, the cell power can be reduced considerably by reducing the cell voltage to -2 volts. This generates only -7 volts across the memory bits and is adequate for holding information in the memory cells. Figure 12 shows typical power dissipation in both the cells and peripheral (decode, I/O) circuitry. In this mode of operation, the total power dissipation is less than 12 mW, and corresponds to less than 50 µW/bit.

(Ex.1023, L. L. Vadasz, *et al*., "Silicon-Gate Technology," IEEE Spectrum, vol. 6 no. 10 at 35 (Oct. 1969).)

66. Such standby voltage-reduction techniques were also used for microprocessors to retain state while reducing leakage power consumption. For example, the µPD751xx microcomputer circuits produced by NEC operate between 2.7 V at 263 kHz and 6.0 V at 1.05 MHz. (*See* Ex.1005, NEC-Databook at 24-75; *see id*. at 61-62 (AC Characteristics and Figure 17).) The NEC microcomputers have standby modes that stop the CPU's clock, including a Data Retention mode that allows the supply voltage to be reduced to 2.0 V while retaining the contents of data memory, including general registers. (*Id*. at 32, 47,

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and 64; *see id*. at 33 (Figures 2, 2a, and 3.) An interrupt can be used to exit Data

Retention mode after the supply voltage is raised to resume normal operation. (*Id*.

at 47 (Figure 10), 48 (Table 7), and 65 (Figure 19B).)

**Table 7. Standby Mode Operation**

| Item | STOP Mode | HALT Mode |
|------|-----------|-----------|
| Setting the mode | STOP Instruction | HALT Instruction |
| Clock oscillator | The main system clock oscillator is stopped | Only CPU clock $\phi$ is stopped (oscillation continues) |
| Basic interval timer | Operation stopped | Can Operate (IRQBT is set by reference time interval) |
| Serial interface | Can operate only when external $\overline{SCK}$ input is selected for serial clock. (Note 1) | Can operate if other than CPU clock $\phi$ is specified as serial clock |
| Timer/event counter | Can operate only when TIn (n = 0, 1) pin input is selected for count clock | Can operate |
| Clock output circuit | Stops operation | Can operate if other than CPU clock $\phi$ is specified |
| CPU | Operation stopped | Operation stopped |
| Retained data | Contents of all registers (general registers, flags, mode registers, and output latches) and contents of data memory retained | |
| Release signal | Interrupt request signal (enabled with interrupt enable flag) from operating hardware or $\overline{RESET}$ | |

**Notes:**

(1) Can also operate with TI0 selected as the serial clock, but only
when Timer/Event Counter 0 is operated with an external TI0
input.

(*Id*. at 48 (Table 7).)

### C.    Voltage Regulation

67.    A voltage regulator is a device or a component that provides regulated

output voltage to circuitry, such as a microprocessor. A voltage regulator can be

an AC-DC converter, where the regulator receives AC input (*e.g.*, from the AC

mains such as 120 VAC, 230 VAC, *etc*.) and provides a regulated DC output (*e.g.*,

12 VDC, 5 V DC, *etc*.) or a DC-DC converter, where the regulators receives and

outputs DC power. A DC-DC converter can be a step-up (boost) converter, where

the output voltage is greater than the input voltage, or a step-down (buck)

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converter, where the output voltage is less than the input voltage.  A DC-DC

converter/regulator is also commonly classified as a "**linear regulator**" or a

"**switching regulator**," which are terms of art.

68.     Generally in a linear regulator, a pass element (typically a transistor,

such as a bipolar junction transistor (BJT) or a power field-effect transistor (power

FET)) is connected in series with a load.  (*See* U.S. Patent No. 5,677,558, 1:26-39;

FIG. 1 (Ex.1026); Bang S. Lee, "*Technical Review of Low Dropout Voltage*

*Regulator Operation and Performance*," Texas Instruments Application Report

SLVA072 at 1 (Aug. 1999) ("Lee-Report") (Ex.1027.)  In a typical linear

regulator, the pass element is operated in its **linear region**, (*see* Ex.1026, 1:26-32;

Ex.1027, 1-2; Figure 2), where the current passing through the pass element is

proportional to a base current supplied to the pass element.  (*See* Ex.1026, 3:61-
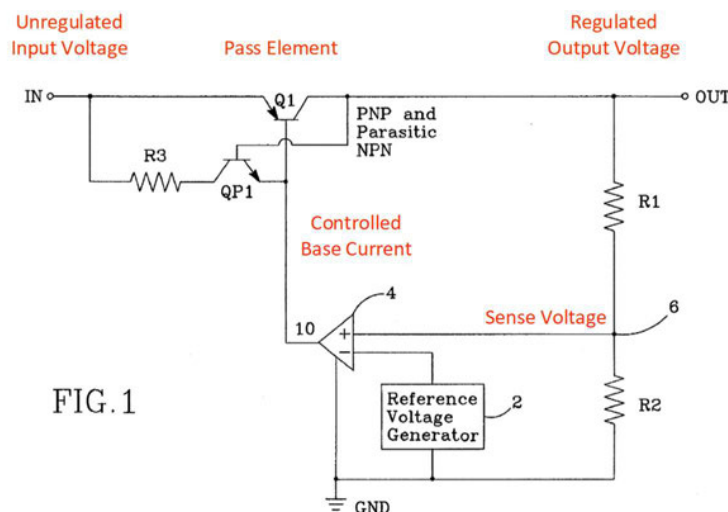
4:3; FIG. 1.)



FIG.1

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(Ex.1026, FIG. 1.)

69.     The base current is controlled such that the output voltage reaches a

desired output voltage.  At that time, the base current is reduced, in substance, to

zero and the pass element is turned off.  As the output voltage dropped below, this

change is sensed using a resistor-divider based feedback network, and the pass

element is turned on again, and operated in the linear mode, until the output

voltage reaches the desired level.  The above describe cycle may continue

indefinitely.  (*See* Bob Wolbert, "Micrel's Guide to Designing With Low-Dropout

Voltage Regulators," at 8 (Dec. 1998) (Ex.1028.)  In a variation of a linear

regulator, called "low drop-out" (LDO) regulator, the pass element may include

only a single transistor.  (*See id*. at 8, Figure 1-1; *see also*, *id.* at 10, Figures 1-

3(A)-(C) (depicting different configurations of a linear regulator, including an

LDO regulator).)

70.     In general, in a "switching regulator" a pass element may be series

connected between an unregulated input voltage and a load, *e.g.*, a microprocessor,

to which the regulator provides a regulated output voltage.  (*See* Jim Williams,

"Step-Down Switching Regulators," Linear Technology Application Note 35 at 1;

Figures 1 and 2 (Aug. 1989) ("Williams-Note") (Ex.1029); U.S. Patent No.

5,731,731, 1:23-26 (Ex.1030.)  A switching regulator is not operated like a linear

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regulator, however, *i.e.*, the pass element is not operated in the linear (or

saturation) region until the output voltage reaches the desired value and is then

turned off until the output voltage drops below the desired value.

71.     Rather, the pass element is switched on and off, *i.e.*, switched between

the saturation and cut-off regions, at a high frequency (*e.g.*, several kilohertz).

(*See* Ex.1030, 1:26-38; Ex.1029 at 18, col. 2 (describing a switching frequency of

100 kHz).)  The rapidly switching current at the output of the pass element is

filtered using an inductor-capacitor (LC) filter that can store the energy supplied

thereto and provide stabilized, regulated voltage to the load.  (*See* Ex.1030, 1:26-
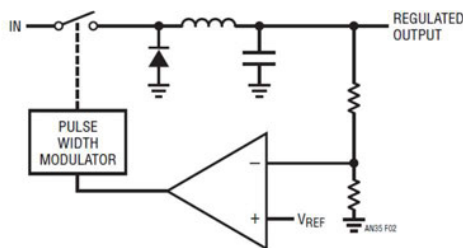
38.)



Figure 2. Conceptual Feedback Controlled Step-Down Regulator

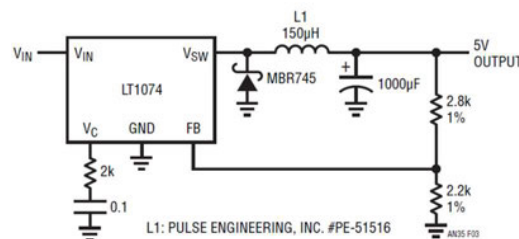Figure 3. A Practical Step-Down Regulator Using the LT1074

(Ex.1029 at 1 (Figure 2), 2 (Figure 3).)

72.     One or more parameters of the switching, *e.g.*, the width of the

switching pulses and/or the frequency of the pulses may be control the output

voltage of the regulator to a desired value.  (*See id.*)  By convention, such a

regulator is called a "switching regulator" because its passed element is switched

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on and off, in order to regulate the output voltage thereof.

73.     The supply voltage for a microprocessor is commonly provided by a

DC-DC converter that receives power at a higher voltage level (such as about 12 V

for power supply of a desktop computer or the battery of a notebook computer) and

outputs a lower voltage(such as 3 V) required by the processor.  The processors

described above, which have dynamic voltage scaling while active and lower

voltage for data retention while idle, place a number of demands on their power

supply.  The output voltage can vary only a limited amount, such as 5%, from a

nominal target value for the processor to operate reliably.  The process of

*regulating* the output voltage within such limits can require different techniques for

efficient operation (that is, with relatively little energy loss) when supplying high

current for peak performance or low current for lower-performance or idle periods.

74.     For example, U.S. Patent No. 5,568,044 ("Bittner") (Ex.1034),

teaches a DC-DC converter that uses **Pulse-Width Modulation (PWM)** when

supplying high current and **Pulse-Frequency Modulation (PFM)** when supplying

low current.  In particular, Bittner states that "the present invention achieves high

efficiency over a wide range of output currents by automatically switching between

PFM mode operation (when the output current is relatively small) and PWM mode

operation (when the output current exceeds a predetermined level)." (Ex.1034,

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5:57-61.)  A block diagram of Bittner's converter is reproduced below.
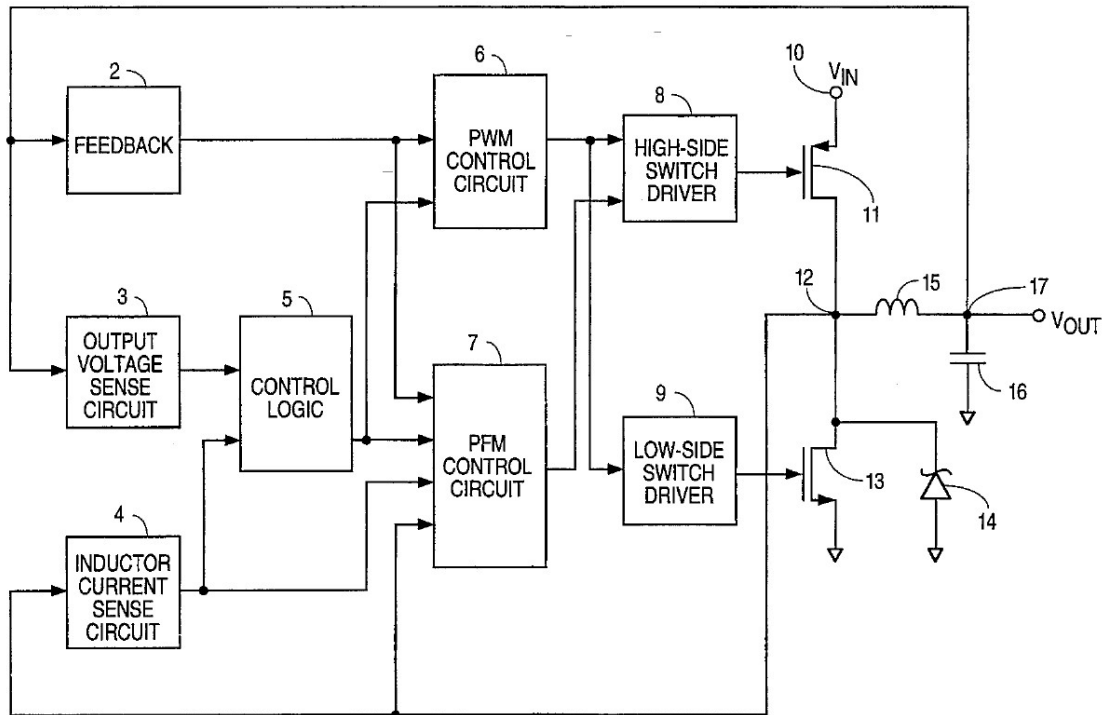


(Ex.1034, FIG. 1.)

75.    In Bittner's regulator, when pMOS transistor 11 (also called a high-side transistor) is switched on, the input voltage $V_{IN}$ is coupled to node 12.  The output voltage $V_{OUT}$ is supplied from node 12 through inductor 15, which together with capacitor 16 comprises a low-pass filter to minimize the effect of high-frequency switching at node 12 on $V_{OUT}$. When operating in PWM mode, $V_{OUT}$ is fed back through circuit 2 to PWM Control Unit 6, which compares $V_{OUT}$ to a reference voltage to adjust the duty cycle of transistor 11 by controlling the width of a pulse at its gate; the bigger the voltage difference, the wider the pulse.

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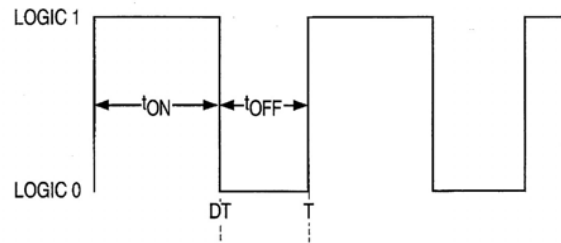Petition for *Inter Partes* Review of
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FIG. 2A



$$I_{OUT} = I_{IND, PK} - \frac{\Delta I_{IND}}{2}$$
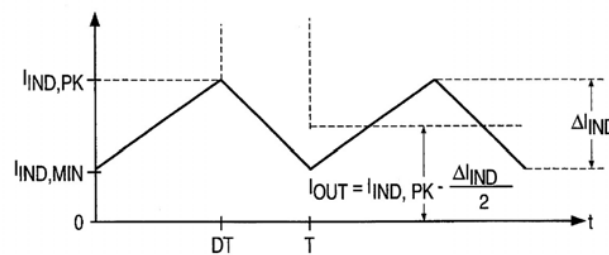
FIG. 2B

(Ex.1034, FIGS. 2A and 2B.)

76.     When transistor 11 switches off, PWM Control Unit switches nMOS

transistor 13 (also called a low-side transistor) on, which couples node 12 to

ground.  FIG. 2A, reproduced above, shows the PWM control signal for transistor

11.  FIG. 2B, also reproduced above, shows the current through inductor 15, which

is rising when transistor 11 is switched on and falling when transistor 13 is

switched on.  Because the inductor is conducting current throughout the

converter's operation (*i.e.*, the inductor's current never goes to zero), PWM mode

of operation is characterized as "continuous."

77.     Every time transistor 11 switches on and off, some energy is

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dissipated. When the supply current is high, a relatively large amount of energy is being consumed by the processor, and the energy wasted by switching is relatively small in comparison. However, when the supply current is low, the energy wasted in switching can be comparable or exceed the energy consumed by the processor. Consequently, when the current supplied is low, it is more efficient to switch transistor 11 on less frequently, in a mode called PFM.

78. Thus, in PFM operation pulses are skipped except when $V_{OUT}$ has dropped by a certain margin below the reference voltage. For example, Bittner states: "This method of regulating the $V_{OUT}$ by preventing switch 11 from turning on when $V_{OUT}$, exceeds its nominal value $V_{OUT,NOM}$ is commonly referred to as "skipping cycles." (Ex.1034, 4:42-45.) Additionally, transistor 13 does not switch on; instead Zener diode 14 can provide a current path to the inductor after transistor 11 switches off. In PFM mode there are periods where the inductor current may drop to zero, and the small amount of current supplied to the processor may only be provided by capacitor 16.

79. Maxim developed a DC-DC converter for notebook computer processors, MAX1711, that supported dynamically variable voltage and PWM/PFM modes selected automatically or by asserting a signal ($\overline{SKIP}$) to force the PWM mode. (*See generally*, Ex.1035, "MAX1710/MAX1711/MAX1712

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High-Speed, Digitally Adjusted Step-Down Controllers for Notebook CPUs,"

Maxim Integrated Products Datasheet 19-4781, Rev 0, 11/98 ("MAX171X-1998-

Datasheet").)  The target reference voltage is specified by a 5-bit binary code,

which is input to a Digital to Analog Converter (DAC).
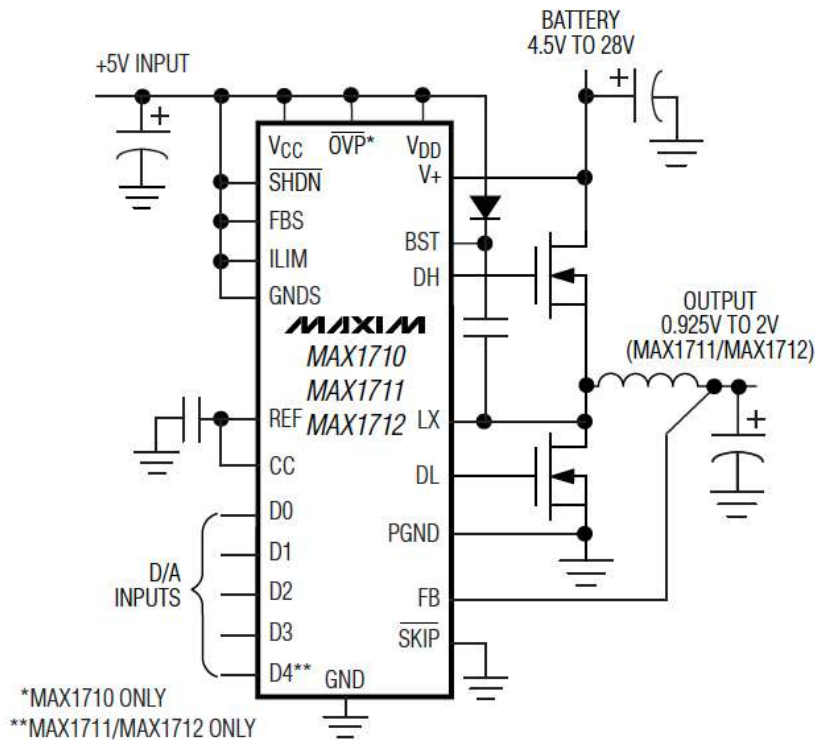


(*Id*. at 1.)

80.     In particular, MAX171X-1998-Datasheet states that the "MAX1711 is

intended for applications where the DAC code may change dynamically."  (*Id*.)

MAX171X-1998-Datasheet further states:

> At light loads, an inherent automatic switchover to PFM takes place.
> This switchover is effected by a comparator that truncates the low-
> side switch on-time at the inductor current's zero crossing. This

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mechanism causes the threshold between pulse-skipping PFM and

nonskipping PWM operation to coincide with the boundary between

continuous and discontinuous inductor-current operation.

(*Id*. at 13.)

81.    Regarding the forced PWM made, MAX171X-1998-Datasheet states:

The low-noise, forced-PWM mode (SKIP driven high) disables the

zero-crossing comparator, which controls the low-side switch on-time.

This causes the low-side gatedrive waveform to become the

complement of the highside gate-drive waveform. This in turn causes

the inductor current to reverse at light loads, as the PWM loop strives

to maintain a duty ratio of VOUT/VIN. The benefit of forced-PWM

mode is to keep the switching frequency fairly constant, but it comes

at a cost: the noload battery current can be as high as 40mA or more.

Forced-PWM mode is most useful for reducing audio-frequency

noise, improving load-transient response, providing sink-current

capability for dynamic output voltage adjustment, and improving the

cross-regulation of multiple-output applications that use a flyback

transformer or coupled inductor.

(*Id*. at 14.)

82.    In describing the use of the modes based on the load, MAX171X-

1998-Datasheet states:

If the minimum load is very light, it may be necessary to assert forced

PWM mode (via $\overline{\text{SKIP}}$) during the transition period to guarantee some

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output sink current capability. Otherwise, the output voltage won't
ramp downwards until pulled down by external load current.

Using forced PWM mode repeatedly to ensure sink current capability
can have side effects, however. The energy taken from the output by
the synchronous rectifier isn't lost, but is instead returned to the input.
If the frequency of the high-to-low output voltage transition is high
enough, efficiency will be degraded by the resistive "friction" losses
associated with shuttling energy between input and output capacitors.
Also, if the output is being overdriven by an external source (such as
an external docking-station power supply), forced PWM mode may
cause the battery voltage to become pumped up, possibly
overvoltaging the battery.

(*Id*. at 23, col. 1.)

83.     Thus, MAX171X-1998-Datasheet teaches that the PWM mode can be
forced when the voltage is being dynamically decreased, in particular when the
processor load is light (*e.g.*, when the processor's clock is stopped), because the
converter does not switch on the high-side transistor (such as Bitnner's transistor
11) in the PFM mode while the output voltage is above the reference voltage.  By
forcing PWM, the high-side transistor will turn on, sinking energy from capacitor
16 and returning it to the input, thereby decreasing the output voltage to the target
reference.

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84. It should be understood that in general, even though a switching regulator is generally more efficient than a linear regulator, the operation of a switching regulator results in some wasted power, regardless of its mode of operation. In general, less power may be wasted in the operation of the regulator in the PFM mode, due to the reduced switching activity of the high-side and low-side transistors in the PFM mode. Nevertheless, when the load is high, *e.g.*, when the processor receiving regulated voltage from a voltage regulator is in the operating state and is performing computations, it is beneficial to operate the regulator in the PWM mode because the loss of power in the regulator is relatively low compared to the power consumed by the processor, and the PWM mode offers benefits such as less noise and quicker adjustments to the output voltage than the PFM mode.

85. When the load is light, *e.g.*, when the processor is in the sleep state and is not performing computations, the CPU power consumption is very low and the power loss in the regulator may become comparable to or may even exceed the power consumption of a CPU in a sleep state. As such, when the load is low, the regulator is typically operated in the PFM, or the so called "high efficiency mode."

86. While the observations described above are generally true when the load is stable, *i.e.*, the load is settled at a high value or a low value, **a peculiar**

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**problem can arise when the voltage supplied by the regulator is transitioning from a high value to low value**, *e.g.*, in response to a change in the load condition from a high load to a light load. In this case, the output capacitor of the regulator already has some charge stored therein, corresponding to the high output voltage that was supplied before the transition to the low voltage commenced. The regulator cannot supply the required low voltage until this stored charged is removed from the output capacitor.

87.     The charge from the output capacitor can be removed in two ways: either by dissipating it in the load (which may be light) or, it can be transferred to some other circuitry for storage. Dissipation of the charge in the load results in a waste of power while transferring (also called shuttling) of the charge avoids such waste, resulting in power saving. (*See* Ex.1035 at 23, (stating that "energy taken from the output by the synchronous rectifier isn't lost, but is instead returned to the input"); Ex.1006 at 2 (Figure 17.4.3 (depicting that the tracking mode is initiated only when the voltage is transitioning)); 1, col. 2 (describing that in the tracking mode "the converter either delivers or removes charge from the capacitor" and that in the regulation mode "only the processor circuits can remove charge").)

88.     Shuttling the charge has an added benefit of faster voltage transition because when the load is light, dissipation of the charge in the load can take longer

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than the time required for shuttling. (Ex.1035 at 12 (describing that unless the PWM mode is forced, "the output voltage won't ramp downwards until pulled down by external load current"); Ex.1012 at 3, col. 2-4, col. 1 (stating that "fast [voltage] transition timing means that the regulator circuit must sink as well as source current" and that is can be accomplished by forcing "PWM mode only during [voltage] transitions").)

89.     Thus, these prior art references teach that although the PFM mode is generally more efficient when the output voltage has settled to a low value, e.g., when the load is light, during the time when the voltage is changing, *e.g.*, from a high value to a low value, it is the otherwise less efficient PWM mode that can save power by shuttling the charge stored at the output capacitor to the input capacitor or the battery, and the "efficient" PFM mode can result in waste of power.

## V.     THE '731 PATENT

### A.     Overview of the '731 patent

90.     The '731 patent is directed, in part, to decreasing the static power consumption of a processor (when the system/processor clock is disabled) by reducing its core voltage. For example, the Abstract of the '731 patent states: "A method for reducing power utilized by a processor" includes "reducing core

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voltage to the processor to a value sufficient to maintain state during the mode in

which system clock is disabled." (Ex.1001, Abstract.) Since the system or

processor clock is stopped, the processor's dynamic power consumption is zero.

By decreasing the core voltage, static power consumption can also be reduced.

91. For instance, the '731 patent states:

> When system clocks for a processor are disabled, the processor must
> remain in a state (sometimes called "deep sleep") in which it is
> capable of rapidly responding to interrupts. Such a state requires the
> application of core voltage to the various circuits. The application of
> this voltage generates a power dissipation referred to in this
> specification as "**static power**" usage because the processor is in its
> static state in which clocks are disabled.

(*Id.*, 1:50-58.) (emphasis added)[3].

92. The '731 patent further states:

> Since a processor is not capable of computing in the mode in which its
> clocks are disabled, it would at first glance appear that the solution
> would be to terminate the application of voltage to the processor.
> However, as suggested above, it is **necessary that the processor** be
> maintained in a condition in which it **can respond rapidly to**
> **interrupts** provided by the circuitry that controls application of the

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[3] Emphasis is added, unless noted otherwise.

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system clocks. To do this, the **processor must maintain state**
sufficient to immediately return to an operating condition. Thus, prior
art processors have been provided sufficient voltage to maintain such
state and to keep their transistors ready to immediately respond to
interrupts. In general, this has been accomplished by **maintaining the
processor core voltage at the same level as the operating voltage**.

(*Id.*, 2:58-3:4.)

93.     The '731 patent further states that "the voltage required to maintain

state in a deep sleep mode may be significantly less [than the operating voltage],

*e.g.*, one volt or less. Since such processors function at the same voltage whether in

a computing or a deep sleep mode, a significant amount of unnecessary power may

be expended." (*Id.*, 3:9-14.)  According to the purported invention, however, the

processor's core voltage may be reduced to a level that allows the processor to

maintain its state but does not allow the processor to perform computations.  This

reduces the processor's static power consumption when the processor clock is

disabled, but allows the processor to resume computations quickly when the

processor clock is reenabled later.

94.     As a purported novel solution to saving such power, the '731 patent

describes decreasing the core voltage supplied to the processor when it is in a sleep

slate, *i.e.*, when the processor clock is stopped, to a value less than the operating

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voltage.  In particular, the '731 patent states:

> The present invention reduces the voltage applied to the processor
> significantly below the lowest voltage normally furnished as a core
> voltage for the processor during the mode in which system clocks are
> disabled thereby reducing the power utilized by the processor in the
> deep sleep state.
>
> FIG. 3 is a circuit diagram illustrating a first embodiment of the
> invention. In the circuit 10 illustrated, a switching voltage regulator 11
> receives an input signal at a terminal 12 which determines its output
> voltage value. Most modern processors utilize a voltage regulator
> which is capable of furnishing a range of core voltages for operating
> transistors; a typical regulator may furnish a range of voltages
> between 2 and 0.925 volts from which a particular core voltage may
> be selected for operation. Typically, a binary signal is provided a the
> terminal 12 which selects the particular output voltage level to be
> furnished by the regulator 11; in such a case, a number of individual
> pins may be utilized as the terminal 12.

(*Id*., 3:18-35; FIG. 3.)

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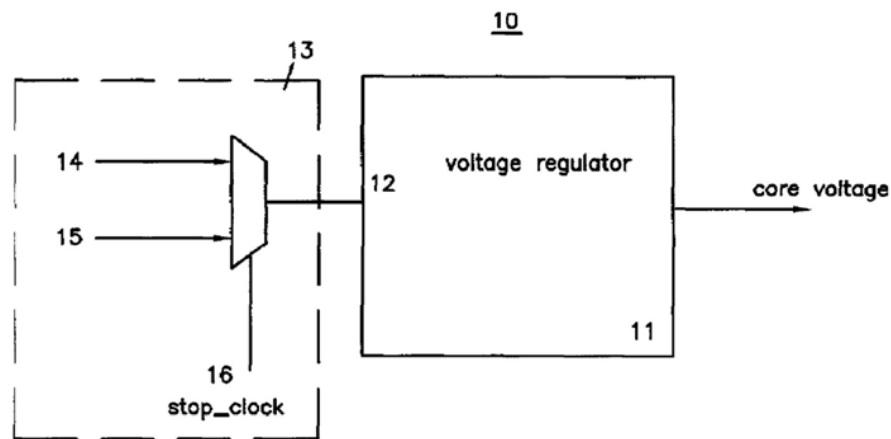U.S. Patent No. 7,260,731



Figure 3

(*Id.*, FIG. 3.)

95.     In the above discussed embodiment, the '731 patent uses a

multiplexor to provide an operating voltage value or a sleep voltage value

(disclosed as a deep sleep voltage value) to an adjustable voltage regulator.  The

operating or the sleep voltage values are provided as inputs to the multiplexor, and

one of these values is selected.  The selected value is provided to the adjustable

voltage regulator, which adjusts its output voltage according to the provided input

value.  (*See Id.*, 3:52-4:13; FIG. 3.)

96.     The '731 patent also describes an "exemplary processor" that "is

specified as capable of conducting computing operations in a core voltage range

from a low voltage of 1.2 volts to a high voltage of 1.6 volts" and, "when operating

in deep sleep mode [the processor] has no problem maintaining th[e] state

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necessary to resume computing even though functioning at a core voltage of 0.925

volts." (*Id*., 4:5-13; *see id*., 4:24-27 (describing an embodiment featuring the same

operating and sleep voltages).)

97.     The '731 patent observes that while the technique above is beneficial,

additional improvement in power saving is possible by further reducing the sleep

voltage, and sets forth conditions for facilitating such voltage reduction.

Specifically, the '731 patent states: "One problem with this approach to reducing

power is that it does not reduce the voltage level as far as might be possible and,

thus, does not conserve as much power as could be saved." (*Id*., 4:38-41.)

98.     Thereafter, the '731 patent states:

> Two criteria control the level to which the core voltage may be
> reduced in deep sleep. The level must be **sufficient to maintain state**
> that the processor requires to function after returning from the deep
> sleep state. The level must be one that can be reached during the times
> allowed for transition to and from the deep sleep mode.

(*Id*., 4:45-51.)

99.     The '731 patent further states:

> The first criterion is met so long as values of state stored are not lost
> during the deep sleep mode. Tests have shown that a core voltage
> significantly below one-half volt allows the retention of the memory

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state of a processor. Thus, using this criterion, it would be desirable to

reduce the core voltage to a value such as one-half volt or lower.

(*Id.*, 4:52-57.)

100. Regarding the second criterion, the '731 patent provides two examples

of operating voltage and corresponding sleep voltages as follows:

> [I]f the exemplary processor is operating at its lowest processing core
> voltage of **1.2 volts**, its core voltage may be lowered in the time
> available to **0.6-0.7 volts**. On the other hand, if the processor is
> operating at a processing core voltage of **1.5 volts**, its core voltage
> may only be lowered in the time available to **0.9-1 volts**.

(*Id.* at 4:64-5:2.)

101. In connection with the examples above, the '731 patent states:

"Consequently, it is desirable that the core voltage furnished during deep sleep be

lowered to a level which may be below the level provided by a typical voltage

regulator but which varies depending on the core operating voltage from which it

transitions." (*Id.*, 5:2-6.)

102. To this end, the '731 patent describes:

> This desirable result may be reached utilizing a circuit such as that
> described in FIG. 4. The circuit of FIG. 4 includes a feedback network
> 41 for controlling the level of voltage at the output of the regulator 11.
> Prior art regulators such as the Maxim 1711 provide a feedback

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terminal and describe how that terminal may be utilized with a resistor-voltage-divider network joined between the output terminal and ground to raise the output voltage level.

The embodiment of the present invention illustrated in FIG. 4 utilizes the same feedback terminal and a similar resistor-voltage-divider network but joins the divider between the output terminal and a source of voltage 42 higher than the normal output voltage of the regulator to force the output voltage level to a lower value rather than a higher level.
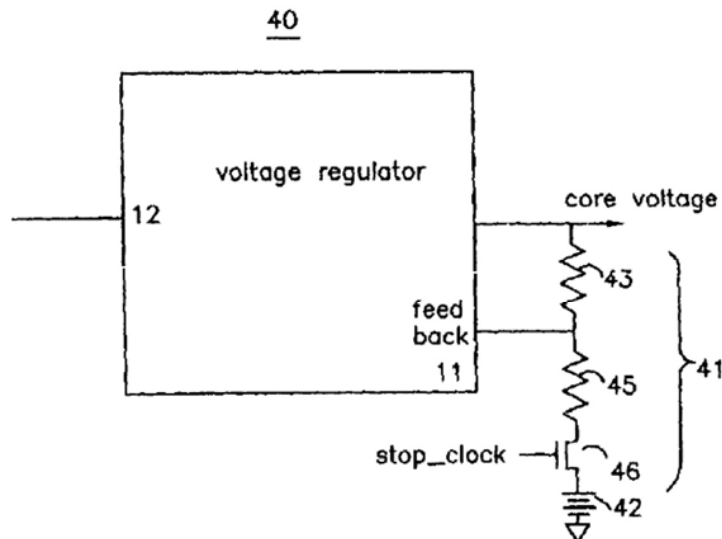
(*Id*., 5:7-21; FIG. 4.)



Figure 4

(*Id*., FIG. 4.)

103.    In the above-described embodiment, a resistor-based voltage divider is selectively provided between the regulator's output voltage and an additional

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voltage source in order to modify the feedback signal and to force the voltage

regulator to output a lower voltage. (*Id.*, 5:7-21; FIG. 4.)

104.  The '731 patent also states: "It should be noted that the circuitry of

FIGS. 3 and 4 may be combined so that both input selection and output adjustment

are both used to adjust the core voltage value produced by a voltage regulator for

deep sleep mode in particular instances where the load capacitance is relatively

low." (*Id.*, 5:43-47; FIGS. 3 and 4.)

105.  Thereafter, the '731 patent describes conventional switching

regulators featuring the "'low noise' or 'continuous' mode" of operation and "

'high efficiency,' 'burst,' or 'skip' mode" of operation, and that it was known to

use these two modes under high and light load conditions, respectively. (*See id.*,

5:48-6:13.)  The '731 patent further states:

> The present invention utilizes the ability of regulators to function in
> both the high efficiency mode and the continuous mode to
> substantially **reduce power wasted by transitioning between a
> computing and a lower voltage deep sleep mode**. Although
> regulators have not been dynamically switched between high
> efficiency and continuous modes, in one embodiment of the invention,
> an **additional controlling input 50** as shown in FIG. 5 is added to the
> regulator **for selecting the mode of operation** of the regulator based
> on whether the processor being regulated is transitioning between
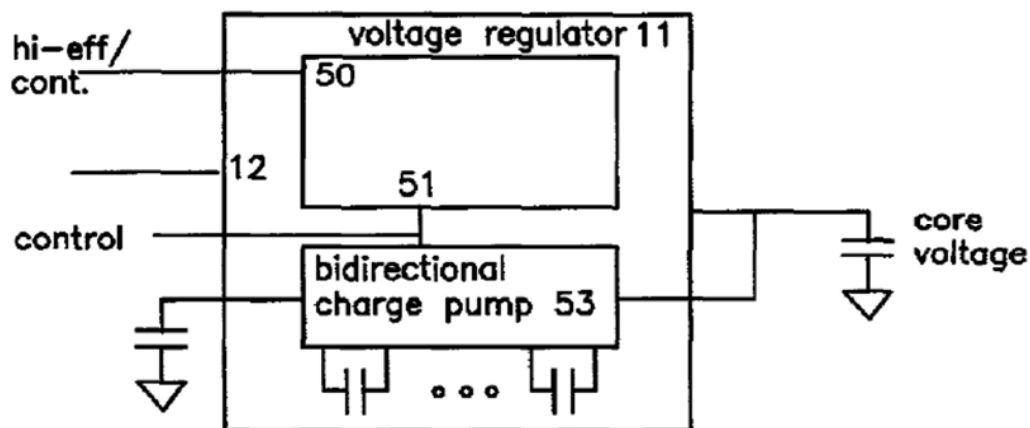
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states. If the regulator receives a control signal 51 indicating that the

processor is to be placed into the deep sleep mode, for example, then a

**regulator operating in the high efficiency mode immediately**

**switches to the continuous mode during the voltage transition**.

Assuming that the regulator **returns the charge to the battery** during

continuous mode, this has the effect of reducing the waste of power

caused during the transition. Once the transition has completed, the

regulator **switches back to the high efficiency state** for operation

during the deep sleep mode of the processor.

(*Id.*, 6:37-56; FIG. 5.)

106.   The '731 patent also states: "For regulators that do not conserve

capacitive charge by transferring the charge to the battery, a circuit for

accomplishing this may be implemented or a capacitor storage arrangement such as

a charge pump 53 for storage may be added." (*Id.*, 6:57-61; FIG. 5.)



(*Id.*, FIG. 5.)

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## B.     Prosecution History

107.   The '731 patent issued on August 21, 2007 from U.S. Application No. 09/694,433 (the "'731 application"), filed on October 23, 2000.  (*Id.,* Ex.1001, face page.)

108.   At filing, the '731 application included 13 claims, (Ex.1004 at 30, 47-50).  In the first Office action issued on July 30, 2003, the Examiner rejected claims 1-13 under 35 U.S.C. § 102(a) or 35 U.S.C. § 102(e) as being anticipated by U.S. Patent No. 6,118,306 ("Orton"). (Ex.1004 at 80-83.)

109.   Applicants filed a response on April 19, 2010, in which the Applicants amended the title, claims 1, 2, 4, 5, 6, 7, 11 and 13.  (*Id.* at 111-117.)   Regarding the rejection of claims 1 and 7, Applicants stated that these claims, as amended, required reducing the voltage of the processor core to a value that is sufficient to maintain state of the processor, but is not sufficient to maintain processing activity in the processor.  Applicant stated further that Orton did not teach or suggest this limitation.  (*Id*. at 118-120.)

110.   Regarding independent claim 4, Applicants stated Orton did not teach or suggest providing a feedback signal to the regulator to reduce its output voltage below a specified output voltage.  (*Id*. at 120-121.)  With respect to independent claim 5, Applicants stated that Orton did not teach or suggest transforming the

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operation of a voltage regulator from a mode in which power is dissipated to a mode in which power is saved.  (*Id*. at 121-122.)

111.  In addressing the rejection of independent claim 11, Applicant stated that Orton did not teach or suggest "reducing the selectable voltage below a level provided by the voltage regulator." (*Id*. at 123-124.)  For independent claim 13, Applicant stated that Orton does not teach or suggest "circuitry for conserving charge stored by the voltage regulator when the selectable voltage decreases."  (Id. at 126-127.)

112.  A final Office action issued on April 19, 2004, in which the Examiner rejected claims 1-3 under 35 U.S.C. § 112, first paragraph, as lacking enablement. The Examiner also rejected claims 1-3 under 35 U.S.C. § 103(a) as being obvious over Orton in view of U.S. Patent No. 5,812,860 ("Horden"), and maintained the rejection of claims 4-11 and 13 as being anticipated by Orton. The Examiner identified claim 12 as containing allowable subject matter but depending from a rejected base claim. (Ex.1004 at 180-188.)

113.  The Applicants filed a response on Aug 03, 2004, in which the Applicants amended claim 12 and added new claims 14-18.  (*Id.* at 205-213.) Regarding the rejection of claims under § 112, Applicant referred to a telephonic interview held with the Examiner on July 7, 2004 and noted that this ground for

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rejection was withdrawn. (*Id*. at 214, 215.)

114. In addressing the rejection of claims 1-3, Applicants stated that the combination of Orton and Horden did not teach or suggest reducing the voltage of the processor core to a value that is sufficient to maintain the state of the processor, but that is not sufficient to maintain processing activity in the processor. (*Id*. at 215-218.)

115. Regarding independent claims 4, 5, 7, 11, and 13, Applicants presented substantially the same arguments that were presented earlier (in the response on April 19, 2010). (*See id*. 218-224.) Regarding new independent claim 14, Applicant stated that the prior art of the record did not teach or suggest the limitation ""a voltage source furnishing a value higher than the selectable voltage; and a feedback circuit coupled to the voltage source." (*Id*. at 224-225.)

116. A non-final Office action issued on September 22, 2004, in which the Examiner rejected claims 1-3 under 35 U.S.C. § 103(a) over Orton in view of the publication "Re: AX64Pro or AK72?11" ("NewsReader"). In addition, the Examiner rejected claims 4, 12, and 14-18 under 35 U.S.C. § 103 (a) as obvious over Orton in view of Applicant Admitted Prior Art (AAPA), and maintained the rejection of claims 5-11 and 13 as anticipated by Orton. (*Id.* at 235-245.)

117. Applicants filed a response on March 22, 2005, amending claim 11

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and adding new claims 19-37. (*Id.* at 253-256.) Regarding claims 1-3, Applicants

stated that the combination of Orton and NewsReader did not teach or suggest

reducing the voltage of the processor core to a value that is sufficient to maintain

the state of the processor, but that is not sufficient to maintain processing activity

in the processor. (*Id*. at 267-271.)

118. In addressing the rejection of independent claim 4, Applicants

discussed the specification of the Maxim 1711 regulator admitted as prior art. (*Id*.

at 272; *see* Ex.1001, 5:10-14.) Applicants stated in particular that "AAPA

('Maxim' specification, page 10) may teach how to raise the output voltage of the

voltage regulator, but not to <u>lower the output voltage, as claimed</u>." (Ex.1004 at

272 (emphasis in original).)

119. Regarding independent claim 12, Applicants stated that Orton and/or

the AAPA do not teach a "voltage divider network joined between the output

terminal and a <u>voltage source furnishing a value *higher* than the selectable

voltage.</u>" (*Id.* at 273 (emphasis in original).) Applicants presented the same

arguments with respect to independent claim 14. (*Id.* at 274.) For independent

claims 5, 7, and 13 Applicants presented substantially the same arguments,

respectively, that were presented earlier (*e.g.*, in the response on April 19, 2010).

(*See id*. 275-276.)

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120.    In addressing the rejection of claim 11, Applicants stated:

Orton may describe causing the voltage regulator to output different

voltages. However, Applicants respectfully assert that Orton is silent

as to causing the voltage regulator to output **a voltage below a lowest**

**level the voltage regulator is specified to output**, as claimed.

Applicants respectfully assert that one of ordinary skill in the art

would understand Orton to teach that the output voltage of the voltage

regulator to be **within a range specified by the voltage regulator**, as

Orton is silent as to causing the voltage regulator to output a voltage

outside of that range. For the foregoing reasons, Applicants

respectfully assert that Orton fails to teach or suggest the limitations,

"means for reducing the selectable voltage **below a lowest level the**

**voltage regulator is specified to output**.

(*Id.* at 277.)

121.    Regarding new independent claims 19, 25, 29, and 22, Applicants

stated that the prior art of the record did not teach or suggest the limitations recited,

respectively, in these claims.  (*Id*. at 279-280.)

122.    Thereafter, a final Office action issued on June 9, 2005.  (*Id*. at 319.)

The Examiner stated that claims 1-18 and 19-37, respectively, were directed to

different inventions and required an election of one set of claims.  (*Id*. at 321-322.).

Regarding claims 1-18, the Examiner maintained the rejections from the previous

Office action.  (*Id*. at 322.)

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123.   Following the final Office action issued on June 9, 2005, the Examiner issued an interview summary on November 10, 2005 according to which the Examiner agreed to reevaluate the rejection of claims 1, 4, 5, and 7.  (*Id*. at 336.)  Applicants filed a response on November 23, 2005, simply stating that the prior art of the record did not teach or suggest limitations recited in claims 1-18. (*Id*. at 340-343.)

124.   A non-final Office action issued thereafter, on December 14, 2005, in which the Examiner maintained the election/restriction requirement from the previous Office action.  The Examiner rejected claims 1-3, 5-11 and 13 under 35 U.S.C. § 102(e) as being anticipated by U.S. patent no. 6,675,304 ("Pole"), and claims 4, 12 and 14-18 under 35 U.S.C. §103 (a) as being unpatentable over Pole in view of AAPA and "High-speed, Digitally adjusted step-down controllers for notebook CPUs" Maxim, July 2000, pages 1-28 ("MAX171X-2000-Datasheet").[4] (*Id.* at 347-357.)

125.   Applicants filed a response on March 6, 2006[5] and filed a corrected

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[4] Provided as Exhibit 1045.

[5] This response was non-compliant.  (*Id*. at 387-389 (Notice of Non-Compliant Amendment).)

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response on July 24, 2006. (*Id*. at 390.) In this response, claims 19-37 were cancelled. (*Id.* at 398-99.) Regarding claims 1 and 7, Applicants stated that "Pole does not teach or fairly suggest the limitation 'reducing core voltage to the processor to a value sufficient to <u>maintain state</u> during the mode in which system clock is disabled.'" (*Id*. at 399 (emphasis in original), 404.) Applicants also stated: "Pole teaches a deep sleep state in which <u>only</u> data stored in the processor's internal caches is maintained (column 1, lines 30-34). As is well known to those of ordinary skill in the art, **a processor's state** is not represented in the processor's internal caches, and **includes**, for example, **the contents of internal registers** which are not represented in the caches." (*Id*. at 400.)

126.  Regarding claim 5, Applicants presented the same arguments as those presented in connection with claim 1. (*Id*. at 401-402.) In addition, Applicants stated that Pole does not teach or suggest "<u>transferring operation of a voltage regulator furnishing core voltage in a mode in which power is dissipated during reductions in core voltage to a mode in which power is saved during a voltage transition</u> when it is determined that a processor is transitioning from a computing mode to a mode is which system clock to the processor is disabled." (*Id*. at 402-403 (emphasis in original).)

127.  Applicants further stated:

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The underscored language refers to modes of operating a voltage regulator (power dissipation mode/power saving mode). Applicants respectfully assert that Pole fails to teach or suggest the limitations of Claim 5. Pole may discuss lowering a voltage level supplied to a processor. However, power savings can be achieved in manners other than reducing frequency and/or reducing voltage of a processor. Applicants have specifically recited in this embodiment that <u>saving power is performed by a choice of mode of operation of the voltage regulator</u>. Pole is silent as to any <u>mode of operation</u> of a voltage regulator, aside from outputting a plurality of voltages. Consequently, Pole is silent as to <u>operating the voltage regulator in a mode in which power is dissipated to a mode in which power is saved</u>, as claimed. Thus, Pole fails to teach or fairly suggest the claimed transferring the operation of a voltage regulator from a mode in which power is dissipated to a mode in which power is saved, during a voltage transition.

(*Id*. at 403 (emphasis in original).)

128.    Regarding claim 11, Applicants stated that Pole is silent as to causing the voltage regulator to output a "voltage below a lowest level the voltage regulator is specified to output." (*Id*. at 405.)  Applicants stated further that "one of ordinary skill in the, art would understand Pole to teach that the output voltage of the voltage regulator to be <u>within</u>, ***e.g.*, neither above nor below, a range specified by the voltage regulator**, as Pole is silent as to causing the voltage regulator to

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**output a voltage outside of that range**.” (*Id.* (emphasis original in part, added in part).)

129. Regarding claim 13 Applicants stated that Pole fails to teach or suggest “circuitry for conserving charge stored by the voltage regulator when the selectable voltage decreases, and means for enabling the circuitry for conserving charge stored by the voltage regulator when the selectable voltage decreases.” (*Id.* at 405-406.)

130. Regarding claim 4, Applicants stated that the combination of Pole, AAPA, and MAX171X-2000-Datasheet fails to teach “providing a feedback signal to the voltage regulator to <u>reduce</u> its output voltage below a specified output voltage.” (*Id*. at 407 (emphasis in original).) Applicant stated that AAPA teaches that “prior art regulators such as the Maxim 1711 provide a feedback terminal and describe how that terminal may be utilized with a resistor-voltage-divider network . . . to <u>raise</u> the output voltage level.” (*Id*. at 381-382 (emphasis in original).) Applicant stated further that “[A]APA actually <u>teaches away</u> from embodiments in accordance with the present invention that recite using feedback to <u>reduce</u> an output voltage as recited by Claim 4.” (*Id*. at 407 (emphasis in original).)

131. Applicants presented substantially the same arguments for claims 12 and 14 as that presented for claim 11 regarding Pole, and stated further that

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"Maxim and [A]APA do[] not remedy this defect." (*Id*. at 382-384.)

132. A Final Office action subsequently issued on September 29, 2006, in which the Examiner maintained the rejection of claims from the previous Office action. (*Id*. 415-417.) Applicants filed a pre-appeal brief request for review, along with the notice of appeal, on January 4, 2007. (*Id*. 437 and 431.) In the pre-appeal brief request Applicants presented substantially the same arguments that were presented in the response filed on July 24, 2006. (*Id*. at 431-436..) In response, the Office reopened prosecution. (*Id*. at 442.)

133. Applicants filed a supplemental response on March 19, 2007, in which the Applicants amended claims 1-3, 5-7, 9, 10 and 13 and cancelled claims 19-37. (*Id*. at –448-458.) Applicants also noted telephonic interviews held with the Examiner on January 23, 2007 and February 8, 2007. Applicants stated that "[a]greement on Claims 1-18 was reached." (*Id*. at 458.) The supplemental response did not present any substantive arguments.

134. Thereafter, the Notice of Allowance was mailed on April 04, 2007. (*Id*. at 462.) In the Notice, the Examiner did not state reasons for allowance. (*See id*. at 462-491.)

**C.    Rebuttal of Applicants' Remarks During Prosecution**

135. In the response filed on July 24, 2006, Applicants stated that

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AAPA/MAX171X-2000-Datasheet teach away from the feature using feedback to

reduce an output voltage. (*Id*. at 390, 407.) AAPA/MAX171X-2000-Datasheet do

not "teach away" reducing the output voltage, because MAX171X-2000-

Datasheet's circuitry can be readily adapted to lower the output voltage, as

discussed below. A POSITA would have known the required modification and

would have found such a modification to be straightforward, as it was disclosed in

a textbook, Nilsson, in 1993. (*See* Ex.1013 at 200.)

136. The '731 patent does not explicitly show the internal circuitry of a

voltage regulator that can supply selectable output voltages. (*See generally*,

Ex.1001.) Such a regulator typically includes an operational amplifier configured

as a difference amplifier. One input of the amplifier is supplied with a reference

voltage from a voltage source, *e.g.*, from a battery or a digital-to-analog converter,

as in the case of Maxim-1710 regulator (*see* Ex.1045[6] at 11 (Figure 2); Ex.1035 at

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[6] Exhibit 1045 is MAX171X-2000-Datasheet, the document showing the version as

"Rev 1" and publication date as "7/00," that was cited during prosecution (*see*

Ex.1045 at 1; Ex.1004 at 354); Exhibit 1035 is an earlier version of MAX171X-

2000-Datasheet, showing the version as "Rev 0" and publication date as "11/98."

(*See* Ex.1035 at 1.)

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11 (Figure 2)) or Texas Instruments TI-TPS5210 controller/regulator. (*See*

Ex.1008 at 2 (Figure "functional block diagram" (depicting "VID MUX and

Decoder" generating the voltage VREF)).) The other input is provided with a

fraction of the output voltage, where the fraction is obtained using a voltage

divider. (*See* Ex.1001, FIG. 4; Ex.1045 at 22 (Figure 8); Ex.1035 at 21 (Figure 8);

Ex.1008 at 2, 19 (Figure 18).)

137.    Nilsson, a text book for example, discloses a configuration of a

difference amplifier employing a resistor-voltage-divider in a similar manner as

that disclosed in the '731 patent (*see* Ex.1001, FIG. 4), in MAX171X-2000-

Datasheet (*see* Ex.1045 at 22 (Figure 8); *see also* Ex.1035 at 21 (Figure 8)), and in

the TI-TPS5210 controller/regulator. (*See* Ex.1008 at 2, 19 (Figure 18).) Nilsson's

configuration uses **two** voltage sources instead of one, where each voltage source

is coupled to a respective input of the amplifier. This allows the output voltage to

be raised or **lowered** with respect to a specified reference voltage. (Ex.1013 at

200; *id*. (Figure 6.14).)

138.  As such, while MAX171X-2000-Datasheet does not explicitly

disclose reducing the regulator's output voltage, it does not teach away from

implementing such a feature. Rather, with the simple addition of a second voltage

source, MAX171X-2000-Datasheet's circuitry is compatible with and readily

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adapted to provide the functionality of reducing the regulator's output voltage.

### D. The Challenged Claims

139. This Declaration addresses claims 1-18 of the '731 patent. The '731 patent has eight independent claims, of which independent claims 1, 4, and 6 are directed to a "method for reducing power utilized by a processor" and independent claims 8, 12, 13, 14, and 15 are directed to a "circuit for providing a regulated voltage to a processor."

140. Claims 1-18 are set forth below:

| Claim / Element | Limitation |
|---|---|
| 1[pre] | A method for reducing power utilized by a processor comprising the steps of: |
| 1[a] | determining that a processor is transitioning from a computing mode to a mode in which a system clock to the processor is disabled, and |
| 1[b] | reducing core voltage to the processor to a value sufficient to maintain state during the mode in which said system clock is disabled, wherein said value of the core voltage is not sufficient to maintain processing activity in said processor, |

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| Claim / Element | Limitation |
|---|---|
| 1[c] | responsive to said determining, at a voltage regulator supplying said core voltage, transitioning from a first regulation mode to a second regulation mode, |
| 1[c.1] | wherein power is dissipated during a voltage transition that reduces said selectable voltage in said first regulation mode and |
| 1[c.2] | power is saved during said voltage transition in said second regulation mode. |
| 2. | The method as claimed in claim 1 in which the step of determining that a processor is transitioning from a computing mode to a mode in which system clock to the processor is disabled comprises monitoring a stop clock signal. |
| 3. | The method as claimed in claim 1 in which the step of reducing core voltage to the processor to a value sufficient to maintain state during the state in which system clock is disabled comprises furnishing an input to reduce an output voltage provided by a voltage regulator furnishing core voltage to the processor. |
| 4[pre] | 4[pre]  A method for reducing power utilized by a processor comprising the steps of: |

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| Claim / Element | Limitation |
|---|---|
| 4[a] | determining that a processor is transitioning from a computing mode to a mode in which system clock to the processor is disabled, and |
| 4[b] | reducing core voltage to the processor to a value sufficient to maintain state during the mode in which system clock is disabled by: |
| 4[b.1] | furnishing an input to reduce an output voltage provided by a voltage regulator furnishing core voltage to the processor, and |
| 4[b.2] | providing a feedback signal to the voltage regulator to reduce its output voltage below a specified output voltage. |
| 5 | The method of claim 4, wherein the output voltage to which said voltage regulator is reduced depends upon output voltage of said voltage regulator prior to furnishing the input to reduce the output voltage provided by the voltage regulator. |
| 6[pre] | 6[pre]  A method for reducing power utilized by a system having a least a processor, comprising the steps of: |
| 6[a] | 6[a]  determining that the processor is transitioning from a computing mode to a mode in which a system clock to the processor is disabled, |

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| Claim / Element | Limitation |
| --- | --- |
| 6[b] | 6[b] reducing core voltage being furnished by a voltage regulator to the processor to a value sufficient to maintain state during the mode in which the system clock is disabled, and |
| 6[c.1] | transferring operation of the voltage regulator furnishing core in a mode in which power is dissipated during a voltage transition in reduction in core voltage |
| 6[c.2] | 6[c.2] to a mode in which power is saved during said voltage transition in the reduction in core voltage |
| 6[c.3] | 6[c.3] when it is determined that the processor is transitioning from the computing mode to the mode in which the system clock to the processor is disabled. |
| 7. | The method as claimed in claim 6 further comprising the steps of returning the voltage regulator to its original mode of operation when the value of the core voltage sufficient to maintain state during the mode in which system clock is disabled is reached. |
| 8[pre] | A circuit for providing a regulated voltage to a processor comprising: |
| 8[a] | a voltage regulator having: |

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| Claim / Element | Limitation |
|---|---|
| 8[a.1] | an output terminal providing a selectable voltage, and |
| 8[a.2] | an input terminal for receiving signals indicating the selectable voltage level; |
| 8[b.1] | means for providing signals at the input terminal of the voltage regulator for selecting a voltage for operating the processor in a computing mode and a voltage of a level less than that for operating the processor in a computing mode, |
| 8[b.2] | wherein the level less than that for operating the processor in a computing mode is sufficient to maintain state of the processor; and |
| 8[c.1] | means for changing the voltage regulator from a mode in which power is dissipated during a voltage transition that reduces said selectable voltage |
| 8[c.2] | to a mode in which power is saved during said voltage transition. |
| 9 | A circuit as claimed in claim 8 in which the means for providing signals at the input terminal of the voltage regulator comprises means for accepting binary signals indicating different levels of voltage. |

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| Claim / Element | Limitation |
|---|---|
| [10.pre] | The circuit as claimed in claim 8 in which the means for providing signals at the input terminal of the voltage regulator comprises: |
| [10.a] | selection circuitry, |
| [10.b] | means for furnishing a plurality of signals at the input to the selection circuitry, and |
| [10.c] | means for controlling the selection by the selection circuitry. |
| 11[pre] | The circuit as claimed in claim 10 in which: |
| 11[a] | the selection circuitry is a multiplexor, and |
| 11[b] | the means for controlling the selection by the selection circuitry includes a control terminal for receiving signals indicating a system clock to the processor is being terminated. |
| 12[pre] | A circuit for providing a regulated voltage to a processor comprising: |
| 12[a] | a voltage regulator having: |
| 12[a.1] | an output terminal providing a selectable voltage, and |
| 12[a.2] | an input terminal for receiving signals indicating the selectable voltage level; |

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| Claim / Element | Limitation |
|---|---|
| 12[b] | means for providing signals at the input terminal of the voltage regulator for selecting a voltage for operating the processor in a computing mode and a voltage of a level less than that for operating the processor in a computing mode; and |
| 12[c] | means for reducing the selectable voltage below a lowest level the voltage regulator is specified to output. |
| 13[pre] | A circuit for providing a regulated voltage to a processor comprising: |
| 13[a] | a voltage regulator having: |
| 13[a.1] | an output terminal providing a selectable voltage; |
| 13[a.2] | an input terminal for receiving signals indicating the selectable voltage level; and |
| 13[a.3] | a voltage regulator feedback circuit; |
| 13[b] | means for providing signals at the input terminal of the voltage regulator for selecting a voltage for operating the processor in a computing mode and a voltage of a level less than that for operating the processor in a computing mode; and |

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| Claim / Element | Limitation |
|---|---|
| 13[c] | means for reducing the selectable voltage below a level provided by the voltage regulator comprising: |
| 13[c.1] | a voltage divider network joined between the output terminal and a voltage source furnishing a value higher than the selectable voltage, and |
| 13[c.2] | the voltage regulator feedback circuit receiving a value from the voltage divider network. |
| 14[pre] | A circuit for providing a regulated voltage to a processor comprising: |
| 14[a] | a voltage regulator having: |
| 14[a.1] | an output terminal providing a selectable voltage, and |
| 14[a.2] | an input terminal for receiving signals indicating the selectable voltage level; |
| 14[b.1] | means for providing signals at the input terminal of the voltage regulator for selecting a voltage for operating the processor in a computing mode and a voltage of a level less than that for operating the processor in a computing mode; |

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| Claim / Element | Limitation |
|---|---|
| 14[c.1] | circuitry for changing the voltage regulator from a mode in which power is dissipated during a voltage transition in reduction of the selectable voltage |
| 14[c.2] | to a mode in which system power is saved during said voltage transition in reduction of the selectable voltage, and |
| 14[d] | means for enabling the circuitry for conserving charge stored by the voltage regulator when the selectable voltage decreases. |
| 15[pre] | A circuit for providing a regulated voltage to a processor comprising: |
| 15[a] | a voltage regulator having: |
| 15[a.1] | an output terminal providing a selectable voltage, and |
| 15[a.2] | an input terminal for receiving signals indicating the selectable voltage level; and |
| 15[a.3] | a voltage regulator feedback circuit; |
| 15[b] | circuitry coupled to said input terminal and configured to provide signals to the input terminal for selecting a first voltage for operating the processor in a first mode and a second voltage for operating the processor in a second mode; |

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| Claim / Element | Limitation |
|---|---|
| 15[c] | a voltage source furnishing a value higher than the selectable voltage; and |
| 15[d] | a feedback circuit coupled to the voltage source, the output terminal, and the voltage regulator feedback circuit. |
| 16. | The circuit of claim 15, wherein the first voltage is for operating the processor in a computing mode and the second voltage is a level less than that for operating the processor in the computing mode. |
| 17. | The circuit of claim 16, wherein the feedback circuit comprises a voltage divider. |
| 18. | The circuit of claim 15, wherein the feedback circuit comprises a voltage divider. |

141.   I have added indices of the form 1[a], 1[b], 1[c], *etc.* to the claim limitations for ease of reference, and to match the indices used in the Petition.

## VI.   APPLICATION OF THE PRIOR ART TO ASSERTED CLAIMS

142.   I have reviewed and analyzed the prior art references and materials listed in Part I(C) above.  In my opinion, the claims of the '731 patent are unpatentable because they are rendered obvious based on the following prior art:

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| Ground | Reference(s) | Claims(s) |
|---|---|---|
| 1 | NEC-Databook in view of Burd | 1, 3, 6, and 7 |
| 2 | NEC-Databook in view of Burd, further in view of Nguyen | 2 |
| 3 | NEC-Databook in view of TI-TPS5210-Datasheet, further in view of Kikinis | 4 and 5 |
| 4 | Helms in view of Maxim-165X-Datasheet, further in view of MAX1711-Kit | 8-11 and 14 |
| 5 | Helms in view of TI-TPS5210-Datasheet, further in view of Nilsson | 12, 13, and 15-18 |

143. I am informed by counsel that each reference listed above qualifies as prior art to the challenged claims because each reference was filed and/or published before the earliest claimed priority date.

A. **Brief Summary of Prior Art**

144. From the prior art discussed below, NEC-Databook, Burd, Nguyen, TI-TPS5210-Datasheet, Helms, Maxim-165X-Datasheet, MAX-1711-Kit, and Nilsson, were not cited and not considered by the Examiner.

145. Kikinis was cited by the Examiner, but the Examiner did not reject any claims using Kikinis and did not discuss Kikinis during prosecution. (*See*

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*generally*, Ex.1004.)

146.   MAX-1711-Kit discusses Maxim Integrated Products' MAX-1711 voltage regulator.  (*See* Ex.1012 at 1.)  During prosecution (as summarized above in the discussion of prosecution history), the Examiner considered the MAX-1711 regulator from a different document – MAX171X-2000-Datasheet (Ex. 1045). MAX-1711-Kit was not cited during the prosecution.  Examiner generally considered MAX171X-2000-Datasheet in connection with the limitations "feedback signal" and "providing a feedback signal to the voltage regulator to reduce its output voltage below a specified output voltage," as claims 4, 12, and 14-18 pending during prosecution recited.  (*See* Ex.1004 at 354-357, 422-426.)

147.   The Examiner's assertion, that MAX171X-2000-Datasheet discloses a resistor-voltage-divider based feedback signal, was correct.  (*See* Ex.1045 at 22, col. 1 (stating that "output voltage can be adjusted with a resistor-divider"), 8 (describing a feedback pin "FB"), and 22 (Figure 8 (depicting that the resistor-voltage-divider can be coupled to the feedback pin FB)); *see also* Ex.1035 at 8, 21, col. 2, 21 (Figure 8) (describing and depicting the same).)

148.   Applicants were also correct in stating that MAX171X-2000-Datasheet teaches the use of its feedback input and resistor-voltage-divider for **raising** the input and not for lowering it below the lowest specified level.  (*See*

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Ex.1004 at 407-408 and 435.)  Applicants were not correct, however, in alleging

that MAX171X-2000-Datasheet teaches away from the feature of reducing the

regulator's output voltage, as required by claims 4, 12, and 13.  I explained this

above in Section V(C), Rebuttal of Applicants' Remarks During Prosecution.

149.    In my analysis below, I have not used MAX171X-1998-Datasheet or

the MAX171X-2000-Datasheet at all.  Rather, I rely on a different document,

MAX-1711-Kit, in the discussion of issued claims 8-10 and 14, which correspond

to claims 7-9 and 13 pending during prosecution.  Moreover, I rely on Maxim-

165X-Datasheet and MAX-1711-Kit not to show the feedback signal or resistor-

voltage-divider limitations, but to show changing the operating mode of a

regulator, where energy is dissipated in one mode but is saved in another mode.

This features derives from forcing of the PWM mode in a regulator that can be

operated in both PWM and PFM modes, as I explain below.

### 1.    NEC-Databook (Ex.1005)

150.   NEC-Databook published in May 1990, more than one year before the

priority date of the '731 patent (October 23, 2000).  I am informed and understand

that NEC-Databook qualifies as prior art under 35 U.S.C. § 102(b) to the '731

patent.

151.   NEC-Databook discloses several families of microcontrollers

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including the μPD751xx/P1xx is a family. (*See* Ex.1005 at 4 and 24.)

Specifically, NEC-Databook states: "μPD751xx/P1xx is a family of high-performance single-chip CMOS microcomputers containing CPU [central processing unit], ROM, RAM, I/O ports, comparator, interval timer, two timer/counters, vectored interrupts, and a serial interface." (*Id*. at 24, col. 1; *see id*. at 35, col. 1 (referring to the CPU as a microprocessor).)

152.   NEC-Databook further discloses that the CPU of the μPD751xx family (the "μPD751xx-CPU") can be operated at different frequencies, to reduce power. For example, NEC-Databook states:

> The minimum instruction execution time is 0.95 μs with a 4.19 MHz clock. The PCC register can be used to program the CPU's minimum instruction cycle time to 0.95, 1.91, or 15.3 μs; **all three speeds** presuppose a 4.19 MHz crystal. **Reducing the CPU clock speed will reduce the microprocessor's power consumption**.

(*Id*. at 35, col. 1; *id*., col. 2 (stating that the "PCC selects **one of four available CPU cycle speeds**"); *see id*. at 24 (describing "High-speed cycle" time of "0.95 μs" and "Lower-voltage cycles" of "1.91 and 15.3 μs" periods).) The processor's operating frequency is the reciprocal of the cycle time.

153.   NEC-Databook also states: "The clock generator (figure 5) uses the crystal inputs X1 and X2 as a time base to provide clocks for the

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μPD751xx/P1xx." (*Id*. at 42, 44 (Figure 5).) Alternatively, the μPD751xx-CPU

can be operated using an external clock. (*See id*. at 54 (Table "Oscillator

Characteristics" (disclosing the use of an external clock having the same frequency

range of 2 to 5 MHz as that of the crystal resonator (oscillator), including the

presupposed oscillation frequency of 4.19 MHz.)), 55 (Figures 15A and 15B

((depicting crystal resonator and external clock configurations, respectively)).)

154.  Moreover, the μPD751xx-CPU can be operated at different voltages.

Specifically, NEC-Databook discloses the "[o]perating voltage range" of several

microcontrollers in the μPD751xx family as 2.7 to 6.0 V. (*Id*. at 31 (Table

"Product Comparison").)

**Product Comparison**

| Item | μPD75104/104A | μPD75106 | μPD75108/108A | μPD75P108 | μPD75112 | μPD75116 | μPD75P116 |
|------|---------------|----------|---------------|-----------|----------|----------|-----------|
| Power-on-reset circuit and power-on flag | Mask option | Mask option | Mask option | Internally provided | Mask option | Mask option | Not included |
| Operating voltage range | 2.7 to 6.0 V | 2.7 to 6.0 V | 2.7 to 6.0 V | 5 V ± 10% | 2.7 to 6.0 V | 2.7 to 6.0 V | 5 V ± 10% |
| Package | See ordering information for a complete list of packages | | | | | | |

(*Id*.)

155.  Figure 17 in NEC-Databook depicts a relationship between "Power

Supply Voltage," $V_{DD}$, that is supplied to a μPD751xx-CPU and that ranges from

2.7 to 6.0 V, and corresponding "Cycle Time[s]," in the "[g]uaranteed operating

range." (*See id*. at 62 (Figure 17 (annotated)).).

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**t$_{CY}$ vs V$_{DD}$ (With main system clock)**
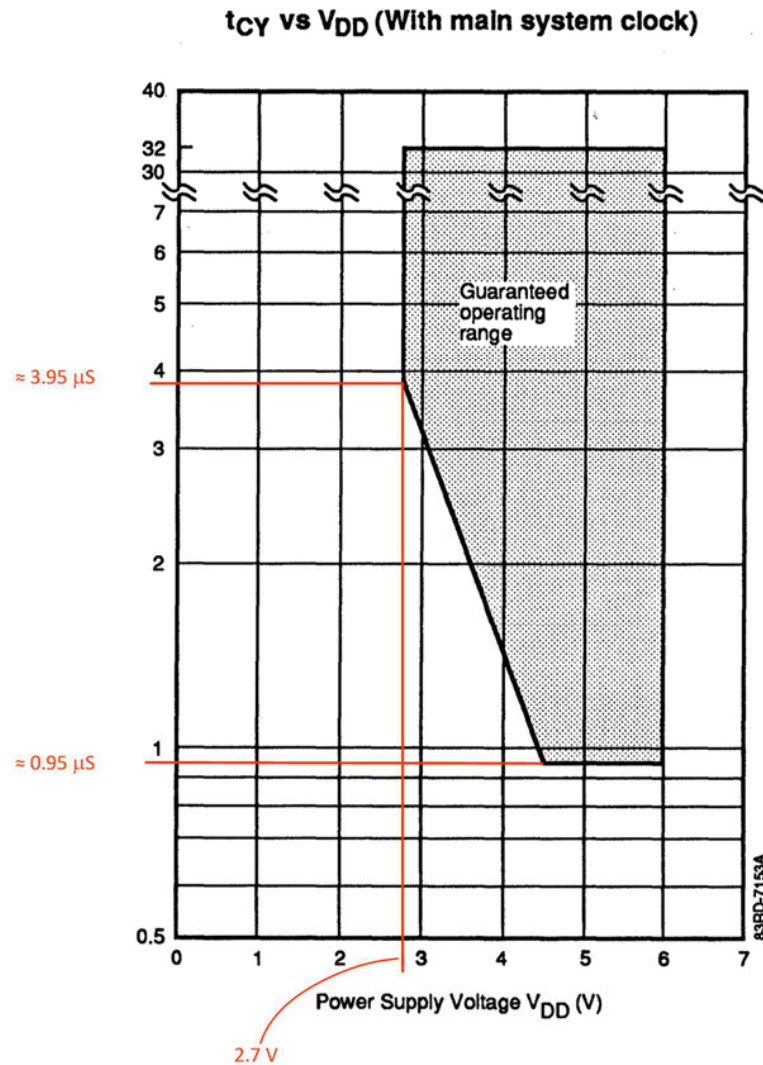


156.   In addition, NEC-Databook describes a "standby mode" for operating

its CPU, where the standby mode "consists of three submodes, HALT, STOP, and

Data Retention."  (*Id*. at 47, col. 1.)  NEC-Databook further states that in the

"HALT mode" "the clock to the CPU is shut off (thus stopping the CPU), while all

other parts of the chip remain fully functional," and that in the "STOP mode" "the

chip's main system oscillator is shut off, thereby stopping all portions of the chip."

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(*Id.*)

157.    Since the clock for the µPD751xx-CPU may be generated from the main system oscillator (*see id*. at 42, col. 1 (describing that a "clock generator" that includes "an oscillator" supplies "frequencies derived from [a] crystal" "to the CPU"); *id*. at 44 (Figure 5 (depicting the clock generator))), the CPU clock would be shutoff when the system oscillator is shut off.

158.    NEC-Databook further states that the "Data Retention mode" "may be entered after entering the STOP mode.  Here the **supply voltage $V_{DD}$ may be lowered to 2 volts** to further reduce power consumption."  (*Id*. at 47, col. 2; *see id*. at 65 (Figure 19 (depicting entering the "Data retention mode" within the "STOP mode" and **lowering the µPD751xx-CPU voltage from $V_{DD}$ to $V_{DDDR}$**)).)

159.    NEC-Databook discloses that the Data Retention mode can be "released by first raising $V_{DD}$ to the proper operating range, then releasing the STOP mode."  (*Id*. at 47, col. 2.)  In addition, NEC-Databook discloses that the STOP mode, from which the Data Retention mode is entered, can be released "by any interrupt request."  (*Id*.)  Figure 19B of NEC-Databook illustrates a release from the Data Retention mode and return to the operating mode in response to an interrupt.  (*Id*. at 65 (Figure 19B).)

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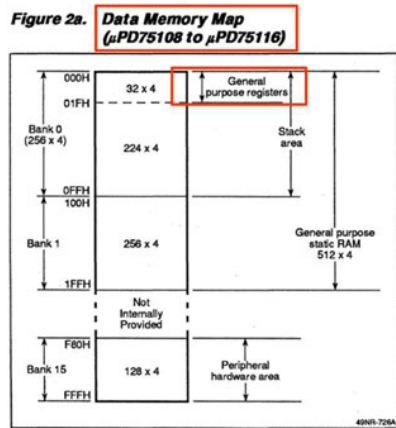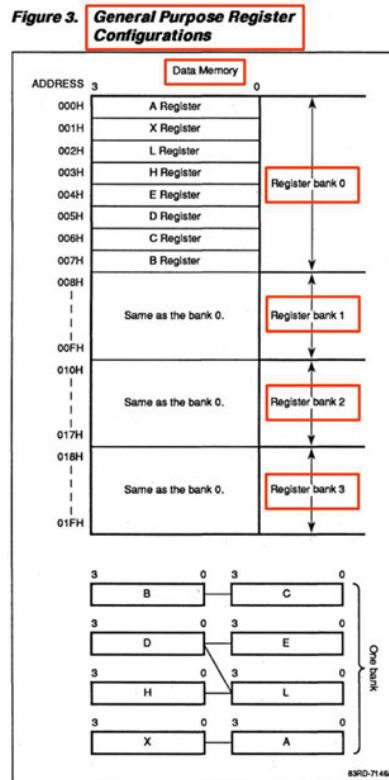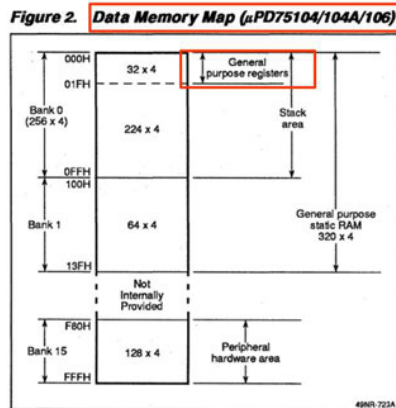Petition for *Inter Partes* Review of
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A. STOP mode is released by $\overline{\text{RESET}}$ input

B. STOP mode is released by interrupt signal
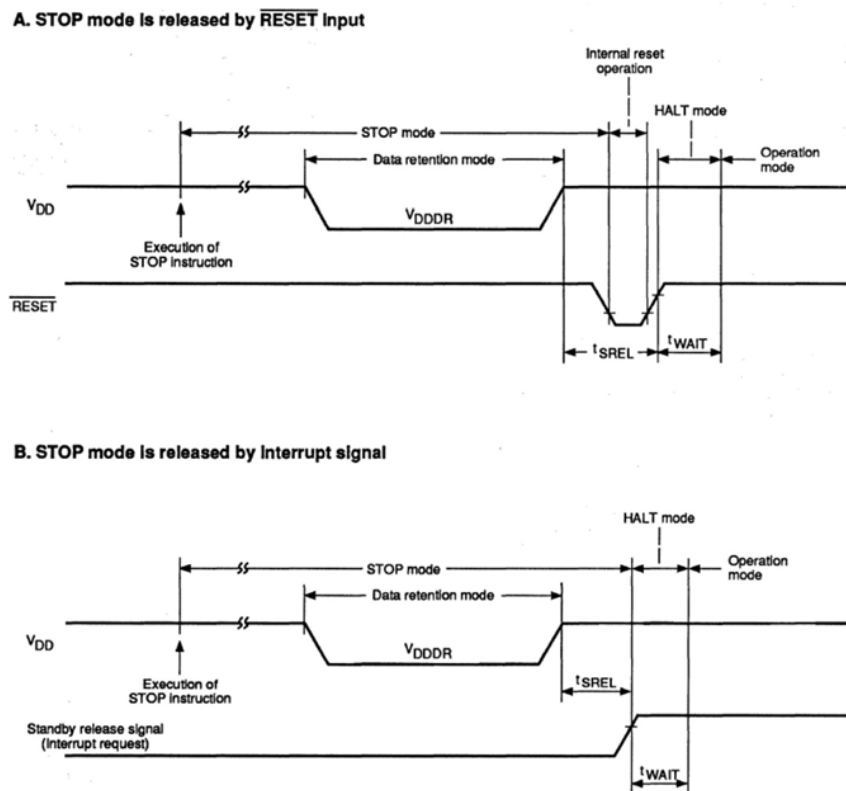
(*Id.*)

160.   NEC-Databook discloses that in the Data Retention mode, the

contents of the general purpose registers of the µPD751xx-CPU would be retained.

Specifically, NEC-Databook refers to its "data memory" as RAM, stating:

**Data Memory (RAM)**

The **data memory** contains three memory banks, 0, 1, and 15. The

RAM memory map is shown in figure 2. The **memory consists of**

general purpose static RAM, **general purpose registers, and**

**peripheral control registers**.

(Ex.1005 at 32, col. 1; *see id*. at 33 (Figures 2, 2a, and 3).)

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Figure 2. Data Memory Map (μPD75104/104A/106)

Figure 2a. Data Memory Map (μPD75108 to μPD75116)

Figure 3. General Purpose Register Configurations

(*Id*. at 33 (Figures 2, 2a, and 3).)

161.   In addition, NEC-Databook states that "data memory is used for
storing processed data [and] **general purpose registers**." (*Id*. at 32, col. 1.) NEC-
Databook further states that "the RAM will **retain its data** when the chip is in the
STOP mode, **provided V$_{DD}$ is at least 2 volts**." (*Id*.) In addition, Table 7 of NEC-
Databook describes "[r]etained data" as "[c]ontents of **all registers**" including
"general registers." (*Id*. at 48 (Table 7).) Thus, the contents of the general purpose
registers (and various other data) would be retained in the "Data Retention" mode,
when the CPU clock is stopped, and when the voltage supplied to the CPU is 2.0 V

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or more.

## 2. Burd (Ex.1006)

162. Burd published in February 2000, before the priority date of the '731 patent (October 23, 2000). I am informed and understand that Burd qualifies as prior art under 35 U.S.C. § 102(a) to the '731 patent.

163. Burd discloses a "voltage scheduler" implementing a "dynamic voltage scaling (DVS)" strategy, where the output voltage of a voltage regulator is adjusted according to a specified desired frequency for a ring oscillator, whose frequency varies directly with supply voltage. (*See* Ex.1006 at 1, col. 1.) Specifically, Burd states:

> If [] clock frequency ($f_{CLK}$) and supply voltage ($V_{DD}$) are dynamically varied in response to computational load demands, then energy consumed per process can be reduced for the low computational periods, while retaining peak performance when required. This strategy, which achieves the highest possible energy efficiency for time-varying computational loads, is called **dynamic voltage scaling (DVS)**.

(*Id.*)

164. Thereafter, Burd discloses: "A prototype DVS-enabled chip-set in 0.6μm 3-metal $V_T \approx 1V$, CMOS contains **a battery-powered (3.3-6.0V) switching**

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**regulator**, a microprocessor, SRAM memory chips, and an interface chip for

connecting to commercial I/O peripherals." (*Id.*; Figure 17.4.2.)  Burd further

describes:

> A regulation feedback loop for setting the variable $V_{DD}$ and $f_{CLK}$ is
> shown in Figure 17.4.2. The ring oscillator, which tracks the critical
> paths of the microprocessor over voltage, outputs $f_{CLK}$ as a function of
> $V_{DD}$. The $f_{CLK}$ signal is digitally quantized in 1MHz steps, and used to
> generate a frequency error, $F_{ERR}$. The loop filter implements a **hybrid
> pulse-width/pulse-frequency modulation algorithm that generates
> an $M_P$ or $M_N$ enable**. The regulated $V_{DD}$, which is fed back to the
> CPU chip to close the loop, is generated across the capacitor [of 5.5 µf
> shown in Figure 17.4.2.]

(*Id.*; Figure 17.4.2.)

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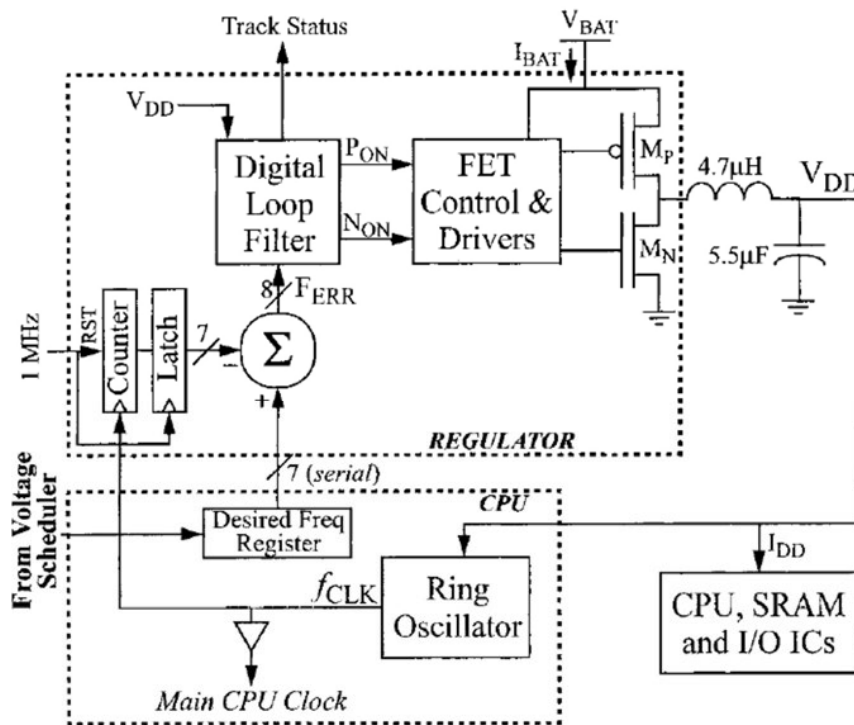U.S. Patent No. 7,260,731

**Figure 17.4.2: Frequency to voltage feedback loop.**

(*Id.*, Figure 17.4.2.)

165.   In addition, Burd states:

> The **converter operates in either tracking or regulation mode**, as
> indicated by the track status signal. A new frequency request initiates
> tracking mode in which the converter either delivers or removes
> charge from the capacitor, depending upon the sign of $F_{ERR}$. When the
> error magnitude is less than 4MHz, the converter switches to the
> regulation mode in which $M_N$ is disabled and only the processor
> circuits can remove charge.

(*Id.* at 1, cols. 1-2.)  Burd also states that in the "**tracking mode**" "**the converter**

**either delivers or removes charge from the capacitor**, depending upon the sign

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of $F_{ERR}$." (*Id.* at 1, cols. 1-2.)

166. In light of the disclosure above, a POSITA would have understood that in the regulation mode, the switching element $M_N$ (a field-effect transistor (FET) (*see id.*, Figure 17.4.2)), is disabled while in the tracking mode, both switching elements $M_P$ and $M_N$ are operated, and that in both modes, the switching of the FETs $M_P$ and/or $M_N$ is controlled by the **hybrid pulse-width/pulse-frequency modulation algorithm**.

### 3. Nguyen (Ex.1007)

167. U.S. Patent No. 5,955,871 to Nguyen ("Nguyen") issued on September 21, 1999, more than a year before the priority date of the '731 patent (October 23, 2000). I am informed and understand that NEC-Databook qualifies as prior art under 35 U.S.C. § 102(b) to the '731 patent.

168. Nguyen "relates to a voltage regulator, such as a switching voltage regulator." (Ex.1007, 1:6-7.) In particular, Nguyen discloses:

> Referring to FIG. 4, an embodiment 200 of a computer system in accordance with the invention includes **voltage regulation circuitry 246** that provides power to components of the computer system 200 via power lines 242. As described below, the voltage regulation circuitry 246 has **features that enhance the output voltage accuracy and power conversion efficiency** of the voltage regulation circuitry

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246 **when the computer system 200 enters a power conservation mode, such as a stop clock mode**, for example.

(Ex.1007, 2:45-53; FIG. 4.)

169.  More specifically, with reference to its FIG. 5, Nguyen teaches that "the controller 42 may use a sampled indication of the average $I_L$ current and regulate the level of the $V_{CORE}$ voltage based on the sampled average," (*id*. 3:22-24) where "controller 42 samples the average $I_L$ current by periodically activating sampling circuitry that may include, for example, a switch 47" to obtain "a sampled Voltage (called $V_{DSPS}$)."  (*Id*., 3:35-43; FIG. 5 (annotated).)



170.  Nguyen further states: "When the computer system 200 is **not in the power conservation mode**, the controller 42 **closes and opens the switch 47 (via**

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**a voltage called DSPS_DR) concurrently with the switch 38** to update the $V_{DSPS}$

voltage" (*id*. 3:45-49) but that:

> For purposes of ensuring that the $V_{DSPS}$ voltage accurately indicates
> the average $I_L$ current, the regulator 30 **does not open the switch 47**
> **during the power conservation mode**.  Instead, the regulator 30
> closes the switch 47 for substantially the entire duration of the power
> conservation mode to continuously provide the voltage across the
> resistor 46 to the capacitor 82.

(*Id*. 4:7-13.)

171.   The above-described power conservation mode based operation of the

switch 47 is achieved using a STP_CLK# signal (*stop clock signal*), as follows:

> Referring to FIG. 16, the drive circuit 44 includes a voltage buffer, or
> driver 144, that furnishes the $V_{SW2}$ voltage at its output terminal. An
> inverted indication of the $V_{SW2}$ voltage is received by an input
> terminal of a NAND gate 140. Another input terminal of the NAND
> gate 140 receives a **STP_CLK# signal which is asserted**, or driven
> low, **to indicate the power conservation mode** and deasserted, or
> driven high, otherwise. The output terminal of the **NAND gate 140**
> **furnishes a DSPS_DR signal that is received by the gate of the**
> **sampling transistor 80**. Therefore, as a result of this arrangement,
> when the computer system 200 is in the power conservation mode, the
> NAND gate 140 asserts the DSPS_DR signal to cause the sampling
> transistor 80 to conduct, and when the computer system 200 is not in

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the power conservation mode, the state of the DSPS_DR signal

closely follows the state of the $V_{SW2}$ voltage.

(*Id.*, 7:23-38; FIG. 16 (annotated).)
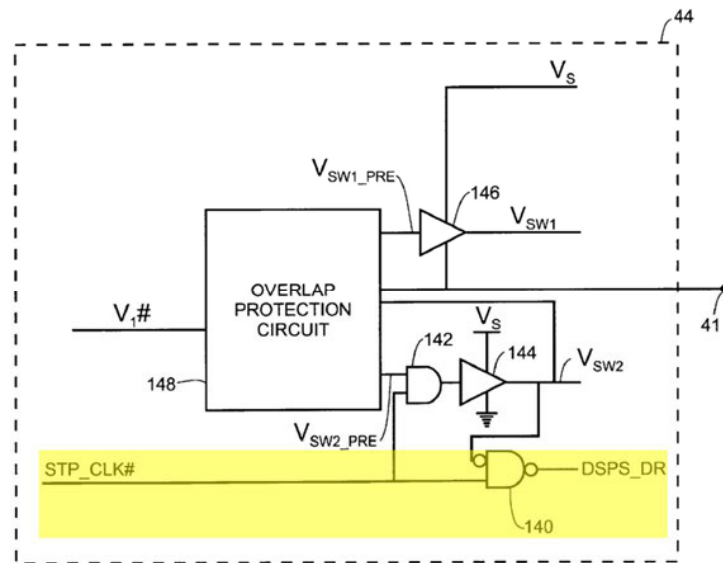


172.   Thus, Nguyen's STP_CLK# signal "**indicate[s] the power**

**conservation mode**."

### 4.      TI-TPS5210-Datasheet (Ex. TI-TPS5210-Datasheet)

173.   Texas Instruments, Inc., "TPS5210 Programmable Synchronous-Buck

Regulator Controller" (May 1999) ("TI-TPS5210-Datasheet") published in May

1999, more than a year before the priority date of the '731 patent (October 23,

2000).  I am informed and understand that TI-TPS5210-Datasheet is prior art under

at least 35 U.S.C. § 102(a) and (b).

174.   TI-TPS5210-Datasheet discloses TPS5210, "a synchronous-buck

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regulator controller," *i.e.*, a voltage regulator.  In particular, TI-TPS5210-Datasheet

states:

> The TPS5210 is a synchronous-buck regulator controller which
> provides an accurate, **programmable supply voltage to**
> **microprocessors**. An internal 5-bit DAC is used to program the
> reference voltage to within a **range of 1.3 V to 3.5 V**. The output
> voltage can be set to be equal to the reference voltage or to some
> multiple of the reference voltage.

(Ex.1008 at 1.)

175.   TI-TPS5210-Datasheet further discloses "Terminal Functions" where

terminals VID0-VID4 are "[d]igital inputs that **set the output voltage** of the

converter."  (*Id*. at 3.)

| VID0 | 27 | I | Voltage Identification input 0 |
|------|----|---|--------------------------------|
| VID1 | 26 | I | Voltage Identification input 1 |
| VID2 | 25 | I | Voltage Identification input 2 |
| VID3 | 24 | I | Voltage Identification input 3 |
| VID4 | 23 | I | Voltage Identification input 4. Digital inputs that set the output voltage of the converter. The code pattern for setting the output voltage is located in Table 1. Internally pulled up to 5 V with a resistor divider biased from V$_{CC}$. |

(*Id*. at 3, Table: Terminal Functions (partially reproduced and annotated); *id*. at 19,

Figure 18 (depicting inputs VID0 through VID4 and stating that these inputs are
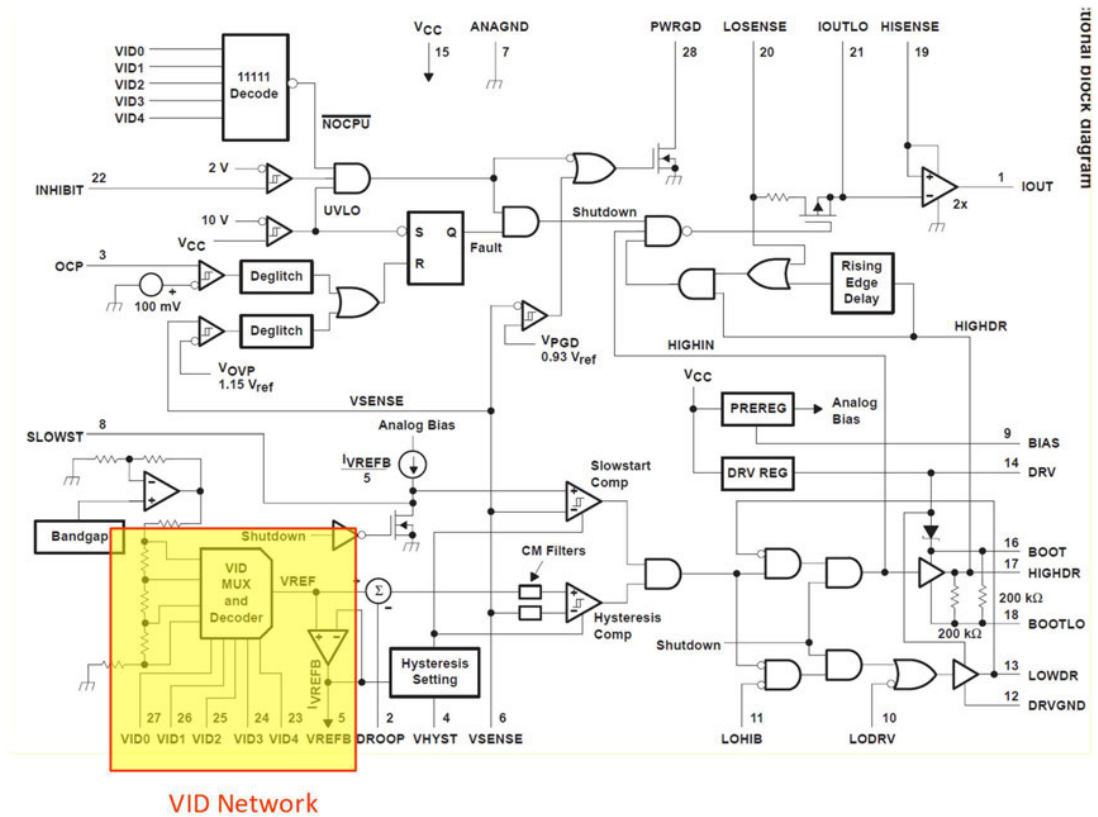
"[u]ser-selected").)

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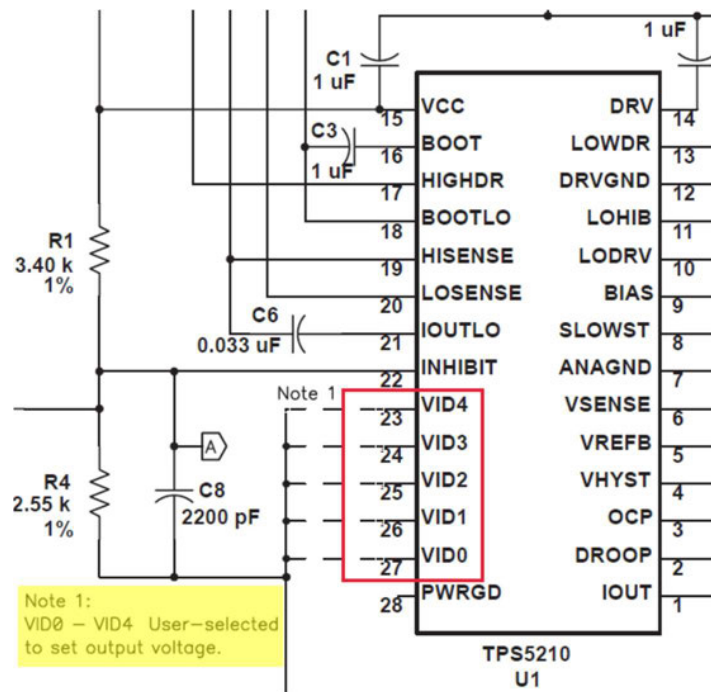


(Ex.1008 at 19, Figure 18 (partial).)

176. With reference to its "functional block diagram" (*see id*. at 2), TI-

TPS5210-Datasheet states: "The reference/voltage identification (VID) section"

includes "a 5-bit voltage selection network" and that the "output voltage of the

VID network, $V_{REF}$, is within ±1% of the nominal setting over the VID range of 1.3

V to [3.5] V," where the VID code settings are shown in Table 1. (*Id*. at 4; *see id*.

at 6, Table 1 (providing several values of VID0-VID4 and the corresponding $V_{REF}$

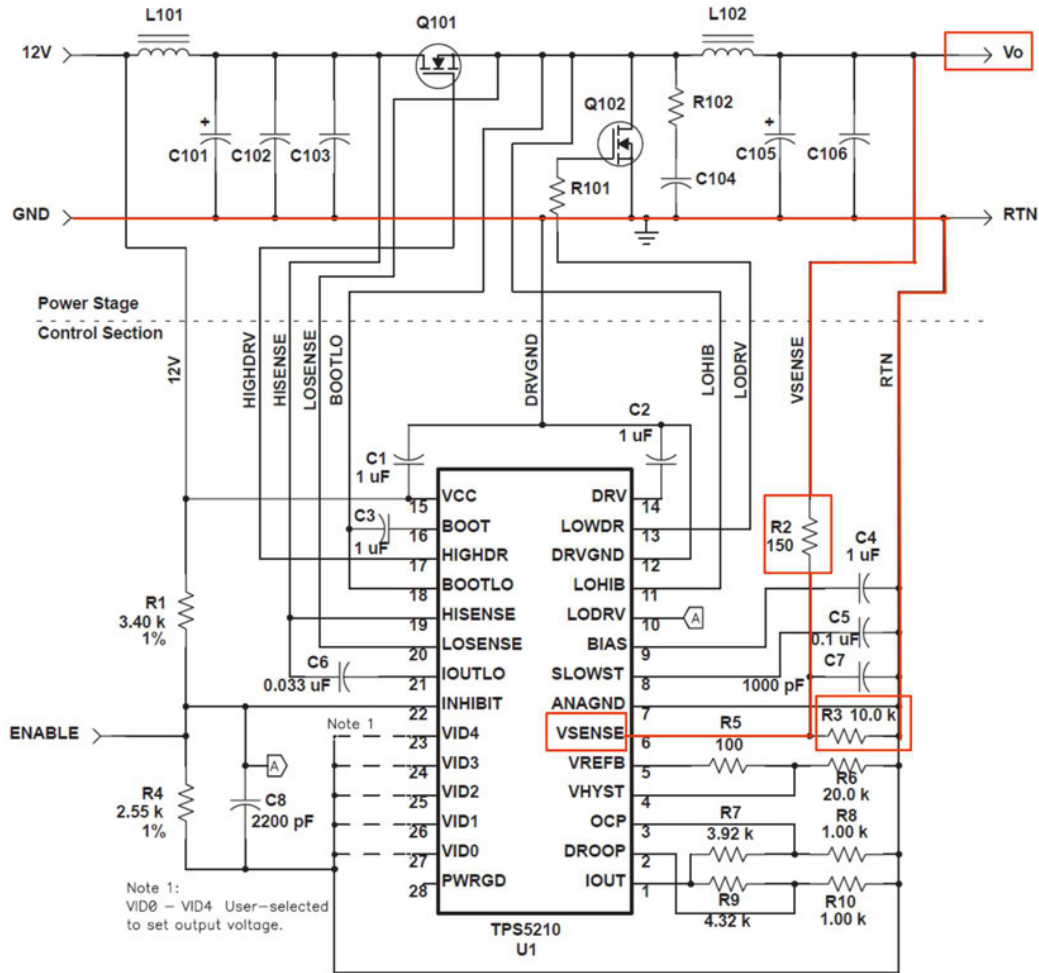values that determine the corresponding output voltages).)

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VID Network

(*Id*. at 2, "functional block diagram.")

177.   TI-TPS5210-Datasheet denotes the output voltage of the synchronous-

buck regulator $V_O$ (*see id*. at 19 (Figure 18) and 21), and states: "$V_O$ is

programmed to a voltage greater than $V_{REF}$ by an external **resistor divider from**

**$V_O$ to VSENSE**."  (*Id*. at 5; *see id*. at 19, Figure 18 (depicting the resistor divider

having resistors R2 and R3 between $V_O$, VSENSE, and ground.)

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(*Id*. at 19, Figure 18 (annotated).)

178. TI-TPS5210-Datasheet further states: "Values above the maximum

reference voltage (3.5 V) can be set by setting the reference voltage to any

convenient voltage within its range and selecting values for **R2 and R3** to give the

correct output." (*Id*. at 21.) In addition, TI-TPS5210-Datasheet states: "R2 and

R3" forming the resistor-voltage-divider "can also be used to make **small adjusts**

**to the output voltage within the reference-voltage range**" according to the

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Equation:

$$V_O = V_{REF}\left(1 + \frac{R2}{R3}\right)$$

(*Id*. at 21.)

179.   In light of the typical configuration of a resistor-voltage-divider and the corresponding regulation of the output voltage, a POSITA would have recognized that the input VSENSE is a feedback input of the TI-TPS5210-Datasheet's synchronous-buck regulator.

### 5.   Kikinis (Ex.1009)

180.   U.S. Patent No. 5,919,262 to Kikinis et al. ("Kikinis") issued on July 6, 1999, more than a year before the priority date of the '731 patent (October 23, 2000).  I am informed and understand that Kikinis is prior art under at least 35 U.S.C. § 102(b).

181.   Kikinis discloses a "voltage regulator with an electrically-erasable programmable read-only memory electronically accessible for storing a feedback reference coefficient for control."  (Ex.1009, Abstract.)  In the "Background of the Invention" Kikinis discloses, with reference to FIG. 3 that is labeled "prior art" the "details of a switching voltage regulator chip with a resistor or **potentiometer**, as used in current art."  (*Id*., 1:62-63; FIG. 3.)  A POSITA would have known that a potentiometer is a variable resistor.  Adjusting the resistor in the resistor-voltage-

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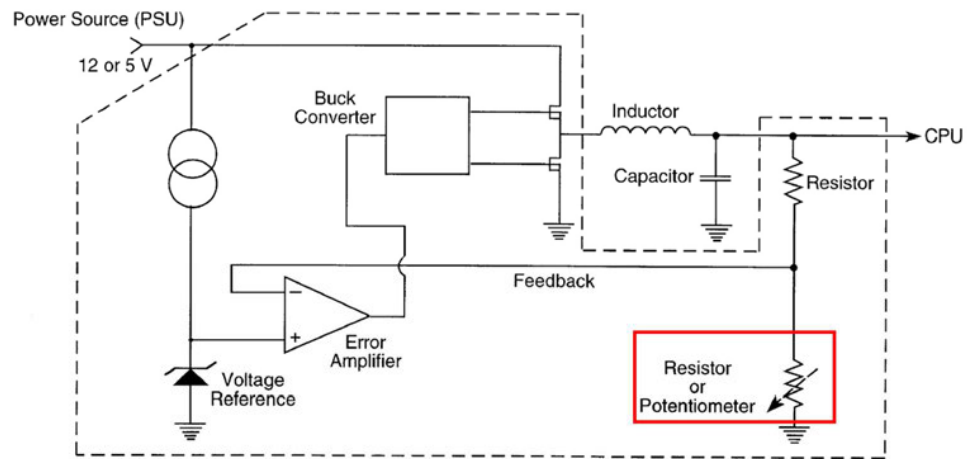divider results in adjusting the regulator's output voltage.



Fig. 3 (Prior Art)

(*Id.*, FIG. 3.)

182.   Kikinis further states:

FIG. 2 shows a switching voltage regulator 11 with an erasable
EPROM (E2) 13 that holds a coefficient for feedback loop voltage
regulation. To **adjust the output** value of the regulator, a serial **data
stream can be clocked into a register 15** until the desired value is
obtained. At this point, that value can be stored in the E2 by means of
a line not shown. The stored value can be read permanently and is
easily changed again, if required, without manual adjustment.

In FIG. 4 the potentiometer of FIG. 3 is replaced by an **external E2
19 and an R-ladder 21 to adjust the output voltage**. **Data** and clock
**values are input to register 23** upon system initialization.

(*Id.*, 2:52-64; FIG. 4.)

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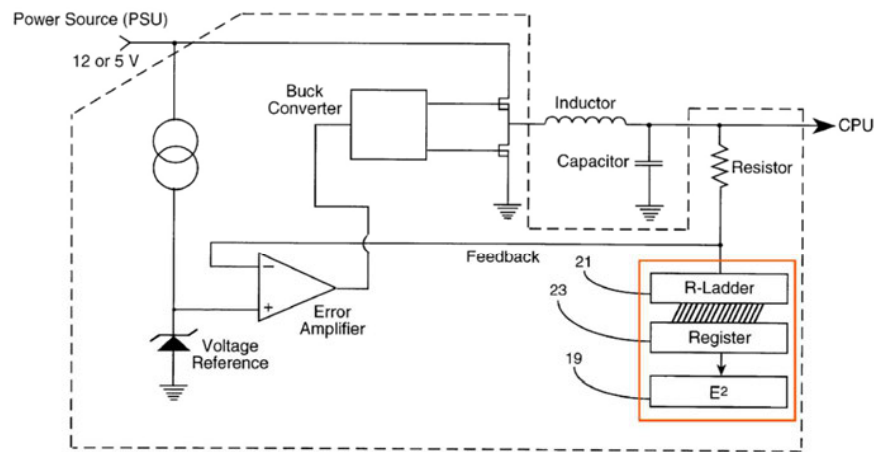U.S. Patent No. 7,260,731



Fig. 4

(*Id.*, FIG. 4.)

183.   In addition, with reference to FIG. 5 Kikinis discloses an enhancement

of the circuitry of FIG. 4 in which:

> Voltage regulator 25 receives a **prewarning based on a wake-up
> mechanism 27**. Signals on interrupt lines (NMI. INT, SMI) to CPU
> 29 are sensed and combined with some logic (e.g., PAL). The
> resulting lines send a **warning on path 31 to voltage regulator 25** of
> imminent activity by the CPU, with dramatically increased current
> requirements. Thus the **voltage regulator can take countermeasures
> in anticipation of CPU activity**.

(*Id.*, 3:6-13; FIG. 5.)

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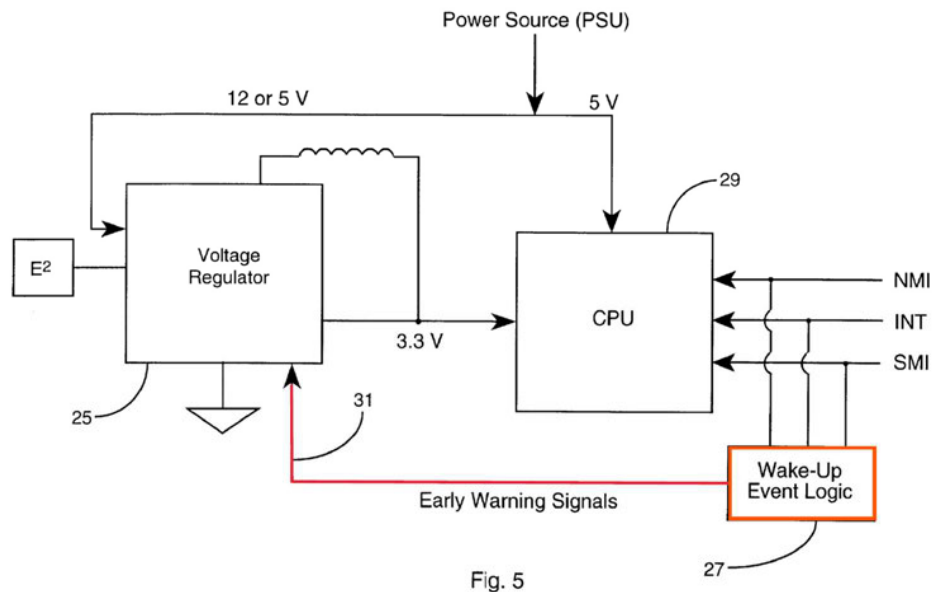


Fig. 5

(*Id.*, FIG. 5.)

184. Claim 1 of Kikinis recites: "the voltage magnitude at the regulated output may be **raised or lowered** by resetting the digital value in the digital register and transferring the digital register value to the programmable non-volatile memory; wherein the **digital value controls a resistor ladder (R-ladder) to manage feedback voltage** to the adjustment circuitry." (*Id.*, 3:49-59; *see id*. 3:31-59 (Claim 1).) As such, a POSITA would have understood that the register 23 may have a default (or reset) value and a programmed value, both stored in the EEPROM 19, where the R-ladder 21 can be controlled according to the default and programmed values to raise or lower the output voltage of the regulator.

### 6. Helms (Ex.1010)

185. U.S. Patent No. 6,748,545 to Helms et al. ("Helms") was filed on July

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24, 2000, before the October 23, 2000 priority date of the '731 patent. I am

informed and understand that Helms is prior art under 35 U.S.C. § 102(e).

186. Helms discloses a "DC/DC converter," (a voltage regulator) supplying

regulated voltages to a processor, where a particular supply voltage is selected via

a selection circuit that receives two inputs indicating an operating voltage and a

sleep voltage. In particular, Helms states:

> [A] system includes a DC/DC converter, a processor, and a selection
> circuit. The DC/DC converter receives a voltage setting signal or
> signals from the selection circuit and provides an adjustable power
> output signal having a voltage indicated by the voltage setting signal.
> The processor is powered by the adjustable power output signal.

(Ex.1010, Abstract.)

187. Helms further states:

> FIG. 1 shows a processor receiving a power supply voltage signal
> (CPUVCC) from a programmable voltage converter (DC/DC). The
> converter receives power (in this case +5V) and a voltage setting
> signal (MVID), and provides a regulated output voltage at the level
> indicated by the voltage setting signal. Because it is desirable to
> provide the system with a power-saving mode in addition to the
> normal operating mode, the voltage setting signal has two possible
> values: SVID for "sleep" mode and OVID for "operating" mode. A
> multiplexer (VID MUX) selects between these two voltage settings in

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response to a mode control signal (CPUSTOP#) which may be

provided from the south bridge.

(Ex.1010, 2:42-54.)
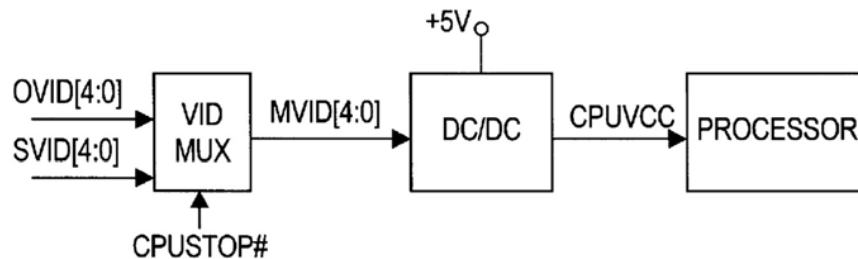


FIG. 1

(*Id.*, FIG. 1.).

188.    Thus, Helms discloses using a multiplexor to select either an

operating voltage value (OVID) or a sleep voltage value (SVID).  The selected

value (now MVID) is supplied to the DC/DC converter (an adjustable-output

voltage regulator), so that the DC/DC converter can supply the specified voltage to

a processor.  (Ex.1010, 2:42-54.)

189.    Helms also states: "One example of a programmable voltage

converter is a **MAXIM MAX1711** High-Speed, Digitally Adjusted Step-Down

Controller or its equivalent."  (*Id.*, 3:18-20.)  Additionally, Helms describes the use

of its techniques in connection with processors such as "AMD's K6-III and **Athlon**

**processors**."  (*See Id.*, 3:57-61 ("It is desirable to provide processors such as

upcoming versions of AMD's K6-III and **Athlon processors** with voltage

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identification (VID) output signals that they will drive to the DC/DC converter that

supplies their operating voltage.").)

### 7. Maxim-165X-Datasheet (Ex.1011)

190. I am informed and understand that Maxim Integrated, Inc., "High-

Efficiency, PWM, Step-Down DC-DC Controllers in 16-Pin QSOP, MAX1652–

MAX1655," Rev. 1 (Jul. 1998) ("Maxim-165X-Datasheet") published in 1998,

more than one year before the priority date of the '731 patent of October 23, 2000.

I am further informed and understand that Maxim-165X-Datasheet is prior art to

the '731 patent under at least 35 U.S.C. § 102(a) and (b).

191. Maxim-165X-Datasheet discloses voltage regulators that can be

operated in two modes, namely the pulse-width modulation (PWM) mode and

pulse-frequency modulation (PFM) mode. Specifically, Maxim-165X-Datasheet

states: "The MAX1652–MAX1655 are high-efficiency, pulse-width-modulated

(PWM), step-down DC-DC controllers," *i.e.*, *voltage regulators*. (Ex.1011 at 1,

col. 1.) Maxim-165X-Datasheet also describes two modes of operation, PWM and

PFM, as follows:

> These devices automatically switch between [pulse-width modulation]
> **PWM operation at heavy loads** and pulse-frequency-modulated
> **(PFM) operation at light loads** to optimize efficiency over the entire

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output current range. The MAX1653/MAX1655 also feature logic-

controlled, **forced PWM operation** for noise-sensitive applications.

(*Id.*)

192.   Maxim-165X-Datasheet further states: "Under heavy loads, the

controller operates in **full PWM mode**" and that if "the load is light in **Idle Mode**

($\overline{\text{SKIP}}$ = low)," "the controller **skips** most of the oscillator pulses" in the PFM

mode.  (*Id.* at 12, col. 1.)  Maxim-165X-Datasheet also states: "Light-load

**efficiency is enhanced by** automatic idle-mode operation—**a variable-frequency**

**pulse-skipping mode** that reduces losses due to MOSFET gate charge."  (*Id.* at 10,

col. 2.)

193.   Maxim-165X-Datasheet refers to the PWM mode as "**continuous-**

**conduction mode**."  (*See id.* at 12, col. 2 ( "If the circuit is operating in

**continuous-conduction mode**, the DL drive waveform is simply the **complement**

of the DH high-side drive waveform (with controlled dead time to prevent cross-

conduction or 'shoot-through.').").)  The DH and DL drives refer to the high-side

and low-side FET drives, respectively. (*See id.* at 9, Table: Pin Description

(describing DH and DL).)  Maxim-165X-Datasheet also describes that it is the

PWM operation in which the drives DH and DL operate in a complementary

manner.  (*See id.* at 12, col. 1 (stating that "in full PWM mode" as "the high-side

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switch turns off, the synchronous rectifier latch is set" and that "60 ns later the

low-side switch turns on.")

194. Moreover, Maxim-165X-Datasheet refers to the idle or pulse-skipping

mode that may be employed when the load is a light as "discontinuous-conduction

mode," (*see id.* at 16 (stating that "[r]inging may be seen at the high-side MOSFET

gate (DH) in **discontinuous-conduction mode (light loads)**"), and the mode in

which PWM operation is forced, as the "low-noise mode." (*See id*. at 16, col. 2.)

195. Maxim-165X-Datasheet also describes a forced transition from the

pulse-skipping PFM mode to the PWM mode when the load is light. In particular,

Maxim-165X-Datasheet states: "The MAX1653 and MAX1655 can reduce

interference due to switching noise by ensuring **a constant switching frequency**

**regardless of load** and line conditions." (*Id*. at 16, col. 2.) To this end, Maxim-

165X-Datasheet states that forcing the "low noise mode ($\overline{\text{SKIP}}$ = high)" "ensures

continuous inductor current flow" "allowing the **inductor current to reverse at**

**very light loads**." (*Id*. at 16, col. 2 – 17, col. 1.)

196. By employing the PWM mode during a voltage transition, charge

sharing between the output capacitor and the regulator's power source (*e.g.*, the

battery) and/or the input capacitor is facilitated. The stored charge can be reused

later, which can save power by minimizing power loss that would otherwise occur

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due dissipation of such charge in the load during a high-to-low voltage transition.

### 8. MAX1711-Kit (Ex.1012)

197. I am informed and understand that Maxim Integrated, Inc.,

"MAX1711 Voltage Positioning Evaluation Kit," Rev. 1 (June 2000) ("MAX1711-

Kit") first published in September 1998, before the October 23, 2000 priority date

of the '731 patent. I am further informed and understand that MAX1711-Kit is

prior art to the '731 patent under at least 35 U.S.C. § 102(a) and (b)

198. MAX1711-Kit (Ex.1012) discusses Maxim's MAX1711 voltage

regulator. This regulator is also discussed in "High-speed, Digitally Adjusted step-

down controllers for notebook CPUs" (Ex.1045) that was used by the Examiner

during prosecution of the '731 patent in rejecting then pending claims 4, 12, 14-17,

and 18 (issued as claims 4, 13, 15-18, and 5, respectively). (*See* Ex.1004 at 354,

466.) MAX1711-Kit was not cited during prosecution. In this Petition, it is used

for claims 8-11 and 14; not for claims 4-5, 13, and 15-18. Also this Petition relies

on the discussion of the operating modes of MAX171X regulators in MAX1711-

Kit – an aspect not discussed during prosecution. (*See generally*, Ex.1004.)

199. MAX1711-Kit describes a voltage regulator similar to those that

Maxim-165X-Datasheet discloses, *i.e.*, a voltage regulator that can be operated in

PWM or PFM modes, and where the PWM operation may be forced, and a

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particular use of forcing the PWM mode to save power.

200. In particular, MAX1711-Kit describes a "buck-regulator" (*i.e.*, a step-down voltage regulator) (*see* Ex.1012 at 2, col. 2), that can be operated in PWM or PFM modes, and where the **PWM mode can be forced via the $\overline{\text{SKIP}}$ input**. (*See id*. at 3, col. 2.)

201. In discussing forced PWM operation, MAX1711-Kit states:

> **Transitions to a lower output voltage require the circuit or the load to sink current**. If $\overline{\text{SKIP}}$ is held low (PFM mode), the **circuit won't sink curren**t, **so the output voltage will decrease only at the rate determined by the load current**. This is often acceptable, but some applications require output voltage transitions to be completed within a set time limit.

(Ex.1012 at 3, col. 2.)

202. MAX1711-Kit further states: "The simplest way of meeting this requirement is to **use the MAX1711's fixed-frequency PWM mode (set $\overline{\text{SKIP}}$ high), allowing the regulator to sink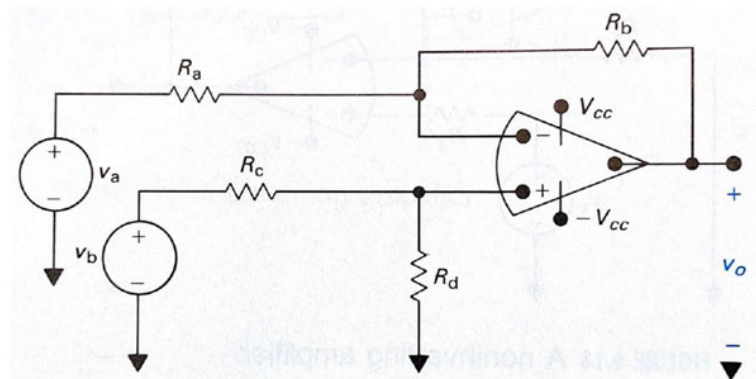** or source **currents equally**. (*Id*.) MAX1711-Kit also states: "A similar but **more clever approach is to use PWM mode only during transitions**. This approach **allows the regulator to sink current when needed and to operate with low quiescent current the rest of the time**." (*Id*. at 4, col. 1.)

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### 9. Nilsson (Ex.1013)

203. I am informed and understand that James W. Nilsson, "Electronic

Circuits," (Addison Wesley, 4th ed.) (1993) ("Nilsson") published in 1993, before

the October 23, 2000 priority date of the '731 patent. I am further informed and

understand that Nilsson is prior art to the '731 patent under at least 35 U.S.C. §

102(a) and (b).

204. Nilsson discloses an operational amplifier configuration for a

difference amplifier. (*See* Ex.1013 at 200.) In Nilsson's disclosed configuration,

the output voltage of a difference amplifier is proportional to the difference

between two input voltages. (*Id.*.) Specifically, Nilsson describes a resistor-

voltage-divider-based feedback circuitry, having resistors $R_a$ and $R_b$, used to

regulate the output voltage of a difference amplifier. (*Id.* (Figure 6.14).) Nilsson's

configuration includes two voltage sources $v_a$ and $v_b$. (*Id.*)



**FIGURE 6.14** A difference amplifier.

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(Ex.1013 at 200 (Figure 6.14).)

**B.** **GROUND 1: Claims 1, 3, 6, and 7 Are Unpatentable as Obvious Over NEC-Databook in View of Burd, further in View of the Knowledge of POSITA**

**1.** **Motivation to Combine NEC-Databook and Burd**

205. A POSITA would have been motivated to combine NEC-Databook

and Burd because a POSITA would have readily recognized and appreciated

several benefits of this combination, as described below.

**a.** **NEC-Databook and Burd disclose optimization techniques in the same field**

206. As a threshold matter, NEC-Databook and Burd both disclose

techniques in the same field of optimizing power/energy consumption of

processors because NEC-Databook discloses a processor that can be operated at

different frequencies and corresponding voltages, to save power, and Burd

discloses dynamically adjusting operating voltages and frequencies. In particular,

NEC-Databook discloses several microcomputer families including the

µPD751XX/75P1xx family, where the CPU therein can be operated at different

voltages and frequencies (*i.e.*, clock speeds) to save power/energy consumption.

(*See* Ex.1005 at 31 (disclosing that the operating voltage ranges from 2.7 to 6.0 V),

35 (disclosing that the CPU can be operated at three different cycle times, *i.e.*, at

three different operating frequencies), and 62 (disclosing an guaranteed operating

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range of operating voltages and cycle times (operating frequencies).)

207. NEC-Databook also discloses that its CPU can be placed in different "standby" modes (also understood as sleep states) where in a mode called the "Data Retention mode" the CPU's static power/energy consumption can be reduced while maintaining its data and state by lowering the supply voltage to 2 V. (*See id*. at 47-48 (describing the standby modes including the Data Retention mode within the STOP mode, and retained data), 32-33 (describing the data memory that is retained), and 42 and 44 (disclosing that stopping the system clock in the Data Retention mode stops the CPU clock).)

208. Before 2000, dynamically adjusting the operating voltages and frequencies of a processor, to save power/energy, was an area of active research. Burd, for instance, discloses a processing system in which a processor that can be operated at different voltages and frequencies is supplied with different voltages using a voltage regulator that can dynamically adjust its output voltage, so as to decrease the power/energy consumption of the processor. (*See* Ex.1006 at 1-2, 2 (Figures 17.4.2 and 17.4.3 (describing and depicting a system employing dynamic voltage scaling (DVS), where the system includes a switching regulator supplies dynamically adjusted voltages to a processor, to save power/energy)).)

209. As such, NEC-Databook and Burd both disclose techniques in the

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same field of optimizing power/energy consumption of processors by dynamically

adjusting operating voltages and frequencies. Furthermore, a POSITA would have

readily recognized that Burd's voltage regulator can be beneficially used with the

microcomputer that NEC-Databook discloses, so that the CPU disclosed in the

NEC-Databook can be operated at different voltages as needed, to save power

and/or energy.

> **b.  Burd's switching regulator (voltage regulator) can supply different voltages to the CPU that NEC-Databook discloses**

210. While the CPU of the μPD751xx family that NEC-Databook discloses

(referred to as the μPD751xx-CPU) is different from the processor that Burd

discloses, particularly in terms of the operating voltages and corresponding

frequencies, as noted below, a POSITA would have understood these processors to

be sufficiently similar, so that Burd's regulator can be readily used to supply and

adjust the required voltages to the μPD751xx-CPU.

211. Specifically, Burd discloses a "microprocessor [that] operates from

1.2-3.8V and 5-80 MHz." (Ex.1006 at 1, col. 1; *see id*., col. 2 (describing an ARM

processor).) Burd also discloses a "switching regulator" (*see id*. , col. 1), also

referred to as a "dc-dc converter" that supplies voltages in the range 1.2-3.8V. (*see*

*id*. at 1, col. 2; 2, Figures 17.4.2 and 17.4.3.)

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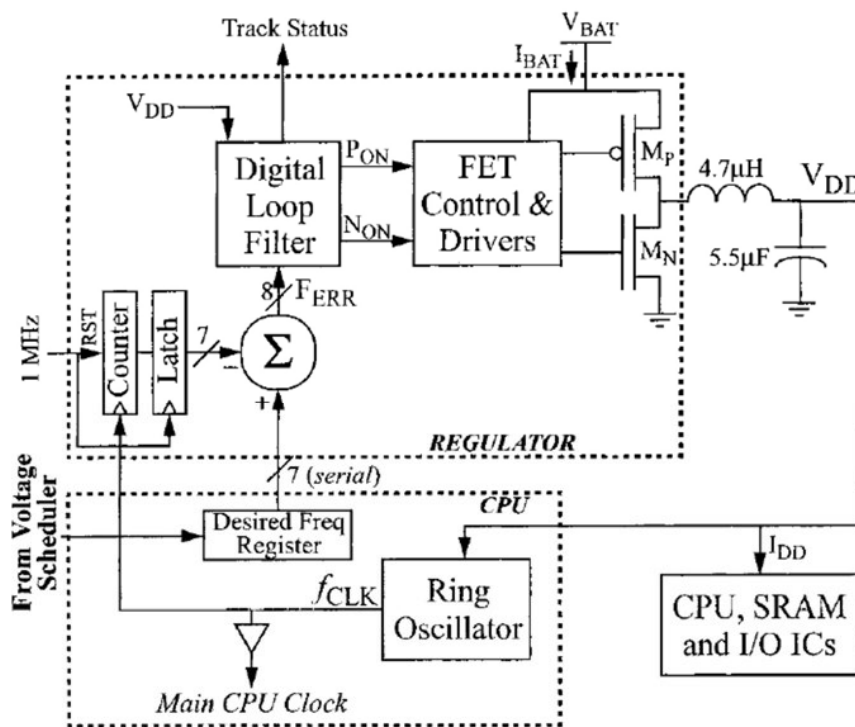Petition for *Inter Partes* Review of
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**Figure 17.4.2: Frequency to voltage feedback loop.**

(*Id*. at 2, Figure 17.4.2.)

212. NEC-Databook discloses that, similar to Burd's processor, the

μPD751xx-CPU can also be operated at different frequencies, to reduce power.

For example, NEC-Databook states:

> The minimum instruction execution time is 0.95 μs with a 4.19 MHz
> clock. The PCC register can be used to program the CPU's minimum
> instruction cycle time to 0.95, 1.91, or 15.3 μs; **all three speeds**
> presuppose a 4.19 MHz crystal. **Reducing the CPU clock speed will**
> **reduce the microprocessor's power consumption**.

(Ex. 1005 at 35, col. 1; *id*., col. 2 (stating that the "PCC selects **one of four**

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**available CPU cycle speeds**"); *see id*. at 24 (describing "High-speed cycle" time

of "0.95 μs" and "Lower-voltage cycles" of "1.91 and 15.3 μs" periods).) These

instruction cycle times correspond to operating frequencies in the range of

approximately 654 kHz-1.052 MHz.

213.    Moreover, the μPD751xx-CPU can be operated at different voltages.

NEC-Databook discloses the "[o]perating voltage range" of several

microcontrollers in the μPD751xx family as 2.7 to 6.0 V. (Ex.1005 at 31 (Table

"Product Comparison").)

**Product Comparison**

| Item | μPD75104/104A | μPD75106 | μPD75108/108A | μPD75P108 | μPD75112 | μPD75116 | μPD75P116 |
|---|---|---|---|---|---|---|---|
| Power-on-reset circuit and power-on flag | Mask option | Mask option | Mask option | Internally provided | Mask option | Mask option | Not included |
| Operating voltage range | 2.7 to 6.0 V | 2.7 to 6.0 V | 2.7 to 6.0 V | 5 V ± 10% | 2.7 to 6.0 V | 2.7 to 6.0 V | 5 V ± 10% |
| Package | See ordering information for a complete list of packages | | | | | | |

214.    A POSITA would have understood that the range of operating

voltages for the microcontrollers applies to the μPD751xx-CPUs therein, because

Figure 17 in NEC-Databook depicts a relationship between "Power Supply

Voltage" and "Cycle Time" in the Guaranteed Operating Range, (*see id*. at 62

(Figure 17 (annotated))), where the power supply voltage $V_{DD}$, that a POSITA

would have understood is supplied to the μPD751xx-CPU, ranges from 2.7 to 6.0

V.

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Figure 17. Guaranteed Operating Range (μPD751xx)
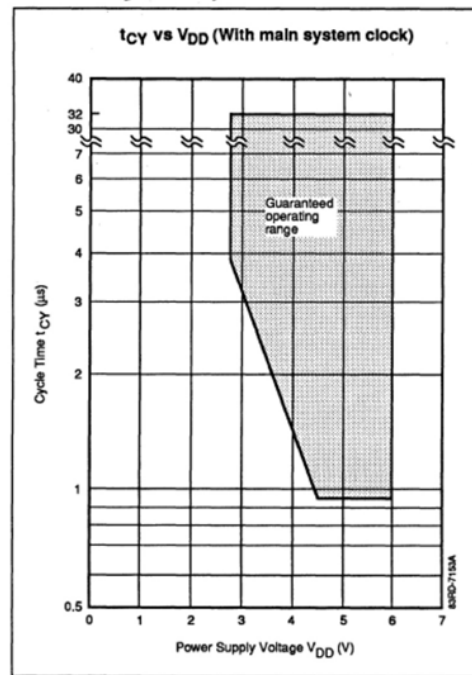
(*Id.*)

215.  Figure 17 shows different cycle times (the respective reciprocals of

which are the different operating frequencies) corresponding to different operating

voltages in the range 2.7-6 V, which includes the subrange of 2.7-3.8 V that Burd's

regulator can provide.  As such, NEC-Databook discloses a CPU that, like the

processor that Burd describes, can be operated at different frequencies and at

voltages, *e.g.*, voltages ranging from 2.7 to 3.8 V that Burd's regulator can provide,

to save power/energy at lower voltages and frequencies or to increase performance

at higher voltages and frequencies.

216.  A POSITA would have also understood that although for the regulator

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that Burd describes the voltage range of 1.2 to 3.8 V corresponds to the operating

frequency range of 5-80 MHz of Burd's processor, Burd's regulator does not

mandate this association between voltages and frequencies.  In other words, a

POSITA would have understood that even though a processor employing dynamic

voltage-frequency scheduling (DVFS) may require a particular supply voltage to

correspond to a particular operating frequency, Burd's regulator (any voltage

regulator supplying multiple output voltages, in general) can be used to supply

voltages to any processor, **regardless of that processor's voltage-frequency**

**association**.

217.   A POSITA would have known this to be true as long as the voltages

required by the processor fall within the range of voltages Burd's regulator is

designed to provide.  The reason is different circuitry, such as the "clock

generator" that NEC-Databook discloses (*see* Ex.1005 at 42 and 44 (Figure 5)),

can operate independently of Burd's regulator and can supply to the µPD751xx-

CPU the different frequencies corresponding to the different voltages supplied by

Burd's regulator.

218.   As such, a POSITA would have known that any voltage output by

Burd's regulator can be associated with any allowed operating frequency specified

for a processor to which the regulator supplies voltages, or even with no operating

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frequency at all.  Accordingly, a POSITA would have understood that Burd's

regulator can be readily controlled to adjust dynamically its output voltage to

correspond to an operating frequency within a different range of frequencies from

that Burd describes, such as those at which the µPD751xx-CPU can be operated, or

even to output one or more voltages that do not correspond to any operating

frequencies at all, *e.g.*, to supply 2 V, when the µPD751xx-CPU is in the Data

Retention mode, where its clock is stopped.

219.   In particular, a POSITA would have understood that Burd's system

can be readily modified and controlled to provide different regulated voltages to

the CPU of NEC-Databook, as discussed below with reference to Burd's modified

Figure 17.4.2.

220.   As a threshold matter, Burd's "digital loop filter" adjusts the output

voltage in the range 1.2-3.8 V corresponding to frequencies in the range 5-80

MHz.  (Ex.1006 at 1, col. 1.)  Therefore, assuming a linear relationship[7] between

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[7] Although a linear relationship is assumed, because it is likely, the discussion

herein applies to other relationship as well.  A POSITA would have understood

that the actual relation can be readily derived by simply observing several different

output voltages and corresponding frequencies.

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the voltage and frequency, the output voltage ($v$) – frequency ($f$) relationship can

be expressed as: $v = 0.035 \cdot f + 1.03$. A voltage of 2.0 V is the minimum data

retention voltage for the µPD751xx-CPU. (*See* Ex.1005 at 47, col. 2, 64.) Based

on its voltage-frequency relationship, Burd's digital loop filter would adjust the

output voltage to approximately 2 V at a presumed desired operating frequency of
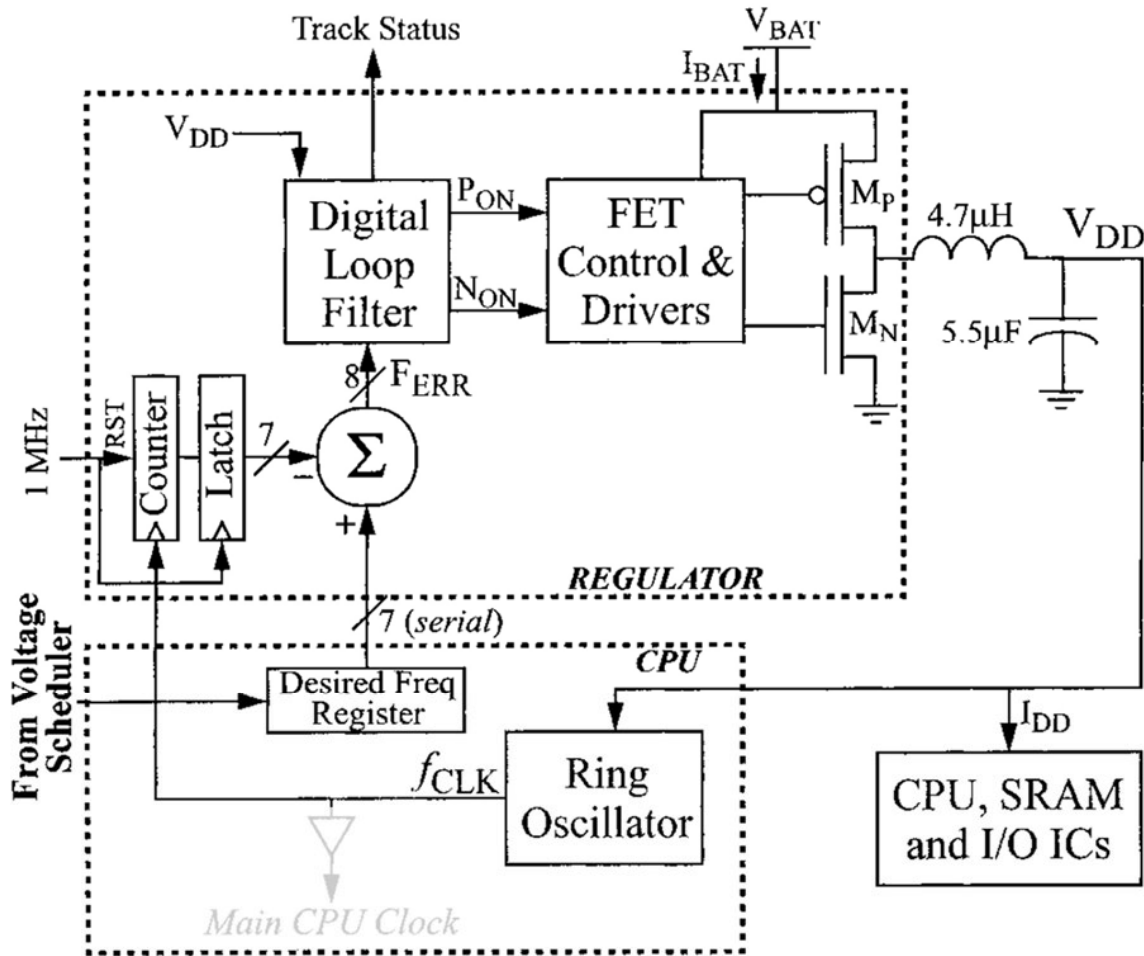
approximately 28 MHz.

221. Therefore, a POSITA would have understood that, if the 7-bit value

provided to Burd's "Desired Freq Register" is that corresponding to 80 MHz, *e.g.*,

"1010000," the converter would output a regulated voltage of approximately 3.8 V.

A POSITA would have further understood that, if the 7-bit value provided to the

"Desired Freq Register" is that corresponding to 28 MHz, *e.g.*, "0011100," Burd's

digital loop filter would cause the converter to lower its output voltage from

approximately 3.8 V to approximately 2.0 V. Likewise, a POSITA would have

understood, that if the 7-bit value provided to the "Desired Freq Register" is

changed again to correspond to 80 MHz ("1010000"), the converter would raise its

output voltage to approximately 3.8 V.

222. A POSITA would have also understood that in all the cases above, the

actual frequency at which the processor receiving the regulated voltage may be

operated need not be 80 or 28 MHz and, instead, can be any frequency specified

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for the processor, or at no frequency at all. In particular, a POSITA would have

understood that in a system in which Burd's controller is to be used to supply

regulated voltages to the µPD751xx-CPU that NEC-Databook discloses, this can

be accomplished in a straightforward manner, simply by not using Burd's "Ring

Oscillator" to supply clock to the µPD751xx-CPU and, instead, using another

clock source such as the µPD751xx-CPU's own crystal oscillator or another

external clock. (*See id*. at 42, 44 (Figure 5), 54 (Table "Oscillator

Characteristics"), 55 (Figures 15A and 15B).)

223. As such, a POSITA would have understood that Burd's system can be

modified merely to disconnect or eliminate the clock buffer supplying a clock

signal generated by the "Ring Oscillator" to the CPU. This is shown below in the

modified Figure 17.4.2, where the clock buffer and its output are grayed-out.

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**Figure 17.4.2: Frequency to voltage feedback loop.**

(Ex.1006 at 2 (Figure 17.4.2 (modified)).)

224. In the modified system, instead of deriving the clock signal for the

$\mu$PD751xx-CPU from the voltage $V_{DD}$ supplied thereto (using the Ring Oscillator),

the clock to the $\mu$PD751xx-CPU may be provided using the "clock generator" that

NEC-Databook itself discloses. (*See* Ex.1005 at 42, cols. 1-2, 44 (Figure 5)).)

When the STOP instruction is to be issued, causing the $\mu$PD751xx-CPU to

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transition to the STOP mode (*see id*. at 42, col. 1), an 8-bit value of "11001100,"

*i.e.*, $F_{ERR}$ = -52, may be provided at the 8-bit input of the digital loop filter.

Conversely, when the STOP mode is to be released, e.g., using the "standby

release signal" in response to an interrupt request, (*see id*. at 65 (Figure 19B)), an

8-bit value of "00110100," *i.e.*, $F_{ERR}$ = 52, may be provided at the 8-bit input of the

digital loop filter.

225. Furthermore, a POSITA would have understood that the status of

PTO0, PTO1, and/or PCL signals can indicate that the μPD751xx-CPU has entered

the STOP mode, and that such status can be used to adjust the output voltage of

Burd's regulator by supplying a desired frequency to the "Desired Freq Register."

(*See* Ex.NEC-Databook at 47, col. 1 (disclosing the "STOP" mode); 29, col. 2

(disclosing the signals PTO0, PTO1, and PCL); 42, col. 1, 44 (Figure 5), 45

(Figure 7), 48 (Table 7) (disclosing and depicting circuitry generating these signals

and controlling them in the STOP mode)

226. A POSITA would have recognized this modification of Burd's

regulator ("*voltage regulator*") to be straightforward, as nothing more than

eliminating a circuitry component and an associated path, and providing certain

binary values as required, which are circuitry configuration activities that a

POSITA would have routinely performed. Using the modified regulator, a voltage

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of 3.8 V may be provided as an operating voltage, and a voltage of 2.0 V may be

provided when the CPU clock is stopped and the µPD751xx-CPU is in the Data

Retention mode.

        c.      **A POSITA would have understood that the NEC-Databook and Burd combination was straightforward and would yield predictable benefits**

227.   In light of the fact that Burd's regulator can readily supply different

regulated voltages to the µPD751xx-CPU disclosed in NEC-Databook, a POSITA

would have recognized and appreciated the predictable benefits of combining the

teachings of these two references.  First, a POSITA would have recognized that

even though NEC-Databook discloses operating voltages in the range 2.7 to 6 V,

and a data retention voltage as low as 2 V, NEC-Databook does not explicitly

disclose an adjustable voltage regulator that can supply such voltages.  A POSITA

would have known that unless the voltages and frequencies supplied to the

µPD751xx-CPU are adjusted as needed, *e.g.*, based on its work load, the potential

of power/energy saving would not materialize.

228.   Burd's regulator can adjust its output voltage dynamically in the range

1.2 to 3.8 V.  As such, a POSITA would have understood that Burd's regulator can

be coupled to a microcontroller of the µPD751xx family, so as to supply

dynamically adjusted voltages in the subrange 2.0 to 3.8 V to the µPD751xx-CPU

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that would allow the CPU to be operated at a voltage of 3.8 V and to allow the

CPU to enter the Data Retention mode at 2.0 V, so as to save power/energy. A

POSITA would have recognized that such a configuration can thus predictably

yield the benefit of achieving the power/energy saving potential of a μPD751xx

family microcontroller. In particular, a POSITA would have understood that

coupling Burd's regulator to the μPD751xx-CPU can minimize its static

power/energy consumption, *i.e.*, power/energy consumption when the clock to the

μPD751xx-CPU is turned off.

229. A POSITA would have known that although some power/energy

would be consumed in this case (as opposed to shutting off the μPD751xx-CPU

entirely in the STOP mode), supplying at least 2.0 V to the μPD751xx-CPU would

place it in the Data Retention mode where, upon returning to the operating mode,

the CPU can resume computations more quickly relative to the case when the CPU

is shut off. Thus, a POSITA would have understood that coupling Burd's regulator

to the μPD751xx-CPU can decrease its static power consumption, while also

avoiding excessive delays and energy consumption in transitioning the μPD751xx-

CPU from the STOP mode to the operating mode.

230. To a POSITA, this combination would have been nothing more than

combining prior art elements according to known methods (coupling a power

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supply or a voltage regulator to a processor), or simple substitution of one known

element for another (Burd's regulator for another voltage regulator used with the

μPD751xx-CPU), to obtain the predictable results described above.

231.   A POSITA would have also understood this combination to be the use

of a known technique (dynamic adjustment of voltages supplied to a processor, as

Burd describes) to improve a system employing a similar technique (a

microcontroller of the μPD751xx family that NEC-Databook discloses) in a similar

way as Burd describes, or applying a known technique (described above) to a

known system (NEC-Databook's) that is ready for improvement, *e.g.*, by using a

dynamically adjustable voltage regulator, to yield predictable results described

above.

232.   Additionally, a POSITA would have understood that these

predictable, beneficial results can be obtained without requiring substantial

changes or modifications to either the microcontroller of the μPD751xx family that

NEC-Databook or Burd's regulator, and without adversely affecting the operation

of these systems or components.  A POSITA would have also been able to apply

known, conventional circuitry configuration techniques to perform the necessary

modifications.  As such, a POSITA would have expected the combination of NEC-

Databook and Burd to succeed.  For these reasons, it would have been obvious to a

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POSITA to combine NEC-Databook and Burd.

### 2. Independent Claim 1

#### a. Element 1[pre] "A method for reducing power utilized by a processor comprising the steps of:"

233. To the extent it is limiting, NEC-Databook teaches a "*method for reducing power utilized by a processor*" because NEC-Databook describes "a family of high-performance single-chip CMOS microcomputers containing CPU" ("*a processor*") and other components where the microcomputer system can be operated in a "standby mode" in which the CPU clock is stopped and the voltage to the CPU may be lowered to "reduce [its] power consumption," *i.e.*, "*reducing power utilized by* [the] *processor*."

234. Specifically, the NEC-Databook states: "µPD751xx/P1xx is a family of high-performance single-chip CMOS microcomputers containing CPU, ROM, RAM, I/O ports, comparator, interval timer, two timer/counters, vectored interrupts, and a serial interface." (Ex.1005 at 24, col. 1.) The CPU of the µPD751xx/P1xx family (referred to hereinafter as the "µPD751xx-CPU"), is a central processing unit, *i.e.*, processor. In fact, NEC-Databook refers to the µPD751xx as a "microprocessor." (*Id*. at 35, col. 1 ("Reducing the CPU clock speed will reduce the microprocessor's power consumption."))

235. The total power consumed by a processor includes dynamic power

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consumption (when the processor clock is running) and static power consumption

(regardless of whether the processor clock is running or stopped).  NEC-Databook

describes a "standby mode" that "consists of three submodes, HALT, STOP, and

Data Retention." (*Id*. at 47, col. 1.)  NEC-Databook further states that in the

"HALT mode" "the clock to the CPU is shut off (thus stopping the CPU), while all

other parts of the chip remain fully functional" and that in the "STOP mode" "the

chip's main system oscillator is shut off, thereby stopping all portions of the chip."

(*Id*.)  Stopping the clock to the CPU or shutting of the main system oscillator

avoids dynamic power consumption by the CPU, which reduces the overall CPU

power consumption.

236.   In addition, NEC-Databook states that the "Data Retention mode"

"may be entered after entering the STOP mode.  Here the supply voltage $V_{DD}$ may

be lowered to 2 volts to **further reduce power consumption**." (*Id*. at 47, col. 2.)

In this case, the CPU's static power consumption is reduced, which reduces further

the overall CPU power consumption.

237.   As such, NEC-Databook teaches the preamble of claim 1.

> b.    **Element 1[a]: "determining that a processor is
> transitioning from a computing mode to a mode in
> which a system clock to the processor is disabled,
> and"**

238.   NEC-Databook teaches "*determining that a processor is transitioning*

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*from a computing mode to a mode in which a system clock to the processor is*

*disabled*" because NEC-Databook describes that "HALT" and "STOP"

instructions can be used to cause the μPD751xx-CPU to enter the HALT and

STOP modes, respectively, and that in these modes, the CPU clock is stopped.

NEC-Databook also discloses that an event counter is stopped in the STOP mode

and that the clock output circuit may be stopped in both STOP and HALT modes,

so that event counter outputs PTO0 and PTO1 and clock output PCL cease from

changing, and thereby indicating that the CPU clock is disabled. Therefore, the

status of the event counter outputs PTO0 and PTO1 and the clock output PCL, that

these signals are not changing, constitutes "*determining that a processor is*

*transitioning from a computing mode to a mode in which a system clock to the*

*processor is disabled*."

239. Specifically, NEC-Databook describes a "standby mode" for

operating its CPU, where the standby mode "consists of three submodes, HALT,

STOP, and Data Retention." (*Id*. at 47, col. 1.) NEC-Databook also states:

> **HALT mode. The HALT mode is entered by executing the HALT**
> **instruction.** In this mode, the **clock to the CPU is shut off (thus**
> **stopping the CPU**), while all other parts of the chip remain fully
> functional.

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> **STOP mode. The STOP mode is entered by executing the STOP**
>
> **instruction.** In this mode, the chip's main system oscillator is shut
>
> off, thereby stopping all portions of the chip.

(Ex.1005 at 47, col. 1; *see id*. at 48 (Table 7 (stating that in both HALT and STOP

modes the status of the CPU is "Operation stopped")).)

240. NEC-Databook further states that in the "HALT mode" "the clock to

the CPU is shut off (thus stopping the CPU), while all other parts of the chip

remain fully functional," and that in the "STOP mode" "the chip's main system

oscillator is shut off, thereby stopping all portions of the chip." (*Id*. at 47.)

241. Since the µPD751xx-CPU clock is generated from the main system

oscillator, (*see id*. at 42, col. 1 (describing that a "clock generator" that includes

"an oscillator" supplies "frequencies derived from [a] crystal" "to the CPU")),

shutting off the main system oscillator would also stop the CPU clock.

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**Figure 5. Clock Generator**
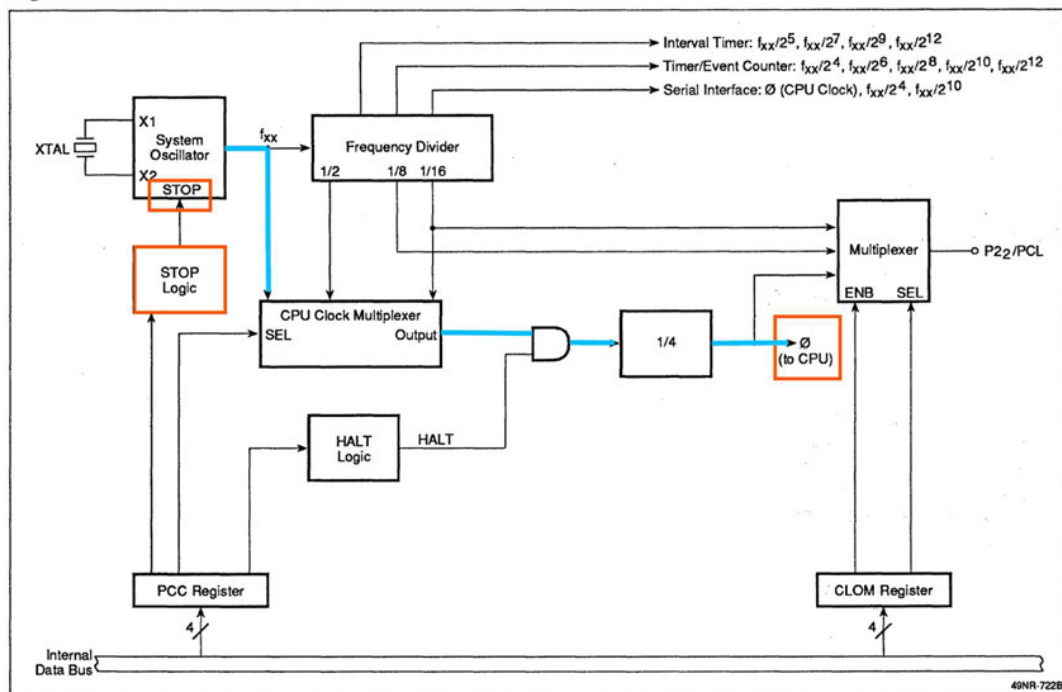


(*Id*. at 44 (Figure 5 (annotated)).)

242.   With the clock stopped, the µPD751xx-CPU cannot execute

instructions.  (*See id*. at 48 (Table 7 (stating that in the STOP and HALT modes

CPU operation is stopped)).)  Thus, a POSITA would have understood that **when**

**the µPD751xx-CPU is in the HALT or STOP modes, it is in a sleep state**,

where the clock to the CPU and CPU operation, *i.e.*, execution of instructions

(computations), are stopped, and dynamic power consumption by the µPD751xx-

CPU is avoided.  Accordingly, a POSITA would have understood that by entering

the HALT or STOP modes the µPD751xx-CPU (*processor*) "*transition[s] from a*

*computing mode to a mode in which a system clock to the processor is disabled*."

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243.   A POSITA would have further understood that one way to determine the occurrence of this transition is from the status of one or more of μPD751xx-CPU outputs, namely, PTO0, PTO1, and PCL.  NEC-Databook states: "PTO0 and PTO1 are the timer/event counter output pins; PCL is the clock output pin."  (*Id*. at 29, col. 2.)
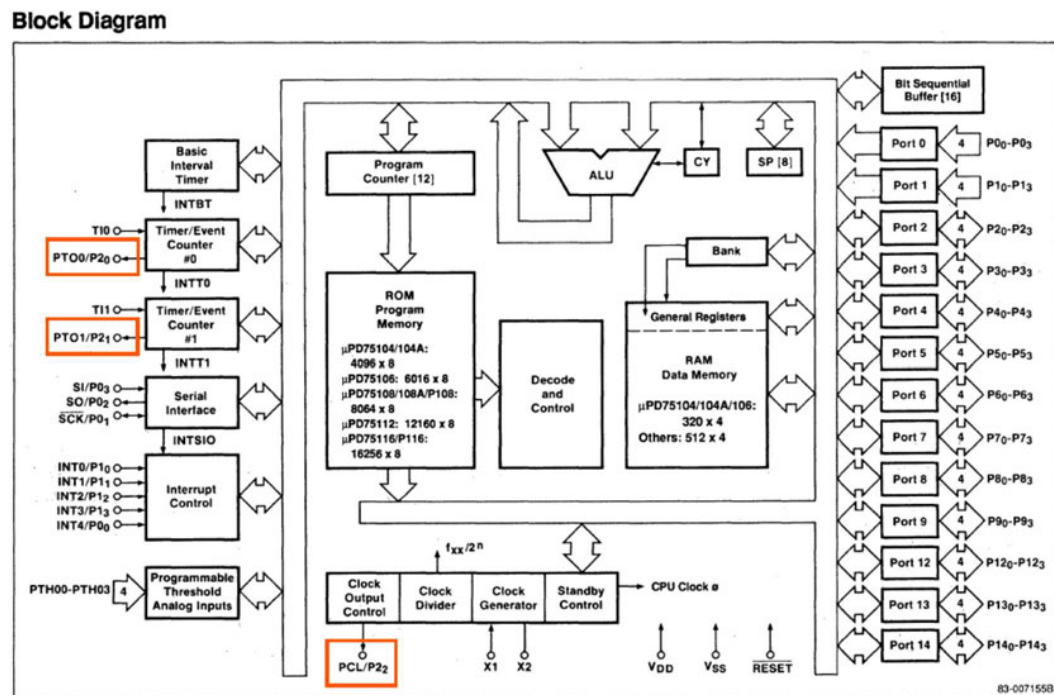


**Block Diagram**

(*Id*. at 28 (Figure "Block Diagram").)

244.   NEC-Databook also states: "By programming [registers] PCC and CLOM, **frequencies derived from the crystal are supplied to** the CPU, the interval timer, the timer/**event counter**, the serial interface, and the output **pin, PCL**."  (*Id*. at 42, col. 1.)

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**Figure 5. Clock Generator**
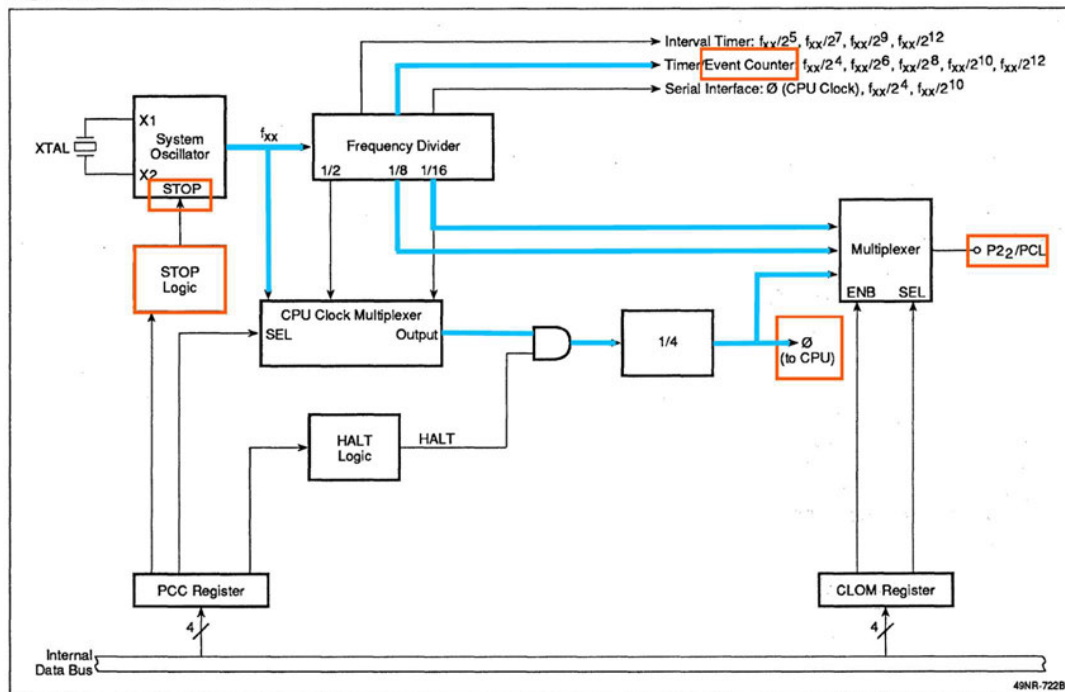


(*Id*. at 44 (Figure 5 (annotated)); *see id*. at 45 (Figure 7 (depicting event counter

circuitry)).)

245.   Thus, a POSITA would have understood that in the STOP mode,

when "the chip's main system oscillator," *e.g.*, the crystal oscillator shown in

Figure 5, "is shut off" (*see id*. at 47, col. 1), the event counter and the clock output

circuit would be stopped.  (*See id*. at 48 (Table 7 (stating the same)).)

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**Table 7. Standby Mode Operation**

| Item | STOP Mode | HALT Mode |
|---|---|---|
| Setting the mode | STOP Instruction | HALT Instruction |
| Clock oscillator | The main system clock oscillator is stopped | Only CPU clock $\phi$ is stopped (oscillation continues) |
| Basic interval timer | Operation stopped | Can Operate (IRQBT is set by reference time interval) |
| Serial interface | Can operate only when external $\overline{SCK}$ input is selected for serial clock. (Note 1) | Can operate if other than CPU clock $\phi$ is specified as serial clock |
| Timer/event counter | Can operate only when TIn (n = 0, 1) pin input is selected for count clock | Can operate |
| Clock output circuit | Stops operation | Can operate if other than CPU clock $\phi$ is specified |
| CPU | Operation stopped | Operation stopped |
| Retained data | Contents of all registers (general registers, flags, mode registers, and output latches) and contents of data memory retained | |
| Release signal | Interrupt request signal (enabled with interrupt enable flag) from operating hardware or $\overline{RESET}$ | |

(*Id*. at 48 (Table 7 (annotated)).)

246. A POSITA would further understand that with the event counter and the clock output circuit stopped, the output signals PTO0, PTO1, and/or PCL would not change. As such, a POSITA would have understood that the status of signals PTO0, PTO1, and/or PCL indicates whether the CPU clock is stopped.

247. Therefore, the status of the event counter output signals PTO0 and PTO1 and the clock output signal PCL, that these signals are not changing, constitutes "*determining that a processor is transitioning from a computing mode to a mode in which a system clock to the processor is disabled*" and , thus, NEC-Databook teaches this claim element.

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      c.      **Element 1[b]: "reducing core voltage to the processor
to a value sufficient to maintain state during the mode
in which said system clock is disabled, wherein said
value of the core voltage is not sufficient to maintain
processing activity in said processor,"**

248.   NEC-Databook teaches "*reducing core voltage to the processor to a value sufficient to maintain state during the mode in which said system clock is disabled*," because NEC-Databook states that in the STOP mode the "supply voltage $V_{DD}$ may be lowered to 2 volts" and that the "**contents of** the RAM and **registers are retained**." NEC-Databook also teaches "*wherein said value of the core voltage is not sufficient to maintain processing activity in said processor*" because NEC-Databook describes the "Operating voltage range" of a number of microcontrollers in the μPD751xx/P1xx family as 2.7-6 V, which is greater than the 2 volts supplied during the "Data Retention mode."
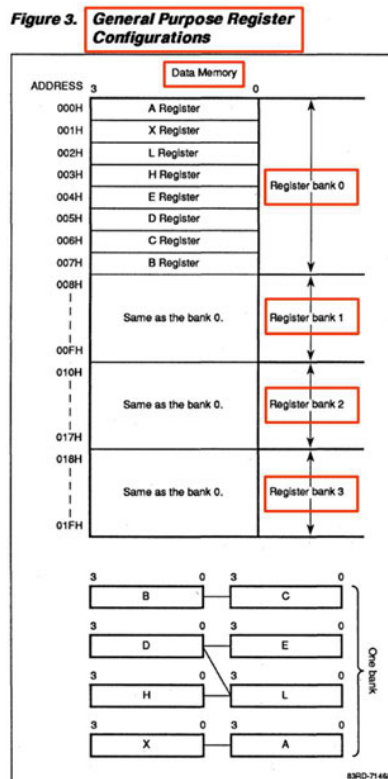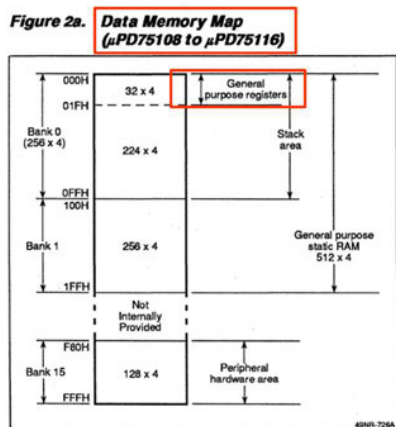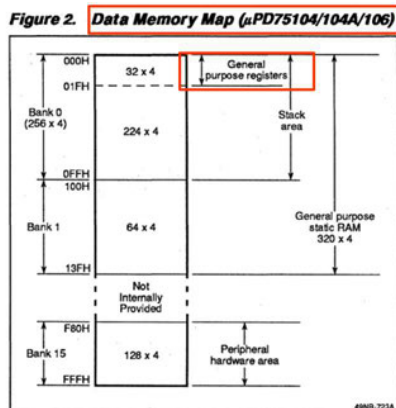
249.   First, NEC-Databook discloses that in the Data Retention mode, the contents of the general purpose registers of the μPD751xx-CPU would be retained. Specifically, NEC-Databook refers to its "data memory" as RAM, stating

**Data Memory (RAM)**

The data memory contains three memory banks, 0, 1, and 15. The RAM memory map is shown in figure 2. The **memory consists of** general purpose static RAM, **general purpose registers, and peripheral control registers**.

<div align="center">136</div>

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(Ex.1005 at 32, col. 1.)



Figure 2. Data Memory Map (μPD75104/104A/106)

Figure 2a. Data Memory Map (μPD75108 to μPD75116)

Figure 3. General Purpose Register Configurations

(*See* Ex.1005 at 33 (Figures 2, 2a, and 3 (depicting "general purpose registers" in "data memory")).)

250. NEC-Databook also states: "The **on-chip peripheral control registers** and ports **reside in** the upper 128 nibbles of **bank 1**" and that there "are four general-purpose register banks in RAM Bank 0." (*Id*. at 32.)

251. Additionally, NEC-Databook states:

The **data memory is used for storing** processed data, **general purpose registers**, and as a stack for subroutine or interrupt service.

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Because of its static nature, the **RAM will retain its data when the chip is in the STOP mode, provided V$_{DD}$ is at least 2 volts**.

(*Id*. at 32, col. 1.)

252.  Furthermore, NEC-Databook states that the "**Data Retention mode**" "may be entered after entering the STOP mode.  Here the supply voltage V$_{DD}$ may be lowered to 2 volts to **further reduce power consumption**."  (*Id*. at 47, col. 2.) Not just the CPU clock, but the system oscillator itself is shut off in the STOP mode.  (*See id*. at 47, col. 1.)

253.  It should be noted that although NEC-Databook refers to the data memory as RAM, and states that "**RAM will retain its data** when the chip is **in the STOP mode, provided V$_{DD}$ is at least 2 volts**" (*id*. at 32, col. 1), NEC-Databook also states explicitly that the memory or RAM "consists of general purpose static RAM, **general purpose registers, and peripheral control registers**."  (*Id*. at 32, col. 1; *see id*. at 48 (Table 7 (describing "**Retained data**" as "**Contents of all registers** (general registers, flags, mode registers, and output latches) and contents of data memory retained")).)

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**Table 7.   Standby Mode Operation**

| Item | STOP Mode | HALT Mode |
|---|---|---|
| Setting the mode | STOP Instruction | HALT Instruction |
| Clock oscillator | The main system clock oscillator is stopped | Only CPU clock $\phi$ is stopped (oscillation continues) |
| Basic interval timer | Operation stopped | Can Operate (IRQBT is set by reference time interval) |
| Serial interface | Can operate only when external $\overline{SCK}$ input is selected for serial clock. (Note 1) | Can operate if other than CPU clock $\phi$ is specified as serial clock |
| Timer/event counter | Can operate only when TIn (n = 0, 1) pin input is selected for count clock | Can operate |
| Clock output circuit | Stops operation | Can operate if other than CPU clock $\phi$ is specified |
| CPU | Operation stopped | Operation stopped |
| Retained data | Contents of all registers (general registers, flags, mode registers, and output latches) and contents of data memory retained | |
| Release signal | Interrupt request signal (enabled with interrupt enable flag) from operating hardware or $\overline{RESET}$ | |

(*Id*. at 48 (Table 7) (annotated).)

254.    Therefore, when the clock and CPU operation including computations are stopped in the STOP mode, the Data Retention mode is entered by reducing $V_{DD}$ supplied to the CPU, *i.e.*, the *core voltage to the processor*, to 2 V.  In the Data Retention mode, the general purpose registers and control registers (that are part of the Data Memory or RAM) retain their respective data.  As such, the state of the μPD751xx-CPU (*processor*) is maintained.  Accordingly, NEC-Databook teaches "*reducing core voltage to the processor to a value sufficient to maintain state during the mode in which said system clock is disabled*."

255.    This is consistent with the arguments the Applicant presented during prosecution of the '731 patent.  In particular, during prosecution, in addressing rejection of claims over U.S. 6,675,304 to Pole II et al. ("Pole"), the Applicant stated:

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In addition, with respect to Claim 1, Pole teaches a deep sleep state in which only data stored in the processor's internal caches is maintained (column 1, lines 30-34). As is well known to those of ordinary skill in the art, a **processor's state** is not represented in the processor's internal caches, and **includes, for example, the contents of internal registers** which are not represented in the caches.

(Ex.1004 at 374; *see id*. at 350 and 373.)

256.    As noted above, NEC-Databook also teaches "*wherein said value of the core voltage is not sufficient to maintain processing activity in said processor*" because NEC-Databook describes the "Operating voltage range" of a number of microcontrollers in the µPD751xx/P1xx family as 2.7-6 V, which is greater than the 2 volts supplied during the "Data Retention mode."

257.    Specifically, NEC-Databook provides a "Product Comparison" of various products in the family:

**Product Comparison**

| Item | µPD75104/104A | µPD75106 | µPD75108/108A | µPD75P108 | µPD75112 | µPD75116 | µPD75P116 |
|---|---|---|---|---|---|---|---|
| Power-on-reset circuit and power-on flag | Mask option | Mask option | Mask option | Internally provided | Mask option | Mask option | Not included |
| Operating voltage range | 2.7 to 6.0 V | 2.7 to 6.0 V | 2.7 to 6.0 V | 5 V ± 10% | 2.7 to 6.0 V | 2.7 to 6.0 V | 5 V ± 10% |
| Package | See ordering information for a complete list of packages | | | | | | |

(Ex.1005 at 31.)  The comparison shows that the "Operating voltage range" of several microcontrollers is 2.7 to 6.0 V and that two types of microcontrollers

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operate at 5.0 V.

258.   NEC Data also discloses "Guaranteed Operating Range" for the

µPD751xx family of microcontroller as 2.7-6 V.  (*See id*. at 62 (Figure 17

(annotated)).)



Figure 17.   Guaranteed Operating Range (µPD751xx)
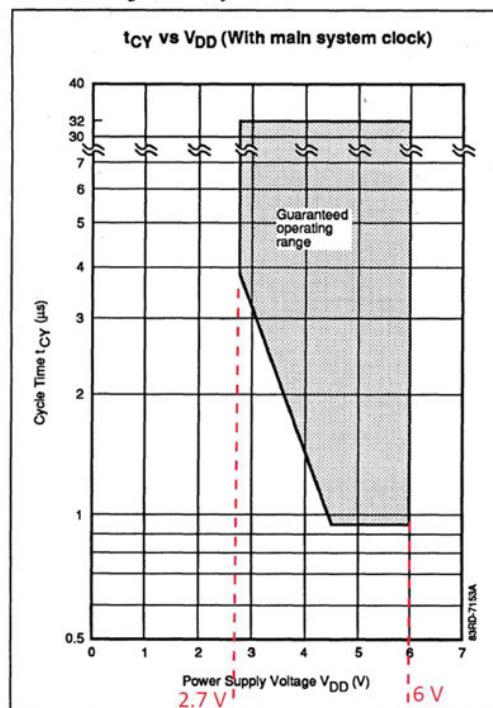
259.   Moreover, for the same family of microcontrollers, NEC-Databook

discloses that before releasing the "STOP mode" by an interrupt, where, within the

STOP mode the microcontroller is operating in the "Data Retention mode," and

entering the "Operation mode" the supply voltage "$V_{DDDR}$" must be increased, *e.g.*,

from 2 V (*see id*. at 32, col. 1) to, *e.g.*, at least 2.7 V (*see id*. at 31), as depicted in

Figure 19 B.  (*Id*. at 65.)

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**B. STOP mode is released by interrupt signal**
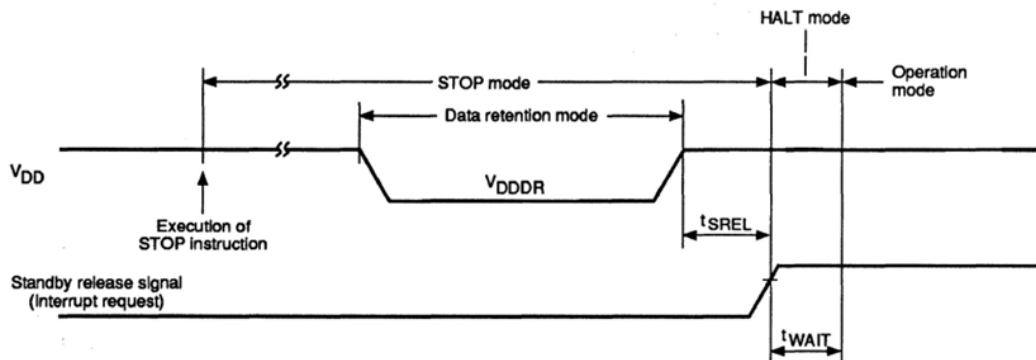


(*Id*. at 65 (Figure 19B).)

260. As such, NEC-Databook teaches that the disclosed microcontrollers would not operate and, thus, the CPU therein would not be able to maintain processing activity at voltages less than 2.7 V.

261. This is consistent with the arguments the Applicant presented during prosecution of the '731 patent. In particular, in addressing the rejection of claims over U.S. 6,118,306 in view of "Re: AX64Pro or AK72?" by NewsReader (June 15, 2000) ("NewsReader") the Applicant stated:

> Moreover, even if it is assumed that Orton's teaching is modified to
> drop the core voltage to Newsreader's 1.0 Volt, Applicants
> respectfully assert that the rejection has not established what would be
> the effect on the processor. For example, the rejection has not
> established what would be the effect of reducing the voltage to the
> processor in Orton (e.g., processor 12 in Figs. 1, 2, and 5) to any
> particular voltage during sleep mode. Applicants assert that it is

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understood that **different processors have different operational characteristics. Therefore, Applicants do not understand the evidence in the record to establish that operating Orton's processor (12) at 1.0 Volt as being "not sufficient to maintain processing activity,"** as claimed. For the foregoing reasons, the art does not suggest combining Orton and Newsreader in such a fashion to arrive at the claimed invention.

(Ex.1004 at 271; *see id*. at 237 and 267.)

262. Accordingly, NEC-Databook also teaches that the 2 V supplied when the CPU clock is stopped constitutes "*said value of the core voltage* [*that*] *is not sufficient to maintain processing activity in said processor*." Thus, NEC-Databook teaches this claim element.

> **d. Element 1[c]: "responsive to said determining, at a voltage regulator supplying said core voltage, transitioning from a first regulation mode to a second regulation mode,"**

263. Burd teaches "*responsive to said determining, at a voltage regulator supplying said core voltage, transitioning from a first regulation mode to a second regulation mode*" because Burd discloses a "switching regulator" (*a voltage regulator*).

264. As an overview, Burd discloses a "switching regulator" (*voltage regulator*) that operates in two modes, a regulation mode (*first regulation mode*) or

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a tracking mode (*second regulation mode*). (Ex.1006 at 1, cols. 1-2.) Burd's

switching regulator supplies selectable voltages in the range 1.2-3.8V to a

microprocessor. (Ex.1006 at 1, col. 1; 2 (Figure 17.4.3 ("$V_{DD}$" graph).) The

voltage to be supplied to the microprocessor can be adjusted via a "new frequency

request." (Ex.1006 at 1, cols. 1-2; 2 (Figure 17.4.2 ("From Voltage Scheduler")).)

When the difference between the new frequency and current frequency is greater

than or equal to 4 MHz, Burd's switching regulator transitions from regulation

mode (*first regulation mode*) to tracking mode (*second regulation mode*) and

adjusts the voltage level output by the switching regulator. (Ex.1006 at 1, cols. 1-

2; 2 (Figure 17.4.3).)

265. As discussed for Element 1[a], a POSITA would have understood the

status of the μPD751xx-CPU's PTO0, PTO1, and/or PCL signals indicate that the

μPD751xx-CPU is transitioning to a STOP mode, and would have used these

signals to send a "new frequency request" to the voltage regulator to reduce the

core voltage supplied to the μPD751xx-CPU. This would cause the regulator to

switch from one regulation mode to another.

266. Specifically, Burd discloses a "voltage scheduler" implementing a

"dynamic voltage scaling (DVS)" strategy, where the output voltage of a voltage

regulator is adjusted according to a specified desired frequency. (*See* Ex.1006 at 1,

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col. 1.)  Burd states:

> If [] clock frequency ($f_{CLK}$) and supply voltage ($V_{DD}$) are dynamically
> varied in response to computational load demands, then energy
> consumed per process can be reduced for the low computational
> periods, while retaining peak performance when required. This
> strategy, which achieves the highest possible energy efficiency for
> time-varying computational loads, is called **dynamic voltage scaling
> (DVS)**.

(*Id.*)

267.   Thereafter, Burd discloses: "A prototype DVS-enabled chip-set in

0.6μm 3-metal $V_T \approx 1V$, CMOS contains a battery-powered (3.3-6.0V) **switching**

**regulator**, a microprocessor, SRAM memory chips, and an interface chip for

connecting to commercial I/O peripherals."  (*Id.*; Figure 17.4.2.)  "The

microprocessor operates from 1.2-3.8 V," and Burd's regulator provides regulated

voltage up to 3.8 V.  (*Id.* at 1, col. 1; Figure 17.4.3.)

268.   Burd further describes:

> A regulation feedback loop for setting the variable $V_{DD}$ and $f_{CLK}$ is
> shown in Figure 17.4.2. The ring oscillator, which tracks the critical
> paths of the microprocessor over voltage, outputs $f_{CLK}$ as a function of
> $V_{DD}$. The $f_{CLK}$ signal is digitally quantized in 1MHz steps, and used to
> generate a frequency error, $F_{ERR}$. The loop filter implements a **hybrid**

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> **pulse-width/pulse-frequency modulation algorithm that generates
> an $M_P$ or $M_N$ enable**. The regulated $V_{DD}$, which is fed back to the
> CPU chip to close the loop, is generated across the capacitor [of 5.5 µf
> shown in Figure 17.4.2.]
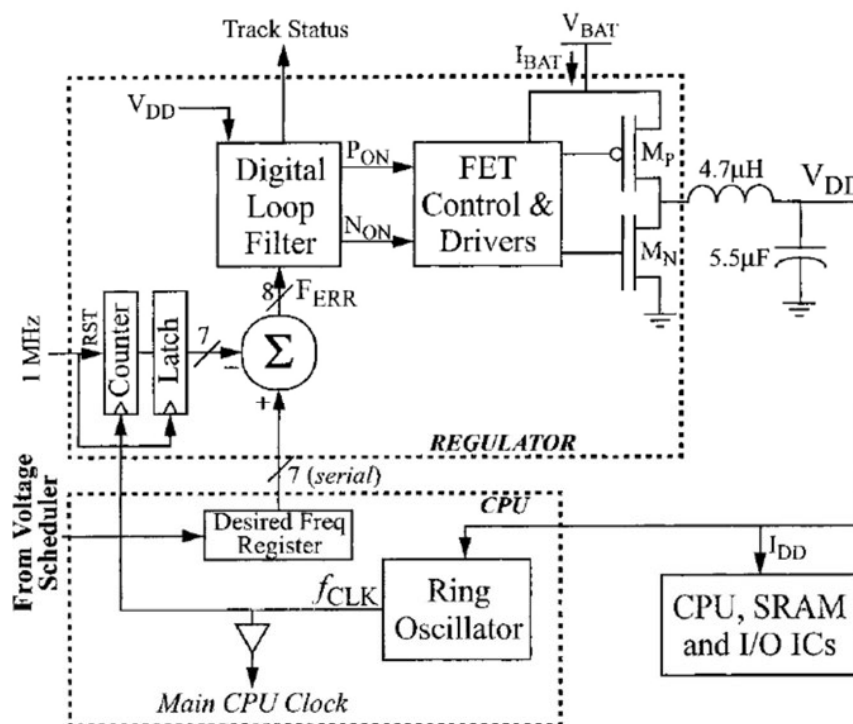
(*Id.*; Figure 17.4.2.)



Figure 17.4.2: Frequency to voltage feedback loop.

(*Id.*at 2 (Figure 17.4.2).)

269.   In addition, Burd states:

> The converter operates in either tracking or regulation mode, as
> indicated by the track status signal. A new frequency request initiates
> tracking mode in which the converter either delivers or removes
> charge from the capacitor, depending upon the sign of $F_{ERR}$. When the

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error magnitude is less than 4MHz, the converter switches to the
regulation mode in which $M_N$ is disabled and only the processor
circuits can remove charge.

(*Id*. at 1, cols. 1-2.)

270.   In light of the disclosure above, a POSITA would have understood
that in the regulation mode, the switching element $M_N$ (a field-effect transistor
(FET) (*see id*. at 2, Figure 17.4.2)), is disabled while in the tracking mode, both
switching elements $M_P$ and $M_N$ are operated, and that in both modes, the switching
of the FETs $M_P$ and/or $M_N$ is controlled by the **hybrid pulse-width/pulse-frequency modulation algorithm**.

271.   Therefore, the "**regulation mode**" in which the voltage regulator
implements the "hybrid pulse-width/pulse-frequency modulation algorithm," *i.e.*,
voltage regulation may be performed using pulse-width modulation or pulse-
frequency modulation, is the "*first regulation mode*."  The "tracking mode" is the
"*second regulation mode*."

272.   Although this claim element recites two "regulation" modes and Burd
describes a "regulation" mode and a "tracking" mode, a POSITA would have
understood that this difference exits only in the names because Burd's regulator
employs the same switching techniques that the '731 patent describes.
Specifically, Burd states that the "loop filter implements a hybrid **pulse-**

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**width/pulse-frequency modulation** algorithm." (*See id*. at 1, col. 1.)

273. Prior to 2000, it was well known that the pulse-width modulation (PWM) scheme is a continuous switching scheme that is generally efficient when the output voltage changes, because it can charge or discharge the output capacitance without relying on the load provided by the processor itself. Indeed, Burd discloses the use of PWM when a "new frequency request" which corresponds to a change in the output voltage, is received because Burd states that in this case, "the converter either delivers or removes charge from the [output] capacitor." (*Id*., cols. 1-2.) Thus, Burd's tracking mode is generally associated with PWM or continuous switching.

274. Prior to 2000, it was also well known that the pulse-frequency modulation (PFM) scheme is a burst-type or skip switching scheme that is generally efficient when the output voltage is relatively stable and when the load current is low. Burd teaches the use of the PFM switching when the voltage is relatively stable because Burd states that when "the error magnitude is less than 4MHz," which indicates that the required change in the output voltage, if any, is relatively small, "the converter switches to the **regulation mode** in which $M_N$ is disabled and **only the processor circuits can remove charge**," which indicates that not PWM but PFM switching is employed.

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275. The '731 patent describes the same switching scheme, as follows:

Prior art voltage regulators function in at least two different modes of operation. A first mode of operation is often referred to as **"low noise" or "continuous" mode**. In this mode, the regulator responds as rapidly as possible to each change in voltage thereby maintaining the output voltage at the desired output level as accurately as possible.

(Ex.1001, 5:48-53). Thus, Burd's "tracking mode," which employs PWM or continuous switching as discussed above, is one mode of the regulator.

276. The '731 patent further states:

A second mode of operation by voltage regulators is often referred to as **"high efficiency," "burst," or "skip" mode**. In this mode, a regulator detects the reduction in load requirements (such as that caused by a transition into the deep sleep state) and switches to a mode whereby the regulator corrects the output voltage less frequently.

(*Id.*, 6:1-6.) Thus, Burd's "regulation mode," which employs PFM or burst or skip switching as discussed above, is another mode of the regulator.

277. In summary, Burd's "tracking mode" and "regulation mode" are both "*regulation modes*" and correspond to the "continuous mode" and "high efficiency mode" of the voltage regulator in the '731 patent. In Burd, the "tracking mode" employs pulse-width modulation (and is thus a continuous mode) and is generally

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used to transition from one voltage level to another. (*See* Ex.1006 1, cols. 1-2; 2

(Figure 17.4.3).) The "Regulation mode" typically employs pulse-frequency

modulation (and is thus a burst or high-efficiency mode) and is generally used to

maintain the voltage level. (*Id*.) This is similar to the '731 patent, where the

"continuous mode" is used during voltage transitions and the "high efficiency

mode" is used otherwise. (Ex.1001 at col. 6:37-56.)

278. As discussed under Motivation to Combine, a POSITA would have

understood that if the output voltage of Burd's regulator is 3.8 V (corresponding to

a presumed operating frequency of 80 MHz, though the actual operating frequency

of the µPD751xx-CPU can be different), Burd's regulator would output 2.0 V at

the presumed operating frequency of 28 MHz.

279. A POSITA would have further understood that providing a 7-bit value

corresponding to 28 MHz (e.g., "0011100 ") would cause Burd's digital loop filter

to lower the output voltage of its regulator from approximately 3.8 V to

approximately 2.0 V. Here again, a POSITA would have understood that in

response to the $F_{ERR}$ corresponding to the difference (28 – 80 = -52 MHz), the

converter would transition to the "**tracking mode**" (the *second regulation mode*)

from the "**regulation mode**" (the *second regulation mode*), as shown in Burd's

Figure 17.4.3 and NEC-Databook's Figure 19B.

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280. Furthermore, as explained in connection with Elements 1[a] and 1[b],

NEC-Databook discloses that executing the STOP instruction causes the

µPD751xx-CPU to transition from the Operation mode to the STOP mode. This

transition would cause a corresponding transition of the status of the output signals

PTO0, PTO1, and/or PCL from a changing/counting state to a stable state (*i.e.*, a

constant value). This state change can be detected and used to present a "new

frequency request" of 28 MHz to Burd's regulator/controller, which corresponds to

a voltage regulator output of approximately 2.0 V. Accordingly, the µPD751xx-

CPU would transition to the Data Retention mode.

281. In Figure 17.4.3, Burd shows a full-range voltage transition from 1.2

to 3.8 V corresponding to a full-range frequency transition from 5 to 80 MHz, and

vice versa. (*See* Ex.1006 at 1, cols. 1-2; 2 (Figure 17.4.3).) A POSITA would

have understood that the requested new frequency can be any frequency in the

range 5-80 MHz and, as such, the corresponding output voltage would change. For

example, a POSITA would understand that Burd's regulator would supply 3.8 V at

"Desired Freq" of 80 MHz, and would supply 2.0 V at "Desired Freq" of 80 and 28

MHz, respectively. (S*ee* Ex.1006 at 2 (Figure 17.4.2).)

282. Therefore, a POSITA would understand that while supplying 3.8 V,

which corresponds to $f_{CLK}$ of 80 MHz, if a "new frequency request" of 28 MHz is

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presented, $F_{ERR}$ would be -52 MHz. Since the magnitude of the error signal is

greater than 4 MHz, Burd's regulator would transition from the "regulation mode"

(*first regulation mode*) to the "tracking mode" (*second regulation mode*). Such a

transition is shown in Burd's Figure 17.4.3, although with a voltage transition of

3.8 to 1.2 V, rather than the 3.8 to 2 V that the combination of NEC-Databook and

Burd teaches. This transition corresponds to NEC-Databook's Figure 19B, where

$V_{DD} \geq 2.7$ V is 3.8 V and $V_{DDDR} \approx 2$ V.

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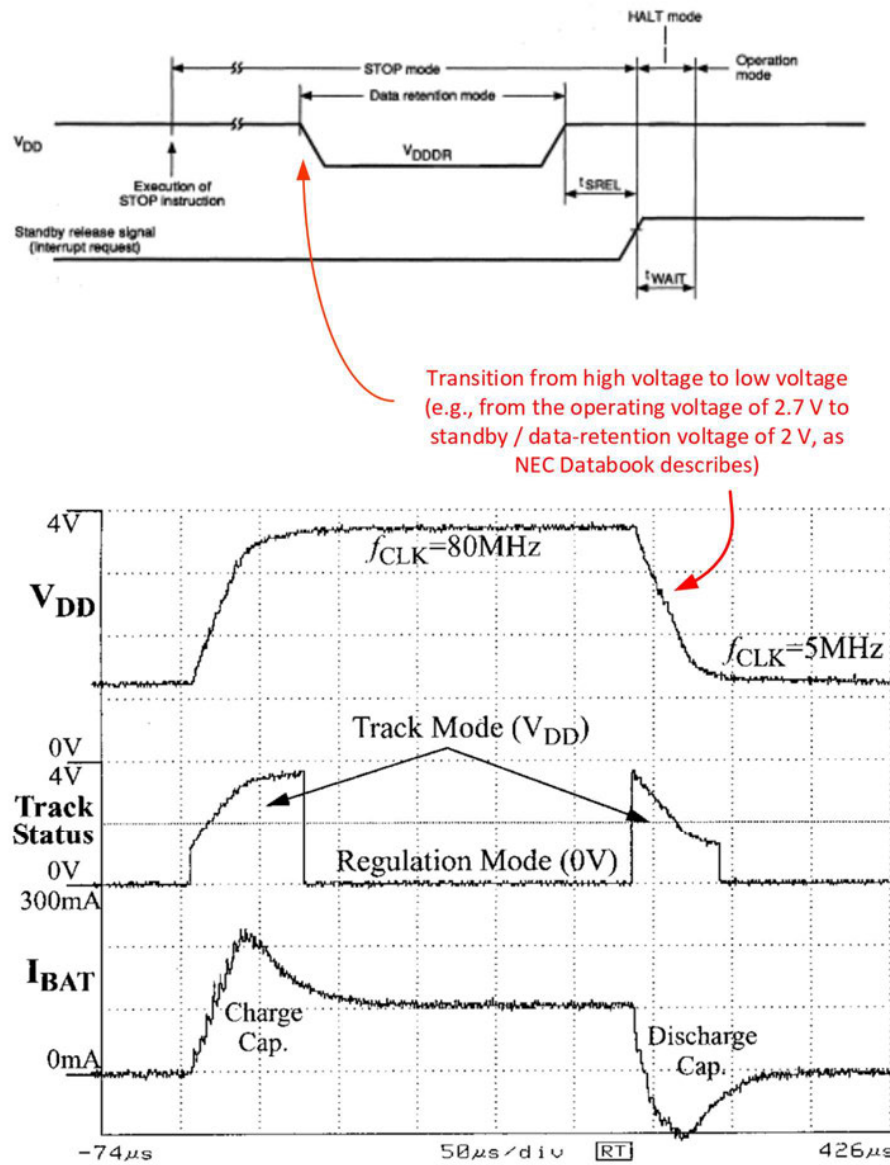


Figure 17.4.3: Transient response of regulation loop.

(Ex.1005 at 65 (Figure 19 B); Ex.1006 at 2, Figure 17.4.3 (annotated).)

283.  As discussed for Element 1[a], the status of NEC-Databook's PTO0,

PTO1, and/or PCL signals indicate, and are one way to determine, that NEC-

Databook's μPD751xx-CPU is transitioning from the Operation mode to the STOP

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mode, where the CPU clock is stopped.  A POSITA would have understood, that in

response to this determination, a "new frequency request" of, *e.g.*, 28 MHz may be

presented to Burd's regulator, causing it to reduce its output voltage down to

approximately 2V and, to switch from the "regulation mode" to the "tracking

mode" during the voltage transition.  Accordingly, the combination of NEC-

Databook and Burd teaches this claim element.

> e. **Element 1[c.1]: "wherein power is dissipated during a voltage transition that reduces said selectable voltage in said first regulation mode and"**

284.   The combination of NEC-Databook and Burd teaches "*wherein power*

*is dissipated during a voltage transition that reduces said selectable voltage in*

*said first regulation mode*," because Burd states that when "the converter switches

to the regulation mode" (*i.e.*, the first regulation mode) "$M_N$ is disabled and **only**

**the processor circuits can remove charge**," *i.e.*, power is dissipated by the

processor circuitry.  (Ex.1006 at 1, col. 1.)

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Figure 17.4.3: Transient response of regulation loop.
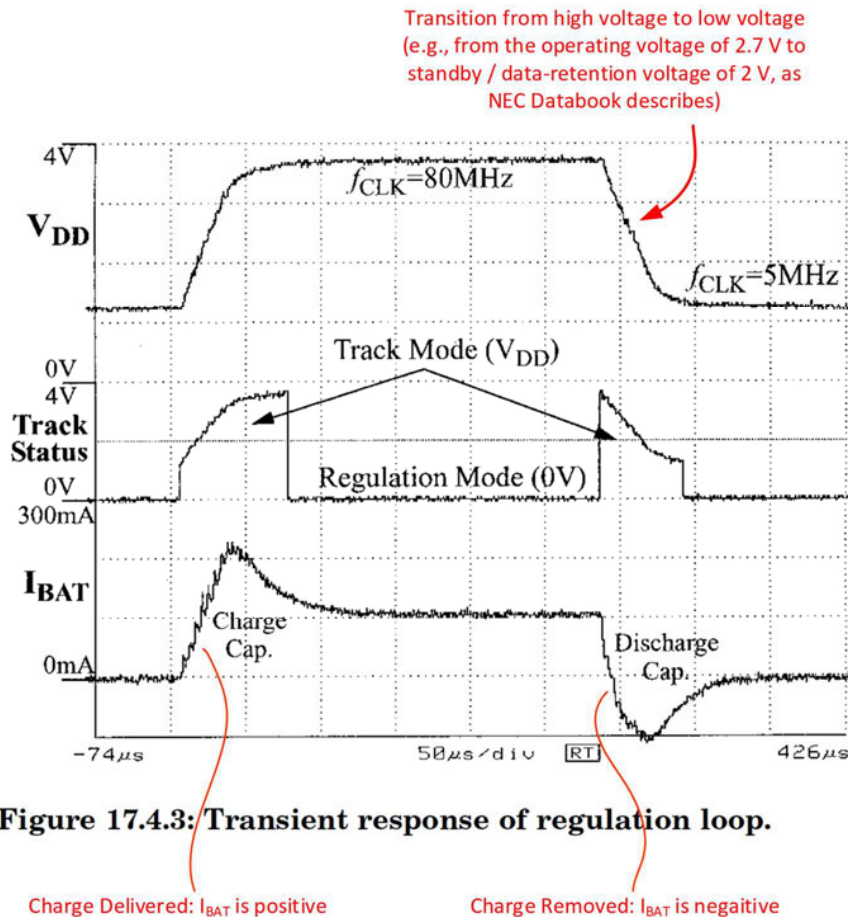
(*Id*. at 2, Figure 17.4.3 (annotated).)

285.   Thus, during a voltage transition from a high voltage to a low voltage,

if Burd's controller were not to transition to the tracking mode, only the processor

can remove the charge from the 5.5 µf output capacitor shown in annotated Figure

17.4.2 below.

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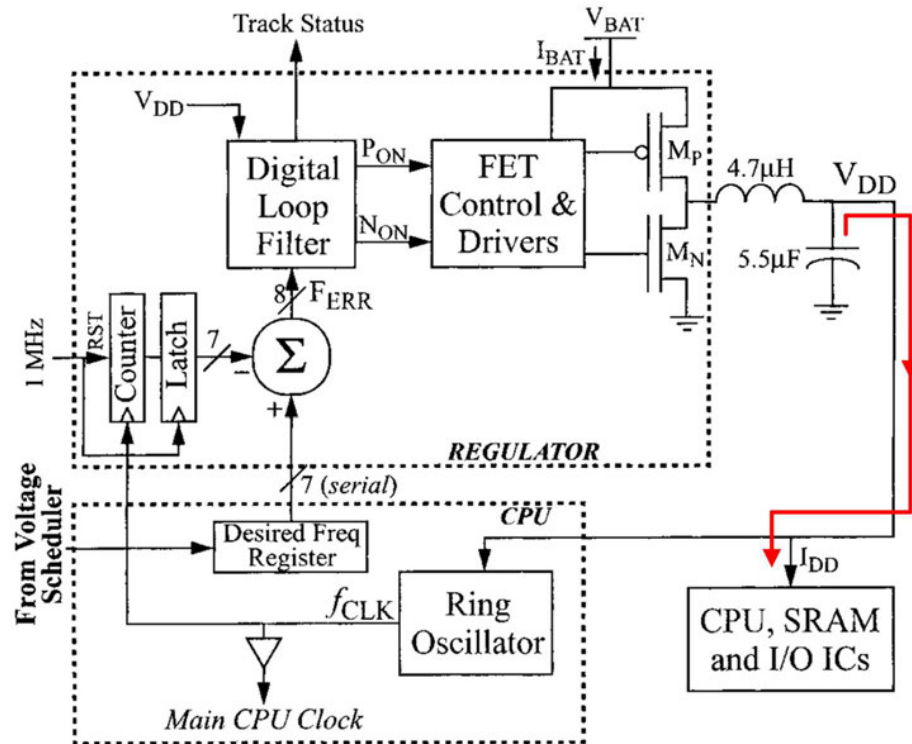U.S. Patent No. 7,260,731



Figure 17.4.2: Frequency to voltage feedback loop.

(*Id.*, Figure 17.4.2 (annotated).)

286. Thus, the combination of NEC-Databook and Burd teaches "wherein power is dissipated" "**during the transition period**," *i.e.*, "during a voltage transition that reduces said selectable voltage in" the "**regulation mode**," i.e., "said first regulation mode."

      **f.**      **Element 1[c.2]: "power is saved during said voltage transition in said second regulation mode."**

287. Burd teaches that "*power is saved during said voltage transition in said second regulation mode*" because Burd describes that in the "tracking mode" (the *second regulation mode*) "**the converter** either delivers or **removes charge**

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**from the [output] capacitor**" which may be stored at the input capacitor of the

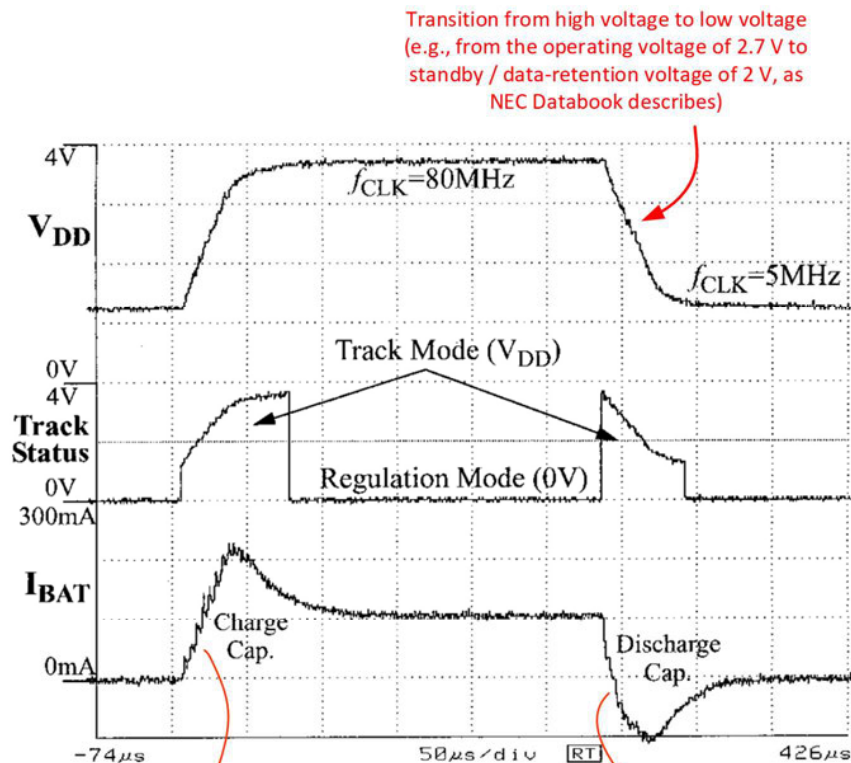battery, thereby avoiding power dissipation, and resulting in power saving.

288.   In particular, Burd states that the "loop filter" of the regulator

"implements a hybrid pulse-width/pulse-frequency modulation algorithm **that**

**generates an $M_P$ or $M_N$ enable**. The **regulated $V_{DD}$**, which is fed back to the CPU

chip to close the loop, **is generated across the capacitor" of 5.5 µf shown in**

**Figure 17.4.2**.  (Ex.1006 at 1, col. 1.)  Burd also states that in the "**tracking**

**mode**" "**the converter either delivers or removes charge from the capacitor**,

depending upon the sign of $F_{ERR}$."  (*Id*. at 1, cols. 1-2.)

289.   Thus, when the output voltage transitions from a low to a high

voltage, the converter "delivers" charge to the 5.5 µf output capacitor, where the

current supplying the charge flows from the battery to the output capacitor.  In

Figures 17.4.2 and 17.4.3, that current together with current supplied directly to the

processor load is denoted $I_{BAT}$, and while charging the output capacitor, $I_{BAT}$ is

positive.

290.   When the output voltage transitions from a high voltage to a low

voltage (*e.g.*, when the processor clock is stopped and the voltage is reduced, as

NEC-Databook teaches, as described for claim element [1.b]), the converter

"**removes** charge from the [5.5 µf output capacitor]."  At least some of the

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removed charge may be transferred to and stored at the input capacitor of the

battery, causing $I_{BAT}$ to flow in the opposite direction (*i.e.*, $I_{BAT}$ is negative), as
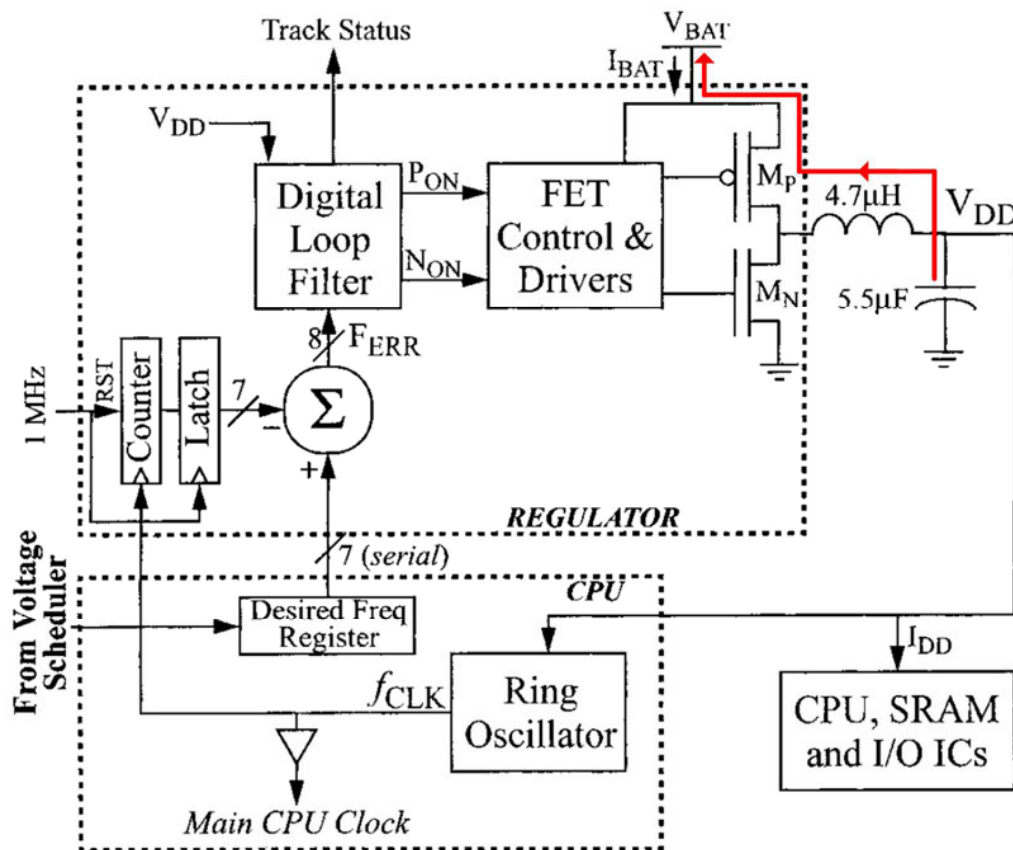
Figures 17.4.2 and 17.4.3 show.



Figure 17.4.3: Transient response of regulation loop.

(*Id*. at 2, Figure 17.4.3 (annotated).)

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**Figure 17.4.2: Frequency to voltage feedback loop.**

(*Id.*, Figure 17.4.2 (annotated).)

291.   The returning and storing of the charge to the input supply and/or the

input capacitor while the voltage is decreasing and the regulator is operating in

tracking mode saves power when compared with dissipating the charge, as would

occur in regulation mode Thus, the combination of NEC-Databook and Burd

discloses this claim element.

292.   In summary, NEC-Databook in view of Burd teaches or at least

suggests each and every element of claim 1 and, thus, renders claim 1 unpatentable

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as obvious.

### 3. Claim 3

293. Claim 3 depends from claim 1 and further recites: "**the step of reducing core voltage to the processor to a value sufficient to maintain state during the state in which system clock is disabled comprises furnishing an input to reduce an output voltage provided by a voltage regulator furnishing core voltage to the processor.**"

294. As a threshold matter, this claim recites "the state in which system clock is disabled," but claim 1, from which claim 3 depends, recites "a mode in which a system clock to the processor is disabled." In my analysis below, I assume that the system clock recited in claim 3 is the same as that recited in claim 1, and that the "state" recited in claim 3 is the same as the "mode" recited in claim 1.

295. NEC-Databook in view of Burd teaches "*the step of reducing core voltage to the processor to a value sufficient to maintain state during the state in which system clock is disabled comprises furnishing an input to reduce an output voltage provided by a voltage regulator furnishing core voltage to the processor*," because Burd describes providing the signal $F_{ERR}$ (an input to reduce and output voltage).

296. As discussed for claim elements 1[pre]-1[b], NEC-Databook discloses

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a "Data Retention mode" in which the clock to the CPU is stopped and the voltage

to the CPU is reduced, *e.g.*, from 2.7 V to 2 V, which is sufficient to maintain the

processor state. (*See* Ex.1005 at 47, cols. 1-2; *see id*. at 32, col. 1.) Thus, NEC-

Databook teaches "*the step of reducing core voltage to the processor to a value*

*sufficient to maintain state during the state in which system clock is disabled*."

297. Moreover, as discussed for claim element 1[c], Burd discloses a

regulator / controller dynamically adjusting the voltage supplied to a processor,

*i.e.*, "*a voltage regulator furnishing core voltage to the processor*." (*See* Ex.1006

at 1, col. 1; *id.* at 2, Figure 17.2.4.) Additionally, Burd describes:

> A voltage scheduler is required in the operating system of a DVS
> system. It controls $f_{CLK}$ (and $V_{DD}$) by **writing a desired frequency (in**
> **MHz) to a coprocessor register**. Individual applications supply a
> completion deadline, and the voltage scheduler uses the applications'
> previous execution history to determine the number of processor
> cycles required and sets $f_{CLK}$ accordingly. By optimally adjusting $f_{CLK}$,
> the CPU system always operates at the minimum performance level
> required by the current active processes and thereby consumes the
> minimal amount of energy.

(*Id*.)

298. Burd further states:

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A regulation feedback loop for setting the variable $V_{DD}$ and $f_{CLK}$ is shown in Figure 17.4.2. The ring oscillator, which tracks the critical paths of the microprocessor over voltage, outputs $f_{CLK}$ as a function of $V_{DD}$. The $f_{CLK}$ signal is digitally quantized in 1MHz steps, and used to **generate a frequency error, $F_{ERR}$.** The loop filter implements a hybrid pulse-width/pulse-frequency modulation algorithm that generates an $M_P$ or $M_N$ enable. The regulated $V_{DD}$, which is fed back to the CPU chip to close the loop, is generated across the capacitor [of 5.5 µf shown in Figure 17.4.2.]

(*Id.*; Figure 17.4.2.)

299.   Moreover, according to Burd a "**new frequency request initiates tracking mode** in which the converter either delivers or removes charge from the capacitor, **depending upon the sign of $F_{ERR}$**. When the error magnitude is less than 4MHz, the **converter switches to the regulation mode**" (*Id.*, at 1, cols. 1-2; *Id.* at 2, Figure 17.4.2 (reproduced and annotated below).)
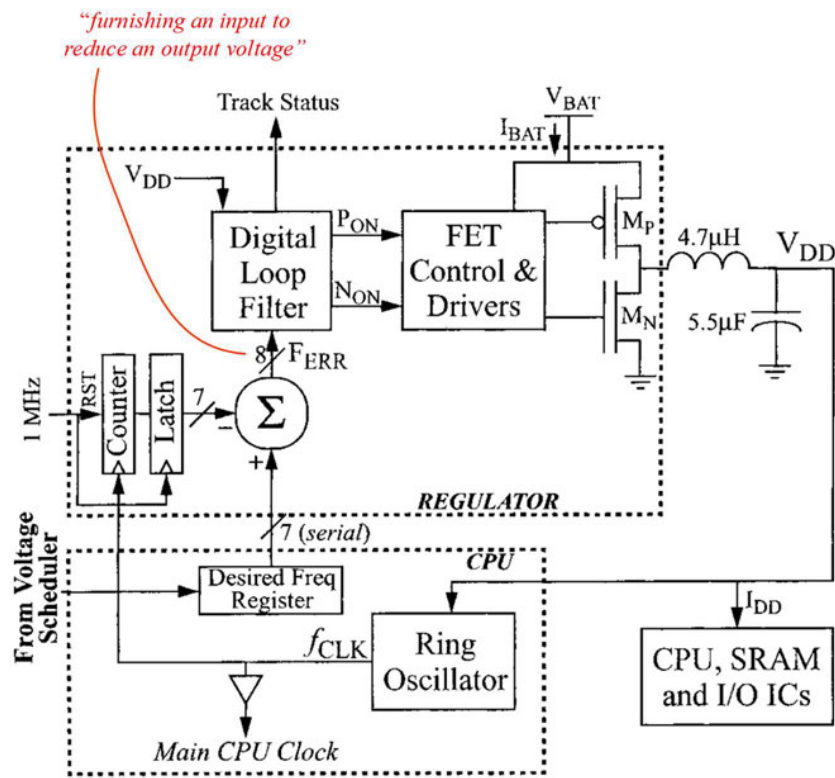
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Figure 17.4.2: Frequency to voltage feedback loop.

300. Thus, the magnitude of the signal "$F_{ERR}$" determines whether the

voltage supplied to the CPU is to be adjusted and whether to enter the tracking

mode for that purpose, and the sign of the signal "$F_{ERR}$" determines whether the

voltage to be supplied is to be increased or reduced. As such, generating and

providing the signal "$F_{ERR}$" constitutes "*furnishing an input to reduce an output*

*voltage provided by a voltage regulator furnishing core voltage to the processor.*"

301. Alternatively, the signal supplied by Burd's "Desired Frequency

Register" also constitutes "*an input to reduce an output voltage provided by a*

*voltage regulator*" because, if the desired frequency is less than the current clock

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frequency $f_{CLK}$, the sign of the signal $F_{ERR}$ generated by the regulator would be

negative and, accordingly, the regulator would remove charge from the 5.5 µF

output capacitor, and would reduce the voltage supplied to the processor. (*See id*.

at 1, col. 1 (stating that "the converter either delivers or **removes charge from the**

**capacitor**, **depending upon the sign of $F_{ERR}$**"); *Id.* at 2, Figure 17.4.2 (depicting a

signal supplied by "Desired Frequency Register" as input to the "Regulator"; and

Figure 17.4.3 (depicting that when desired clock frequency of 5 MHz is less than

the current frequency of 80 MHz, the capacitor is discharged, and the supplied
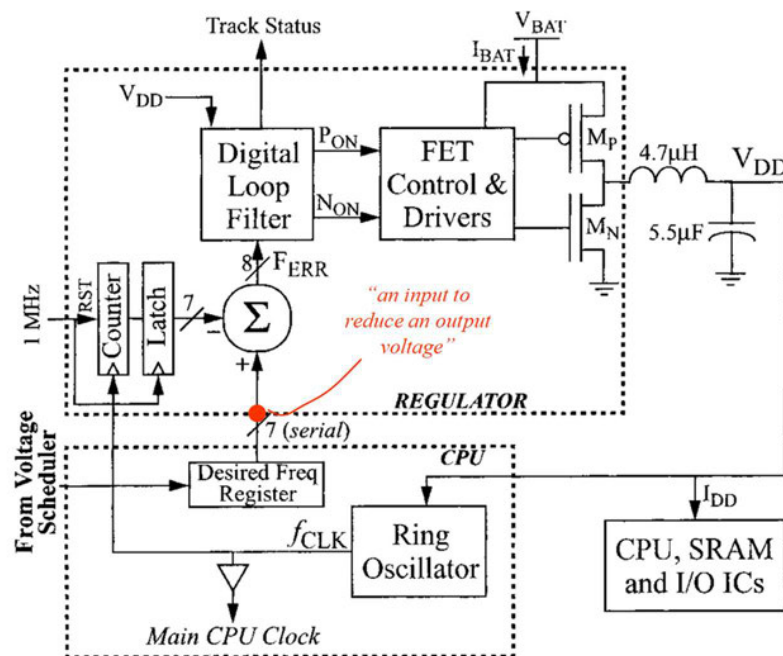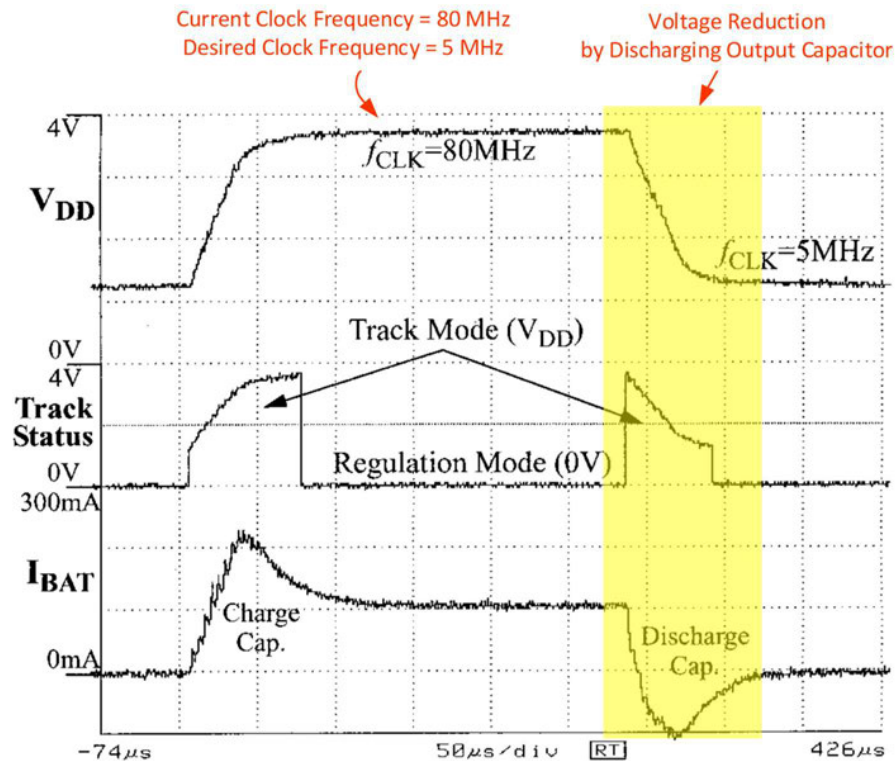
voltage is reduced).)



Figure 17.4.2: Frequency to voltage feedback loop.

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**Figure 17.4.3: Transient response of regulation loop.**

302. As such, Burd discloses furnishing an input from a "voltage

scheduler" into a "Desired Freq Register" to control (*e.g.*, reduce) the output

voltage of the voltage regulator. Specifically, the "voltage scheduler" "**writ[es] a**

**desired frequency (in MHz) to a coprocessor register**." (Ex.1006 at 1, col. 1; 2

(Figure 17.4.2 (disclosing the "Desired Freq register")).) The voltage regulator

generates an error signal ($F_{ERR}$) as a difference between the desired frequency and

the frequency $f_{CLK}$ currently generated by the "Ring Oscillator." (*Id*.)

303. Based on the error signal $F_{ERR}$, the Loop Filter controls the switching

of the FETs $M_P$ and $M_N$ to adjust the regulator's output voltage $V_{DD}$, which the

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voltage regulator then uses to adjust $f_{CLK}$. The operation of the "regulation

feedback loop" (controlling $M_P$ and $M_N$ and adjusting $f_{CLK}$) continues until

$F_{ERR} \approx 0$, so that $V_{DD}$ is raised or reduced to correspond to the "desired

frequency." (*See* Ex.1006 at 1, col. 1; *id.* at 2 (Figure 17.4.2).)

304.　Thus, to reduce the voltage supplied to the µPD751xx-CPU to, *e.g.*, 2

V ("*a value sufficient to maintain state during the state in which* [*the CPU*] *clock is*

*disabled*") a corresponding frequency value may be supplied to the "Desired Freq.

Register," which constitutes "*furnishing an input to reduce an output voltage*

*provided by a voltage regulator furnishing core voltage to the processor*." Thus,

the combination of NEC-Databook and Burd teaches the limitations of this claim,

and renders it unpatentable as obvious.

### 4.　Independent Claim 6

#### a.　Elements 6[pre] and 6[a]

305.　Elements 6[pre] through 6[a] are substantially the same, respectively,

as Elements 1[pre] through 1[a], as set forth below:

| 1[pre]  A method for reducing power utilized by a processor comprising the steps of: | 6[pre]  A method for reducing power utilized by a system having a least a processor, comprising the steps of: |
|---|---|
| 1[a]  determining that a processor is transitioning from a computing mode | 6[a]  determining that the processor is transitioning from a computing mode |

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| to a mode in which a system clock to the processor is disabled, and | to a mode in which a system clock to the processor is disabled, |
|---|---|

306. The differences between the respective Elements are indicated by the underlining.

307. For the preamble of claim 6, a POSITA would have understood a µPD751xx/P1xx family microcomputer of NEC-Databook to be a system having at least a processor, because the microcomputer includes "CPU, ROM, RAM, I/O ports, comparator, interval timer, two timer/counters, vectored interrupts, and a serial interface." (Ex.1005 at 24, col. 1.) Additionally, a POSITA would have understood that a method for reducing power utilized by a processor would reduce power utilized by a system having a processor. As such, for the reasons provided for the preamble of claim 1 and Element 1[a], NEC-Databook teaches the preamble of claim 6 and Element 6[a].

### b. Element 6[b]

308. Element 6[b] is similar to Element 1[b], as set forth below, with the differences therebetween underlined:

| 1[b] reducing core voltage to the processor to a value sufficient to maintain state during the mode in | 6[b] reducing core voltage <u>being furnished by a voltage regulator</u> to the processor to a value sufficient to |
|---|---|

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| which said system clock is disabled, <u>wherein said value of the core voltage is not sufficient to maintain processing activity in said processor</u>, | maintain state during the mode in which the system clock is disabled, and |
|---|---|

309. The combination of NEC-Databook and Burd discloses this Element because, as discussed for Element 1[b], NEC-Databook teaches "*reducing core voltage*" supplied to the µPD751xx-CPU, and Burd teaches voltages "*furnished by a voltage regulator*" because Burd discloses a switching regulator that may supply different core voltages to a processor by reducing (or raising) the supplied voltages.

310. As discussed for Element 1[b], NEC-Databook teaches "*reducing core voltage to the processor to a value sufficient to maintain state during the mode in which said system clock is disabled*."

311. Burd discloses a "microprocessor [that] operates from 1.2-3.8V and 5-80 MHz." (Ex.1006 at 1, col. 1; *see id*. at 2, col. 2 (describing an ARM processor).) Burd also discloses a "switching regulator" (*see id*. at 1, col. 1), also referred to as a "dc-dc converter" that supplies voltages in the range 1.2-3.8V. (*see id*. at 1, col. 2; 2, Figure 17.4.2.)

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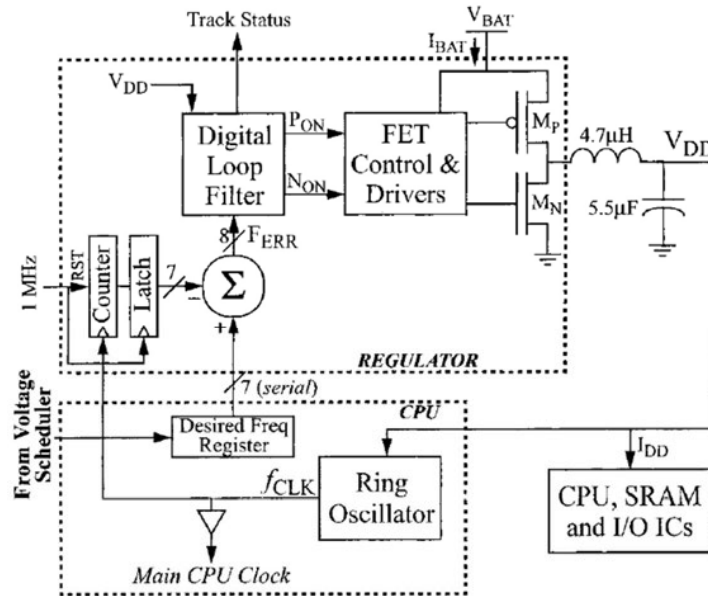U.S. Patent No. 7,260,731



Figure 17.4.2: Frequency to voltage feedback loop.

(*Id*. at 2, Figure 17.4.2.)

312.   Burd also discloses that the output voltage of its regulator can be

raised or reduced.  (*See id*. at 2. Figure 17.4.3.)
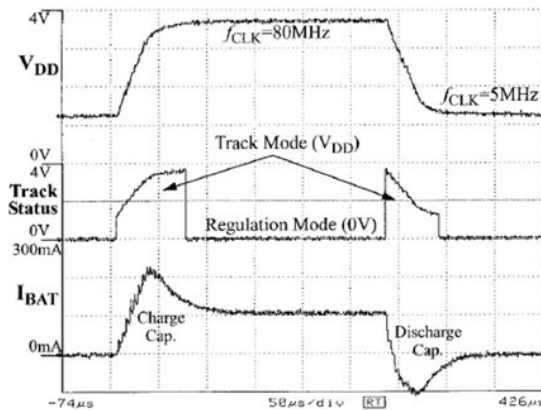


Figure 17.4.3: Transient response of regulation loop.

(*Id*. at 2, Figure 17.4.3.)

313.   Element 1[b] recites an additional limitation underlined for Element

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1[b] that Element 6[b] does not recite. As discussed for Element 1[b], NEC-Databook teaches Element 1[a], including "*reducing core voltage to the processor to a value sufficient to maintain state during the mode in which said system clock is disabled*" that Element 6[b] recites. As such, the combination of NEC-Databook and Burd teaches this Element.

        c.        **Element 6[c.1]: "transferring operation of the voltage regulator furnishing core in a mode in which power is dissipated during a voltage transition in reduction in core voltage"**

314. The combination of NEC-Databook and Burd teaches this Element as discussed for Elements 1[c] and 1[c.1].

315. In particular, a POSITA would have understood that "*transferring operation of the voltage regulator furnishing core [voltage]*" is the same as "*at a voltage regulator supplying said core voltage, transitioning from a first regulation mode to a second regulation mode*," as Element 1[c] recites. Moreover, Element 1[c.1] recites "*power is dissipated during a voltage transition that reduces said selectable voltage in said first regulation mode*" and, thus the "*first regulation mode*" recited in Elements 1[c] and 1[c.1] is "*a mode in which power is dissipated during a voltage transition in reduction in core voltage*" that Element 6[c.1] recites.

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        **d.**      **Element 6[c.2]: "to a mode in which power is saved during said voltage transition in the reduction in core voltage"**

316.   The combination of NEC-Databook and Burd teaches this Element as discussed for Element 1[c.2].  Specifically, Element 1[c.2] recites "power is saved during said voltage transition in said second regulation mode" and, thus, the "second regulation mode" recited in Element 1[b] is "a mode in which power is saved during said voltage transition in the reduction in core voltage" that Element 6[c.2] recites.

317.   Moreover, "transferring operation of the voltage regulator . . . in a mode in which power is dissipated during a voltage transition . . . to a mode in which power is saved during said voltage transition," as Elements 6[c.1]-6[c.2] recite, is substantially the same as "transitioning from a first regulation mode to a second regulation mode" "wherein power is dissipated during a voltage transition . . . in said first regulation mode and power is saved during said voltage transition," as Elements 1[c]-[c.2] recite.

318.   As such, the combination of NEC-Databook and Burd teaches these Elements as discussed for Elements 1[c]-1[c.2].

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e.  **Element 6[c.3]: "when it is determined that the
processor is transitioning from the computing mode
to the mode in which the system clock to the processor
is disabled."**

319.  The combination of NEC-Databook and Burd teaches this Element as discussed for Elements 1[a] and 1[c].

320.  In particular, "*responsive to said determining,*" as Element 1[c] recites, is the same as "*when it is determined,*" as Element 6[c.3] recites, and Element 1[a] recites "*determining that a processor is transitioning from a computing mode to a mode in which a system clock to the processor is disabled.*"

321.  In summary, the combination of NEC-Databook and Burd teaches each and every element of claim 6 and, thus, renders claim 6 unpatentable as obvious.

### 5. Claim 7

322.  Claim 7 depends from claim 6 and further recites: "***the step[] of returning the voltage regulator to its original mode of operation when the value of the core voltage sufficient to maintain state during the mode in which system clock is disabled is reached.***"

323.  The combination of NEC-Databook and Burd teaches "*the* step[] *of returning the voltage regulator to its original mode of operation when the value of the core voltage sufficient to maintain state during the mode in which system clock*

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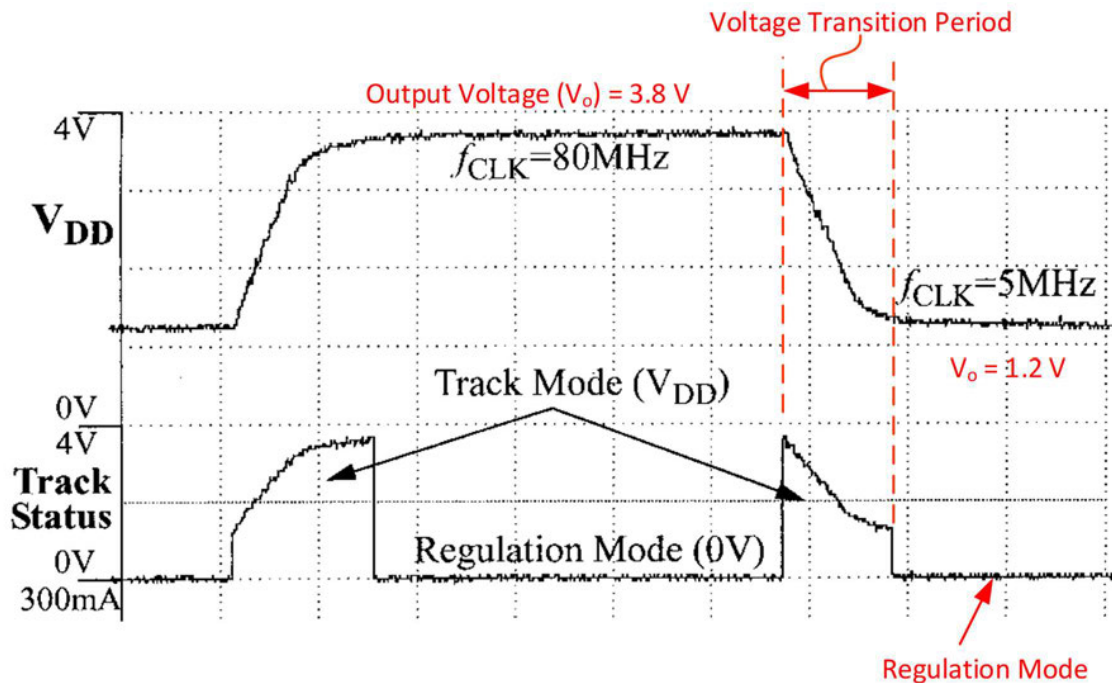U.S. Patent No. 7,260,731

*is disabled is reached*" because Burd discloses operating a regulator/controller in

in the "regulation mode" prior to a voltage transition from a high voltage to a low

voltage, operating the controller in the "tracking mode" during the voltage

transition, and returning to the "regulation" mode (*i.e.*, "*returning the voltage*

*regulator to its original mode of operation*") when the voltage transition to the low

voltage is complete (*i.e.*, *when the value of the core voltage sufficient to maintain*

*state during the mode in which system clock is disabled is reached*").

324.   Specifically, Burd states:

> The **converter operates in either tracking or regulation mode**, as
> indicated by the track status signal. **A new frequency request**
> **initiates tracking mode** in which the converter either delivers or
> removes charge from the capacitor, depending upon the sign of $F_{ERR}$.
> **When the error magnitude is less than 4MHz, the converter**
> **switches to the regulation mode** in which $M_N$ is disabled and only
> the processor circuits can remove charge.

(Ex.1006 at 1, cols. 1-2; 2 (Figure 17.4.3).)

325.   Burd also states: "The transition time is at most 70 µs, shown by the

**maximum 5-80 MHz transition** in Figure 17.4.3." (Ex.1006 at 1, col. 2.)  The

frequency transition from 5-80 MHz corresponds to a voltage transition from 1.2 to

3.8 V.  (*Id*. at 1, col. 1 (stating that the "microprocessor operates from **1.2-3.8 V**

**and 5-80 MHz**").)

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(*Id.*, Figure 17.4.3 (partially reproduced and annotated).)

326.   Thus, Burd teaches that when the high voltage of 3.8 V is provided,

the controller operates in the "regulation mode," as indicated by the "Track Status"

in Figure 17.4.3.  When the transition to the low voltage of 1.2 V begins, the

operation of the controller transitions to the "tracking mode," as indicated by the

"Track Status" in Figure 17.4.3.  When the voltage transition is complete and the

output voltage becomes 1.2 V, the operation of the controller returns to the

"regulation mode," as indicated by the "Track Status" in Figure 17.4.3.

327.   A POSITA would have understood that the same mode transitions

would occur if the Burd's controller were initially operated to provide 2.7 V to the

CPU described in NEC-Databook, and then to provide 2 V, after the CPU clock is

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stopped. Accordingly, the combination of NEC-Databook and Burd teaches the

limitations of claim 7, rendering it unpatentable as obvious.

**C. GROUND 2: Claim 2 Is Unpatentable as Obvious Over NEC-Databook in View of Burd, Further in View of Nguyen**

**1. Motivation to Combine NEC-Databook, Burd, and Nguyen**

328. The motivation to combine NEC-Databook and Burd is discussed

above under Ground 1. A POSITA would have been motivated to combine

Nguyen with NEC-Databook and Burd. First, like NEC-Databook and Burd,

which disclose techniques and components for voltage regulation and power

saving, Nguyen also discloses techniques and circuitry in the same field. (*See e.g.*,

Ex.1007, 1:6-7, 2:45-53, and 7:23-38; FIGS. 4 and 16.)

329. Specifically, like Burd, which discloses a "switching regulator" (*see*

Ex.1006 at 1, col. 1), Nguyen also discloses "a voltage regulator, such as a

switching voltage regulator." (Ex.1007, 1:6-7.) Moreover, like NEC-Databook,

which discloses the STOP and Data Retention modes of its CPU to save power

(*see* Ex.1005 at 47, col. 2; 65 (Figure 19)), Nguyen also discloses operating a

voltage regulator in a "**power conservation mode**." (Ex.1007, 2:45-53 and 7:23-

38; FIGS.4 and 16.)

330. NEC-Databook discloses signals PTO0, PTO1, and/or PCL, the status

of which, that they are not changing, indicates that the clock to the μPD751xx-

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CPU has stopped, indicating further that the µPD751xx-CPU may be in the power

saving STOP or Data Retention modes (*see* Ex.1005 at 29, col. 2; 42, col. 1, 47 col.

2; 48 (Table 7); 28 (Figure "Block Diagram"); 44 (Figure 5); 45 (Figure 7).)

Nguyen discloses a signal that may more directly provide these indications, *e.g.*,

without having to check whether the signals PTO0, PTO1, and/or PCL are

changing.

331.   Specifically, Nguyen discloses "a **STP_CLK# signal**" that can

directly indicate a power saving mode in which the CPU clock is stopped.  In

particular, Nguyen states that the "**STP_CLK# signal** [] is asserted, or driven low,

**to indicate the power conservation mode** and deasserted, or driven high,

otherwise." (Ex.1007, 7:23-38; FIG. 16.)  Not only does the name "STP_CLK#"

indicate that clock is stopped, Nguyen also refers to its "**power conservation**

**mode,**" such as "**a stop clock mode**."

332.   As such, a POSITA would have recognized and appreciated the

predictable benefit of combining the teachings of Nguyen with those of NEC-

Databook and Burd, that the determination that the µPD751xx-CPU has entered

the STOP or Data Retention mode and that the clock to the CPU has stopped, can

be made readily simply relying on the level (low or high) of a single "STP_CLK#"

signal.

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333. To a POSITA, this combination would have been nothing more than combining prior art elements according to known methods (coupling a signal to a voltage regulator), or simple substitution of one known element for another (a signal indicating the status of the PTO0, PTO1, and/or PCL signals of the µPD751xx-CPU with Nguyen's "STP_CLK#" signal), to obtain the predictable results described above.

334. A POSITA would have also understood this combination to be the use of a known technique (use of power saving modes, as NEC-Databook and Nguyen both describe) to improve a system employing a similar technique (a system in which power supplied to the µPD751xx-CPU that NEC-Databook discloses is regulated using Burd's regulator) in a similar way as NEC-Databook and Nguyen both describe, or applying a known technique (described above) to a known system (NEC-Databook's CPU in combination with Burd's regulator) that is ready for improvement, *e.g.*, by using a readily available STP_CLK# signal, to yield predictable results described above.

335. Additionally, a POSITA would have understood that these predictable, beneficial results can be obtained without requiring substantial changes or modifications to either the microcontroller of the µPD751xx family that NEC-Databook or Burd's regulator, and without adversely affecting the operation

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of these systems or components. A POSITA would have also been able to apply

known, conventional circuitry configuration techniques to perform the necessary

modifications. As such, a POSITA would have expected the combination of NEC-

Databook, Burd, and Nguyen to succeed. For these reasons, it would have been

obvious to a POSITA to combine NEC-Databook, Burd, and Nguyen.

### 2. Claim 2

336. Claim 2 depends from claim 1, and further recites "***the step of***

***determining that a processor is transitioning from a computing mode to a mode***

***in which system clock to the processor is disabled comprises monitoring a stop***

***clock signal.***"

337. The combination of NEC-Databook, Burd, and Nguyen teaches

"*determining that a processor is transitioning from a computing mode to a mode in*

*which system clock to the processor is disabled comprises monitoring a stop clock*

*signal*" because Nguyen discloses using a "**STP_CLK#**" signal (*stop clock signal*)

to control the operation of a voltage regulator.

338. Nguyen "relates to a voltage regulator, such as a switching voltage

regulator." (Ex.1007, 1:6-7.) In particular, Nguyen discloses:

> Referring to FIG. 4, an embodiment 200 of a computer system in
> accordance with the invention includes **voltage regulation circuitry**
> **246** that provides power to components of the computer system 200

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via power lines 242. As described below, the voltage regulation

circuitry 246 has **features that enhance the output voltage accuracy**

**and power conversion efficiency** of the voltage regulation circuitry

246 **when the computer system 200 enters a power conservation**

**mode, such as a stop clock mode**, for example.

(Ex.1007, 2:45-53; FIG. 4.)

339.    More specifically, with reference to its FIG. 5, Nguyen teaches that

"the controller 42 may use a sampled indication of the average $I_L$ current and

regulate the level of the $V_{CORE}$ voltage based on the sampled average," (*id*. 3:22-

24) where "controller 42 samples the average $I_L$ current by periodically activating

sampling circuitry that may include, for example, a switch 47" to obtain "a

sampled voltage (called $V_{DSPS}$)[8]."  (*Id*., 3:35-43; FIG. 5 (annotated).)

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[8] A POSITA would have known "DSPS" to mean "dynamic set point switch" and

"DSPS_DR" to mean "dynamic set point switch drive."  (*See e.g.*, High Speed

Synchronous Power MOSFET Smart Driver SC1405 at 5, Table "Pin Description"

(describing Pin 11 "DSPS_DR").) (Ex.1042).

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340. Nguyen further states: "When the computer system 200 is **not in the power conservation mode**, the controller 42 **closes and opens the switch 47 (via a voltage called DSPS_DR) concurrently with the switch 38** to update the $V_{DSPS}$ voltage" (*id*. 3:45-49) but that:

> For purposes of ensuring that the $V_{DSPS}$ voltage accurately indicates the average $I_L$ current, the regulator 30 **does not open the switch 47 during the power conservation mode**. Instead, the regulator 30 closes the switch 47 for substantially the entire duration of the power conservation mode to continuously provide the voltage across the resistor 46 to the capacitor 82.

(*Id*. 4:7-13.)

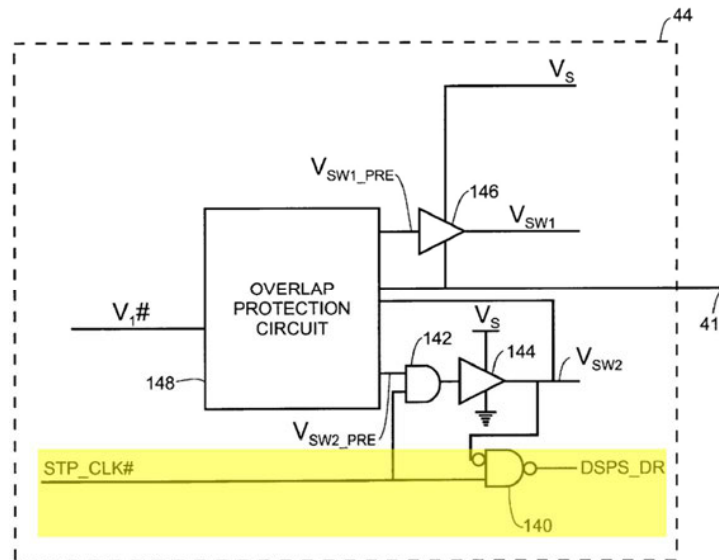341. The above-described power conservation mode based operation of the

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switch 47 is achieved using a STP_CLK# signal (*stop clock signal*), as follows:

> Referring to FIG. 16, the drive circuit 44 includes a voltage buffer, or driver 144, that furnishes the $V_{SW2}$ voltage at its output terminal. An inverted indication of the $V_{SW2}$ voltage is received by an input terminal of a NAND gate 140. Another input terminal of the NAND gate 140 receives a **STP_CLK# signal which is asserted**, or driven low, **to indicate the power conservation mode** and deasserted, or driven high, otherwise. The output terminal of the **NAND gate 140 furnishes a DSPS_DR signal that is received by the gate of the sampling transistor 80**. Therefore, as a result of this arrangement, when the computer system 200 is in the power conservation mode, the NAND gate 140 asserts the DSPS_DR signal to cause the sampling transistor 80 to conduct, and when the computer system 200 is not in the power conservation mode, the state of the DSPS_DR signal closely follows the state of the $V_{SW2}$ voltage.

(*Id.*, 7:23-38; FIG. 16 (annotated).)

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342.    Thus, not only does Nguyen teach a **STP_CLK#** signal, the

STP_CLK# signal also "**indicate[s] the power conservation mode**." This is

analogous to the "stop clock" signal of the '731 patent because, according to the

'731 patent, the "stop clock" signal "signal[s] entry into the deep sleep condition,"

where power consumption is minimized . (Ex.1001, 3:60-65 (describing the use of

the "stop clock" signal for controlling a multiplexor selecting the input to be

provided to a voltage regulator, and specifying the voltage to be provided by the

voltage regulator in the operating mode or sleep mode); FIG. 3; *see id*. 4:19-24

(describing reduction in power usage in the deep sleep state).)  As such, Nguyen

teaches monitoring and using the **STP_CLK# signal**, *i.e.*, "monitoring the stop

clock signal" to control the load current sampling operation of the voltage

controller based on the power conservation mode.

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343. According to Burd a "**new frequency request initiates tracking
mode** in which the converter either delivers or removes charge from the capacitor,
depending upon the sign of $F_{ERR}$. When the error magnitude is less than 4MHz, the
**converter switches to the regulation mode**." (Ex.1006 at 1, cols. 1-2.) The new
frequency request causes Burd's regulator to change (*e.g.*, lower) its output
voltage.

344. In light of Nguyen's teachings, a POSITA would have readily
understood that the transition of Burd's controller from the "regulation mode" to
the "tracking mode" can be controlled using the Nguyen's STP_CLK# signal (a
*stop clock signal*), because the STP_CLK# signal would indicate that the processor
is entering the Data Retention mode, where the voltage to be supplied to the
processor is to be reduced, as NEC-Databook teaches (as discussed for Elements
1[pre]-1[b].

345. As discussed for Element 1[a], NEC-Databook discloses that the
status of output signals PTO0, PTO1, and/or PCL indicates that the STOP
instruction is issued to the µPD751xx-CPU, and the CPU clock is stopped. As
discussed for Element 1[c], these signals can be used to provide a new frequency
request to Burd's regulator, causing it to change (*e.g.*, lower) its output voltage. A
POSITA would have understood that Nguyen's "STP_CLK#" signal can readily

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indicate what the status of NEC-Databook's PTO0, PTO1, and/or PCL signals

indicates, *i.e.*, the clock to the CPU has stopped. As such, the combination of

NEC-Databook, Burd, and Nguyen teaches the limitations of this claim.

346. In summary, the combination of NEC-Databook, Burd, and Nguyen

teaches all the limitations of claim 2, rendering this claim unpatentable as obvious.

**D. GROUND 3: Claim 4 Is Unpatentable as Obvious Over NEC-Databook in View of TI-TPS5210-Datasheet, Further in View of Kikinis**

**1. Motivation to Combine NEC-Databook, TI-TPS5210-Datasheet, and Kikinis**

347. As a threshold matter, NEC-Databook, TI-TPS5210-Datasheet, and

Kikinis disclose techniques in related, in fact, complementary fields. In particular,

NEC-Databook discloses several microcomputer families including the

µPD751XX/75P1xx family, where the CPU therein can be operated at different

voltages in the range of 2.7 to 6.0 V. (*See* Ex.1005 at 31 (disclosing the 2.7 to 6.0

V range) and 62 (disclosing a guaranteed operating range of operating voltages and

cycle times.)

348. NEC-Databook also discloses that its CPU can be placed in different

"standby" modes (also understood as sleep states). In the "Data Retention mode,"

the CPU's static power/energy consumption can be reduced while maintaining its

data and state by lowering the supply voltage to 2 V. (*See* Ex.1005 at 47-48

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(describing the standby modes including the data retention mode within the STOP

mode, and retained data), 32-33 (describing the data memory that is retained), and

42, and 44 (disclosing that stopping the system clock in the data retention mode

stops the CPU clock).)

349.   TI-TPS5210-Datasheet discloses TPS5210, "a synchronous-buck

regulator controller," *i.e.*, a voltage regulator, that "provides an accurate,

**programmable supply voltage to microprocessors**," where the output voltage

can be adjusted to a value "within a **range of 1.3 V to 3.5 V**" or a multiple thereof.

(Ex.1008 at 1.)  TI-TPS5210-Datasheet's regulator employs an "external **resistor**

**divider** from $V_O$ to VSENSE" to regulate the output voltage $V_O$, (*see* TI-TPS5210-

Datasheet at 5 and 21; 19 (Figure 18).)  Kikinis also discloses a resistor divider for

regulating the output voltage of a voltage regulator.  (*See* Ex.1009, 1:62-63; 2:52-

64; FIGS. 3 and 4.)  Moreover, like NEC-Databook, which discloses the STOP and

Data Retention modes of its CPU to save power (*see* Ex.1005, at 47, col. 2; 65,

Figure 19), Kikinis also discloses a processor that can wake up from a sleep mode

to an operating mode.  (*See* Ex.1009, 3:6-13; FIG. 5.)

350.   NEC-Databook, TI-TPS5210-Datasheet, and Kikinis thus disclose

related and complementary systems/techniques because NEC-Databook discloses a

processor that can save power/energy using different operating and standby

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voltages, TI-TPS5210-Datasheet discloses a regulator that can provide several

regulated voltages that partially overlap the voltages required by the processor,

Kikinis discloses a technique for dynamically adjusting a regulator's output

voltage based on its operating state.

351. In particular, while TI-TPS5210-Datasheeet discloses a resistor-

voltage-divider having fixed resistors R2 and R3 (*see* TI-TPS5210-Datasheet at 5;

19, Figure 18), Kikinis teaches that one of these resistors can be adjusted as

needed, allowing for dynamic adjustments to the output voltage. (*See* Ex.1009,

1:62-63 (describing such as technique as prior art); FIG. 3.) Kikinis further

discloses that the value of one of the resistors in a resistor divider can be adjusted

using an electronically controller resistor ladder, depending on whether the CPU in

a sleep state is about to wake up where the CPU activity would increase, and that

by anticipating such increased activity, the voltage regulator can provide an

increased voltage in response to the adjusted value of the resistor in the resistor

divider. (*See id*., 3:6-13; FIG. 5.)

352. In light this, a POSITA would have recognized and appreciated the

predictable benefits of combining the teachings of these references. First, a

POSITA would have recognized that even though NEC-Databook discloses

operating voltages in the range 2.7 to 6 V, and a data retention voltage as low as 2

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V, NEC-Databook does not explicitly disclose an adjustable voltage regulator that can supply such voltages. A POSITA would have known that unless the voltages supplied to the µPD751xx-CPU are adjusted as needed, *e.g.*, based on its workload, the potential of power/energy saving would not materialize.

353. The TPS5210 regulator can adjust its output voltage in the range 1.3 to 3.5 V, and Kikinis teaches a technique for dynamically adjusting the voltage depending on whether the processor to which the voltage is supplied is in an operating state or sleep state. As such, a POSITA would have understood that the TPS5210 regulator can be configured to include Kikinis's R-ladder, and can be coupled to a microcontroller of the µPD751xx family to supply dynamically adjusted voltages in the subrange 2.0 to 3.5 V to the µPD751xx-CPU. This would allow the CPU to be operated at a voltage of 3.5 V and allow the CPU to enter the Data Retention mode at 2.0 V, when the CPU clock is stopped.

354. A POSITA would have recognized that such a configuration can thus predictably yield the benefit of achieving the power/energy saving potential of a µPD751xx family microcontroller. In particular, a POSITA would have understood that configuring the TPS5210 regulator according to Kikinis's teachings and coupling that regulator to the µPD751xx-CPU can minimize its static power/energy consumption, *i.e.*, power/energy consumption when the clock

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to the μPD751xx-CPU is turned off.

355. To a POSITA, this combination would have been nothing more than combining prior art elements according to known methods (coupling a power supply or a voltage regulator to a processor), and/or simple substitution of one known element for another (the TPS5210 regulator for another voltage regulator used with the μPD751xx-CPU, or replacing a fix resistor in a resistor divider with an R-ladder), to obtain the predictable results described above.

356. A POSITA would have also understood this combination to be the use of a known technique (using a power supply that provides several, selectable output voltages, and dynamically adjusting a regulator's feedback voltage using an R-ladder) to improve a system employing a similar technique (a microcontroller of the μPD751xx family that NEC-Databook discloses) in a similar way as TI-TPS5210-Datasheet and Kikinis describe, or applying a known technique (described above) to a known system (NEC-Databook's) that is ready for improvement, *e.g.,* by using a dynamically adjustable voltage regulator, to yield predictable results described above.

357. Additionally, a POSITA would have understood that these predictable, beneficial results can be obtained without requiring substantial changes or modifications to the microcontroller of the μPD751xx family of NEC-

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Databook, TI-PS5210-Datasheet's regulator, or Kikinis's R-ladder circuitry, and

without adversely affecting the operation of these systems or components. A

POSITA would have also been able to apply known, conventional circuitry

configuration techniques to perform the necessary modifications. As such, a

POSITA would have expected the combination of NEC-Databook, TI-TPS5210-

Datasheet, and Kikinis to succeed. For these reasons, it would have been obvious

to a POSITA to combine NEC-Databook, TI-TPS5210-Datasheet, and Kikinis.

### 2. Independent Claim 4

#### a. Elements 4[pre] through 4[b]

358. Elements 4[pre] through 4[b] are substantially the same, respectively,

as Elements 1[pre] through 1[b], as set forth below:

| 1[pre] "A method for reducing power utilized by a processor comprising the steps of:" | 4[pre] "A method for reducing power utilized by a processor comprising the steps of:" |
|---|---|
| 1[a] "determining that a processor is transitioning from a computing mode to a mode in which a system clock to the processor is disabled, and" | 4[a] "determining that a processor is transitioning from a computing mode to a mode in which system clock to the processor is disabled, and" |
| 1[b] "reducing core voltage to the processor to a value sufficient to maintain state during the mode in which said system clock is disabled, | 4[b] "reducing core voltage to the processor to a value sufficient to maintain state during the mode in which system clock is disabled _by:_" |

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| | |
|---|---|
| wherein said value of the core voltage is not sufficient to maintain processing activity in said processor," | |

359.    The differences between the above-listed elements of claims 1 and 4 are indicated by the underlining.  Elements 1[pre] and 4[pre] are identical and so are Elements 1[a] and 4[a].  Element 4[b] is different from Element 1[b] in that Element 1[b] includes the additional limitation "*wherein said value of the core voltage is not sufficient to maintain processing activity in said processor*" that Element 4[b] does not recite.

360.    Therefore, for the reasons provided above in connection with Elements 1[pre]-1[b], NEC-Databook teaches Elements 4[pre]-4[b].

> **b.    Element 4[b.1]: "furnishing an input to reduce an output voltage provided by a voltage regulator furnishing core voltage to the processor, and"**

361.    TI-TPS5210-Datasheet teaches this Element because TI-TPS5210-Datasheet discloses furnishing inputs VID0-VID4 to reduce the TPS5210 regulator's output voltage, which may be supplied as core voltage to NEC-Databook's µPD751xx-CPU.  (Ex.1002, ¶____.)

362.    TI-TPS5210-Datasheet states: "The TPS5210 is a synchronous-buck **regulator** controller which provides an accurate, **programmable supply voltage**

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**to microprocessors**. An internal 5-bit DAC is used to program the reference

voltage to within a **range of 1.3 V to 3.5 V**. The output voltage can be set to be

equal to the reference voltage or to some multiple of the reference voltage."

(Ex.1008 at 1.)  The VID0-VID4 inputs can be adjusted to reduce the reference

voltage $V_{REF}$, and thus, to reduce the output voltage $V_O$ provided by the voltage
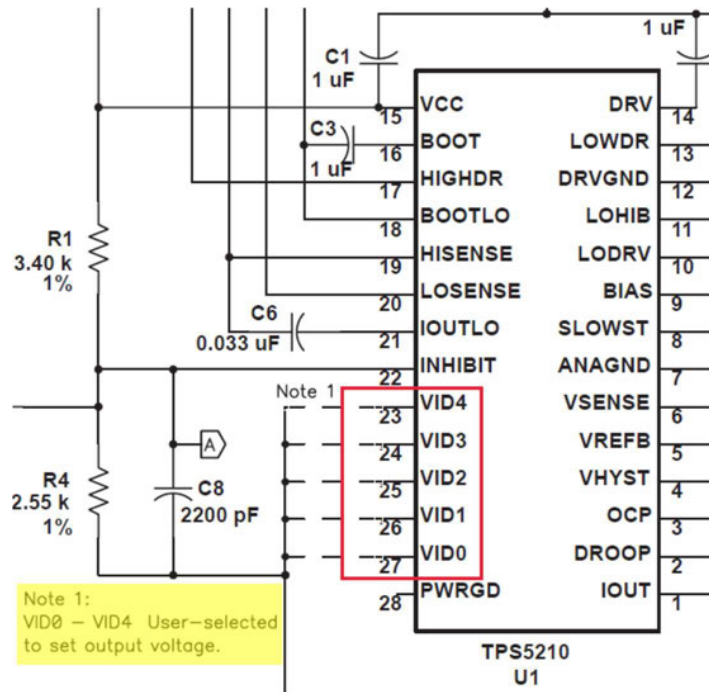
regulator to the processor.

363.   TI-TPS5210-Datasheet states that VID0-VID4 are "[d]igital inputs

that **set the output voltage** of the converter."  (Ex.1008 at 3.)

| VID0 | 27 | I | Voltage Identification input 0 |
|------|----|----|--------------------------------|
| VID1 | 26 | I | Voltage Identification input 1 |
| VID2 | 25 | I | Voltage Identification input 2 |
| VID3 | 24 | I | Voltage Identification input 3 |
| VID4 | 23 | I | Voltage Identification input 4. Digital inputs that set the output voltage of the converter. The code pattern for setting the output voltage is located in Table 1. Internally pulled up to 5 V with a resistor divider biased from $V_{CC}$. |

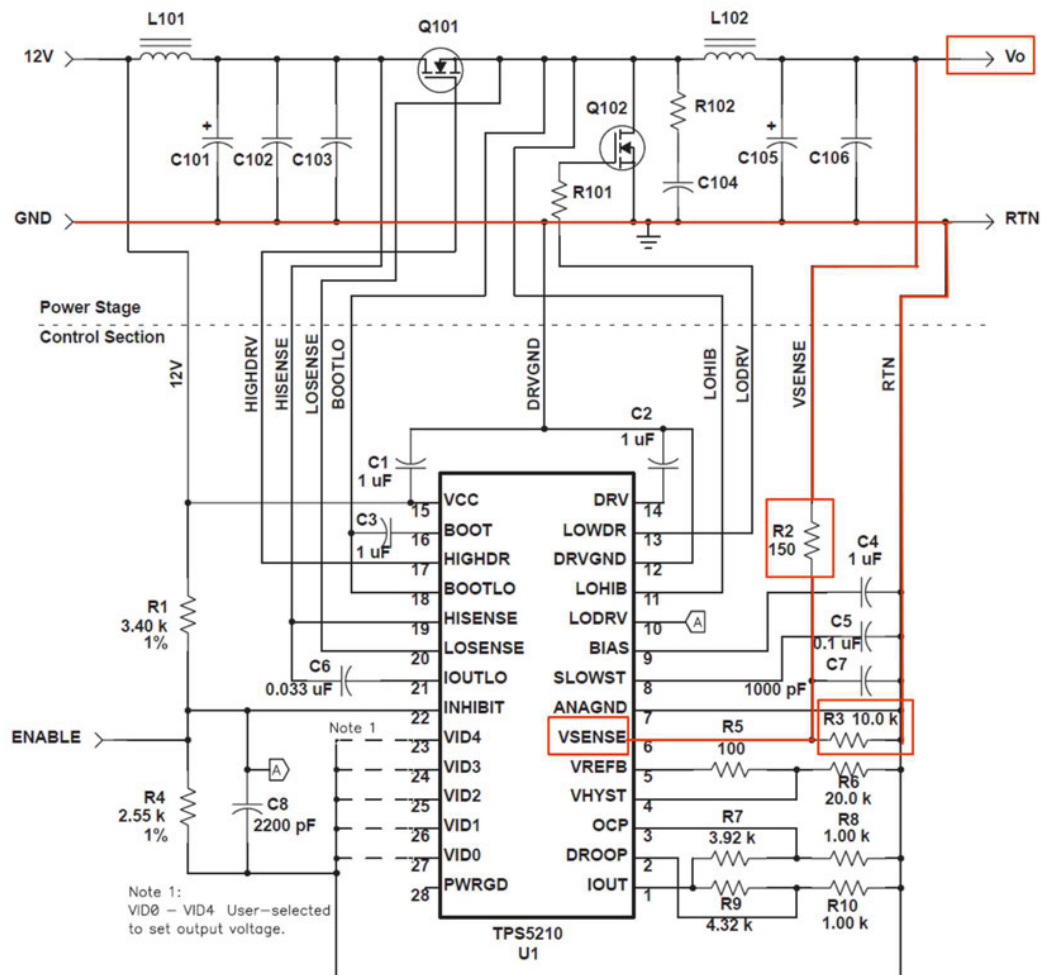(*Id*. at 3, Table: Terminal Functions (partially reproduced and annotated).)

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(*Id*. at 19 (Figure 18 (partial)).)

364.   Table 1 of TI-TPS5210-Datasheet discloses several values of input

VID0-VID4 and the corresponding values of the reference voltage VREF.  (*Id*. at

6-7 (Table 1).)  Additionally, TI-TPS5210-Datasheet discloses "an external

**resistor divider**" coupled between the output voltage $V_O$, a signal VSENSE, and

ground (*Id*. at 5; *see id*. at 19, Figure 18 (depicting the resistor divider having

resistors R2 and R3.)

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(*Id*. at 19, Figure 18 (annotated).)

365.   TI-TPS5210-Datasheet further discloses that "R2 and R3 can [] be used to make small adjusts to the output voltage within the reference-voltage range" according to the Equation:

$$V_O = V_{REF}\left(1 + \frac{R2}{R3}\right)$$

(*Id*. at 21.)

366.   For example, setting VID0-VID4 to "11000" sets $V_{REF}$ to 2.7 V,

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which provides $V_O = 2.7 \times (1 + R2/R3)$ V. Changing VID0-VID4 to "00001"

sets $V_{REF}$ to 2.0 V, providing $V_O = 2.0 \times (1 + R2/R3)$ V. Likewise, changing

VID0-VID4 to "00010" sets $V_{REF}$ to 1.95 V, providing $V_O = 2.7 \times (1 + R2/R3)$

V. (*See* Ex.1008 at 6-7 (Table 1).)

367. Since resistor values are greater than or equal to zero, for any given

pair of values of resistors R2 and R3, $V_O$ can be reduced by changing VID0-VID4,

*e.g.*, from "11000" to "00001" or to "00010." Thus, by furnishing the input VID0-

VID4, TPS5210 regulator's output voltage can be reduced. (*See* Ex.1008 at 21

(stating that "[v]alues between 1.3 V and 3.5 V can be easily set by shorting the

correct VID inputs to ground").)

368. Thus, TI-TPS5210-Datasheet discloses "*furnishing an input* [VID0-

VID4] *to reduce an output voltage* [$V_O$] *provided by* [the TPS5210] *voltage*

*regulator furnishing core voltage to the processor*," *e.g.*, NEC-Databook's

µPD751xx-CPU and, thus, teaches this Element. (Ex.1002, ¶____.)

   c. **Element 4[b.2]: "providing a feedback signal to the**
     **voltage regulator to reduce its output voltage below a**
     **specified output voltage."**

369. The combination of NEC-Databook, TI-TPS5210-Datasheet, and

Kikinis teaches this Element. The following is an overview of the discussion

below. As discussed for Element 4[b.1], TI-TPS5210-Datasheet discloses

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providing a feedback signal VSENSE to regulate the output voltage $V_O$ of its

regulator. The signal VSENSE is derived using a resistor divider.

370. Kikinis teaches a similarly configured voltage regulator, but where

one of the resistors in the resistor divider is replaced with an electronically

controller R-ladder. This allows the feedback signal to be changed dynamically, so

that the regulator's output voltage can be raised or lowered dynamically.

Moreover, Kikinis discloses that the voltage adjustment can be performed based on

whether the processor is in the sleep mode or operating mode, which can save

power. As discussed under Ground 1 for Element 1[a], NEC-Databook discloses

that the status of the signals PTO0, PTO1, and/or PCL can determine whether the

µPD751xx-CPU is in the STOP mode.

371. Accordingly, a POSITA would have understood that one of the

resistors in TI-TPS5210-Datasheet's resistor divider can be replaced with Kikinis's

R-ladder, and that R-ladder can be controlled using the status of NEC-Databook's

PTO0, PTO1, and/or PCL, *i.e.*, based on whether the µPD751xx-CPU is in the

Operation or STOP mode. A POSITA would have also understood that controlling

the R-ladder in this manner would cause the TPS5210 regulator's feedback signal

VSENSE to change.

372. Therefore, a POSITA would have further understood that controlling

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the R-ladder could cause the TPS5210 regulator's output voltage to be lowered

below one or more specified output voltages, and would thus constitute "*providing*

*a feedback signal to the voltage regulator to reduce its output voltage below a*

*specified output voltage.*"

> i. **TI-TPS5210-Datasheet discloses "providing a feedback signal to the voltage regulator"**

373.  As discussed for Element 4[b.1], the output voltage of TI-TPS5210-

Datasheet's regulator ($V_O$) is given by $V_O = V_{REF}\left(1 + \frac{R2}{R3}\right)$.  (*See* Ex.1008 at 21.)

Therefore, $V_O$ is determined in part by $V_{REF}$ and in part by the values of resistors

R2 and R3.

374.  R2 and R3, which form "an external resistor divider," determine the

voltage VSENSE at the input terminal VSENSE.  (*See* Ex.1008 at 5, 19 (Figure

18).)  Because R2 and R3 form a resistor divider, a POSITA would have

understood that the voltage VSENSE is given by $VSENSE = V_O\left(\frac{R2}{R2+R3}\right)$.

VSENSE is a feedback signal because it is derived from the output voltage $V_O$ and

is also used to determine $V_O$.

375.  Specifically, in TI-TPS2110-Datasheet, the "Terminal Functions"

table lists an input VSENSE that is to "be **connected to converter output voltage**

bus **to sense and control output voltage**."  (Ex.1008 at 3, Table: Terminal

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Functions (partially reproduced).)

| VSENSE | 6 | I | Voltage sense Input. To be connected to converter output voltage bus to sense and control output voltage. It is recommended an RC low pass filter be connected at this pin to filter noise. |
|--------|---|---|---|

376.    TI-TPS5210-Datasheet depicts that the input VSENSE is connected to

the converter output voltage not directly but via a resistor-voltage-divider formed

by the resistors R2 and R3, to provide the voltage VSENSE at the input VSENSE.
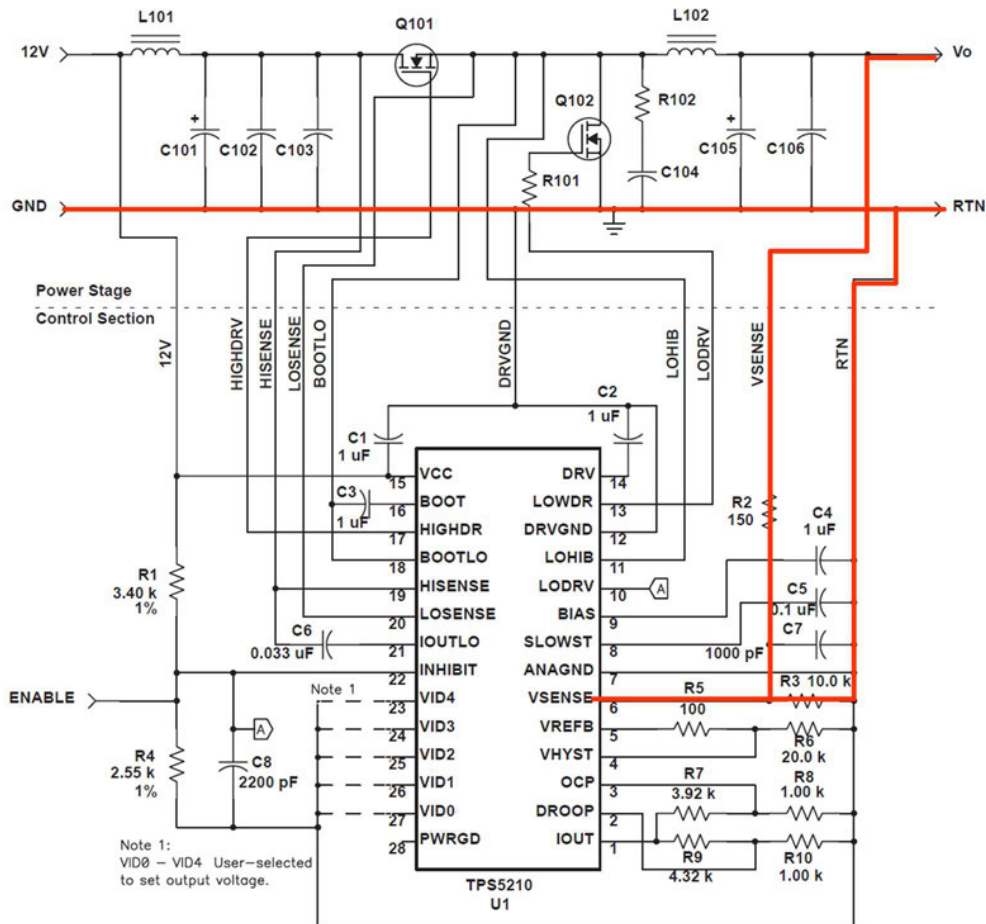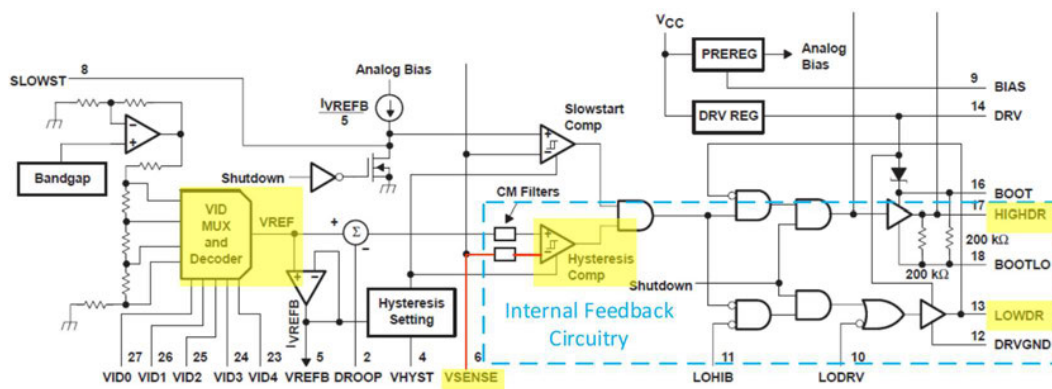
(Ex.1008 at 19, Figure 18.)



Figure 18. Standard Application Schematic

(Ex.1008 at 19, Figure 18 (annotated).)

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377. TI-TPS5210-Datasheet also depicts in Figure "functional block

diagram" and in "Figure 18" that the input VSENSE is electrically connected to the

output voltage $V_O$ in a feedback loop, because the input VSENSE and the signal

$V_{REF}$ are supplied to the difference amplifier "Hysteresis Comp" that controls two

drive signals, namely, HIGHDR and LOWDR. These drive signals control high-

side and low-side "power switching FETs" that, in turn, regulate the output voltage

$V_O$.



(Ex.1008 at 2, "functional block diagram" (partial, annotated); at 3 (Table:

"Terminal Functions" (describing HIGHDR as "Output drive to high-side power

switching FETs" and LOWDR as "Output drive to synchronous rectifier FETs")).)

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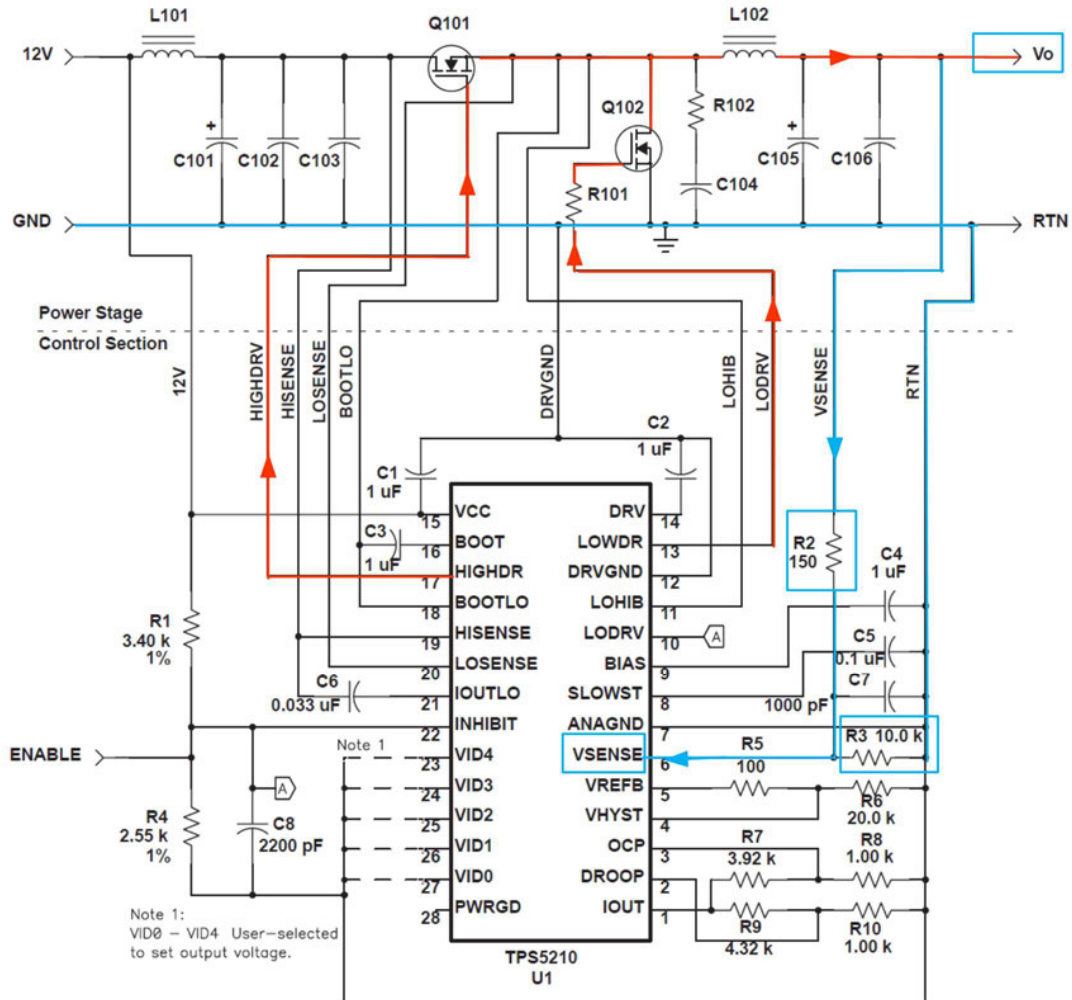


(Ex.1008 at 19, Figure 18 (annotated to show electrical paths from HIGHDR and

LOWDR to V$_O$).)

378.    Thus, since VSENSE is derived from V$_O$ and also controls V$_O$, it is a

"*feedback signal to*" TPS5210, "*the voltage regulator*."  Specifically, the resistor

divider R2/R3 generates **VSENSE from V$_O$**, circuitry that is internal to the

TPS5210 regulator controller and that is driven by the voltage signal **VSENSE**

**provides the signals HIGHDR and LOWDR**, and the external circuitry including

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high-side FET and low-side FET that are driven by the signals HIGHDR and

LOWDR, together, **control the output voltage $V_O$** in a loop and, together,

constitutes a feedback circuit.  Therefore, TI-TPS5210-Datasheet discloses

"*providing a feedback signal to the* [TPS5210] *voltage regulator*."

> ii.   **Kikinis teaches that this feedback signal can be adjusted, based on whether or not the processor to which the regulator's output voltage is supplied is in the sleep state, to reduce the output voltage**

379.   Kikinis discloses a configuration similar to that of TI-TPS5210-

Datasheet, where the output of a voltage regulator is controlled via a resistor

divider based feedback, but where the resistor coupled between the regulator's

feedback input (VSENSE of TI-TPS5210-Datasheet) and ground, *i.e.*, resistor R3

of TI-TPS5210-Datasheet, is adjustable, so that the output voltage can be raised or

lowered, as needed.

380.   Specifically, Kikinis discloses a "voltage regulator with an

electrically-erasable programmable read-only memory electronically accessible for

storing a feedback reference coefficient for control."  (Ex.1009, Abstract.)  In

discussing FIG. 3 in the "Background of the Invention," Kikinis discloses the

"details of a switching voltage regulator chip with a resistor or **potentiometer**."

(Ex.1009, 1:62-63; FIG. 3.)  A POSITA would have known that a potentiometer is

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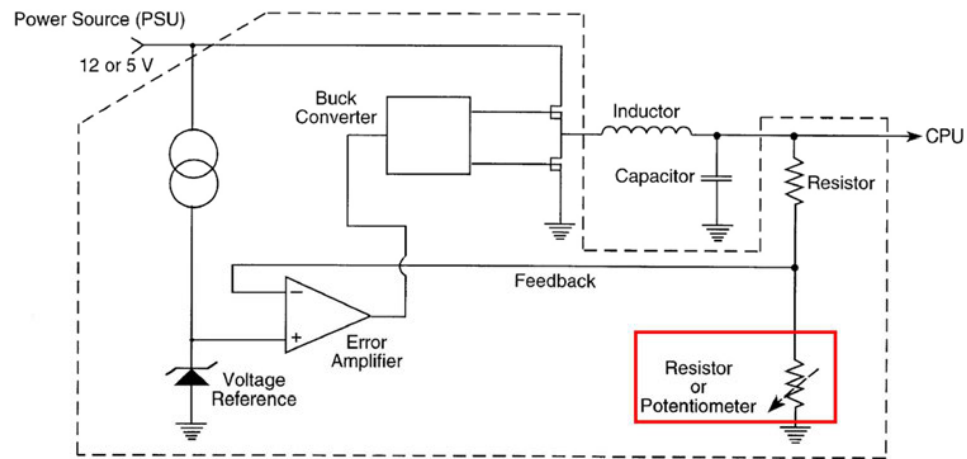U.S. Patent No. 7,260,731

a variable resistor.



Fig. 3 (Prior Art)

(Ex.1009, FIG. 3.)

381. Kikinis further states:

FIG. 2 shows a switching voltage regulator 11 with an erasable
EPROM (E$^2$) 13 that holds a coefficient for feedback loop voltage
regulation. To **adjust the output** value of the regulator, a serial **data
stream can be clocked into a register 15** until the desired value is
obtained. At this point, that value can be stored in the E$^2$ by means of
a line not shown. The stored value can be read permanently and is
easily changed again, if required, without manual adjustment.

In FIG. 4 the potentiometer of FIG. 3 is replaced by an **external E$^2$ 19
and an R-ladder 21 to adjust the output voltage**. **Data** and clock
**values are input to register 23** upon system initialization.

(Ex.1009, 2:52-64; FIG. 4.)

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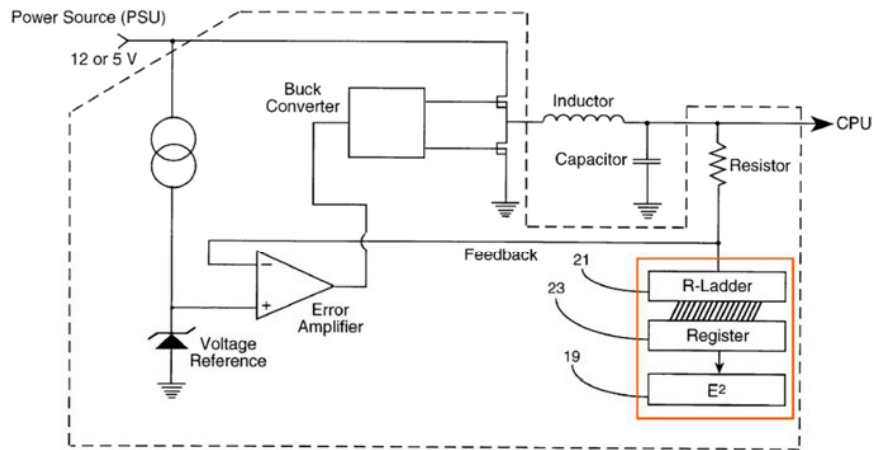U.S. Patent No. 7,260,731



Fig. 4

(Ex.1009, FIG. 4.)

382. In addition, with reference to FIG. 5 Kikinis discloses receiving a signal indicating that CPU activity is about to change (entering or leaving a sleep state), allowing the voltage regulator to adjust the output voltage:

> Voltage regulator 25 receives a **prewarning based on a wake-up mechanism 27**. Signals on interrupt lines (NMI. INT, SMI) to CPU 29 are sensed and combined with some logic (e.g., PAL). The resulting lines send a **warning on path 31 to voltage regulator 25** of imminent activity by the CPU, with dramatically increased current requirements. Thus the **voltage regulator can take countermeasures in anticipation of CPU activity**.

(Ex.1009, 3:6-13; FIG. 5.)

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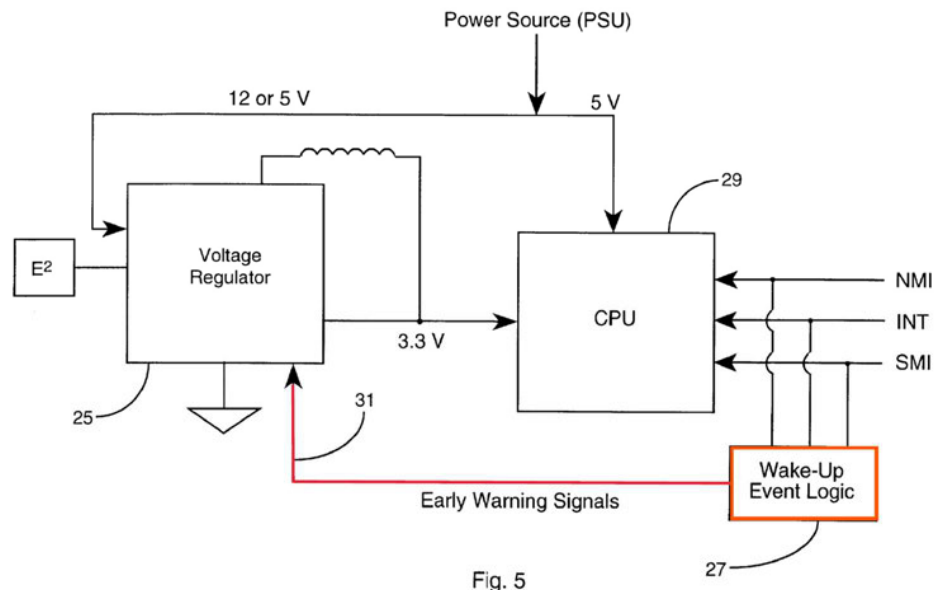U.S. Patent No. 7,260,731



Fig. 5

(Ex.1009, FIG. 5.)

383. Claim 1 of Kikinis recites: "the voltage magnitude at the regulated output may be **raised or lowered** by resetting the digital value in the digital register and transferring the digital register value to the programmable non-volatile memory; wherein the **digital value controls a resistor ladder (R-ladder) to manage feedback voltage** to the adjustment circuitry." (Ex.1009, 3:49-59; *see id.* 3:31-59 (Claim 1).) As such, a POSITA would have understood that the register 23 may have a default (or reset) value and a programmed value, both stored in the EEPROM 19, where the R-ladder 21 can be controlled according to the default and programmed values to raise or lower the output voltage of the regulator.

384. In addition, a POSITA would have understood the "early warning signals" 31 of Kikinis to be functional equivalents of the signals PTO0, PTO1,

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and/or PCL disclosed by NEC-Databook, because the "early warning signals" 31

indicate that the processor is about to wake up from a sleep state, and the outputs

PTO0, PTO1, and/or PCL can indicate that the μPD751xx-CPU has entered the

STOP or data retention mode (sleep state). (*See* Ex.1005 at 29, col. 2; 28 (Figure

"Block Diagram"); 42, col. 1; 44 (Figure 5); 45 (Figure 7); 48 (Table 7).)

> iii. **The combination of NEC-Databook, TI-TPS5210-Datasheet, and Kikinis teaches providing a feedback signal to the TPS5210 voltage regulator to reduce its output voltage below a specified output voltage**

385. In light of TI-TPS5210-Datasheet's output voltage equation $V_O =$

$V_{REF}\left(1 + \frac{R2}{R3}\right)$ (TI-TPS5210-Datasheet at 21), a POSITA would have readily

understood that if R3 is much larger than R2, *e.g.*, 100 times larger, the scaling

factor $\left(1 + \frac{R2}{R3}\right) \approx 1$ and, hence, $V_O \approx V_{REF}$. For example, suppose R2 = 1 Ω and

R3 = 100 kΩ. Additionally, suppose VID0-VID4 = "11000," setting $V_{REF}$ to 2.7

V. (Ex.1008 at 6-7 (Table 1).) This would provide $V_O \approx 2.7$ V, which is one

specified output voltage of the TPS5210 regulator.

386. From TI-TPS5210-Datasheet's output voltage equation $V_O =$

$V_{REF}\left(1 + \frac{R2}{R3}\right)$ (Ex.1008 at 21), a POSITA would have also understood that instead

of R3 being 100 times larger than R2, if R3 is only four times (or two times) as

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large as R2, $V_O$ would be (1.25 × $V_{REF}$) (or (1.5 × $V_{REF}$)). A POSITA would

have further understood that to obtain such dynamic control of the output voltage,

the resistor R3 disclosed in TI-TPS5210-Datasheet may be replaced with the

Kikinis' circuitry including the resistor ladder (R-ladder 21), the register 23, and

the EEPROM 19, and that the "early warning signals" 31 in combination with the

signals PTO0, PTO1, and/or PCL that NEC-Databook discloses can be used to

control the register 23 and the R-ladder 21.

387. Additionally, a POSITA would have understood that the register 23

can have a small default value, *e.g.*, four (or two) times R2 of TI-TPS2510-

Datasheet, and a relatively large programmed value, *e.g.*, 100 times R2, so that the

output voltage $V_O$ of the TI-TPS5210-Datasheet's voltage regulator can be

dynamically adjusted (raised or lowered) based on the "early warning signals" 31

and the signals PTO0 and PTO1, *i.e.*, when the μPD751xx-CPU is in the operating

state or data retention state, respectively.

388. As one example, a POSITA would have understood for the values of

VID0-VID4 of TI-TPS5210-Datasheet of "00001," the value of $V_{REF}$ would be 2.0

V. (*See* TI-TPS5210-Datasheet at 6-7, Table 1.) For a value of R2 of 100 Ω and a

default value of R-ladder 21 of 200 Ω (two times R2), a POSITA would have

recognized that per the Equation $V_O = V_{REF}\left(1 + \frac{R2}{R3}\right)$ (TI-TPS5210-Datasheet at

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21), $V_O = 1.5 \times V_{REF} = 3.0$ V. A POSITA would have also recognized that a programmed value of R-ladder 21 of 10 kΩ (100 times R2), $V_O = 1.01 \times V_{REF} = 2.02$ V.

389. As such, a POSITA would have recognized that when the "early warning signals" input indicate that the processor (*e.g.*, μPD751xx-CPU) is about to wake up, the R-ladder 21 would be reset and controlled by the default value of the register 23. The R-ladder 21 would be controlled to a resistance value that is a relatively small multiple of R2 (*e.g.*, two times according to the foregoing example). In this case, a POSITA would have recognized that the output voltage $V_O$ would be raised above $V_{REF}$ (*e.g.*, ($1.5 \times V_{REF}$) or 3.0 V in the foregoing example). Here, the output voltage $V_O$ is greater then **"a specified output voltage" of 2.7 V (corresponding to VID0-VID4 set to "11000")**. (Ex.1008 at 6-7 (Table 1).)

390. A POSITA would have also recognized that for the same VID0-VID4 value of "00001," a programmed R-ladder 21 value of 10 kΩ (100 times R2) results in an output voltage of 2.02 V ($V_O = 1.01 \times V_{REF} = 2.02$ V), which is **below the "specified output voltage" of 2.7 V**.

391. It is discussed under Ground 1 for Element 1[a], that NEC-Databook discloses output signals PTO0, PTO1, and/or PCL, the status of which may be used

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to determine that the μPD751xx-CPU is transitioning from the Operation mode to

the STOP mode in which the CPU clock is stopped or disabled. In this

combination, a POSITA would have understood that the status of NEC-Databook's

signals PTO0, PTO1, and/or PCL (indicating that the μPD751xx-CPU has entered

the STOP mode), can be used to switch the values of R-ladder 21. This would

change the feedback signal VSENSE, causing the output voltage to reduce below

"a specified output voltage" of 2.7 V. Accordingly, the "*feedback signal*"

VSENSE is provided "t*o the* [TPS5210] *voltage regulator to reduce its output*

*voltage below a specified output voltage*."

392. In summary, NEC-Databook in view of TI-TPS5210-Datasheet,

further in view of Kikinis teaches or at least suggests each and every element of

claim 4, rendering claim 4 unpatentable as obvious.

### 3.  Claim 5

393. Claim 5 depends from claim 4, and further recites: "***the output voltage***

***to which said voltage regulator is reduced depends upon output voltage of said***

***voltage regulator prior to furnishing the input to reduce the output voltage***

***provided by the voltage regulator.***"

394. The '731 patent describes this as dropping from 1.2 V down to 0.6-0.7

V, but dropping from 1.5 V down to 0.9-1 V. The output voltage is reduced to

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either 0.6-0.7 V or to 0.9-1 V depending on whether the output voltage started at

1.2 V or 1.5 V prior to the reduction. (Ex.1001, 4:63-5:6.)

395.  The combination of NEC-Databook, TI-TPS5210-Datasheet, and

Kikinis teaches this claim element. Specifically, the two values of R3 (as provided

by the R-ladder) in the resistor-voltage-divider cause the high and reduced output

voltages to depend on each other. For instance, using a $V_{REF}$ of 2.0 V, the output

voltage drops from 3.0 V to 2.02 V. Using a $V_{REF}$ of 2.2 V (corresponding to

VID0-VID4 of "11101") (Ex.1008 at 6), the output voltage drops from 3.3 V to

2.222 V. Thus, the voltage to which the TPS5210 regulator's output voltage is

reduced (*e.g.*, 2.02 V or 2.222 V) "*depends upon*" the regulator's prior output

voltage (e.g., 3.0 V or 3.3 V), *i.e.*, output voltage "*prior to furnishing the input to*

*reduce the output voltage provided by the voltage regulator*."

396.  As discussed above for claim 4, for a selected value of TI-TPS5210-

Datasheet's VID0-VID4, and for a low R-ladder value of Kikinis, the output

voltage $V_O$ of the TPS5210 regulator is high (*e.g.*, NEC-Databook's $V_{DD}$). For the

same values of VID0-VID4, when the R-ladder is switched to a high value, $V_O$ is

reduced from the high value to a low value (*e.g.*, from $V_{DD}$ to $V_{DDDR}$, per NEC-

Databook). This change occurs in response to supplying the status of NEC-

Databook's PTO0, PTO1, and/or PCL as an input to switch the value of Kikinis's

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R-ladder included in the TPS5210 regulator's feedback network.

397. In both cases, since the VID0-VID4 value is the same, the reference voltage $V_{REF}$ of the TPS5210 is also the same. Since $V_O$ is a respective multiple of the same $V_{REF}$ for both the high and low output voltage values, the reduced value of $V_O$ depends on the higher value thereof, *i.e.*, the "*output voltage of said voltage regulator prior to furnishing the input to reduce the output voltage.*"

398. As discussed under this Ground for Element 4[b.2], when Kikinis's early warning signals input becomes active and, thereafter, the status of the signals PTO0, PTO1, and/or PCL that NEC-Databook discloses indicates that these signals are not changing, the output voltage $V_O$ of the TPS5210 controller ("*voltage regulator*") is adjusted as a multiple of $V_{REF}$, where the particular multiple is determined by the default value of Kikinis' controllable resistor ladder 21. In the example discussed for Element 4[b.2], that multiple is 1.5 and $V_O = 1.5 \times V_{REF}$. (*See* Ex.1008 at 21.)

399. When the status of the signals PTO0, PTO1, and/or PCL that NEC-Databook discloses indicates that these signals are not changing, indicating that the µPD751xx-CPU has entered the STOP mode (sleep state), the output voltage $V_O$ of the TPS5210 controller is determined as another, different multiple of $V_{REF}$, where the other multiple is determined by the programmed value of Kikinis' controllable

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resistor ladder 21. In the example discussed for Element 4[b.2], that multiple is

1.01 and $V_O = 1.01 \times V_{REF}$. (*See* Ex.1008 at 21.)

400. Since in both cases the output voltage $V_O$ is a respective multiple of

$V_{REF}$, and because $V_{REF}$ is determined by inputs VID0-VID4 (*see* TI-TPS5210-

Datasheet at 6-7 (Table 1)), for a specified value of VID0-VID4, *e.g.*, "00001" as

also discussed under this Ground for Element 4[b.2], the value to which the output

voltage $V_O$ reduces when the status of the signals PTO0, PTO1, and/or PCL that

NEC-Databook discloses indicates that these signals are not changing, depends on

the value of the output voltage $V_O$ when the status of the signals PTO0, PTO1,

and/or PCL indicated that those signals were changing.

401. For instance, in the example above, the lowered value of $V_O$ is $\frac{1.01}{1.50} =$

0.6733 times the prior value of $V_O$, before the status of the signals PTO0, PTO1,

and/or PCL indicated that those signals were not changing, *i.e.*, "*input to reduce*

*the output voltage provided by the voltage regulator*" was provided. Thus, the

lowered value of $V_O$ is a fraction of the prior value of $V_O$ and, thus, depends on the

prior value. Accordingly, NEC-Databook in view of TI-TPS5210-Datasheet,

further in view of Kikinis teaches all of the limitations recited this claim, rendering

it unpatentable as obvious.

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**E.** **GROUND 4: Claims 8-10 and 14 Are Unpatentable as Obvious Over Helms in View of Maxim-165X-Datasheet, Further in View of MAX1711-Kit**

**1.** **Motivation to Combine Helms, Maxim-165X-Datasheet, and MAX1711-Kit**

402. Helms, Maxim-165X-Datasheet, and MAX1711-Kit all disclose systems and techniques in the closely related field of regulated power/voltage systems for processors. In particular, Helms discloses a system in which core voltage is supplied to a processor using a voltage regulator that can output a voltage as specified at the regulator's input. (*See* Ex.1010, Abstract; 2:42-54.) Helms also states that "[o]ne example of a programmable voltage converter is a MAXIM MAX1711 High-Speed, Digitally Adjusted Step-Down Controller or its equivalent," (*id*., 3:18-20.) Maxim-165X-Datasheet and MAX1711-Kit both disclose efficient step-down controllers (voltage regulators) for powering notebook computers / CPUs. (*See* Ex.1011 at 1, col. 1; Ex.1012 at 1, col. 1.)

403. Helms discloses selection circuitry coupled to the voltage regulator, where the selection circuitry can select between a value (OVID) indicating an operating voltage and a value (SVID) indicating a sleep voltage, and where the selected value (MVID) is provided to the input of the voltage regulator, so that the regulator may supply a core voltage corresponding to the selected value, *i.e.*, an operating voltage or a sleep voltage. (*See* Ex.1010, 2:42-54.)

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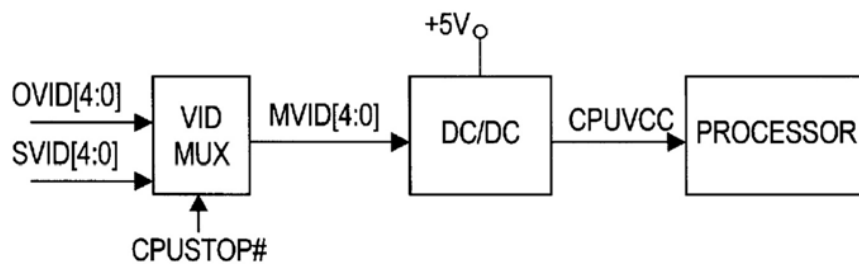


FIG. 1

(*Id.*, FIG. 1.).

404.   A POSITA would have recognized that in addition to the benefit of

the selection circuitry that Helms describes, "ensuring that the processor is always

supplied with a voltage at which it will be operational when the system is powered

on," (*id.*, 4:28-31; *see id.*, 1:35-37), providing different voltages to a processor

when it is in different modes can provide another benefit of saving power/energy.

Specifically, a POSITA would have known that the sleep voltage provided to a

processor can be less than the operating voltage, and it was well known before

2000 that the power consumption of a processor is proportional to the square of the

supplied core voltage.  As such, a POSITA would have recognized that even a

small reduction in the core voltage can result in a significant power/energy saving.

405.   Maxim-165X-Datasheet discloses step-down controllers (voltage

regulators) that can be operated in two modes, namely the pulse-width modulation

(PWM) mode and pulse-frequency modulation (PFM) mode.  (*See* Ex.1011 at 1,

col. 1.)  A POSITA would have recognized the PWM and PFM as common modes

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of operating a switching regulator (which is a term of art, as discussed under

Technology Background).

406.  Maxim-165X-Datasheet also describes that the PWM mode is

preferred under heavy load conditions and that the PFM mode may be more

efficient under light load conditions.  (*See id*. at 1, col. 1; 10, col. 2, and 12, col. 1.)

Regardless, Maxim-165X-Datasheet discloses that using the $\overline{\text{SKIP}}$ input, the PWM

mode can be forced even under light load conditions, *e.g.*, to reduce noise.  (*see id*.

at 16, col. 2-17, col. 1.)

407.  MAX1711-Kit discloses MAX1711, a "buck-regulator" (*i.e.*, a step-

down voltage regulator) that, like the regulators that Maxim-165X-Datasheet

discloses, can be operated in PWM or PFM modes, and where the **PWM mode**

**can be forced via the $\overline{\text{SKIP}}$ input**.  (*see* Ex.1012 at 2, col. 2; 3, col. 2.)  In

addition to the benefit of reducing the noise by forcing the PWM mode, as Maxim-

165X-Datasheet discloses (*see* Ex.1011 at 16, col. 2 – 17, col. 1), MAX1711-Kit

discloses another benefit of forcing the PWM mode when transitioning from a high

to a low voltage.

408.  In particular, as Maxim-165X-Datasheet describes, the PFM mode is

typically an efficient mode of operation when the load is light, *e.g.*, when the

voltage supplied by the regulator is low.  (*See id*. at 1, col. 1 (describing switching

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to the PFM mode when the load is light).) A POSITA would have known this to

be generally true when the load and the output voltage of a regulator are stable.

409. MAX1711-Kit discloses, however, that when the voltage regulator is

required to decrease it output voltage, the PFM mode can be inefficient **during the**

**time it takes for the high-to-low voltage transition**, even though the PFM mode

may be more efficient than the PWM mode once the transition is complete. (*See*

Ex.1012 at 3, col. 2.) To address this inefficiency **during the time of voltage**

**transition**, MAX1711-Kit discloses forcing the PWM mode using the $\overline{\text{SKIP}}$ **input**.

(*See id*. at 4, col. 1.)

410. A POSITA would have therefore recognized and appreciated the

predictable benefits of combining the teachings of these three references. First,

even though Helms discloses supplying operating and sleep voltages to a processor

in the operating and sleep modes, respectively, and a POSITA would have

recognized that this can reduce the processor's power consumption, a POSITA

would have also recognized that the voltage regulator also consumes some power

for its operation and that reducing such power can be beneficial.

411. Therefore, a POSITA would have considered using a voltage regulator

such as those that Maxim-165X-Datasheet describes, that can automatically select

an efficient mode of operation when the load is light, and can thus predictably

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consume less power.  (*See* Ex.1011 at 1, col. 1 (describing regulators that

"automatically switch between PWM operation at heavy loads and pulse-

frequency-modulated (PFM) operation at light loads to optimize efficiency over

the entire output current range").)

412.   A POSITA would have further understood that while allowing the

PFM operation when the output voltage is stable, forcing the PWM mode while the

voltage is transitioning from a high value to a low value can predictably reduce the

power consumption of the regulator further, as MAX1711-Kit teaches.  (*See*

Ex.1012 at 3, col. 2.)

413.   To a POSITA, this combination would have been nothing more than

combining prior art elements according to known methods (incorporating the

different operating modes and a strategy for their use into Helms' voltage

regulator), to obtain the predictable results described above.

414.   A POSITA would have also understood this combination to be the use

of a known technique (using a regulator that can be operated in two modes, based

on its load, and controlling the mode transition to maximize regulator efficiency) to

improve a system employing a similar technique (Helms' system) in a similar way

as Maxim-165X-Datasheet and MAX1711-Kit describe, or applying a known

technique (described above) to a known system (Helms') that is ready for

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improvement, *e.g.*, operating a regulator in two modes in a controlled manner, to yield predictable results described above.

415.   Additionally, a POSITA would have understood that these predictable, beneficial results can be obtained without requiring substantial changes or modifications to either the regulator that Helms describes (because Helms explicitly contemplates a regulator similar to MAX1711 (*see* Ex.1010, 3:18-20), or the regulators that Maxim-165X-Datasheet and MAX1711-Kit describe, and without adversely affecting the operation of these systems or components.

416.   A POSITA would have also been able to apply known, conventional circuitry configuration techniques to perform the necessary modifications.  As such, a POSITA would have expected the combination of Helms, Maxim-165X-Datasheet, and MAX1711-Kit to succeed.  For these reasons, it would have been obvious to a POSITA to combine Helms, Maxim-165X-Datasheet, and MAX1711-Kit.

### 2.   Independent Claim 8

#### a.   Element 8[pre] "A circuit for providing a regulated voltage to a processor comprising:"

417.   To the extent this preamble is limiting, Helms teaches a "*circuit for providing a regulated voltage to a processor*" because Helms discloses a system
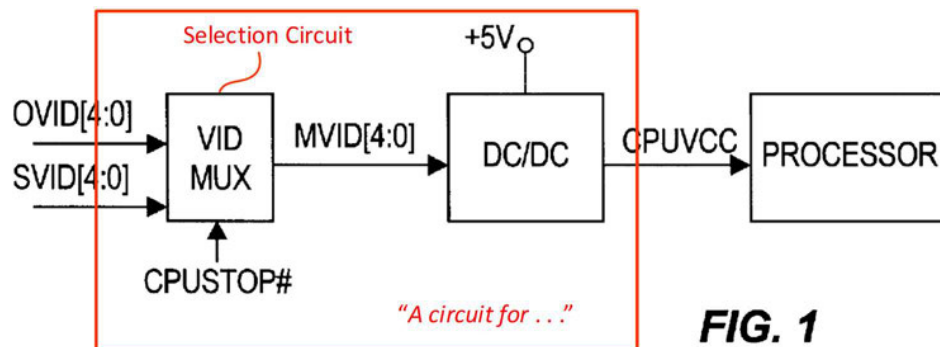
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that "includes a DC/DC power converter, a processor, and a selection circuit."  The

DC/DC power converter provides to the processor a "power output signal having a

voltage indicated by [a] voltage setting signal" (*regulated voltage*).  As such, the

DC/DC power converter" and the "selection circuit" together constitute a "*circuit*

*for providing a regulated voltage to a processor*."

> 418.   In particular, Helms states:
>
> [A] system includes **a DC/DC converter, a processor, and a**
> **selection circuit. The DC/DC converter** receives a voltage setting
> signal or signals from the selection circuit and **provides an**
> **adjustable power output signal having a voltage indicated by the**
> **voltage setting signal**. The processor is powered by the adjustable
> power output signal.

(Ex.1010, Abstract.)



(Helms, FIG. 1 (annotated)).

419.   Helms's DC/DC converter (a voltage converter) can be a voltage

regulator such as "MAXIM MAX1711" "or its equivalent" providing a regulated

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voltage to the processor. (*See* Ex.1010, 3:18-20.) Providing the "adjustable power output signal having a **voltage indicated by the voltage setting signal**" constitutes providing a "*regulated voltage*." Therefore, the selection circuit and the DC/DC converter together form a "*circuit for providing a regulated voltage to a processor*" and, thus, Helms teaches the preamble of claim 8.
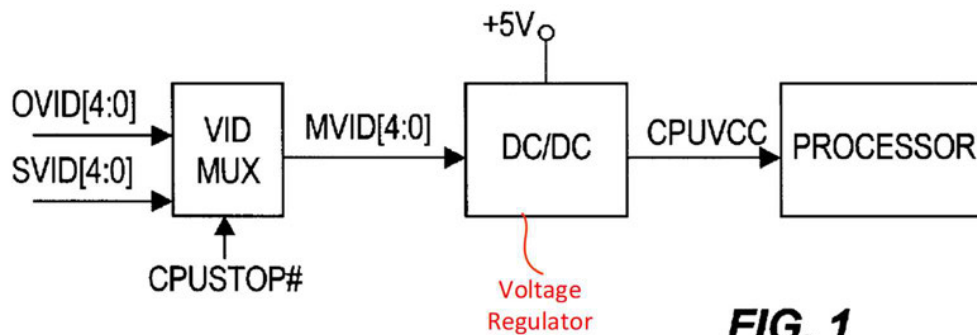
### b. Element 8[a] "a voltage regulator having:"

420. Helms teaches "*a voltage regulator*" because Helms describes a "**DC/DC power converter**" that provides to a processor a "power output signal having a **voltage indicated by [a] voltage setting signal**." As such, the DC/DC power converter is a voltage regulator.

421. Specifically, Helms states:

> FIG. 1 shows a processor receiving a power supply voltage signal (CPUVCC) from a **programmable voltage converter (DC/DC)**. The **converter** receives power (in this case +5V) and a voltage setting signal (MVID), and **provides a regulated output voltage at the level indicated by the voltage setting signal**.

(Ex.1010, 2:42-47; FIG. 1 (annotated).)

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FIG. 1

422. Helms also states: "One example of a programmable voltage converter is a **MAXIM MAX1711** High-Speed, Digitally Adjusted Step-Down Controller or its equivalent." (*Id.*, 3:18-20.) Well before 2000, MAX1711 was a well-known voltage regulator. Thus, Helms teaches "*a voltage regulator.*"

      c.      **Element 8[a.1] "an output terminal providing a selectable voltage, and"**

423. Helms teaches "*an output terminal providing a selectable voltage*" because the DC/DC converter that Helms describes has a terminal (*output terminal*) connected to a processor, where the terminal provides a regulated voltage signal CPUVCC, and where the output voltage is selected based on the specified inputs.
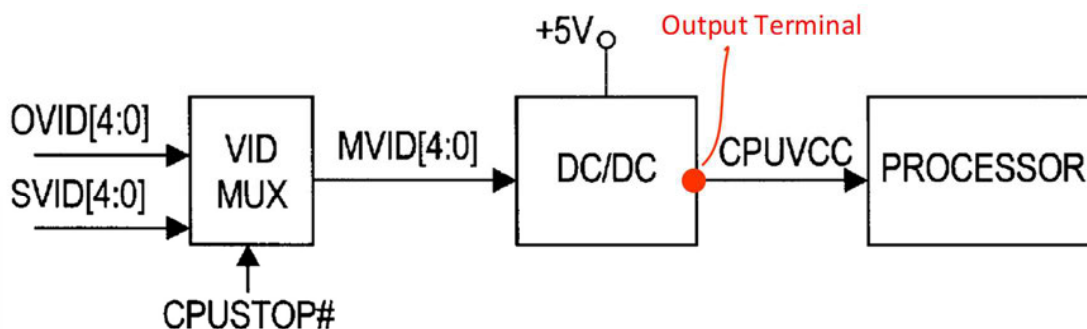
424. Specifically, Helms describes:

FIG. 1 shows a processor **receiving a power supply voltage signal (CPUVCC) from a programmable voltage converter (DC/DC)**. The converter receives power (in this case +5V) and a voltage setting signal **(MVID)**, and provides a **regulated output voltage at the level**

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**indicated by the voltage setting signal**. Because it is desirable to
provide the system with a power-saving mode in addition to the
normal operating mode, the voltage setting signal has two possible
values: **SVID** for "sleep" mode and **OVID** for "operating" mode. A
**multiplexer (VID MUX) selects between these two voltage settings**
in response to a mode control signal (CPUSTOP#) which may be
provided from the south bridge.

(Ex.1010, 2:42-54; FIG. 1 (annotated).)



FIG. 1

425.    Thus, CPUVCC is based on SVID or OVID voltage settings received
via MVID, and is therefore a "*selectable voltage*."  As such, Helms teaches "*an
output terminal providing a selectable voltage*."

>    d.    **Element 8[a.2] "an input terminal for receiving
>    signals indicating the selectable voltage level;"**

426.    Helms teaches "*an input terminal for receiving signals indicating the
selectable voltage level*" because Helms discloses a "programmable voltage
converter" having a terminal that receives a "voltage setting signal (MVID), *i.e.*,

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"*an input terminal for receiving signals indicating the selectable voltage level*."

427.    In particular, Helms states:

[A] system includes **a DC/DC converter, a processor**, and a selection circuit. **The DC/DC converter receives a voltage setting signal or signals** from the selection circuit and **provides an adjustable power output signal having a voltage indicated by the voltage setting signal**. The processor is powered by the adjustable power output signal.

(Ex.1010, Abstract.)

428.    In addition, Helms states:

FIG. 1 shows a processor **receiving a power supply voltage signal (CPUVCC) from a programmable voltage converter (DC/DC)**. The converter receives power (in this case +5V) and **a voltage setting signal (MVID)**, and provides a regulated output voltage at the level indicated by the voltage setting signal. Because it is desirable to provide the system with a power-saving mode in addition to the normal operating mode, **the voltage setting signal has two possible values: SVID for "sleep" mode and OVID for "operating" mode. A multiplexer (VID MUX) selects between these two voltage settings** in response to a mode control signal (CPUSTOP#) which may be provided from the south bridge.

(Ex.1010, 2:42-54; FIG. 1 (annotated).)

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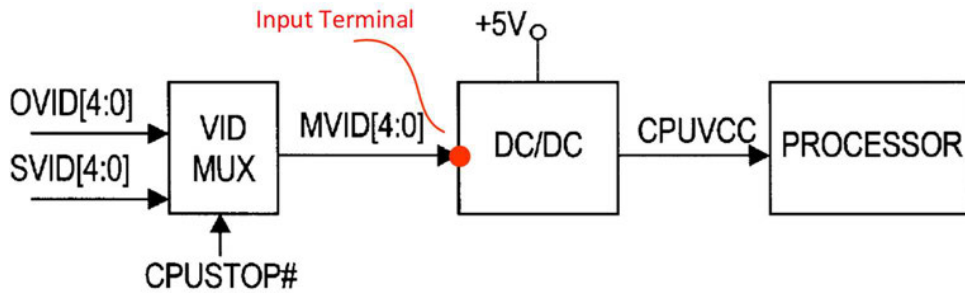
*FIG. 1*

429. Thus, Helms describes that the output voltage is regulated as specified by the input "**voltage setting signal (MVID)**," which can have "**two possible values: SVID for 'sleep' mode and OVID for 'operating' mode.**" In FIG. 1, Helms discloses an input terminal of the DC/DC voltage regulator receiving signals labeled "MVID[4:0]," which indicate a selectable voltage level. As such, Helms teaches "*an input terminal for receiving signals indicating the selectable voltage level.*"

> e.  Element 8[b.1] "**means for providing signals at the input terminal of the voltage regulator for selecting a voltage for operating the processor in a computing mode and a voltage of a level less than that for operating the processor in a computing mode,**"

430. Helms teaches this element because Helms describes performing the function recited in this claim element ("*providing signals . . .*") using the structure a multiplexor **VID MUX** having inputs **OVID** and **SVID**, which is a structure equivalent to that described in the '731 patent as performing the recited function.

431. This claim element recites "*means for . . .*" and the function recited is

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"*providing signals at the input terminal of the voltage regulator for selecting a voltage for operating the processor in a computing mode and a voltage of a level less than that for operating the processor in a computing mode*." The '731 patent discloses "a circuit 13 such as a **multiplexor**" having an "**input 14**" and "**an input 15**" as the structure that is clearly linked to performing the claimed function.

432. Specifically, the '731 patent states: "FIG. 3 is a circuit diagram illustrating a first embodiment of the invention. In the circuit 10 illustrated, a switching voltage regulator 11 receives an input signal at a terminal 12 which determines its output voltage value." (Ex.1001, 3:23-26; FIG. 3.) The '731 patent further states:

> In the circuit of FIG. 3, input to the terminal 12 is furnished via a **circuit 13 such as a multiplexor** that is capable of providing one or more input values. In the embodiment illustrated, a value is provided at **a first input 14** to the circuit 13 by the processor (or other circuitry) which **determines the operating condition of the processor in its computing range**; and a second value is provided at a **second input 15 which is selected especially for the deep sleep condition**. Either of these input values may be selected by a control signal provided at a control terminal 16 of the circuit 13.

(*Id.*, 3:52-62; FIG. 3.)

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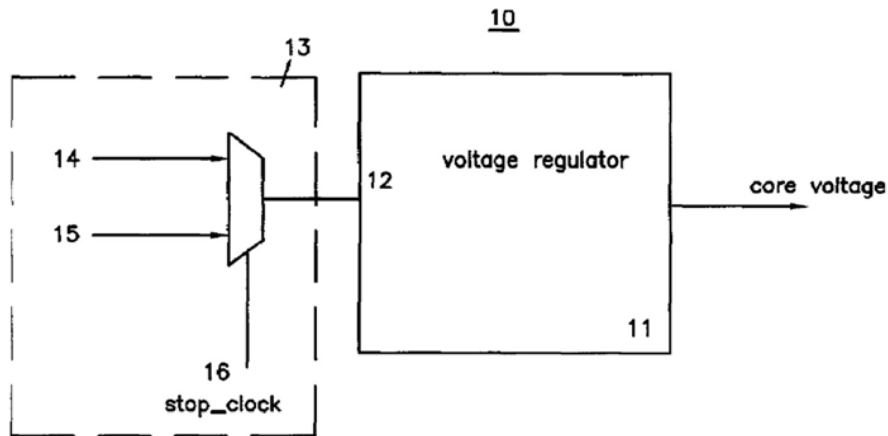U.S. Patent No. 7,260,731



Figure 3

(*Id.*, FIG. 3.)

433.   Helms describes performing the function this claim element recites

using substantially the same structure that the '731 patent describes.  Specifically,

Helms states:

> FIG. 1 shows a processor receiving a power supply voltage signal
> (CPUVCC) from a programmable voltage converter (DC/DC). The
> **converter receives** power (in this case +5V) and **a voltage setting
> signal (MVID)**, and provides a regulated output voltage at the level
> indicated by the voltage setting signal. Because it is desirable to
> provide the system with a power-saving mode in addition to the
> normal operating mode, **the voltage setting signal has two possible
> values: SVID for "sleep" mode and OVID for "operating" mode.
> A multiplexer (VID MUX) selects between these two voltage
> settings** in response to a mode control signal (CPUSTOP#) which
> may be provided from the south bridge.

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(Ex.1010, 2:42-54; FIG. 1 (annotated).)
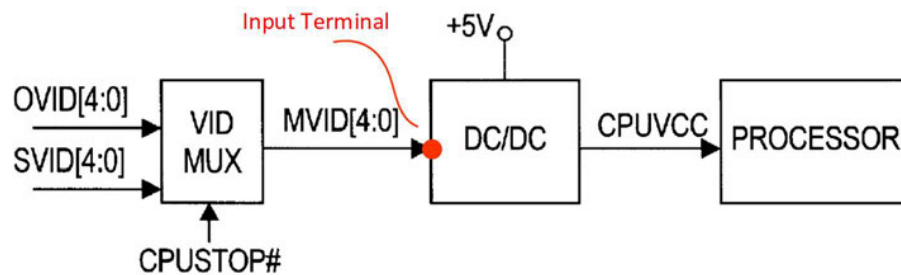


*FIG. 1*

434. Thus, Helms describes providing to the DC/DC converter the "**voltage setting signal (MVID)**" that indicates the level of the regulated output voltage to be provided to the processor (*i.e.*, "*providing signals at the input terminal of the voltage regulator for selecting a voltage*"). Moreover, the MVID can have "two possible values" namely, "**OVID for 'operating' mode**" and "**SVID for 'sleep' mode.**" The VID MUX is "*for selecting a voltage*" between the OVID and SVID values. As discussed below, a POSITA would have understood that the OVID values may be "*for operating the processor in a computing mode*," and that the SVID values may specify "*a voltage of a level less than that for operating the processor in a computing mode*."

435. Specifically, Helms describes the use of its techniques in connection with processors such as "AMD's K6-III and **Athlon processors**." (*See Id.*, 3:57-61 ("It is desirable to provide processors such as upcoming versions of AMD's K6-III and **Athlon processors** with voltage identification (VID) output signals that

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they will drive to the DC/DC converter that supplies their operating voltage.").)

436.   Prior to the priority date of the '731 patent (Oct. 23, 2000), a POSITA

would have known that the **operating voltage** of an Athlon processor, depending

on its model, to be in the range **1.5-1.9 V**, and the **sleep voltage** to be as low as **1.2**

**V**.  (*See* Ex.1036 at 42, Table 9 ("Operating Ranges"); Ex.1037 at 38, Table 8

("Operating Ranges").)

**Table 9.   Operating Ranges**

| Parameter | Description | Min | Max | Notes |
|---|---|---|---|---|
| VCC_CORE | AMD Athlon™ processor core supply | 1.5 V | 1.7 V | 1 |
| VCC_CORE | AMD Athlon™ processor core supply in Sleep state | 1.2 V | 1.7 V | 2 |
| VCC_SRAM | 2.5 V SRAM core supply | 2.475 V | 2.625 V | 3 |
| VCC_SRAM | 3.3 V SRAM core supply | 3.15 V | 3.45 V | 4 |
| $T_{PLATE}$ | Temperature of thermal plate | | 70° C | |

Notes:
1.  For normal operating conditions (nominal VCC_CORE is 1.6 V)
2.  For Sleep state operating conditions
3.  Value of VCC_SRAM when VCC2SEL is High
4.  Value of VCC_SRAM when VCC2SEL is Low

(Ex.1036 at 42, Table 9 (annotated).)

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**Table 8.    Operating Ranges**

| Parameter | Description | | Min | Nominal | Max | Notes |
|---|---|---|---|---|---|---|
| VCC_CORE | AMD Athlon™ processor **Model 1** core supply | 500–700 MHz | 1.5 V | 1.6 V | 1.7 V | 1 |
| | AMD Athlon processor **Model 2** core supply | 550–750 MHz | 1.5 V | 1.6 V | 1.7 V | |
| | | 800–850 MHz | 1.6 V | 1.7 V | 1.8 V | |
| | | 900–1000 MHz | 1.7 V | 1.8 V | 1.9 V | |
| | AMD Athlon processor **Model 4** core supply | 650–850 MHz | 1.6 V | 1.7 V | 1.8 V | |
| | | 900–1000 MHz | 1.65 V | 1.75 V | 1.85 V | |
| VCC_CORE$_{SLEEP}$ | AMD Athlon processor core supply in Sleep state | | 1.2 V | 1.3 V | 1.4 V | 2 |
| VCC_SRAM | 2.5 V SRAM core supply | | 2.475 V | 2.5 V | 2.625 V | 3 |
| | 3.3 V SRAM core supply | | 3.15 V | 3.3 V | 3.45 V | 4 |
| T$_{PLATE}$ | Temperature of thermal plate | | | | 70° C | |

Notes:
1. *Normal operating conditions*
2. *For Sleep state operating conditions*
3. *Value of VCC_SRAM when VCC2SEL is High*
4. *Value of VCC_SRAM when VCC2SEL is Low*

(Ex.1037 at 38, Table 8 (annotated).)

437.   A POSITA would have also known that the operating frequencies for an Athlon processor would range from 500-1000 MHz.  (*See id*.; Ex.1036 at 43, Table 11 (describing a frequency range of 500-700 MHz).)

438.   Helms also describes that "MAX1711 uses its D4 through D0 inputs to determine the output voltage level" in the range **2.0 to 0.925 V**.  (*Id*., 3:21-56.) As such, a POSITA would have readily understood that the "DC/DC converter" that Helms discloses can be a MAX1711 voltage regulator, and that the 5-bit output "MVID[4:0]" of the VID MUX can be coupled to the D4-D0 inputs of the MAX1711 voltage regulator.

439.   A POSITA would have further understood that "**OVID for**

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**'operating' mode**" that Helms describes may correspond to voltages in the range

1.5-1.9 V (which is within the range of voltages that MAX1711 can provide), so

that an Athlon processor available around 2000 could be operated at frequencies

ranging from 500-1000 MHz and would perform computations.  Therefore,

"**OVID for 'operating' mode**" represents "*a voltage for operating the processor*

*in a computing mode*."

440.   A POSITA would have also understood that the "**SVID for 'sleep'**

**mode**" that Helms describes may correspond to voltages such as 1.2 V, 1.3 V, *etc.*

(which are also within the range of voltages that MAX1711 can provide), and that

at these voltages, an Athlon processor available around 2000 could not be

operated, because the minimum operating voltage was 1.5 V, but would be placed

in a sleep mode.  Therefore, "**SVID for 'sleep' mode**" represents "*a voltage of a*

*level less than that for operating the processor in a computing mode*."

441.   As discussed above, since the MVID selected by Helms's "VID

MUX" can have "two possible values" namely, "**OVID for 'operating' mode**"

and "**SVID for 'sleep' mode**," Helms teaches the recited function of "*providing*

*signals at the input terminal of the voltage regulator for selecting a voltage for*

*operating the processor in a computing mode and a voltage of a level less than that*

*for operating the processor in a computing mode*."

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442. The structure for performing this function that Helms describes

includes the multiplexor "VID MUX," having inputs "OVID" and "SVID"

representing two voltage settings, that "selects between these two voltage settings"

and provides the selected voltage setting as "MVID" to the "programmable voltage

converter (DC/DC)." This structure is substantially the same as the structure that

the '731 patent provides, as the side-by-side comparison below shows.



The '731 Patent, FIG. 3                                    Helms, FIG. 1
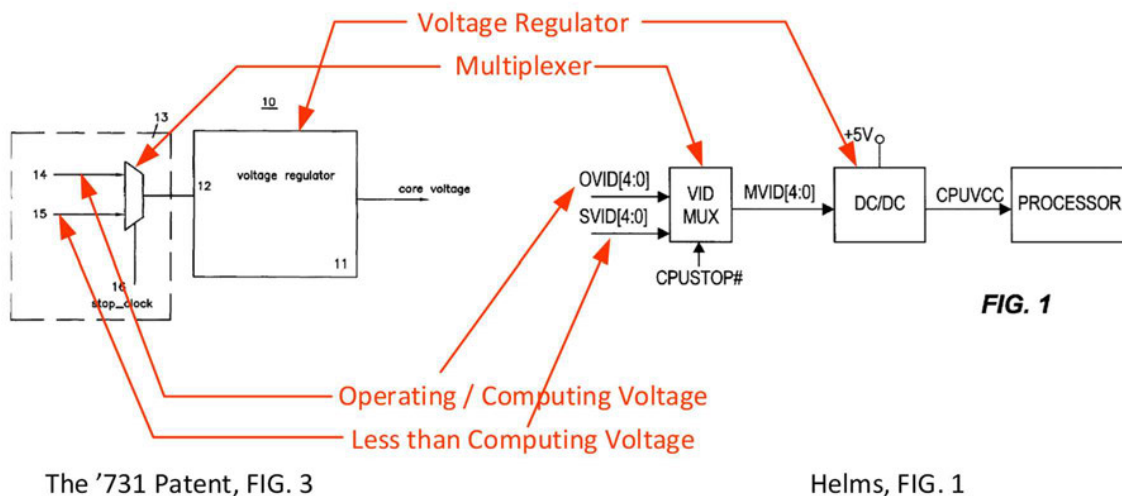
443. Thus, Helms describes performing the recited function using a

structure that is the same as or equivalent to that discloses in the '731 patent and,

thus, teaches this claim element.

    **f.    Element 8[b.2] "wherein the level less than that for
operating the processor in a computing mode is
sufficient to maintain state of the processor; and"**

444. Helms teaches "*wherein the level less than that for operating the*

*processor in a computing mode is sufficient to maintain state of the processor,*"

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because Helms discloses the use of Athlon processor and providing voltages in the range of 2.0 to 0.925 V, and because a POSITA would have known that the sleep voltage of an Athlon processor is at least 1.2 V, which was known to be "*sufficient to maintain state of the processor*."

445.   As discussed for claim element [8.b.1], prior to the priority date of the '731 patent (Oct. 23, 2000), a POSITA would have known that the **operating voltage** of an Athlon processor, depending on its model, to be in the range **1.5-1.9 V**, and the **sleep voltage** to be as low as **1.2 V**.  (*See* Ex.1036 at 42 (Table 9) ("Operating Ranges"); Ex.1037 at 38 (Table 8) ("Operating Ranges").)

446.   Helms also describes that "MAX1711 uses its D4 through DO inputs to determine the output voltage level" in the range **2.0 to 0.925 V**.  (Ex.1010, 3:21-56.)  As such, a POSITA would have also understood that while the OVID would have been 1.5-1.9 V, the "**SVID for 'sleep' mode**" that Helms describes can be 1.2 V, 1.3 V, *etc*. (which is within the range of voltages that MAX1711 can provide).

447.   A POSITA would have understood that a sleep voltage of 1.2 V would be "*sufficient to maintain state of the [Athlon] processor*" for at least two reasons.  First, the '731 patent itself states:

> Two criteria control the level to which the core voltage may be
> reduced in deep sleep. The **level must be sufficient to maintain state**
> that the processor requires to function after returning from the deep

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sleep state. The level must be one that can be reached during the times
allowed for transition to and from the deep sleep mode.

The first criterion is met so long as values of state stored are not lost
during the deep sleep mode. **Tests have shown that a core voltage
significantly below one-half volt allows the retention of the
memory state of a processor.** Thus, using this criterion, it would be
desirable to reduce the core voltage to a value such as one-half volt or
lower.

(Ex.1001, 4:45-57.)  A POSITA would have understood that since a voltage of less

than "one-half volt" would maintain processor state, so would the sleep voltage of

1.2 V of an Athlon processor.

448.    Second, a POSITA would have also known that in the sleep states of

an Athlon processor, the processor's general-purpose registers may be retained, so

that the processor state would be maintained.  The reason is, the Athlon processors

employ several power states that "conform to the **industry-standard** Advanced

Configuration and Power Interface **(ACPI) requirements** for processor power

states."  (Ex.1036 at 25; Ex.1037 at 23.)  These states include sleep state C3, in

which the processor clock is disabled, as indicated by "STPCLK# asserted."

(Ex.1036 at 25, Figure 3 (reproduced an annotated below); Ex.1037 at 23, Figure

3.)

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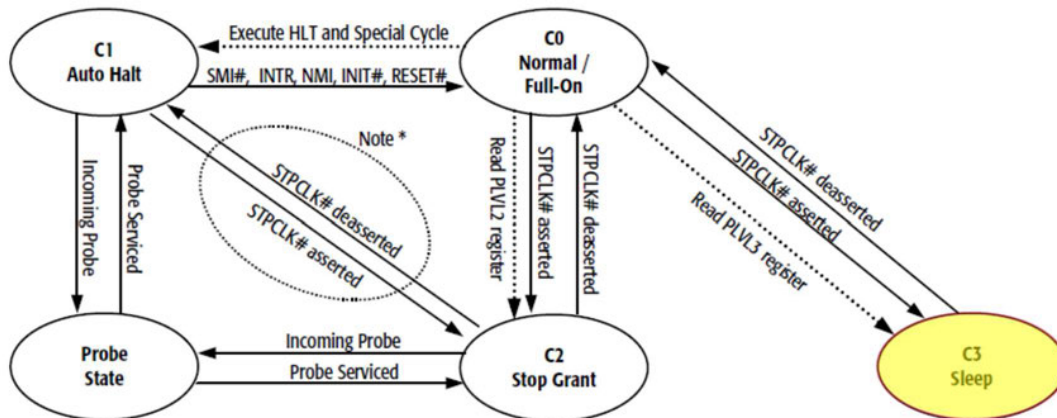


449.    The "industry-standard" ACPI states that in sleep state C3 "in the C3

state, the **processor's caches maintain state** but ignore any snoops." (Ex.1039 at

30 and 160.)

450.    During prosecution, while addressing the rejection of claims over U.S.

6,675,304 to Pole II et al. ("Pole"), which referred to the ACPI, the Applicant

relied upon the above-quoted disclosure of the ACPI.  In particular, the Applicant

stated: "Pole teaches a deep sleep state in which only data stored in the processor's

internal caches is maintained. (Ex.1004 at 374 (emphasis in the original) (citing to

Pole's discussion of the ACPI.)  The Applicant further stated: "As is well known to

those of ordinary skill in the art, a processor's state is not represented in the

processor's internal caches, and includes, for example, the **contents of internal**

**registers** which are not represented in the caches." (*Id*.)

451.    The Applicant did not take into consideration all the relevant

discussion of the processor sleep states in the ACPI, however.  In particular, a

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POSITA would have known that the industry-standard ACPI defines systems states

and also states: "Global **system states apply to the entire system**, and are visible

to the user. The various global system states are labeled G0 through G3 in the

ACPI specification."  (Ex.1039 at 24.)  Regarding the state "G0" the ACPI states:

> The ACPI specification defines a **working state, labeled G0**, in
> which the processor executes instructions. Processor low power states,
> labeled C1 through C3, are also defined. In the low power states the
> processor executes no instructions, thus reducing power consumption
> and, potentially, operating temperatures.

(*Id*. at 22.)

452.   The ACPI further states: "Processor power states (Cx states) [*i.e.*, C0

through C3] are processor power consumption and thermal management states

**within the global working state, G0**."  (*Id*. at 29; *see id*. at 29-30 (defining

"Processor Power State[s]" C0 through C3).)  The ACPI refers to the global system

state G0 as S0.  (*See id*. at 32, Figure 3-1.)

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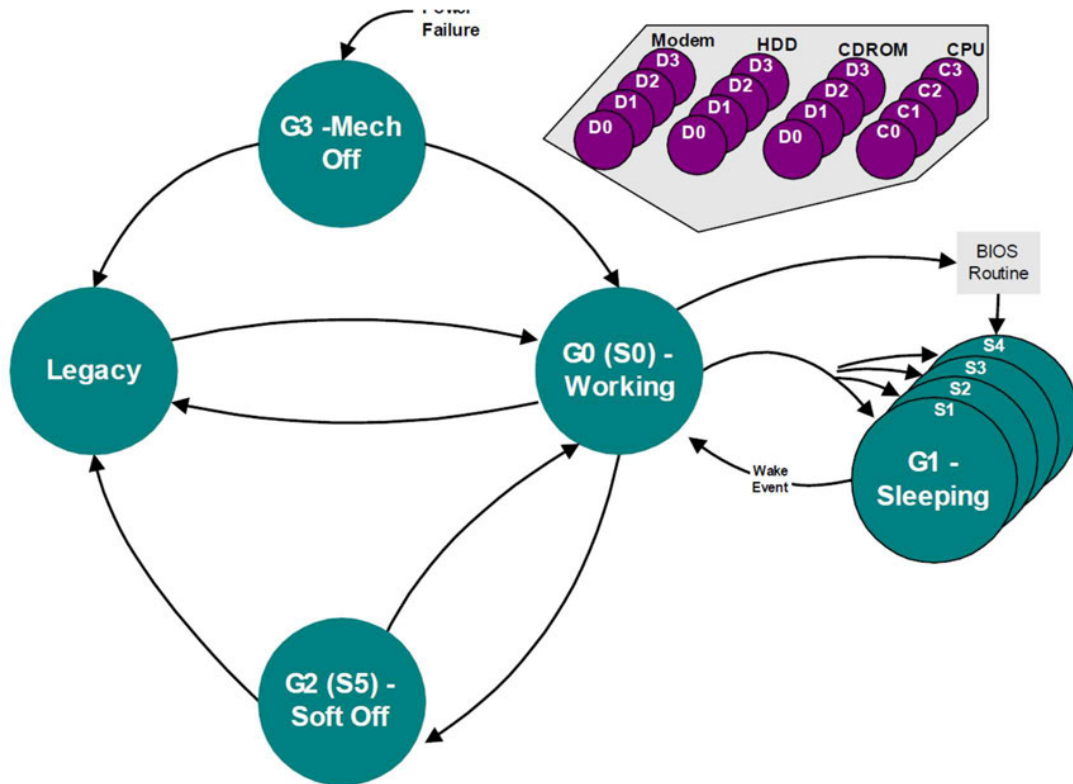


Figure 3-1  Global System Power States and Transitions

453.   With respect to the state S0, the ACPI states: "While the system is in

the S0 state, it is in the system working state. The behavior of this state is defined

as: The processors are in the C0, C1, C2, or C3 states. The **processor complex**

**context is maintained** and instructions are executed as defined by any of these

processor states." (*Id*. at 155.)

454.   Thus, the ACPI explicitly states that **while in the global working**

**state G0 or S0, the CPU can be** in the processor state C0, in which instructions

are executed (*see id*. at 29), or **in the processor state C3, in which the CPU clock**

**is stopped and instructions are not executed**.  (*See id*. at 29-30 and 39 (stating

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that to "save power in the Working state, the OS puts the CPU into low-power

states (C1, C2, and C3) when the OS is idle. In these low-power states, the **CPU**

**does not run any instructions, and wakes when an interrupt**, such as the pre-

empt interrupt, occurs").)  The ACPI also explicitly states that while "the system is

in the S0 state," **which includes the sleep state C3**, the "processor complex

context **is maintained**."

455.  A POSITA would have known that the "processor complex context"

would include data such as contents of the program counter, stack pointer,

processor's general purpose registers, *etc*.  Therefore, a POSITA would have

readily understood that by maintaining the processor complex context the

processor state would be maintained.

456.  As such, a POSITA would have known that in an ACPI-compliant

Athlon processor, when in sleep mode (identified as the ACPI C3 state) the

processor complex context, *i.e.*, the processor state, would be retained.

457.  Thus, Helms in view of the knowledge of a POSITA (as evidenced by

the '731 patent itself, Athlon-99-Datasheet, Athlon-00-Datasheet, and the ACPI),

teach that the sleep voltage of at least 1.2 V specified by the SVID, which is a

"*level less than that for operating the processor in a computing mode*" as discussed

for claim element [8.b.1], "*is sufficient to maintain state of the processor*."

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g. **Element 8[c.1] "means for changing the voltage regulator from a mode in which power is dissipated during a voltage transition that reduces said selectable voltage"**

458. The combination of Maxim-165X-Datasheet and MAX1711-Kit teaches "*means for changing the voltage regulator from a mode in which power is dissipated during a voltage transition that reduces said selectable voltage*," because Maxim-165X-Datasheet describes the function "*changing the voltage regulator [from one] mode*" to another, that this claim element recites. Maxim-165X-Datasheet also discloses a controller (*voltage regulator*) configured to operate in PWM (continuous) and skipped PWM (skip or efficient) modes. Moreover, Maxim-165X-Datasheet describes that the structure used to perform the recited function includes an input $\overline{\text{SKIP}}$ to force the PWM (continuous) mode of operation of the controller during a voltage transition reducing a voltage, which is substantially the same as that structure that the '731 patent describes for performing the recited function.

459. This claim element recites the function of "*changing the voltage regulator from a mode in which power is dissipated during a voltage transition that reduces said selectable voltage*." The '731 patent discloses a voltage regulator configured to operate in continuous and burst (also called high efficiency) modes. Additionally, the '731 patent discloses an input pin to select the mode of operation,

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where the input pin is used to operate the regulator in the continuous mode during

a voltage transition reducing a voltage, as the structure that is clearly linked to

performing the claimed function.

460.   In particular, the '731 patent states:

Prior art voltage regulators function in at least two different modes of
operation. A first mode of operation is often referred to as **"low
noise" or "continuous" mode**. In this mode, the regulator responds
as rapidly as possible to each change in voltage thereby maintaining
the output voltage at the desired output level as accurately as possible.

(Ex.1001, 5:48-53).

461.   The '731 patent further states:

A second mode of operation by voltage regulators is often referred to
as **"high efficiency," "burst," or "skip" mode**.  In this mode, a
regulator detects the reduction in load requirements (such as that
caused by a transition into the deep sleep state) and switches to a
mode whereby the regulator corrects the output voltage less
frequently.

(*Id.*, 6:1-6.)

462.   Additionally, the '731 patent describes:

The present invention utilizes the ability of **regulators to function in
both the high efficiency mode and the continuous mode** to
substantially reduce power wasted by transitioning between a

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computing and a lower voltage deep sleep mode. Although regulators

have not been dynamically switched between high efficiency and

continuous modes, in one embodiment of the invention, an **additional**

**controlling input 50 as shown in FIG. 5 is added to the regulator**

**for selecting the mode of operation** of the regulator based on

whether the processor being regulated is transitioning between states.

If the regulator receives a control signal 51 indicating that the

processor is to be placed into the deep sleep mode, for example, then a

**regulator operating in the high efficiency mode immediately**

**switches to the continuous mode during the voltage transition**.

Assuming that the regulator returns the charge to the battery during

continuous mode, this has the effect of reducing the waste of power

caused during the transition. **Once the transition has completed, the**

**regulator switches back to the high efficiency state** for operation

during the deep sleep mode of the processor.

(*Id*., 6:37-56.)

463.   It should be noted that even though the "burst" or "skip" mode is

referred to as the "high efficiency mode," (*see id*., 6:1-6) during a voltage

transition (a high-to-low voltage transition in particular), it is this mode that wastes

power and the "continuous" mode saves power because the "regulator returns the

charge to the battery during continuous mode." (*See id*., 6:37-56.)

464.   Thus, the '731 patent discloses a voltage regulator configured to

operate in the PWM/continuous mode or the PFM/high-efficiency mode, and an

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input causing the regulator to change its mode. (*See* Ex.1001 5:48-6:6, 6:41-46.)

The '731 patent also describes that although the PFM mode is otherwise efficient,

it dissipates power during a voltage transition, when the voltage is being lowered.

(*See* Ex.1001, 6:14-18.) To save power, using the "controlling input 50" the
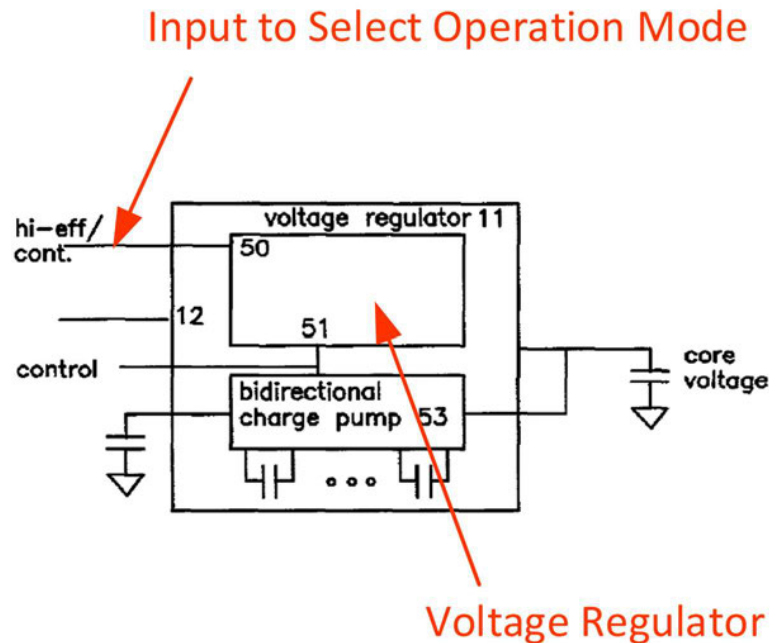
regulator is switched to the continuous mode during the voltage transition, and then

it is switched back to the high-efficiency mode after the transition is complete. (*See*

Ex.1001, 6:37-56.)

465. Thus, the structure that the '731 patent describes as corresponding to

the recited function includes an input that switches the operation of voltage

regulator between continuous and high-efficiency modes. Specifically, "an

**additional controlling input 50 as shown in FIG. 5 [] added to the regulator**

**for selecting the mode of operation**," (*see id.*, 6:37-56; FIG. 5), as the structure

that is clearly linked to performing the claimed function.

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**Input to Select Operation Mode**



**Voltage Regulator**

(*Id*., FIG. 5 (annotated).)

466. Maxim-165X-Datasheet discloses performing the function recited in

this claim element: "*changing the voltage regulator from* [*one*] *mode*" to another.

Specifically, Maxim-165X-Datasheet states: "The MAX1652–MAX1655 are high-

efficiency, pulse-width-modulated (PWM), step-down DC-DC controllers," *i.e.*,

*voltage regulators*. (Ex.1011 at 1, col. 1.)

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Figure 2. MAX1652–MAX1655 Functional Diagram

(*Id*. at 13 (Figure 2).)

467.   Maxim-165X-Datasheet also describes two modes of operation as

follows:

These devices automatically switch between [pulse-width modulation]
**PWM operation at heavy loads** and pulse-frequency-modulated
**(PFM) operation at light loads** to optimize efficiency over the entire

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output current range. The MAX1653/MAX1655 also feature logic-
controlled, **forced PWM operation** for noise-sensitive applications.

(*Id*.)

468.   Maxim-165X-Datasheet further states: "Under heavy loads, the

controller operates in **full PWM mode**" and that if "the load is light in **Idle Mode**

($\overline{\text{SKIP}}$ = low)," "the controller **skips** most of the oscillator pulses" in the PFM

mode.  (*Id*. at 12, col. 1.)  Maxim-165X-Datasheet also states: "Light-load

**efficiency is enhanced by** automatic idle-mode operation—**a variable-frequency**

**pulse-skipping mode** that reduces losses due to MOSFET gate charge."  (*Id*. at 10,

col. 2.)

469.   Maxim-165X-Datasheet refers to the PWM mode as "**continuous-**

**conduction mode**."  (*See id*. at 12, col. 2 ( "If the circuit is operating in

**continuous-conduction mode**, the DL drive waveform is simply the **complement**

of the DH high-side drive waveform (with controlled dead time to prevent cross-

conduction or 'shoot-through.').").)  The DH and DL drives refer to the high-side

and low-side FET drives, respectively. (*See id*. at 9, Table: Pin Description

(describing DH and DL).)  Maxim-165X-Datasheet also describes that it is the

PWM operation in which the drives DH and DL operate in a complementary

manner.  (*See id*. at 12, col. 1 (stating that "in full PWM mode" as "the high-side

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switch turns off, the synchronous rectifier latch is set" and that "60 ns later the

low-side switch turns on.")

470.    Moreover, Maxim-165X-Datasheet refers to the idle or pulse-skipping

mode that may be employed when the load is a light as "discontinuous-conduction

mode," (*see id*. at 16 (stating that "[r]inging may be seen at the high-side MOSFET

gate (DH) in **discontinuous-conduction mode**"), and the mode in which PWM

operation is forced, as the "low-noise mode."  (*See id*. at 16, col. 2.)

471.    This is consistent with the '731 patent in that what is referred to as the

"'high efficiency,' 'burst,' or **'skip' mode**" in the '731 patent (*see* the '731 Patent,

6:1-6), is described as the "**PFM**" operation, "**idle mode**," or "**pulse-skipping**

**mode**," that can enhance efficiency when the load is light, in Maxim-165X-

Datasheet, and what is referred to as the "'low noise' or **'continuous'** mode" in the

'731 patent (*see id*., 5:48-53) is described as the "**full PWM mode**" or

"**continuous-conduction mode**" in Maxim-165X-Datasheet, as described above.

472.    In addition, Maxim-165X-Datasheet describes an input pin to force a

transition from the pulse-skipping PFM mode to the PWM mode even when the

load is light.  In particular, Maxim-165X-Datasheet states: "The MAX1653 and

MAX1655 can reduce interference due to switching noise by ensuring **a constant**

**switching frequency regardless of load** and line conditions."  (*Id*. at 16, col. 2.)

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To this end, Maxim-165X-Datasheet states that forcing the "low noise mode ($\overline{\text{SKIP}}$

= high)" "ensures continuous inductor current flow" "allowing the **inductor**

**current to reverse at very light loads**." (*Id.* at 16, col. 2–17, col. 1.)

473.    Synchronous switching voltage regulators employing PWM have been

known well before 2000. (*See, e.g.*, Ex.1043, U.S. Patent No. 5,565,761 to Hwang

(issued on Oct. 15, 1996); Ex.1044, U.S. Patent 5,627,460 to Bazinet *et al.* (issued

on May 6, 1997).) As such, a POSITA would have known that if a voltage

regulator is not operated in the PWM mode during a transition from regular/heavy

load to light load, the inductor current would not be allowed to reverse.

474.    As such, the output capacitor would discharge mostly through the load

(*e.g.*, the CPU) and, since the load is "light" (e.g., the CPU is in a sleep state) such

a discharge would take a long time, extending the time required for the output

voltage to transition from a high value to a low value. A POSITA would have also

known that the **energy/charge stored in the capacitor would be dissipated** in the

load, and thus be wasted in the "pulse-skipping mode," also called the PFM mode,

by **not** "allowing the inductor current to reverse."

475.    MAX1711-Kit recognizes the problems discussed above, that a

POSITA would have known, and presents a solution similar to that Maxim-165X-

Datasheet describes, with a further improvement. In particular, MAX1711-Kit

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describes a "buck-regulator" (*i.e.*, a step-down voltage regulator) (*see* Ex.1012 at

2, col. 2), that can be operated in PWM or PFM modes, and where the **PWM**

**mode can be forced via the $\overline{\text{SKIP}}$ input**. (*See id*. at 3, col. 2.) Maxim-165X-

Datasheet also describes a "buck converter" (*see* Ex.1011 at 10, col. 1-col. 2) that

can be operated in PWM or PFM modes, where **the PWM mode can be forced**

**using the $\overline{\text{SKIP}}$ input**. (*See id*. at 1, col. 1, *id*. at 12, cols. 1-2, *id*. at 16, col. 2 –

17, col. 1.) Thus, MAX1711-Kit describes a synchronous switching voltage

regulator that is similar to those described in Maxim-165X-Datasheet.

476. In discussing forced PWM operation, MAX1711-Kit states:

> **Transitions to a lower output voltage require the circuit or the**
> **load to sink current**. If $\overline{\text{SKIP}}$ is held low (PFM mode), the **circuit**
> **won't sink curren**t, **so the output voltage will decrease only at the**
> **rate determined by the load current**. This is often acceptable, but
> some applications require output voltage transitions to be completed
> within a set time limit.

(Ex.1012 at 3, col. 2.)

477. MAX1711-Kit further states: "The simplest way of meeting this

requirement is to **use the MAX1711's fixed-frequency PWM mode (set $\overline{\text{SKIP}}$**

**high), allowing the regulator to sink** or source **currents equally**." (*Id*.)

MAX1711-Kit also states: "A similar but **more clever approach is to use PWM**

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**mode only during transitions**. This approach **allows the regulator to sink current when needed and to operate with low quiescent current the rest of the time**." (*Id*. at 4, col. 1.)

478.    Thus, the combination of Maxim-165X-Datasheet and MAX1711-Kit teaches that while otherwise beneficial in a settled light load condition (*e.g.*, when the CPU is in a sleep state), the pulse-skipping (PFM) mode of the voltage regulator would sink current in the load (*e.g.*, the CPU) and dissipate/ waste power during a voltage transition.  The combination also teaches that setting $\overline{\text{SKIP}}$ **high** would force or change the operation mode of the voltage regulator from the pulse-skipping (also called PFM) mode to the PWM mode.  In the PWM mode, the power is not dissipated in the load and, instead, is saved, as discussed below. Accordingly, the combination of Maxim-165X-Datasheet and MAX1711-Kit discloses the function of "*changing the voltage regulator from a mode in which power is dissipated during a voltage transition that reduces said selectable voltage*."

479.    The structure that Maxim-165X-Datasheet discloses for forcing the PWM operation during a voltage transition (*e.g.*, while transitioning to a low-load condition resulting from the processor entering a sleep state), includes an input pin/terminal $\overline{\text{SKIP}}$ of a MAX1653 controller (a *voltage regulator*) that forces the

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PWM operation of the regulator, *e.g.*, during a voltage transition (such as while

transitioning to a low-load condition resulting from the processor entering a sleep

state). The "Pin Description" Table in Maxim-165X-Datasheet states: that Pin 2

"$\overline{\text{SKIP}}$" "Disables pulse-skipping mode when high" forcing the regulator to operate

in the PWM mode. (Ex.1011 at 9.)
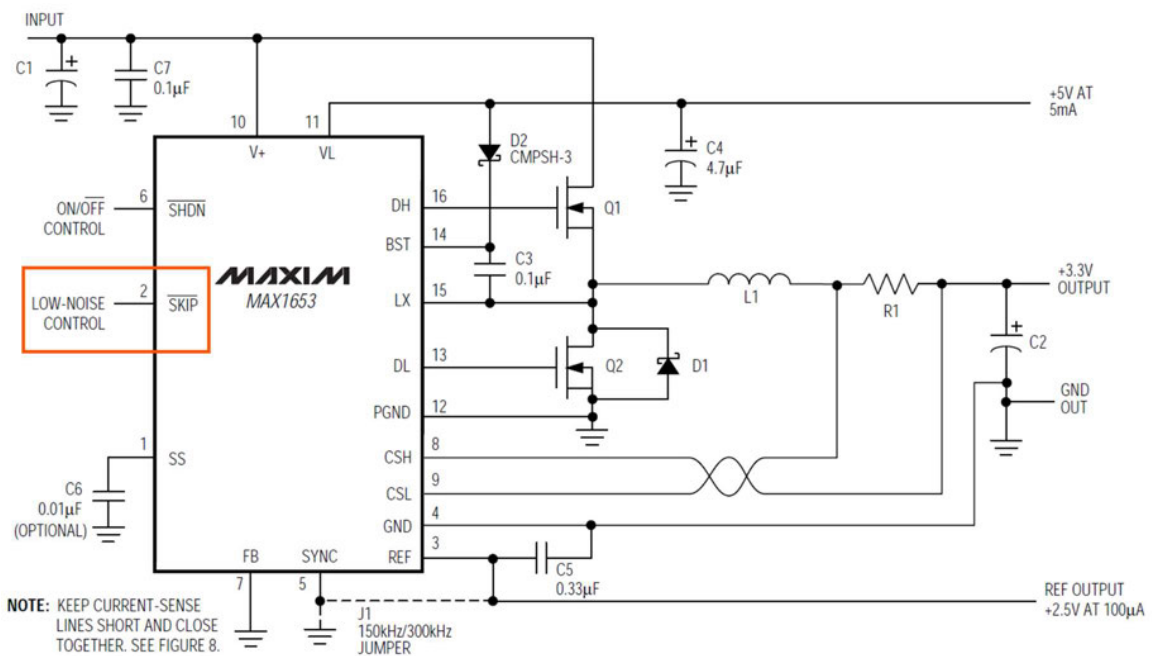


(*Id*. at 10 (Figure 1 (annotated)).)

480. In describing the "$\overline{\text{SKIP}}$ **Pin**" Maxim-165X-Datasheet states that

"$\overline{\text{SKIP}}$ can be driven from an external logic signal." (*Id*. at 16, col. 2.)

481. As noted above, the structure that the '731 patent describes as

corresponding to the recited function includes a regulator that is able to "function

in both the high efficiency mode and the continuous mode" and "an **additional**

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**controlling input 50 as shown in FIG. 5 [] added to the regulator for selecting**

**the mode of operation**.” (*See* the ’731 patent, 6:37-56; FIG. 5.)

482. The above-described structure that Maxim-165X-Datasheet discloses

is substantially the same as or at least equivalent to that the ’731 patent describes,

as a side-by-side comparison below shows.
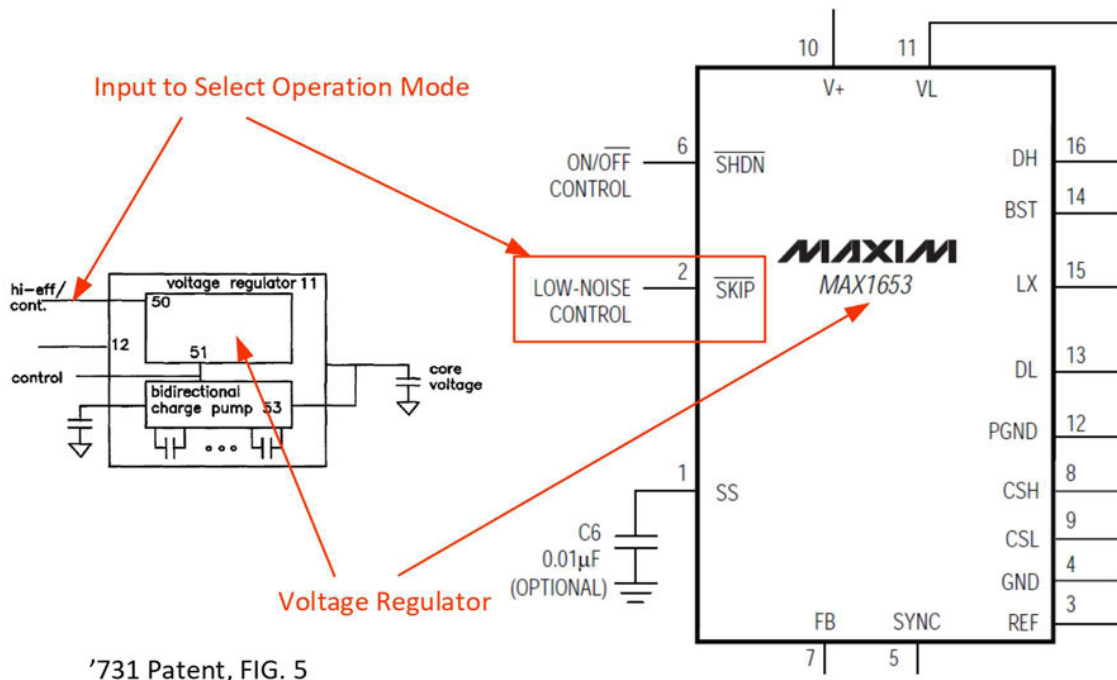


Maxim-165X-Datasheet, Figure 1 (partial)

483. Thus, the combination of Maxim-165X-Datasheet and MAX1711-Kit

teaches this claim element.

> h.    **Element 8[c.2]: “to a mode in which power is saved
> during said voltage transition.”**

484. The combination of Maxim-165X-Datasheet and MAX1711-Kit

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teaches "*to a mode in which power is saved during said voltage transition*"

because Maxim-165X-Datasheet describes that forcing the PWM mode when the

load is light (*e.g.*, when the output voltage is low) allows the "inductor current to

reverse," so that the charge of the output capacitor can be transferred to the input

capacitor, thereby avoiding power dissipation and, thus, saving of power.

MAX1711-Kit describes that PWM operation can be forced "only during" a

voltage transition.

485. A voltage regulator typically includes an output capacitor that is

charged to the regulated output voltage. When the regulator's output voltage

transitions from a higher value to a lower value, the excess charge at the output

capacitor, corresponding to the higher voltage value, must be removed. Two

common ways to accomplish the removal of excess charge include (1) dissipating

the charge via the load or (2) transferring the charge elsewhere, *e.g.*, to the

regulator's input capacitor or a battery providing power to the regulator.

486. The first option results in dissipation and waste of power. The second

option results in conservation of charge, which can be transferred back to the

regulator's output capacitor as needed, saving power. As discussed below, the

Maxim-165X-Datasheet teaches operating a voltage regulator in this manner.

MAX1711-Kit also teaches operating a voltage regulator in this manner, especially

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while reducing, the regulator's output voltage.

487.   In particular, Maxim-165X-Datasheet states: "The MAX1653 and MAX1655 can reduce interference due to switching noise by ensuring **a constant switching frequency regardless of load** and line conditions." (Ex.1011 at 16, col. 2.)  To this end, Maxim-165X-Datasheet states that **forcing the** "**low noise mode ($\overline{\text{SKIP}}$ = high)**" "ensures continuous inductor current flow" "allowing the **inductor current to reverse at very light loads**. (*Id*. at 16, col. 2-17, col. 1.)

488.   As noted for claim element [8.c.1], synchronous switching voltage regulators employing PWM have been known well before 2000.  (*See, e.g.*, U.S. Patent No. 5,565,761 to Hwang (issued on Oct. 15, 1996) (Ex.1043); U.S. Patent No. 5,627,460 to Bazinet *et al*. (issued on May 6, 1997) (Ex.1044).)  As such, a POSITA would have known at least two benefits of "allowing the inductor current to reverse."  First, the output capacitor of the regulator can be discharged faster than it otherwise would because, without such reversal, the output capacitor may discharge only through the load and, since the load is "light" such a discharge would take a long time, extending the time required for the output voltage to transition from a high value to a low value.

489.   Second, a POSITA would have also known rather than dissipating the energy stored by the capacitor in the load, and thus be wasted, by "allowing the

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inductor current to reverse," the energy stored in the output capacitor can instead

be transferred to and stored in the inductor, or in a parasitic capacitor, when the

low-side FET is ON, or in the input capacitor, when the high-side FET is ON.

490.　In fact, in discussing forced PWM operation, MAX1711-Kit states:

> **Transitions to a lower output voltage require the circuit or the**
>
> **load to sink current**. If $\overline{\text{SKIP}}$ is held low (PFM mode), the **circuit**
>
> **won't sink curren**t, so the output voltage will decrease only at the
>
> rate determined by the load current.  This is often acceptable, but
>
> some applications require output voltage transitions to be completed
>
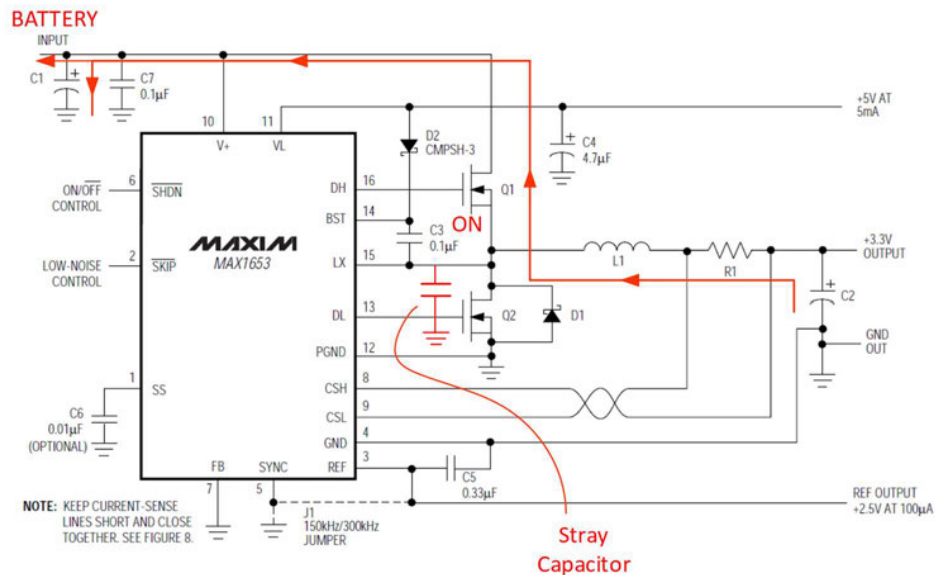> within a set time limit.

(Ex.1012 at 3, col. 2.)

491.　MAX1711-Kit further states: "The simplest way of meeting this

requirement is to **use the MAX1711's fixed-frequency PWM mode (set $\overline{\text{SKIP}}$**

**high**), **allowing the regulator to sink** or source **currents equally**.  (*Id*.)

MAX1711-Kit also states: "A similar but **more clever approach is to use PWM**

**mode only during transitions**. This approach **allows the regulator to sink**

**current when needed and to operate with low quiescent current the rest of the**

**time**."  (*Id*. at 4, col. 1.)

492.　A POSITA would have readily understood that "allowing the

regulator to sink" current means "allowing the inductor current to reverse," as

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Maxim-165X-Datasheet teaches (*see* Ex.1011 at 16, col. 1-17, col. 2), where rather

than dissipating the energy (charge) stored in the output capacitor in the load can

instead be saved. For example, the charge can be transferred to and stored in the

inductor and/or in a parasitic capacitor, when the low-side FET is ON, or in the

input capacitor, when the high-side FET is ON, as illustrated below. A POSITA

would have also understood that the PWM mode may be forced "**only during [the**

**voltage] transition**," allowing a faster transition and which power is saved, and

employing the efficient PFM mode when the transition is complete and the load is

low. (*See* Ex.1012 at 4, col. 1.)



(Ex.1011 at 10, Figure 1 (annotated to show the reversed inductor current, where

energy from the output capacitor may be stored in the inductor L1 and/or a stray

capacitor, when the low-side FET is ON).)

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(Ex.1011 at 10, Figure 1 (annotated to show the reversed inductor current, where energy from the output capacitor may be stored in a stray capacitor and/or the input capacitor, or may charge the battery, when the high-side FET is ON).)

493. Here, the switching regulator that Maxim-165X-Datasheet discloses operates when the PWM mode is forced in the same way as Burd's converter (*voltage regulator*) operates, as discussed under Ground 1 for Element 1[c.2]. Specifically, when the magnitude of the signal $F_{ERR}$ that Burd discloses is greater than 4MHz and the sign of $F_{ERR}$ is negative, Burd's converter "removes charge from the capacitor" (*see* Ex.1006 at 1, col. 2), at least a part of which is returned to the battery, as indicated in annotated Figures 17.4.2 and 17.4.3 below by negative battery current $I_{BAT}$.

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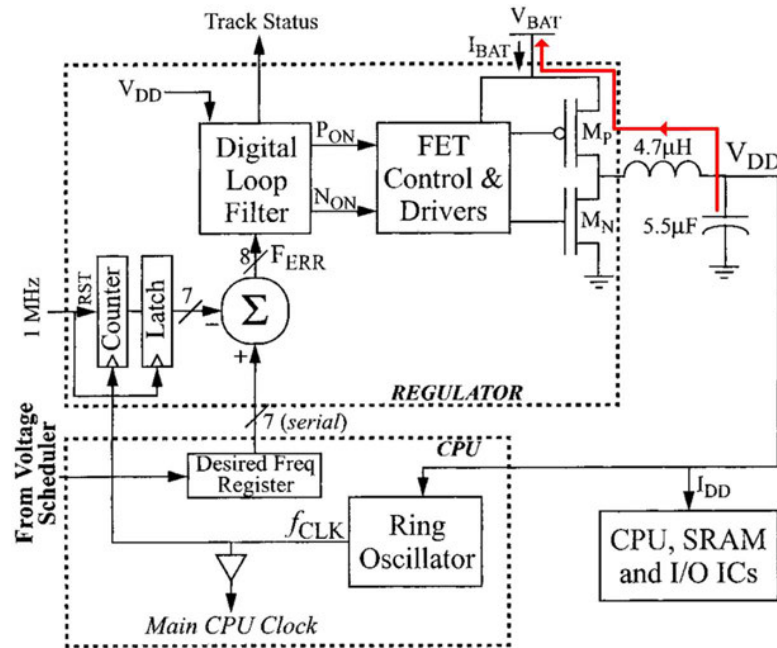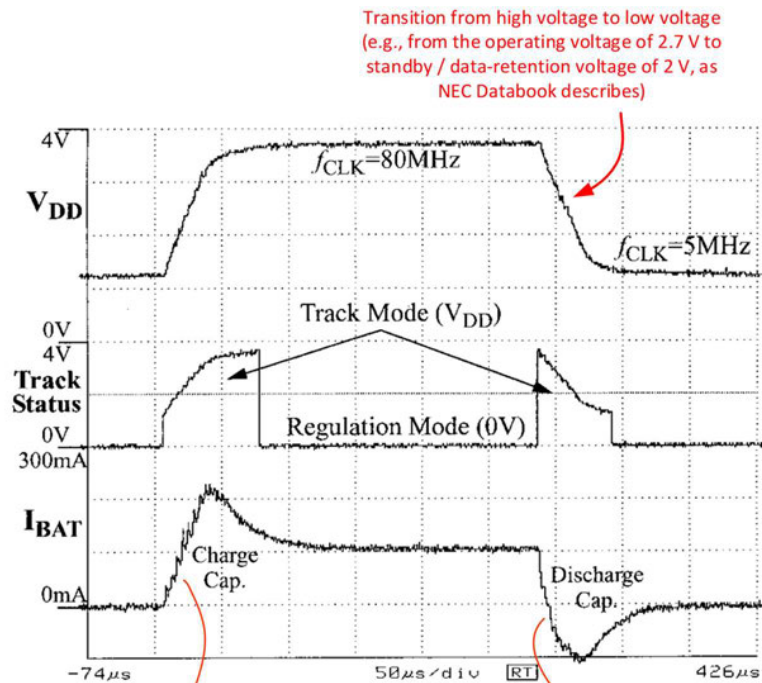Petition for *Inter Partes* Review of
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**Figure 17.4.2: Frequency to voltage feedback loop.**

(*Id.*, Figure 17.4.2 (annotated).)

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Figure 17.4.3: Transient response of regulation loop.

(*Id*. at 2, Figure 17.4.3 (annotated).)

494.    The above-discussed forcing of the PWM mode of the switching

regulator that Maxim-165X-Datasheet discloses only during the voltage transition

that the combination of Maxim-165X-Datasheet and MAX1711-Kit teaches is

consistent with the '731 patent, which states:

> If the regulator receives a control signal 51 indicating that the
> processor is to be placed into the deep sleep mode, for example, then a
> **regulator operating in the high efficiency mode immediately
> switches to the continuous mode during the voltage transition**.
> Assuming that the **regulator returns the charge to the battery**

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**during continuous mode**, this has the effect of reducing the waste of

power caused during the transition. Once the transition has completed,

the regulator switches back to the high efficiency state for operation

during the deep sleep mode of the processor.

(Ex.1001, 6:37-56.)

495.   Thus, even though the '731 patent refers to the "burst" or "skip" mode

as the "high efficiency mode" (*see id*. 6:1-6), during a voltage transition (a high-to-

low voltage transition in particular), it is this mode that wastes power and the

"continuous" mode saves power because the "regulator returns the charge to the

battery during continuous mode." (*See id*., 6:37-56.)

496.   As such, the combination of Maxim-165X-Datasheet and MAX1711-

Kit discloses this claim element.

497.   In summary, Helms in view of Maxim-165X-Datasheet, further in

view of MAX1711-Kit discloses all of the limitations of claim 8 and renders claim

8 unpatentable as obvious.

### 3.    Claim 9

498.   Claim 9 depends from claim 8, and further recites: "*the means for

providing signals at the input terminal of the voltage regulator comprises means

for accepting binary signals indicating different levels of voltage*."

499.   Helms teaches this limitation because, as discussed for Element

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8[b.1], Helms discloses the multiplexor "VID MUX" as "*the means for providing signals at the input terminal of the voltage regulator for selecting a voltage for operating the processor in a computing mode and a voltage of a level less than that for operating the processor in a computing mode*." Moreover, Helms describes performing the function recited in this claim element ("*accepting binary signals indicating different levels of voltage*") using the multiplexor **VID MUX** having inputs **OVID** and **SVID** that can receive or accept binary signals and, thus, using a structure that is equivalent to that described in the '731 patent as performing the recited function.

500. In addition to the "*the means for providing signals at the input terminal of the voltage regulator . . .*" already recited in Element 8[b.1], this claim element additionally recites "*means for accepting binary signals indicating different levels of voltage*." The additional function recited is "*accepting binary signals indicating different levels of voltage*."

501. The '731 patent discloses "a circuit 13 such as a **multiplexor**" having an "**input 14**" and "**an input 15**," where the multiplexor selects one of the inputs 14 and 15, and provides the selected input to the input 12 of the voltage regulator, as the structure that is clearly linked to performing the claimed function.

502. Specifically, the '731 patent states: "FIG. 3 is a circuit diagram

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illustrating a first embodiment of the invention. In the circuit 10 illustrated, a

switching voltage regulator 11 receives an input signal at a terminal 12 which

determines its output voltage value." (Ex.1001, 3:23-26; FIG. 3.) The '731 patent

further states:

> In the circuit of FIG. 3, input to the terminal 12 is furnished via a
> **circuit 13 such as a multiplexor** that is capable of providing one or
> more input values. In the embodiment illustrated, a value is provided
> at **a first input 14** to the circuit 13 by the processor (or other
> circuitry) which **determines the operating condition of the
> processor in its computing range**; and a second value is provided at
> a **second input 15 which is selected especially for the deep sleep
> condition**. Either of these input values may be selected by a control
> signal provided at a control terminal 16 of the circuit 13.
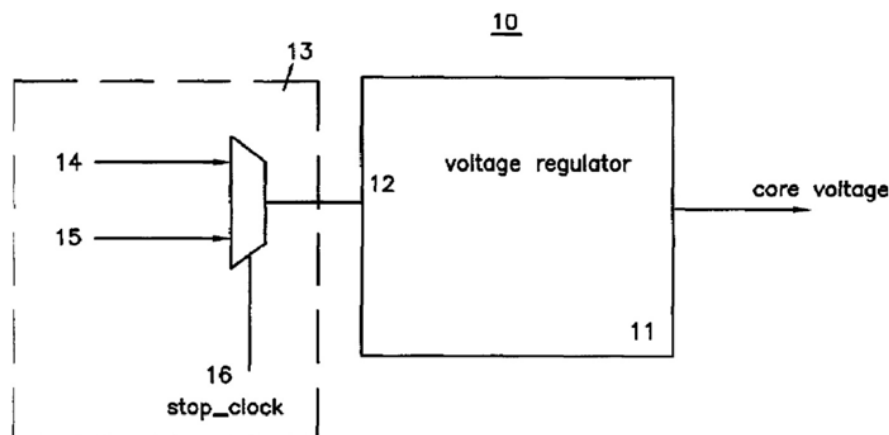
(*Id.*, 3:52-62; FIG. 3.)



Figure 3

(*Id.*, FIG. 3.)

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503.   In addition, the '731 patent states:

Most modern processors utilize a voltage regulator which is capable

of furnishing a range of core voltages for operating transistors; a

typical regulator may furnish a range of voltages between 2 and 0.925

volts from which a particular core voltage may be selected for

operation. Typically, **a binary signal is provided a the terminal 12**

which selects the particular output voltage level to be furnished by the

regulator 11; in such a case, a number of individual pins may be

utilized as the terminal 12.

(*Id.*, 3:26-35.)

504.   A POSITA would have understood that since a binary signal is

provided at terminal 12, and since the signal provided at the terminal 12 is either

the input 14 or input 15, indicating operating and deep sleep voltages, respectively,

the inputs 14 and 15 would also be binary signals and, in particular, "*binary*

*signals indicating different levels of voltage*."  As such, a POSITA would have

understood that the structure that the '731 patent describes as performing the

recited function of "*accepting binary signals indicating different levels of voltage*"

includes a multiplexor having two inputs where each input can be a multi-bit

binary signal indicating a respective voltage.

505.   Helms describes performing the function this claim element recites

using substantially the same structure that the '731 patent describes – a

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multiplexor. Specifically, as discussed for Element 8[b.1], Helms discloses the

multiplexor "VID MUX" *i.e.*, "*the means for providing signals at the input

terminal of the voltage regulator*." The VID MUX has inputs "OVID" and

"SVID" representing two voltage settings, and the VID MUX "selects between

these two voltage settings" and provides the selected voltage setting as "MVID" to

the "programmable voltage converter (DC/DC)" at its input terminal. (*See*

Ex.1010, 2:42-54; FIG. 1.) A POSITA would have known that the signals OVID,

SVID, and MVID are 5-bit binary signals due to the identified indices "[4:0]."
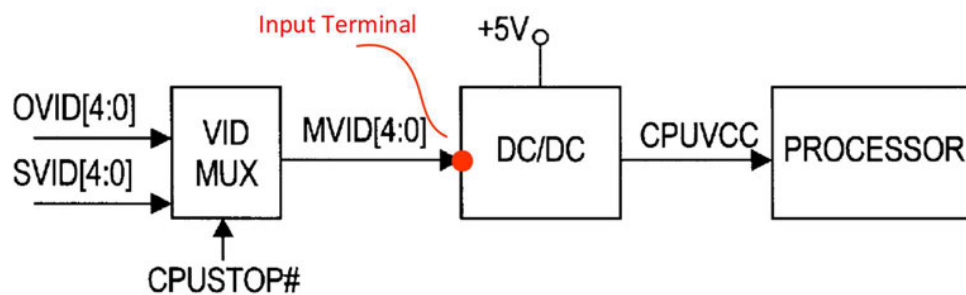


**FIG. 1**

(*Id.*, FIG. 1 (annotated).)

506. As also discussed for Element 8[b.1], Helms discloses that the

"processor" of FIG. 1 can be an Athon[TM] processor (*see Id.*, 3:57-61), and that the

signals OVID and SVID may specify an operating voltage in the range 1.5-1.9 V

and a sleep voltage as low as 1.2 V, respectively, for an Athlon[TM] processor. (*See*

*id.* 2:42-54; *see also* Ex.1036 at 42, Table 9 (disclosing ranges of operating mode

and sleep mode voltages), Ex.1037 at 38, Table 8 (disclosing the same).)

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507. As further discussed for Element 8[b.1], Helms discloses that the "DC/DC converter" of FIG. 1 can be a MAX1711 voltage regulator, and that the 5-bit output "MVID[4:0]" of the VID MUX can be coupled to the D4-D0 inputs of the MAX1711 voltage regulator. (*See* Ex.1010, 3:21-56.)

508. Helms further discloses that the D4-D0 inputs of the MAX1711 voltage regulator receive different binary signals, each representing a respective value of the output voltage. (*See id*., 3:25-54 (Table of D4-D0 and corresponding output voltages).) In the table below, each input signal is a 5-bit binary signal, so that each 5-bit input can be collectively considered as a binary signal, or each bit can individually be considered a binary signal, where a particular input value is represented by five binary signals.

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| D4:D0 | Output Voltage |
|---|---|
| 00000 | 2.00 |
| 00001 | 1.95 |
| 00010 | 1.90 |
| 00011 | 1.85 |
| 00100 | 1.80 |
| 00101 | 1.75 |
| 00110 | 1.70 |
| 00111 | 1.65 |
| 01000 | 1.60 |
| 01001 | 1.55 |
| 01010 | 1.50 |
| 01011 | 1.45 |
| 01100 | 1.40 |
| 01101 | 1.35 |
| 01110 | 1.30 |
| 01111 | Shutdown |
| 10000 | 1.275 |
| 10001 | 1.250 |
| 10010 | 1.225 |
| 10011 | 1.200 |
| 10100 | 1.175 |
| 10101 | 1.150 |
| 10110 | 1.125 |
| 10111 | 1.100 |
| 11000 | 1.075 |
| 11001 | 1.050 |
| 11010 | 1.025 |
| 11011 | 1.000 |
| 11100 | 0.975 |
| 11101 | 0.950 |
| 11110 | 0.925 |
| 11111 | Shutdown |

(*Id.*, 3:25-54 (Table of D4-D0 and corresponding output voltages).)

509. As such, a POSITA would have understood that OVID values can be

"00010" or "00110," specifying operating voltages of 1.9 V or 1.7 V, respectively,

and that an SVID value can be "10011," specifying a sleep voltage of 1.2 V. A

POSITA would have further understood that upon selection of OVID or SVID,

MVID, provided as input to the DC/DC converter (*e.g.*, a MAX1711 voltage

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regulator) can be any of these binary values.  A 5-bit value of any of the inputs

OVID, SVID, and MVID can be considered a single binary value of five bits or

any of these inputs can be considered a set of five binary values.

510.   As such, Helms discloses a multiplexor VID MUX having two inputs

OVID and SVID, where each input is a binary signal indicating an operating

voltage and a sleep voltage, respectively, which is a structure substantially the

same as the one that the '731 patent describes as performing the function recited in

this claim, as shown in a side-by-side comparison below.



1: Binary Signal Indicating Output Voltage to Be Supplied
2: Binary Signal Indicating Operating / Computing Voltage
3: Binary Signal Indicating Sleep Voltage
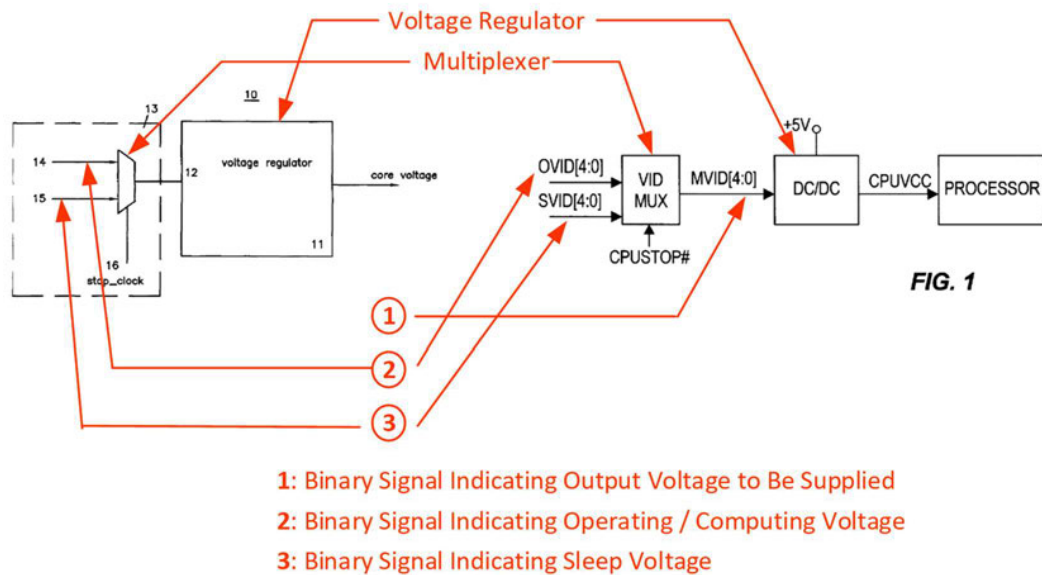
The '731 Patent, FIG. 3                                    Helms, FIG. 1

511.   Accordingly, Helms teaches "*means for accepting binary signals*

*indicating different levels of voltage*" and, thus, teaches the limitations of this

claim.

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### 4. Claim 10

#### a. Element 10[pre]: "The circuit as claimed in claim 8 in which the means for providing signals at the input terminal of the voltage regulator comprises:"

512. As discussed for Element 8[b.1], Helms teaches VID MUX as the "*means for providing signals at the input terminal of the voltage regulator*."
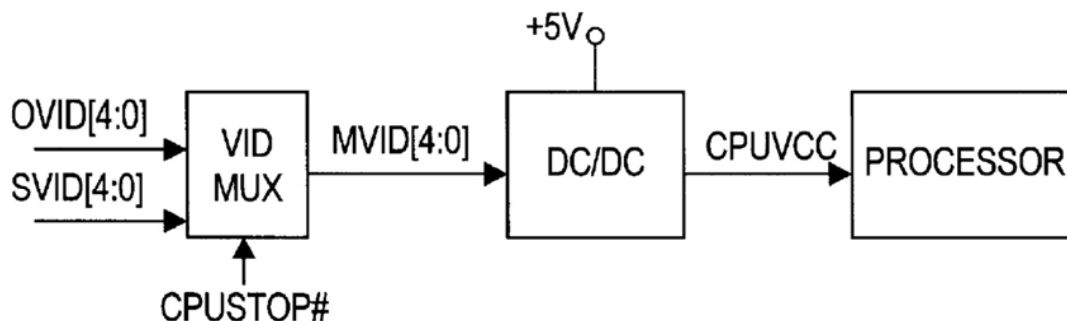
#### b. Element 10[a]: "selection circuitry,"

513. Helms teaches this Element because VID MUX is a multiplexor that selects its output from its inputs and, thus, constitutes "*selection circuitry*."

514. In particular, Helms states:

FIG. 1 shows a processor receiving a power supply voltage signal (CPUVCC) from a programmable voltage converter (DC/DC). The converter receives power (in this case +5V) and a voltage setting signal (MVID), and provides a regulated output voltage at the level indicated by the voltage setting signal. Because it is desirable to provide the system with a power-saving mode in addition to the normal operating mode, **the voltage setting signal has two possible values: SVID for "sleep" mode and OVID for "operating" mode. A multiplexer (VID MUX) selects between these two voltage settings** in response to a mode control signal (CPUSTOP#) which may be provided from the south bridge.

(Ex.1010, 2:42-54; FIG. 1.)

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*FIG. 1*

(*Id*. FIG. 1.)

515.  Thus, Helms explicitly states that the VID MUX "selects between" the OVID and SVID "voltage settings" and, hence, constitutes "*selection circuitry*."

### c.   Element 10[b]: "means for furnishing a plurality of signals at the input to the selection circuitry, and"

516.  Helms teaches this limitation because, Helms describes performing the function recited in this claim element ("*furnishing a plurality of signals at the input to the selection circuitry*") using a structure equivalent to that the '731 patent describes as performing the recited function.

517.  This claim element recites the function "*furnishing a plurality of signals at the input to the selection circuitry*."  The '731 patent discloses "a circuit 13 such as a multiplexor" having an "input 14" and "an input 15," where the multiplexor selects one of the inputs 14 and 15, and provides the selected input to the input 12 of the voltage regulator.  As discussed for Element 10[a], the

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multiplexor constitutes the "*selection circuitry*."

518. The inputs to the multiplexor may be provided "by the processor (or other circuitry)." Therefore, the '731 patent discloses a processor, *e.g.*, the processor receiving core voltage from the regulator, or "other circuitry" as the structure for "*furnishing a plurality of signals at the input to the selection circuitry*."

519. Specifically, the '731 patent states: "FIG. 3 is a circuit diagram illustrating a first embodiment of the invention. In the circuit 10 illustrated, a switching voltage regulator 11 receives an input signal at a terminal 12 which determines its output voltage value." (Ex.1001, 3:23-26; FIG. 3.) The '731 patent further states:

> In the circuit of FIG. 3, input to the terminal 12 is furnished via a circuit 13 such as a multiplexor that is capable of providing one or more input values. In the embodiment illustrated, **a value is provided at a first input 14** to the circuit 13 **by the processor (or other circuitry) which determines the operating condition** of the processor in its computing range; and a second value is provided at a second input 15 which is selected especially for the deep sleep condition. Either of these input values may be selected by a control signal provided at a control terminal 16 of the circuit 13.

(*Id.*, 3:52-62; FIG. 3.)

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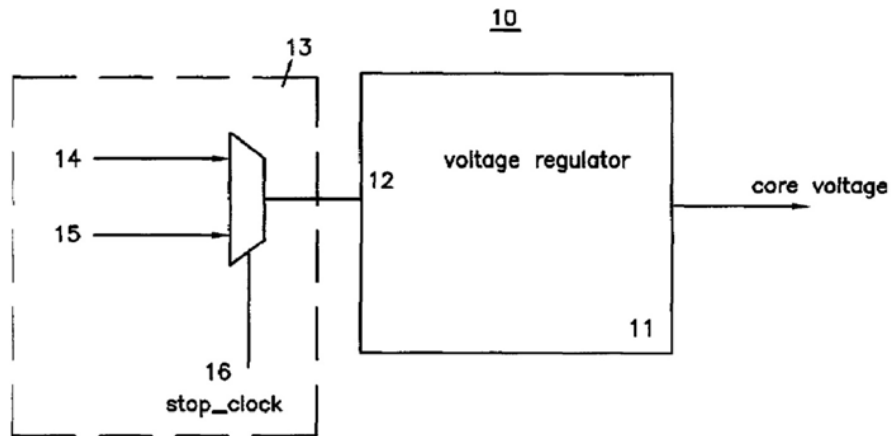U.S. Patent No. 7,260,731

Figure 3

(*Id.*, FIG. 3.)

520.   As such, a POSITA would have understood that the structure that the

'731 patent describes as performing the recited function of "*furnishing a plurality*

*of signals at the input to the selection circuitry*," where the multiplexor constitutes

the "*selection circuitry*," includes a processor, *e.g.*, the processor to which the

regulator provides the core voltage, or another circuitry.  (*See* Ex.1001, 3:54-60.)

521.   Helms describes performing the function this claim element recites

using substantially the same structure that the '731 patent describes.  Specifically,

as discussed for Elements 8[b.1] and 10[a], Helms discloses the multiplexor "VID

MUX"  as "*the means for providing signals at the input terminal of the voltage*

*regulator*" and the "*selection circuitry*."  The VID MUX has two inputs "OVID"

and "SVID" representing two different voltage settings, and the VID MUX

"selects between these two voltage settings" and provides the selected voltage

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setting as "MVID" to the "programmable voltage converter (DC/DC)" at its input

terminal. (*See* Ex.1010, 2:42-54; FIG. 1.)
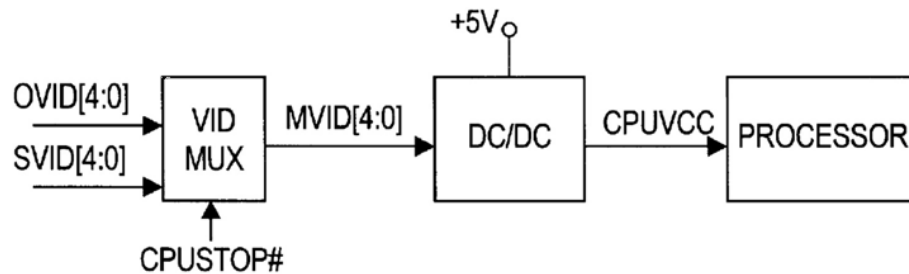


*FIG. 1*

(*Id.*, FIG. 1.)

522. As also discussed for Element 8[b.1], Helms discloses that the

"processor" of FIG. 1 can be an Athon$^{TM}$ processor (*see Id.*, 3:57-61), and that the

signals OVID and SVID may specify an operating voltage in the range 1.5-1.9 V

and a sleep voltage as low as 1.2 V, respectively, for an Athlon$^{TM}$ processor. (*See*

*id.* 2:42-54; *see also* Ex.1036 at 42, Table 9 (disclosing ranges of operating mode

and sleep mode voltages); Ex.1037 at 38, Table 8 (disclosing the same).)

523. In addition, in describing the embodiment of FIG. 2, Helms states that

"the **sleep voltage setting signals SVID are [] hardwired**, but the **operating**

**voltage setting signals are provided by the processor**." (Ex.1010, 4:31-33; FIG.

2.)

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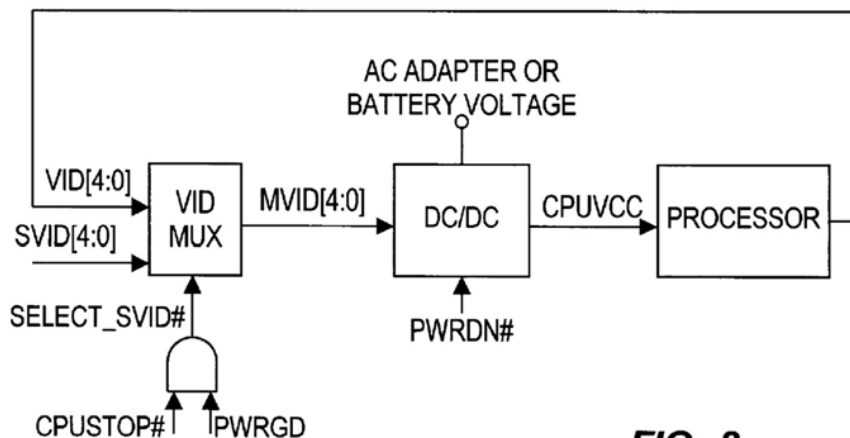


*FIG. 2*

(*Id*. FIG. 2.)

524.    As such, Helms discloses a multiplexor VID MUX having two inputs

OVID and SVID, where the OVID signal indicating an operating voltage at one

input may be specified by a processor.  The SVID signal indicating a sleep voltage

at the other input may be hardwired, *i.e.*, supplied via circuitry, such as fuses, that

provides "1" or "0" values to the respective input bits of SVID.  This a structure

substantially the same as the one that the '731 patent describes as performing the

function recited in this claim, as shown in side-by-side comparisons below to

Helms' FIGS. 1 and 2.

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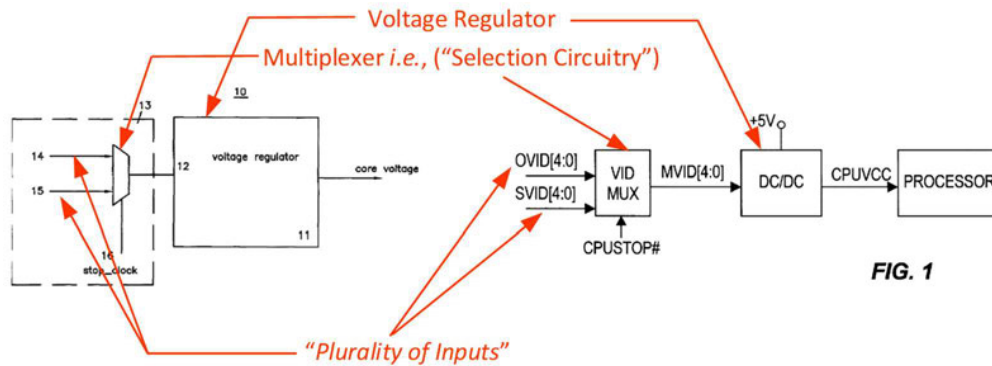Petition for *Inter Partes* Review of
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The '731 Patent, FIG. 3                    Helms, FIG. 1
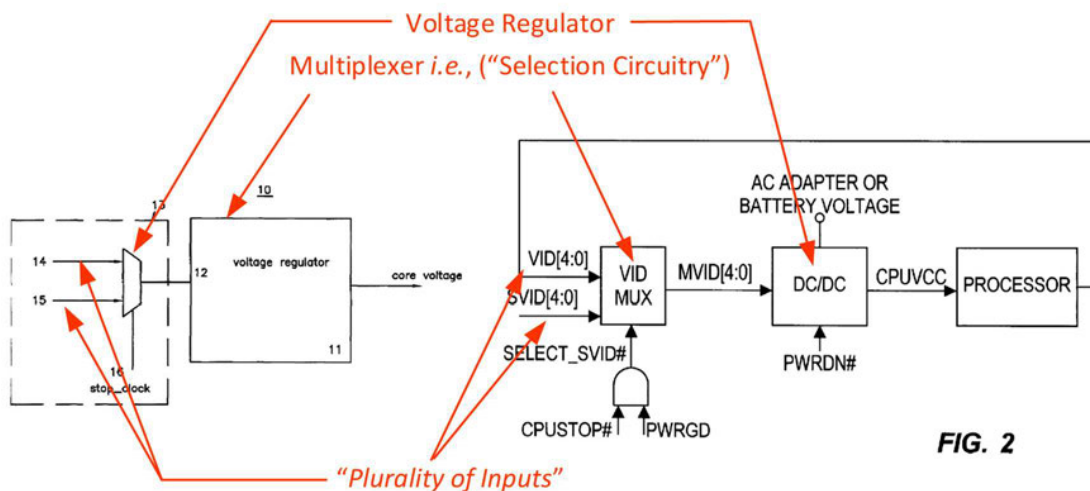


The '731 Patent, FIG. 3                    Helms, FIG. 2

525. Accordingly, Helms teaches "*means for furnishing a plurality of signals at the input to the selection circuitry*" and, thus, teaches this Element.

> **d.** **Element 10[c]: "means for controlling the selection by the selection circuitry."**

526. Helms teaches this limitation because, Helms describes performing the function recited in this claim element ("*controlling the selection by the*

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*selection circuitry*") by providing a control input "CPUSTOP#" to the multiplexor

**VID MUX** ("*selection circuitry*") for selecting from the inputs OVID and SVID,

and, thus, discloses a structure that is equivalent to that described in the '731 patent

as performing the recited function.

527.   This claim element recites the function "*controlling the selection by

the selection circuitry*."  The '731 patent discloses "a circuit 13 such as a

**multiplexor**" having an "input 14" and "an input 15," where the multiplexor

selects one of the inputs 14 and 15 using "a control signal provided at a control

terminal 16," and provides the selected input to the input 12 of the voltage

regulator.  Therefore, the '731 patent discloses "a control signal provided at a

control terminal 16" as the structure that is clearly linked to performing the

claimed function.

528.   Specifically, the '731 patent states: "FIG. 3 is a circuit diagram

illustrating a first embodiment of the invention. In the circuit 10 illustrated, a

switching voltage regulator 11 receives an input signal at a terminal 12 which

determines its output voltage value." (Ex.1001, 3:23-26; FIG. 3.)  The '731 patent

further states:

> In the circuit of FIG. 3, input to the terminal 12 is furnished via a
> circuit 13 such as a multiplexor that is **capable of providing one or
> more input values**. In the embodiment illustrated, a value is provided

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at a first input 14 to the circuit 13 by the processor (or other circuitry)
which determines the operating condition of the processor in its
computing range; and a second value is provided at a second input 15
which is selected especially for the deep sleep condition. **Either of
these input values may be selected by a control signal provided at
a control terminal 16** of the circuit 13. In one embodiment, a system
control signal normally utilized to signal entry into the deep sleep
condition (a stop clock signal) is used as the control signal to be
furnished at the control terminal 16.

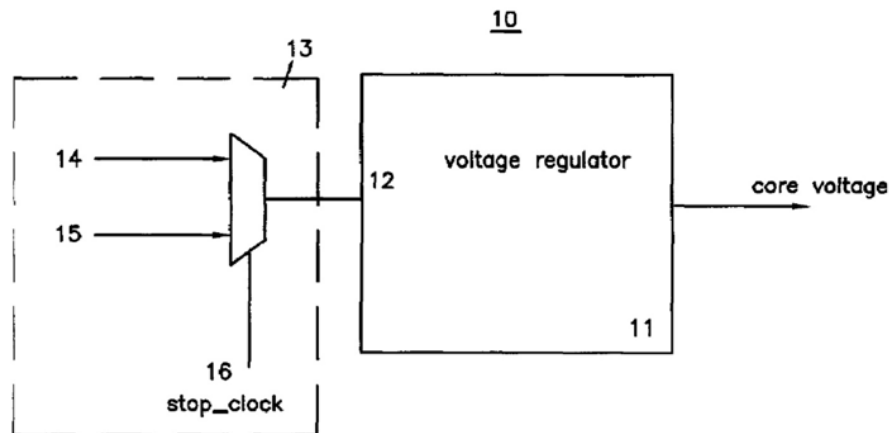(*Id.*, 3:52-65; FIG. 3.)



Figure 3

(*Id.*, FIG. 3.)

529. As such, a POSITA would have understood that the structure that the
'731 patent describes as performing the recited function of "*controlling the
selection by the selection circuitry*" includes a control signal, such as a "stop clock
signal" provided at a control terminal of the multiplexor.

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530. Helms describes performing the function this claim element recites

using substantially the same structure that the '731 patent describes. Specifically,

as discussed for Element 8[b.1], Helms discloses the multiplexor "VID MUX" *i.e.*,

"*the means for providing signals at the input terminal of the voltage regulator*."

The VID MUX has inputs "OVID" and "SVID" representing two voltage settings,

and the VID MUX "selects between these two voltage settings in response to a

mode **control signal (CPUSTOP#)** which may be **provided from the south**

**bridge**." (*See* Ex.1010, 2:42-54; FIG. 1.)

531. A POSITA would have readily understood that the control signal of a

multiplexor is provided at the multiplexor's control input or terminal. The VID

MUX provides the selected voltage setting as "MVID" to the "programmable

voltage converter (DC/DC)" at its input terminal. (*Id.*)
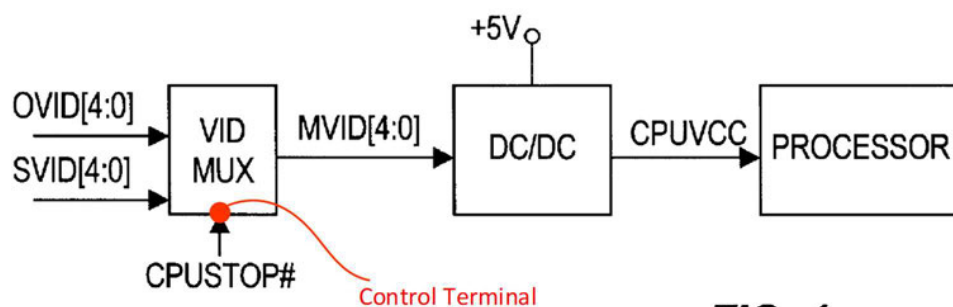


FIG. 1

(*Id.*, FIG. 1 (annotated).)

532. Helms further states:

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It is noted that **computer systems typically have multiple buses
with devices called "bridges"** that allow communications between
components on different buses. It is also noted that computer systems
typically have support circuitry that perform administrative functions
such as interrupt management (the interrupt controller),
clock/calendar/timer functions (the clock), configuration management,
power supply control, and power-on signal sequencing. **This support
circuitry has commonly been placed in the bridge** from the **PCI
bus to the peripherals** and lower bandwidth busses, *i.e.* **the "south
bridge."**

(*Id.*, 2:57-67.)

533.   A POSITA would have known the "south bridge" circuitry because,
prior to 2000, it was a standardized component that was widely used in computer
systems, as Helms states.  (*See id.*)  In fact, the '731 patent itself acknowledges that
"southbridge" circuitry in discussing "History of the Prior Art."  (*See* Ex.1001,
1:12 and 1:32-38.)  In particular, the '731 patent states:

**In the typical case**, disabling the processor is accomplished by
terminating the system clocks furnished to the processor. When
processor clocks have been disabled, controlling circuitry (typically a
portion of the **"Southbridge" circuitry** of an X86-processor-based
computer) remains enabled to detect interrupts requiring processor
operation.

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(*Id.*, 1:32-38.)

534.  The south bridge circuitry that Helms describes, and would have been

known to a POSITA, includes the CPUSTOP# control signal controlling Helms'

VID MUX.  In particular, AMD 756 Peripheral Bus Control Datasheet (Ex.AMD-

756-Datasheet) ("AMD-756-Datasheet") discloses that AMD-756 includes a "**PCI-**

**to-ISA Bridge** " and an "[e]nhanced master-mode **PCI IDE controller**" and, as

such, is a "south bridge" described in Helms.  (Ex.1038 at 21, 23, 22 (Figure 1);

*see* Ex.1010, 2:57-67 (describing that "south bridge" is a "bridge from the **PCI bus**

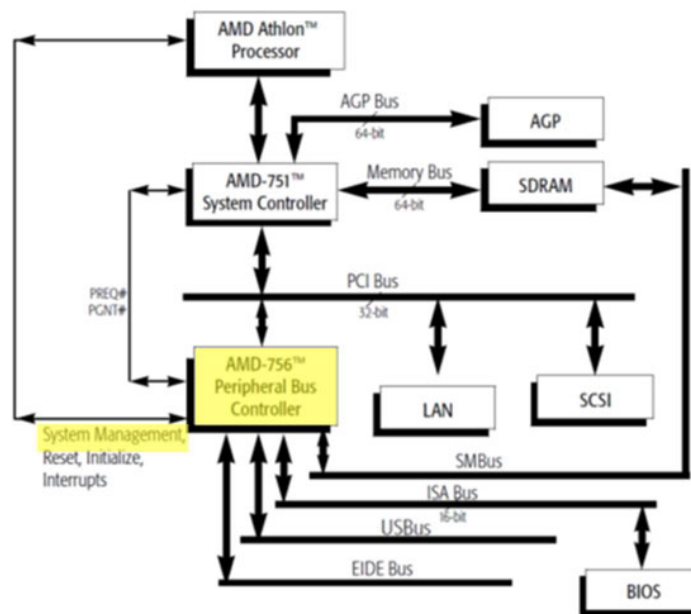**to the peripherals and lower bandwidth busses**").)



**Figure 1.    AMD-750™ Chipset System Block Diagram**

(Ex.1038 at 22, Figure 1 (depicting AMD-756 as a south bridge to an Athlon™

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processor) (annotated).)

535. AMD-756 provides a system management signal "CPUSTOP#" (*see*

Ex.1038 at 34 (Figure 3), 68.) AMD-756-Datasheet describes the "CPUSTOP#"

signal as a "processor clock stop" signal (*id*. at 6), and states that "CPUSTOP# []

**halts the CPU's clock** via the system PLL chip." (*Id*. at 140.)
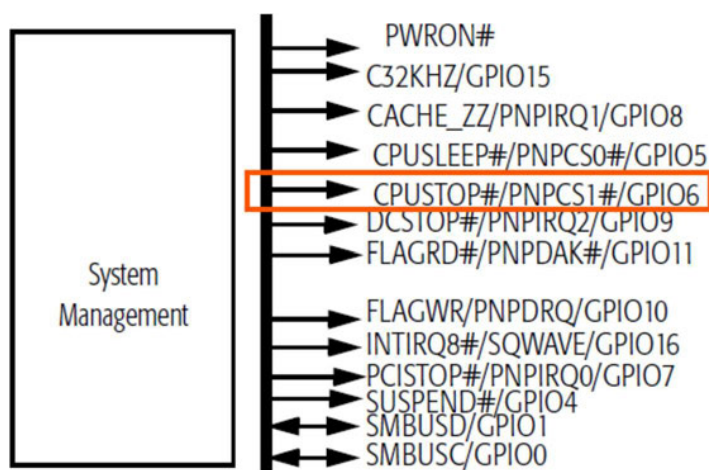


(*Id*. at 34, Figure 3 (partial, annotated).)

536. AMD-756-Datasheet also discloses that the CPUSTOP# signal, that

halts the CPU clock, can be asserted in the context of power management, *e.g.*, in

the "C3" state (*see id*. at 68 and 139 (Figure 28)) which, a POSITA would have

known, based on the ACPI standard, to be a sleep state for an Athlon processor.

(*See* Ex.1039 at 30 and 160; Ex.1036 at 25; Ex.1037 at 23.) These states include

sleep state C3. (Ex.1036 at 25, Figure 3 (reproduced an annotated below); Ex.1037

at 23, Figure 3.)

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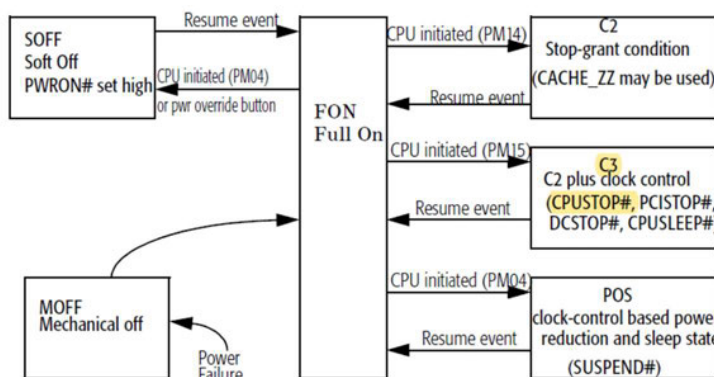U.S. Patent No. 7,260,731



**Figure 28. Power State Transitions**

(Ex.1038, 139 (Figure 28) (annotated).)

537.   As such, a POSITA would have understood the "CPUSTOP#" signal

that Helms discloses to be the typical south bridge signal "CPUSTOP#."  A

POSITA would have also known (as evidenced by AMD-756-Datasheet) that the

CPUSTOP# signal is used to disable the CPU clock and, thus, indicates disabled or

stopped CPU clock, when active.

538.   As such, Helms discloses a multiplexor VID MUX having two inputs

OVID and SVID, and where the signal CPUSTOP# received at a control input /

terminal indicates, when active, that the CPU clock is stopped.  The CPUSTOP# is

used to select one of the two inputs OVID and SVID.  This a structure substantially

the same as the one that the '731 patent describes as performing the function

recited in this claim, as shown in a side-by-side comparison below.

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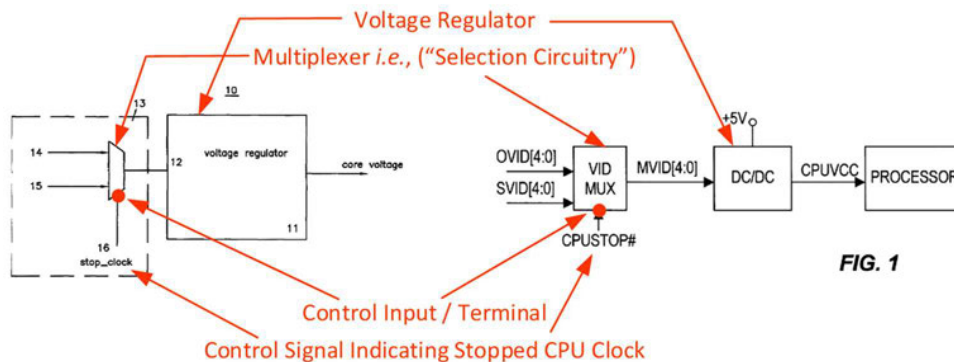


The '731 Patent, FIG. 3                    Helms, FIG. 1

539. Accordingly, Helms teaches "*means for controlling the selection by the selection circuitry*" and, thus, teaches the limitations of this claim. Helms thus teaches all of the elements of claim 10.

### 5. Claim 11

#### a. Element 11[pre]: "The circuit as claimed in claim 10 in which:"

540. As discussed for claim 10, the combination of Helms, Maxim-165X-Datasheet, and MAX1711-Kit teaches all of the limitations of claim 10.

#### b. Element 11[a]: "the selection circuitry is a multiplexor, and"

541. Helms teaches that the VID MUX ("selection circuitry") is a multiplexor. Specifically, Helms states:

Because it is desirable to provide the system with a power-saving mode in addition to the normal operating mode, the voltage setting signal has two possible values: SVID for "sleep" mode and OVID for

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"operating" mode. **A multiplexer (VID MUX) selects** between these two voltage settings in response to a mode control signal (CPUSTOP#) which may be provided from the south bridge.

(Ex.1010, 2:47-54; FIG. 1 (annotated).) Thus, Helms teaches this claim element.

> c.   **Element 11[b]: "the means for controlling the selection by the selection circuitry includes a control terminal for receiving signals indicating a system clock to the processor is being terminated."**

542.   As discussed for Element 10[c], the control input / terminal of Helms' VID MUX, where the control input / terminal receives the control signal CPUSTOP# and the VID MUX selects one of its inputs OVID and SVID accordingly, constitutes "*the means for controlling the selection by the selection circuitry.*"

543.   As also discussed for Element 10[c], a POSITA would have recognized (as evidenced by AMD-756-Datasheet) the signal CPUSTOP# as a southbridge signal that, when active, can be used to stop the CPU clock and, thus, may also indicate that the CPU clock is stopped or terminated. (*See* Ex.1010, 2:42-54 (describing the control signal "CPUSTOP#" and that this signal "may be provided from the south bridge"); FIG. 1; *see also*, *id*., 2:57-67 (describing that south bridge may be a "bridge from the PCI bus to the peripherals"); *see* Ex.1038 at 140 (stating that "CPUSTOP# [] halts the CPU's clock").)

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544. As such, Helms teaches that "*the means for controlling the selection by the selection circuitry includes*" the control input whether the signal CPUSTOP#, that may indicate that the CPU clock is stopped, is received, *i.e.*, "*a control terminal for receiving signals indicating a system clock to the processor is being terminated*" and, hence, teaches this claim element. Helms thus teaches all of the limitations of claim 11.

545. In summary, the combination of Helms, Maxim-165X-Datasheet, and MAX1711-Kit teaches each and every element of claims 8-11, and renders these claims unpatentable as obvious.

### 6.     Independent Claim 14

### a.     Elements 14[pre] through 14[c.2]

546. Elements 14[pre] through 14[b] are identical, respectively, to Elements 8[pre] through 8[b.1] and Elements 14[c.1] and 14[c.2] are substantially the same, respectively, as Elements 8[c.1] and 8[c.2], as set forth below:

| | |
|---|---|
| 8[pre]  A circuit for providing a regulated voltage to a processor comprising: | 14[pre]  A circuit for providing a regulated voltage to a processor comprising: |
| 8[a]  a voltage regulator having: | 14[a]  a voltage regulator having: |

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| | |
|---|---|
| 8[a.1]  an output terminal providing a selectable voltage, and | 14[a.1]  an output terminal providing a selectable voltage, and |
| 8[a.2]  an input terminal for receiving signals indicating the selectable voltage level; | 14[a.2]  an input terminal for receiving signals indicating the selectable voltage level; |
| 8[b.1]  means for providing signals at the input terminal of the voltage regulator for selecting a voltage for operating the processor in a computing mode and a voltage of a level less than that for operating the processor in a computing mode, | 14[b]  means for providing signals at the input terminal of the voltage regulator for selecting a voltage for operating the processor in a computing mode and a voltage of a level less than that for operating the processor in a computing mode; |
| 8[c.1]  <u>means</u> for changing the voltage regulator from a mode in which power is dissipated during a voltage transition <u>that reduces said selectable voltage</u> | 14[c.1]  <u>circuitry</u> for changing the voltage regulator from a mode in which power is dissipated during a voltage transition <u>in reduction of the selectable voltage</u> |
| 8[c.2]  to a mode in which power is saved during said voltage transition. | 14[c.2]  to a mode in which <u>system</u> power is saved during said voltage transition <u>in reduction of the selectable voltage, and</u> |

547.   The respective differences between Elements 14[c.1]-14[c.2] and

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Elements 8[c.1]-8[c.2] are indicated by underlining.

548.   As discussed for Element 8[c.1] "*means for changing*" the mode of

the voltage regulator, an input $\overline{\textbf{SKIP}}$ of a voltage regulator to select or force the

PWM/continuous mode of operation of the voltage regulator when the regulator's

output voltage is transitioning to a lower value (*e.g.*, in a light load condition), is

"*circuitry*" for changing the mode.  Moreover, a voltage transition that "*reduces*

*said selectable voltage*" is the same as a voltage transition "*in reduction of the*

*selectable voltage*."

549.   Therefore, for the reasons provided for Elements 8[pre] through 8[b.1]

and Elements 8[c.1] and 8[c.2], the combination of Helms, Maxim-165X-

Datasheet, and MAX1711-Kit teaches Elements 14[pre] through 14[c.2].

> **b.     Element 14[d]: "means for enabling the circuitry for conserving charge stored by the voltage regulator when the selectable voltage decreases."**

550.   The combination of Maxim-165X-Datasheet and MAX1711-Kit

teaches "*means for enabling the circuitry for conserving charge stored by the*

*voltage regulator when the selectable voltage decreases*" because Maxim-165X-

Datasheet in view of MAX1711-Kit describes forcing the operation of a MAX1653

controller (*voltage regulator*) in the forced PWM mode during a voltage transition

when the load is light (*i.e.*, *when the selectable voltage decreases*), where in the

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forced PWM mode charge stored by the output capacitor is conserved by the

inductor or input capacitor of MAX1653 controller.

551.   Thus, the combination of Maxim-165X-Datasheet and MAX1711-Kit

teaches the function of "*enabling the circuitry for conserving charge stored by the*

*voltage regulator when the selectable voltage decreases*." Maxim-165X-Datasheet

also discloses a controller input "$\overline{\text{SKIP}}$ [that] can be driven from an external logic

signal" to force transition to the PWM mode, which is a structure that is

substantially the same as that disclosed in the '731 patent for performing the

function recited in this claim element.

552.   This claim element recites the function of "*enabling the circuitry for*

*conserving charge stored by the voltage regulator when the selectable voltage*

*decreases*." The '731 patent discloses a voltage regulator configured to operate in

continuous and burst or efficient modes. (*See* Ex.1001, 5:48-53 and 6:1-6.) The

'731 patent further describes a "controlling input 50" for selecting the continuous

mode during a voltage transition as the structure that is clearly linked to

performing the claimed function.

553.   In particular, the '731 patent states:

The present invention utilizes the ability of **regulators to function in**

**both the high efficiency mode and the continuous mode** to

substantially reduce power wasted by transitioning between a

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computing and a lower voltage deep sleep mode. Although regulators

have not been dynamically switched between high efficiency and

continuous modes, in one embodiment of the invention, an **additional**

**controlling input 50 as shown in FIG. 5 is added to the regulator**

**for selecting the mode of operation** of the regulator based on

whether the processor being regulated is transitioning between states.

If the regulator receives a control signal 51 indicating that the

processor is to be placed into the deep sleep mode, for example, then a

**regulator operating in the high efficiency mode immediately**

**switches to the continuous mode during the voltage transition**.

Assuming that the regulator returns the charge to the battery during

continuous mode, this has the effect of reducing the waste of power

caused during the transition.

(*Id.*, 6:37-54; FIG. 5.)
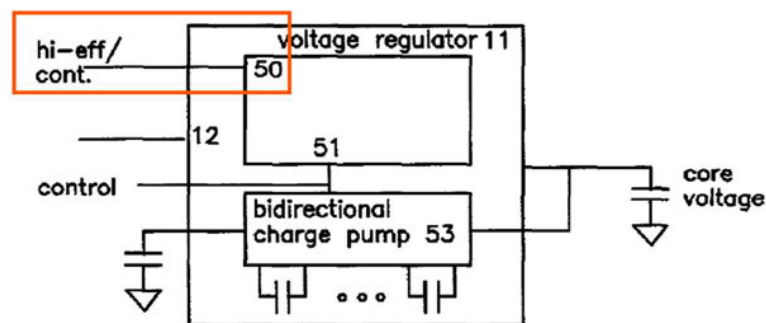


(*Id.*, FIG. 5 (annotated).)

554.   The original FIG. 5 labels the control input 50 as "high-eff / cont."

indicating a transition from the high-efficiency or burst mode to the continuous

mode.  It should be noted that even though the "burst" or "skip" mode is referred to

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as the "high efficiency mode," (*see id*., 6:1-6) during a voltage transition (a high-to-low voltage transition in particular), it is this mode that wastes power and the "continuous" mode saves power because the "regulator returns the charge to the battery during continuous mode."  (*See id*., 6:37-56.)

555.   It is noted that FIG. 5 depicts and the '731 patent describes "a charge pump 53 for storage" of charge, but this is provided only for "**regulators that do not conserve capacitive charge by transferring the charge to the battery**." (*See id*. 6:57-61; FIG. 5.)  Moreover, the "charge pump 53 for storage" of charge is properly understood as "*circuitry for conserving charge stored by the voltage regulator*" and not "*means for enabling*" such circuitry.  Since the charge can be transferred to the battery, *i.e.*, the battery supplying unregulated voltage to the regulator, the battery may also constitute the "*circuitry for conserving charge stored by the voltage regulator*."

556.   Thus, the '731 patent describes a regulator having a **control input 50** that can direct a transition from an otherwise high-efficiency pulse skipping mode to the continuous mode as the structure for performing the function recited in this claim element.
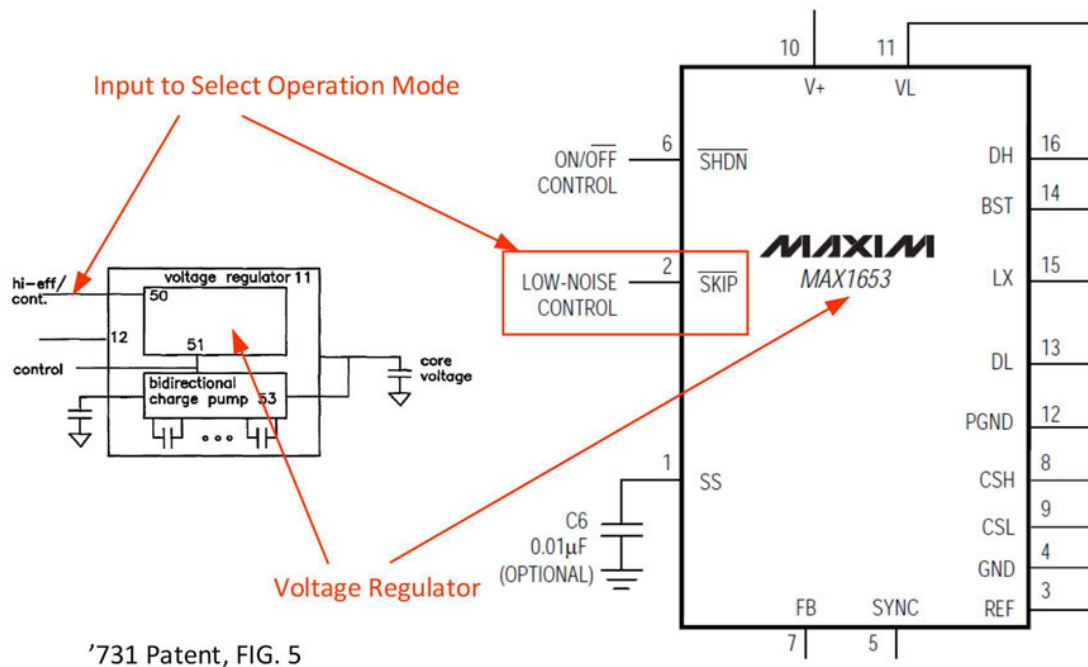
557.   Maxim-165X-Datasheet in view of MAX1711-Kit describes forcing the operation of a MAX1653 controller (*voltage regulator*) into the forced PWM

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mode during a high-to-low voltage transition (*i.e.*, *when the selectable voltage decreases*).  In the forced PWM mode charge stored by the output capacitor is conserved by the inductor or the input capacitor of MAX1653 controller, or may be returned to the battery.  This is explained above for Elements 8[c.1] and 8[c.2].  Thus, the combination of Maxim-165X-Datasheet and MAX1711-Kit teaches the function of "*enabling the circuitry for conserving charge stored by the voltage regulator when the selectable voltage decreases*."

558.    Moreover, Maxim-165X-Datasheet discloses that the MAX1653 controller has an input pin "$\overline{\text{SKIP}}$ [that] can be driven from an external logic signal" to force transition from the "pulse-skipping mode," which improves controller efficiency at light loads, to the PWM mode (also called the "**continuous-conduction mode**").  This is also explained above for claim element 8[c.1].  The purpose of the input pin "$\overline{\text{SKIP}}$" is the same as that of the control input 50 of the '731 patent.  Therefore, Maxim-165X-Datasheet teaches a structure that is substantially the same as that disclosed in the '731 patent for performing the function recited in this claim element, as a side-by-side comparison below shows.

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Maxim-165X-Datasheet, Figure 1 (partial)

559. Accordingly, the combination of Maxim-165X-Datasheet and MAX1711-Kit teaches this claim element.

560. In summary, Helms in view of Maxim-165X-Datasheet, further in view of MAX1711-Kit, teaches or at least suggests each and every element of claim 14, rending claim 14 unpatentable as obvious.

F. **GROUND 5: Claim 12, 13, and 15-18 Are Unpatentable as Obvious Over Helms in View of TI-TPS5210-Datasheet, Further in View of Nilsson**

1. **Motivation to Combine Helms, TI-TPS5210-Datasheet, and Nilsson**
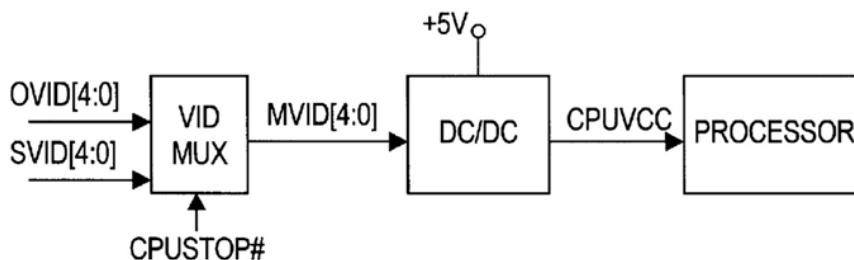
561. Helms and TI-TPS5210-Datasheet disclose systems and techniques in a closely related field of regulated power/voltage systems for processors. TI-

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TPS5210-Datasheet's voltage regulator employs an operational-amplifier-based

feedback network for voltage regulation. Nilsson is a textbook disclosing

difference amplifier/operational amplifier configurations.

562. In particular, Helms discloses a system in which core voltage is

supplied to a processor using a voltage regulator that can output a voltage as

specified at the regulator's input. (*See* Ex.1010, Abstract; 2:42-54.) Helms also

discloses selection circuitry coupled to the voltage regulator, where the selection

circuitry can select between a value (OVID) indicating an operating voltage and a

value (SVID) indicating a sleep voltage, and where the selected value (MVID) is

provided to the input of the voltage regulator, so that the regulator may supply a

core voltage corresponding to the selected value, *i.e.*, an operating voltage or a

sleep voltage. (*See id*., 2:42-54.)



FIG. 1

(*Id.*, FIG. 1.).

563. TI-TPS5210-Datasheet discloses "a synchronous-buck regulator

controller which provides an accurate, **programmable supply voltage to**

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**microprocessors**." (Ex.1008 at 1.) Similar to Helms' regulator, which receives

MVID as input and adjusts the output voltage accordingly, TI-TPS5210-Datasheet

discloses terminals VID0-VID4 that are "[d]igital inputs that **set the output**

**voltage** of the converter." (*Id*. at 3; 19 (Figure 18).)

564. TI-TPS5210-Datasheet also describes that the inputs VID0-VID4 can

be used to set a reference voltage $V_{REF}$, (*see id*. at 2, Figure "functional block

diagram"; 4; and 6, Table 1), and that, using a resistor-voltage-divider based

feedback network having resistors R2 and R3, the output voltage $V_O$ can be

adjusted as function of $V_{REF}$, as $V_O = V_{REF}(1 + \frac{R2}{R3})$. (*See id*. at 5; 19 (Figure 18);

21.)

565. While the output voltage $V_O$ can be raised above $V_{REF}$ using TI-

TPS5210-Datasheet's feedback network, Nilsson discloses a generic configuration

of such a feedback network. Nilsson states that the "output voltage of a difference

amplifier is proportional to the difference between the two input voltages."

(Ex.1013 at 200.)

566. A POSITA would have been motivated to consider the TPS5210

regulator as the voltage regulator in Helms' circuitry because Helms contemplates

such a combination. In particular, Helms states that "[o]ne example of a

programmable voltage converter is a MAXIM MAX1711 High-Speed, Digitally

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Adjusted Step-Down Controller or its **equivalent**." (Ex.1010, 3:18-20.) The

MAX1711 regulator is a "buck-regulator" that allows the selection of output

voltage via pins D0-D4. (*See* MAX-1711-Kit at 2, col. 2.)

567. As noted above, the TPS5210 regulator is also a buck regulator, the

output voltage of which can be set in a similar manner as for MAX1711, using

inputs VID0-VID4. (Ex.1008 at 1, 3, 19, Figure 18.) As such, a POSITA would

have understood that the TPS5210 regulator is equivalent to the MAX1711

regulator and, hence, suitable and intended to be used as Helms' voltage regulator.

568. Moreover, a POSITA would have been motivated to modify the

resistor-voltage-divider feedback network that TI-TPS5210-Datasheet discloses

according to a design that Nilsson discloses because such a modification would

allow regulating the output voltage according to a difference between two input

voltages (*see* Ex.1013 at 200), allowing the output voltage of the TPS5210

regulator to be both raised and lowered relative to $V_{REF}$, thus providing greater

flexibility and fine voltage tuning capabilities.

569. A POSITA would have recognized and appreciated these predictable

benefits of combining the teachings of these three references. To a POSITA, this

combination would have been nothing more than combining prior art elements

according to known methods (using the TPS5210 regulator as Helms' voltage

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regulator, and modifying the feedback network of that regulator as Nilsson

teaches), to obtain the predictable results described above.

570.   A POSITA would have also understood this combination to be the use

of a known technique (using a regulator that allows adjusting the output voltage

according to specified inputs and a resistor-voltage-divider based feedback

network) to improve a system employing a similar technique (Helms' system) in a

similar way as TI-TPS5210-Datasheet and Nilsson describe, or applying a known

technique (described above) to a known system (Helms') that is ready for

improvement, to yield predictable results described above.

571.   Additionally, a POSITA would have understood that these

predictable, beneficial results can be obtained without requiring substantial

changes or modifications to either Helms' system, or the regulator that TI-

TPS5210-Datasheet describes, and without adversely affecting the operation of

these systems or components.

572.   A POSITA would have also been able to apply known, conventional

circuitry configuration techniques to perform the necessary modifications.  As

such, a POSITA would have expected the combination of Helms, TI-TPS5210-

Datasheet, and Nilsson to succeed.  For these reasons, it would have been obvious

to a POSITA to combine Helms, TI-TPS5210-Datasheet, and Nilsson.

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## 2. Independent Claim 12

### a. Elements 12[pre] through 12[b]

573. Elements 12[pre] through 12[b] are identical, respectively, to

Elements 8[pre] through 8[b.1], as set forth below:

| | |
|---|---|
| 8[pre]  A circuit for providing a regulated voltage to a processor comprising: | 12[pre]  A circuit for providing a regulated voltage to a processor comprising: |
| 8[a]  a voltage regulator having: | 12[a]  a voltage regulator having: |
| 8[a.1]  an output terminal providing a selectable voltage, and | 12[a.1]  an output terminal providing a selectable voltage, and |
| 8[a.2]  an input terminal for receiving signals indicating the selectable voltage level; | 12[a.2]  an input terminal for receiving signals indicating the selectable voltage level; |
| 8[b.1]  means for providing signals at the input terminal of the voltage regulator for selecting a voltage for operating the processor in a computing mode and a voltage of a level less than that for operating the processor in a computing mode, | 12[b]  means for providing signals at the input terminal of the voltage regulator for selecting a voltage for operating the processor in a computing mode and a voltage of a level less than that for operating the processor in a computing mode; and[9] |

---

[9] This difference is insubstantial.

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574. As such, for the reasons provided under Ground 4 for Elements 8[pre] through 8[b.1], Helms teaches Elements 12[pre] through 12[b].

>   **b.      Element 12[c]: "means for reducing the selectable voltage below a lowest level the voltage regulator is specified to output."**

575. The combination of TI-TPS5210-Datasheet and Nilsson teaches "*means for reducing the selectable voltage below a lowest level the voltage regulator is specified to output*" because Nilsson teaches providing a bias voltage in a voltage-divider based feedback, that can reduce the output voltage below the lowest the regulator is specified to output, *i.e.*, the function recited in this claim element. Moreover, and the combination of TI-TPS5210-Datasheet and Nilsson discloses a controller (*voltage regulator*) using a resistor-voltage-divider-based feedback loop, where the resistor-voltage-divider is coupled to an offset voltage source, *i.e.*, a structure equivalent to that shown in the '731 patent for performing the recited function.

576. This claim element recites "*means for reducing the selectable voltage*" and the function recited is "*reducing the selectable voltage below a lowest level the voltage regulator is specified to output*." The '731 patent discloses a basic resistor-voltage-divider network feeding back the output voltage to the regulator, modified to include a voltage source, as the structure that is clearly

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linked to performing the claimed function. *See* Ex.1001, 5:2-22; FIG. 4.

577. Specifically, the '731 patent states that "it is desirable that the core voltage furnished during deep sleep be lowered to a level which may be below the level provided by a typical voltage regulator." (*Id.*, 5:2-6.) To this end, the '731 patent states:

> This desirable result may be reached utilizing a circuit such as that described in FIG. 4. The circuit of FIG. 4 includes a feedback network 41 for controlling the level of voltage at the output of the regulator 11. Prior art regulators such as the **Maxim 1711 provide a feedback terminal and describe how that terminal may be utilized with a resistor-voltage-divider network joined between the output terminal and ground to raise the output voltage level**.
>
> The embodiment of the present invention illustrated in 15 FIG. 4 utilizes the same feedback terminal and **a similar resistor-voltage-divider network but joins the divider between the output terminal and a source of voltage 42** higher than the normal output voltage of the regulator to force the output voltage level to a lower value rather than a higher level.

(*Id.*, 5:7-21; FIG. 4.)

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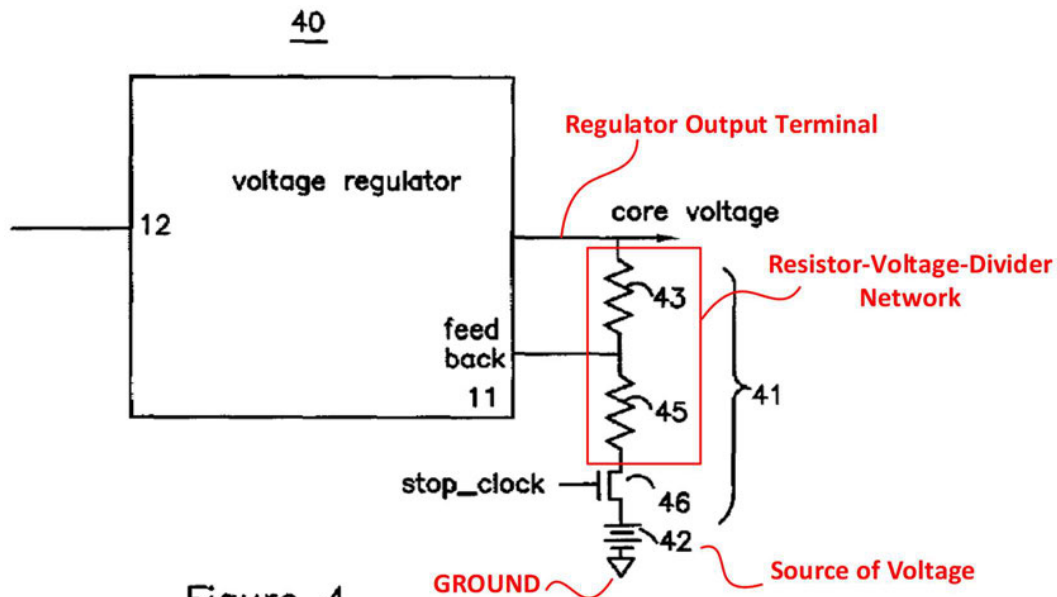U.S. Patent No. 7,260,731



Figure 4

(*Id*., FIG. 4 (annotated).)

578.   In basic configurations, the resistor-voltage-divider is connected

directly between an output terminal at which voltage is to be regulated and

GROUND (0 V).  The terminal between the two resistors of the divider is used as a

feedback terminal connected to a difference amplifier/operational amplifier that

controls additional circuitry and regulate the voltage at the output terminal.

579.   In FIG. 4, the resistor-voltage-divider is coupled to a voltage source

42 (via a switch 46).  (*See* Ex.1001, 5:10-21; FIG. 4.)  This configuration merely

introduces in the resistor-voltage-divider expression an offset-voltage term

corresponding to the voltage of the source 42, as opposed to zero corresponding to

the GROUND voltage, as discussed below.  Thus, the structure that performs the

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function recited in this claim element includes a "**resistor-voltage-divider
network**" that includes resistors 43 and 45, and that is joined "**between the output
terminal and a source of voltage** [] higher than the normal output voltage of the
regulator" (source of voltage 42).

580.   Recall that the discussion for the limitation "*means for providing
signals at the input terminal . . .*" that Elements 12[b] and 8[b.1] recite, the
corresponding structure from the '731 patent was identified in the discussion under
Ground 4 for Element 8[b.1] as a circuit shown in FIG. 3 of the '731 patent, *i.e.*, "a
circuit 13 such as a **multiplexor**" having an "**input 14**" and "**an input 15**."  The
discussion for this Element, however, relies on a structure shown in FIG. 4 of the
'731 patent.  This is consistent with the '731 patent, which states that "the circuitry
of FIGS. 3 and 4 may be combined so that **both input selection and output
adjustment are both used** to adjust the core voltage value produced by a voltage
regulator for deep sleep mode."  (Ex.1001, 5:43-47.)

581.   The combination of TI-TPS5210-Datasheet and Nilsson teach the
recited function of "*reducing the selectable voltage below a lowest level the
voltage regulator is specified to output.*"  Specifically, as discussed below, the TI-
TPS5210-Datasheet discloses a voltage regulator employing the basic
configuration of the resistor-voltage-divider, where the resistor-voltage-divider is

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coupled between the regulator's output and GROUND, and to a

difference/operational amplifier. Nilsson discloses a text-book configuration of a

difference/operational amplifier where the amplifier's output voltage can be scaled

using two input voltages. This allows the output voltage to be both raised and

lowered relative to one of the input voltages (*e.g.*, a reference voltage), resulting in

substantially the same structure that the '731 patent discloses in FIG. 4.

> 582.   In particular, TI-TPS5210-Datasheet states:

> The TPS5210 is a synchronous-buck regulator controller which
> provides an accurate, **programmable supply voltage to
> microprocessors**. An internal 5-bit DAC is used to program the
> reference voltage to within a **range of 1.3 V to 3.5 V**. The output
> voltage can be set to be equal to the reference voltage or to some
> multiple of the reference voltage.

(Ex.1008 at 1.) TI-TPS5210-Datasheet further discloses "Terminal Functions"

where terminals VID0-VID4 are [d]igital inputs that set the output voltage of the

converter.)

| VID0 | 27 | I | Voltage Identification input 0 |
| VID1 | 26 | I | Voltage Identification input 1 |
| VID2 | 25 | I | Voltage Identification input 2 |
| VID3 | 24 | I | Voltage Identification input 3 |
| VID4 | 23 | I | Voltage Identification input 4. Digital inputs that set the output voltage of the converter. The code pattern for setting the output voltage is located in Table 1. Internally pulled up to 5 V with a resistor divider biased from $V_{CC}$. |

(*Id*. at 3, Table: Terminal Functions (partially reproduced and annotated); *id*. at 19,

Figure 18 (depicting inputs VID0 through VID4 and stating that these inputs are

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"[u]ser-selected") (partially reproduced and annotated); *see id*. at 6, Table 1

(providing several values of VID0-VID4 and the corresponding $V_{REF}$ values that

determine the corresponding output voltages).)
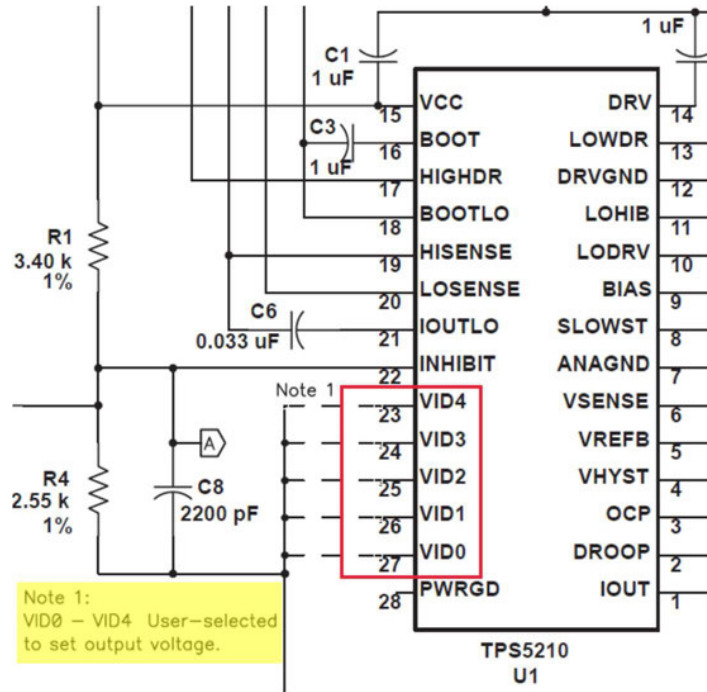


583.  TI-TPS5210-Datasheet discloses providing a sense voltage signal

VSENSE (*a feedback signal to the voltage regulator*) on an input pin (also called

VSENSE), where VSENSE is obtained from the output voltage $V_O$ via a resistor-

voltage-divider and, via a feedback circuitry, controls the output voltage $V_O$ such

that $V_O$ can be reduced "*below a specified output voltage.*"

584.  Specifically, the "Terminal Functions" table lists an input VSENSE

that is to "be **connected to converter output voltage** bus **to sense and control**

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**output voltage**." (Ex.1008 at 3, Table: Terminal Functions (partially

reproduced).)

| VSENSE | 6 | I | Voltage sense Input. To be connected to converter output voltage bus to sense and control output voltage. It is recommended an RC low pass filter be connected at this pin to filter noise. |
|--------|---|---|---|

585.  TI-TPS5210-Datasheet depicts that the input VSENSE is "connected

to the converter output voltage" not directly but via a resistor-voltage-divider

formed by the resistors R2 and R3, and via the resistor R5, to provide the voltage

VSENSE at the input VSENSE. (*Id*. at 19, Figure 18 (annotated).)



Figure 18. Standard Application Schematic

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586. TI-TPS5210-Datasheet also depicts in Figures "functional block diagram" and "Figure 18" that the input VSENSE is electrically connected to the output voltage $V_O$, because the input VSENSE controls two drive signals, namely, HIGHDR and LOWDR, that control high-side and low-side "power switching FETs" that, in turn, regulate the output voltage $V_O$.



(*Id*. at 2, "functional block diagram" (annotated to show electrical paths from VSENSE to HIGHDR AND LOWDR); at 3 Table: "Terminal Functions" (describing HIGHDR as "Output drive to high-side power switching FETs" and LOWDR as "Output drive to synchronous rectifier FETs").)

587. Thus, the resistor-voltage-divider includes resistor R2 coupled

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between the output voltage terminal $V_O$ and the feedback input VSENSE, and

resistor R3 coupled between VSENSE and ground (GND). (*See id*. at 19 (Figure

18).) VSENSE provides the feedback path for controlling HIGHDR and LOWDR

via an operational amplifier "Hysteresis Comp," as depicted in the functional block

diagram of TPS5210. (*See id*. at 2 ("functional block diagram").)
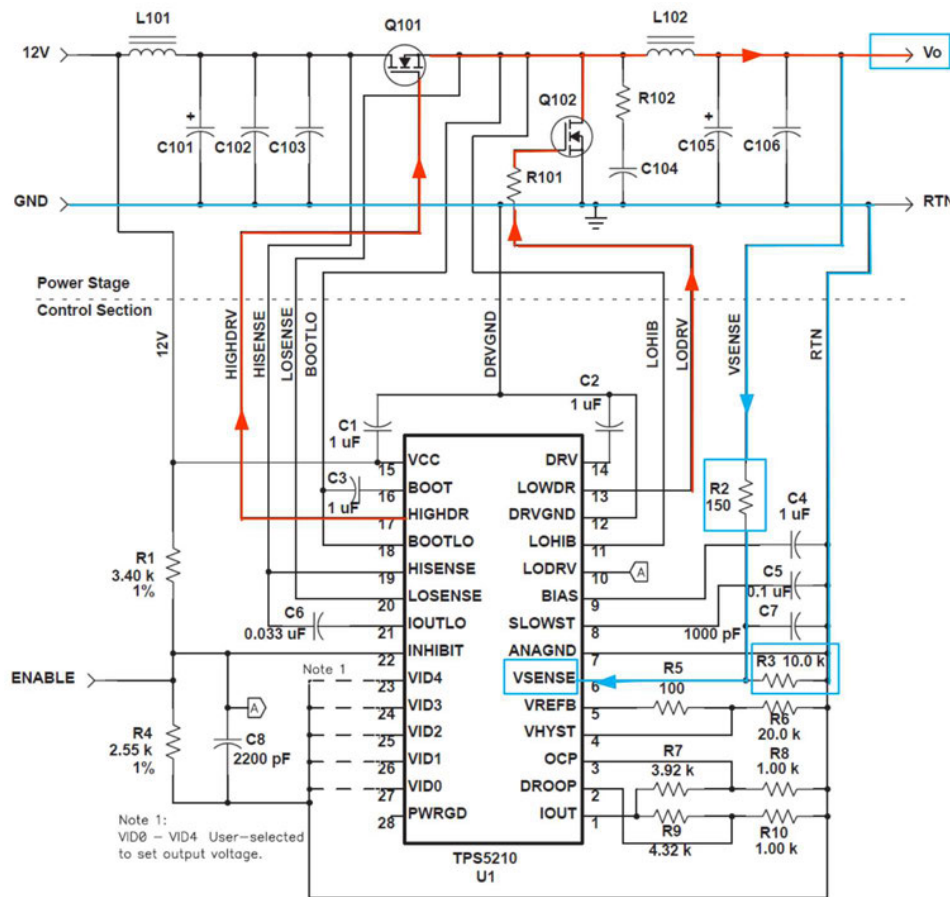


(*Id*. at 19, Figure 18 (annotated to show electrical paths from HIGHDR and

LOWDR to $V_O$).)

588.   Thus, since VSENSE is derived from $V_O$ and also controls $V_O$, it is a

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"*feedback signal to*" TPS5210, "*the voltage regulator*." In particular, TI-

TPS5210-Datasheet states: "$V_O$ is programmed to a voltage greater than $V_{REF}$ by an

external **resistor divider from $V_O$ to VSENSE**." (*Id*. at 5; *see id*. at 21 ("Values

above the maximum reference voltage (3.5 V) can be set by setting the reference

voltage to any convenient voltage within its range and selecting values for **R2 and**

**R3** to give the correct output"); at 19, Figure 18.) In addition, TI-TPS5210-

Datasheet states: "R2 and R3" forming the resistor-voltage-divider "can also be

used to make **small adjusts to the output voltage within the reference-voltage**

**range**" according to the Equation – a typical, well-known expression of a non-

inverting difference amplifier employing a resistor-voltage divider:

$$V_O = V_{REF}\left(1 + \frac{R2}{R3}\right)$$

(*Id*. at 21.)

589. The VSENSE pin, the circuitry that is internal to the TPS5210

regulator controller and that is driven by the voltage signal VSENSE which

provides the signals HIGHDR and LOWDR, and the external circuitry including

high-side FET and low-side FET that are driven by the signals HIGHDR and

LOWDR, together, constitutes a feedback circuit. The feedback circuit includes an

operational amplifier labeled "Hysteresis Comp" that receives VSENSE at the

inverting input and $V_{REF}$ at the non-inverting input. (*See id*. at 2, "functional block

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diagram.")  Thus, TI-TPS5210-Datasheet discloses a voltage regulator employing a

basic resistor-voltage-divider configuration that regulates the output voltage using

an operational-amplifier-based feedback circuitry.
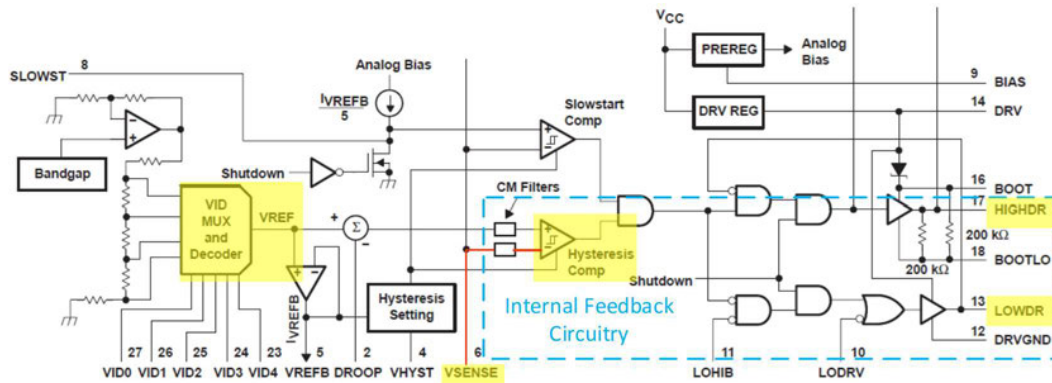


(*See id*. at 2, "functional block diagram" (partially reproduced and annotated).)

590.   TI-TPS5210-Datasheet also discloses a "VID network" and states that

the "output voltage of the VID network, $V_{REF}$, is within ±1% of the nominal setting

over the VID range of 1.3 V to 2.5 V."  (*Id*. at 4; *see id*. at 6, Table 1 (providing

several values of VID0-VID4 and the corresponding $V_{REF}$ values).)

591.   Thus, if VID is selected as "01111," the corresponding $V_{REF}$ would be

1.30 V, the lowest the TPS5210 controller (*voltage regulator*) is designed to

provide.  From the Equation above, a POSITA would have understood that the

output voltage would be slightly higher than $V_{REF}$, *e.g.*, greater than 1.30 V, when

VID is selected as "01111."

592.   Nilsson teaches the conventional difference amplifier / operational

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amplifier circuitry and states that "the output voltage of a difference amplifier is

proportional to the difference between the two input voltages." (Ex.1013 at 200.)



**FIGURE 6.14** A difference amplifier.
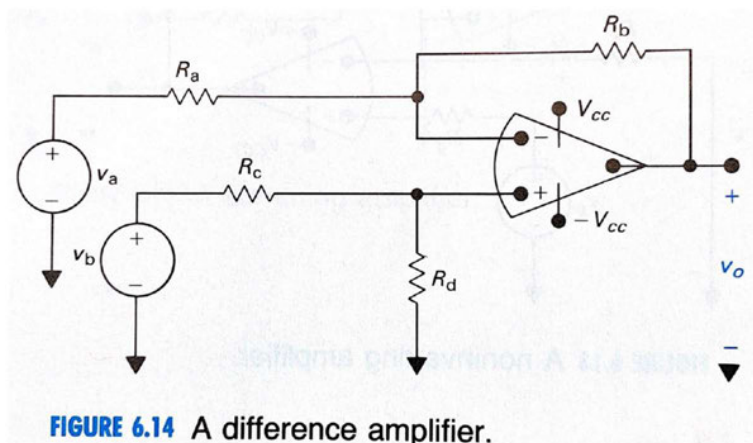
(Ex.1013 at 200 (Figure 6.14) (depicting two input voltages $v_a$ and $v_b$.)

593.   Nilsson discloses Equations 6.18 through 6.21 that govern the

operation of the "op amp" circuitry shown in Figure 6.14. (*See id*..) Nilsson

further discloses that when the ratio of resistors Ra and Rb is equal to that of

resistors Rc and Rd, (*see id*. (Equation 6.22)), the output voltage is given by:

$$v_o = \frac{R_b}{R_a}(v_b - v_a)$$
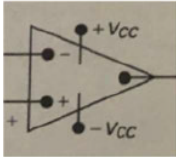
(*Id*. (Equation 6.23).)
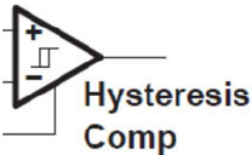
594.   A POSITA would have understood that when the non-inverting

terminal of the op-amp is not grounded via the resistor $R_d$ and is left open, the

effective value resistor $R_d$ is ∞. In that case, a POSITA would have understood

that Nilsson's Equations 6.18 through 6.21 take the form:

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$$v_o = v_b - (v_a - v_b)\left(\frac{R_b}{R_a}\right)$$

Thus, in this configuration also, the output voltage of the op-amp is proportional to a difference between two input voltages $v_a$ and $v_b$. Moreover, a POSITA would have understood that for any values of $R_b$ and $R_a$, if $v_a$ is greater than $v_b$, $v_o$ would be less than $v_b$.

595. The circuitry associated with a resistor-voltage-divider that TI-TPS5210-Datasheet discloses is based on Nilsson's text-book op-amp configuration, as shown in the table below:

| Component of TPS5210 | Corresponding Component in Circuitry of Nilsson's Figure 6.14 |
|---|---|
| Hysteresis Comp  | Op-amp  |
| Voltage $V_{REF}$ supplied to op-amp's non-inverting terminal | Voltage $v_b$ supplied to op-amp's non-inverting terminal |

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FIGURE 6.14 A difference amplifier.

| | |
|---|---|
| Resistor R2 connected between $V_O$ an VSENSE (inverting terminal) | Resistor $R_b$ connected between the output voltage and the inverting terminal |
| Resistor R3 connected between VSENSE (inverting terminal) and GROUND | Resistor $R_b$ connected between the inverting terminal and voltage $v_a$ |

(*See* Ex.1008 at 2 ("functional block diagram"), 19 (Figure 18); Ex.1013 at 200

(Figure 6.14).)

596.   The TI-TPS5210-Datasheet does not explicitly disclose the resistors

$R_c$ and $R_d$ that Nilsson discloses.  A POSITA would have understood, however,

that the resistance of the coupling between $V_{REF}$ and the non-inverting input

terminal would effectively provide the resistance $R_c$, and that the open circuit

between the non-inverting terminal and GROUND would effectively provide

resistance $R_d = \infty$.

597.   Thus, the only manner in which the circuitry of TPS5210-Datasheet is

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functionally different from Nilsson's circuitry is that it lacks the voltage source $v_a$

coupled between the resistor R3 and GROUND.  Coupling a voltage source

between the resistor R3 and GROUND would have been obvious to a POSITA

because first, such a configuration is consistent with a well-known, text-book

configuration that Nilsson discloses.  (*See* Ex.1013 at 200.)

598.   Second, TI-TPS5210-Datasheet explicitly contemplates "small adjusts

to the output voltage within the reference-voltage range." (Ex.1008 at 21.)  While

TI-TPS5210-Datasheet's configuration only allows **raising** $V_O$ relative to $V_{REF}$,

Nilsson's configuration facilitates **both raising and lowering** the output voltage

relative to the reference voltage, allowing fine control of the output voltage.

599.   Third, the modification of TI-TPS5210-Datasheet's circuitry accruing

to Nilsson is straightforward, requiring only the addition of a voltage source

between the resistor R3 and GROUND, as shown below.

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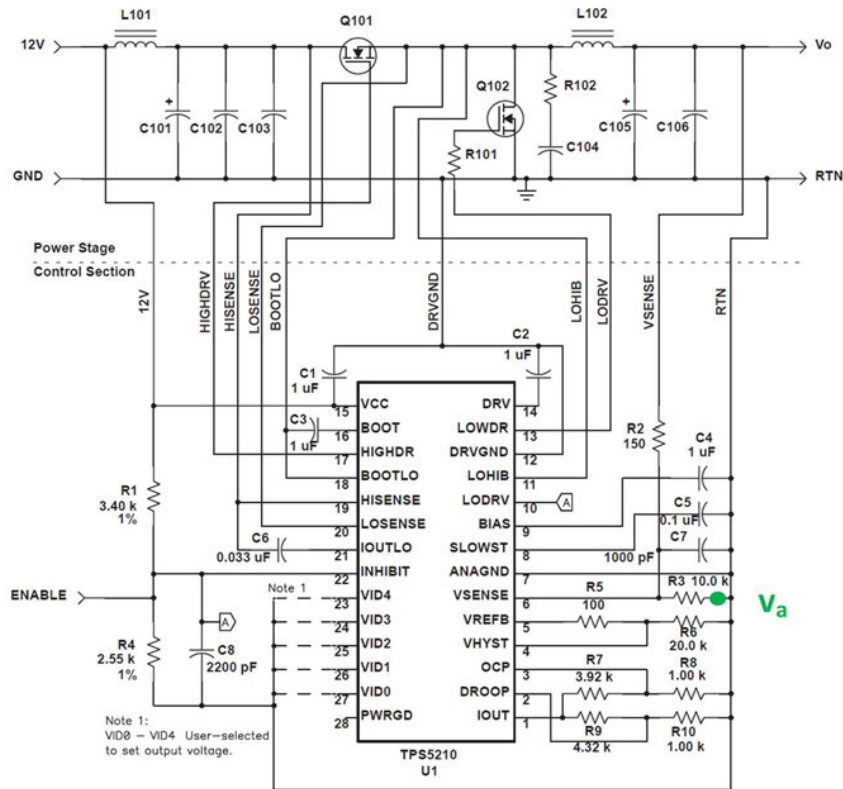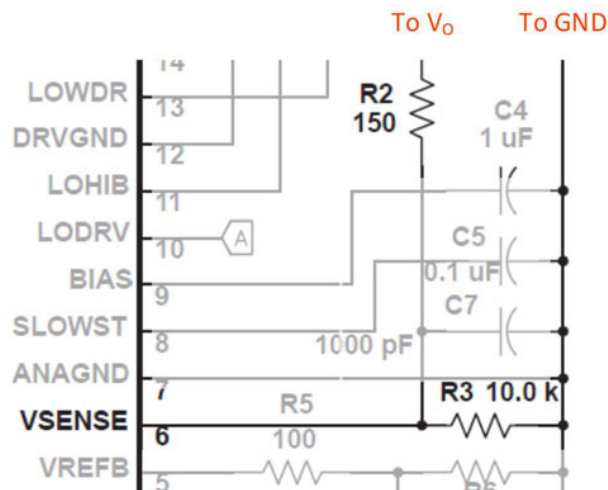Petition for *Inter Partes* Review of
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Figure 18. Standard Application Schematic

Ex.1008 at 19, Figure 18 (modified to include the voltage source $v_a$ in the same manner as Nilsson discloses).)



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(Ex.1008 at 19, Figure 18 (partial and annotated to highlight the resistor-voltage-
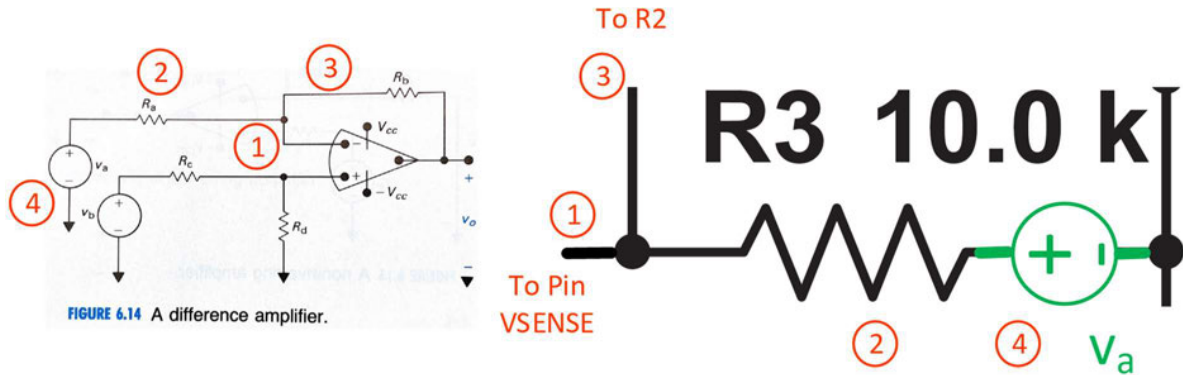
divider).)



FIGURE 6.14 A difference amplifier.

(1) To Feedback Input of Regulator

(2) "Lower" Resistor of Resistor Divider

(3) To "Upper" Resistor of Resistor Divider

(4) Biasing Voltage Source

(Ex.1013 at 200 (Figure 6.14); Ex.1008 at 19 (Figure 18) (partial and modified to

include the voltage source $v_a$ in the same manner as Nilsson discloses).)

600. With this modification, a POSITA would have understood that the

output voltage of the controller TPS5210 (*voltage regulator*) can be written as:

$$V_O = V_{REF} - (v_a - V_{REF})\left(\frac{R2}{R3}\right)$$

601. Thus, a POSITA would have understood that for any values of R2 and

R3 (*e.g.*, 150 Ω and 10 kΩ, respectively, as Figure 18 shows (*see* Ex.1008 at 19)),

**if $v_a$ is greater than V$_{REF}$, V$_O$ would be less than V$_{REF}$.**

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602.    As an example, a POSITA would have understood that if the inputs

VID0-VID4 are set as "01111" according to Table 1 (Ex.1008 at 6), $V_{REF}$ would be

1.3 V and, if $v_a$ is selected to be 2 V, per the Equation above, $V_O$ would be

approximately equal to 1.29 V.  As another example, if $v_a$ is selected to be 4 V,

per the Equation above, $V_O$ would be approximately equal to 1.26 V.  In general, a

POSITA would have understood that as long as the voltage $v_a$ is **greater than**

**$V_{REF}$** (1.3 V), which is the lowest selectable voltage of TPS5210 controller,

specified by the inputs VID0-VID4 set as "01111," the output voltage $V_O$ would be

"*below* [*the*] *lowest level* [*of 1.3 V*] *the voltage regulator is specified to output*."

603.    As such, TI-TPS5210-Datasheet in view of Nilsson discloses the

function recited in this claim element.

604.    The structure that the combination of TI-TPS5210-Datasheet in view

of Nilsson describes includes an external resistor-voltage-divider coupled between

the output voltage pin $V_O$ and pin VSENSE (*see* Ex.1008 at 19 (Figure 18)), where

a voltage source $v_a$ is added between the resistor R3 and ground, as Nilsson

teaches.  (*See* Ex.1013 at 200 (Figure 6.14.)  As explained above, pin VSENSE is a

feedback input, because it is connected to the op amp "Hysteresis Comp" the

output of which drives internal feedback circuitry that ultimately regulates the

output voltage $V_O$. (*See* Ex.1008 at 2, "functional block diagram," and at 19

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(Figure 18 (depicting that signals HIGHDR and LOWDR provided by TPS5210

control the output voltage $V_O$ via the high-side and low-side FETs)).)

605.　As also discussed above, the structure that the '731 patent discloses as

performing the recited function includes a resistor-voltage-divider coupled

between the output voltage and a feedback input of the regulator, where a voltage

source 42 is coupled between the resistor 45 and ground.  (Ex.1001, 5:7-21; FIG.

4.)  While FIG. 4 also includes a transistor/switch 46 controlled by the signal

"STOP_CLK," a POSITA would have understood that the resistor-voltage-divider

circuitry would function only when the switch 46 is turned ON and, in that case,

the source 42 would effectively be connected directly to the resistor 45, *i.e.*, in the

same manner as the modification discussed above.

606.　Thus, the structure that the combination of TI-TPS5210-Datasheet and

Nilsson describes is substantially the same as the structure that the '731 patent

provides for performing the function recited in this claim element, as a side-by-side

comparison below shows.

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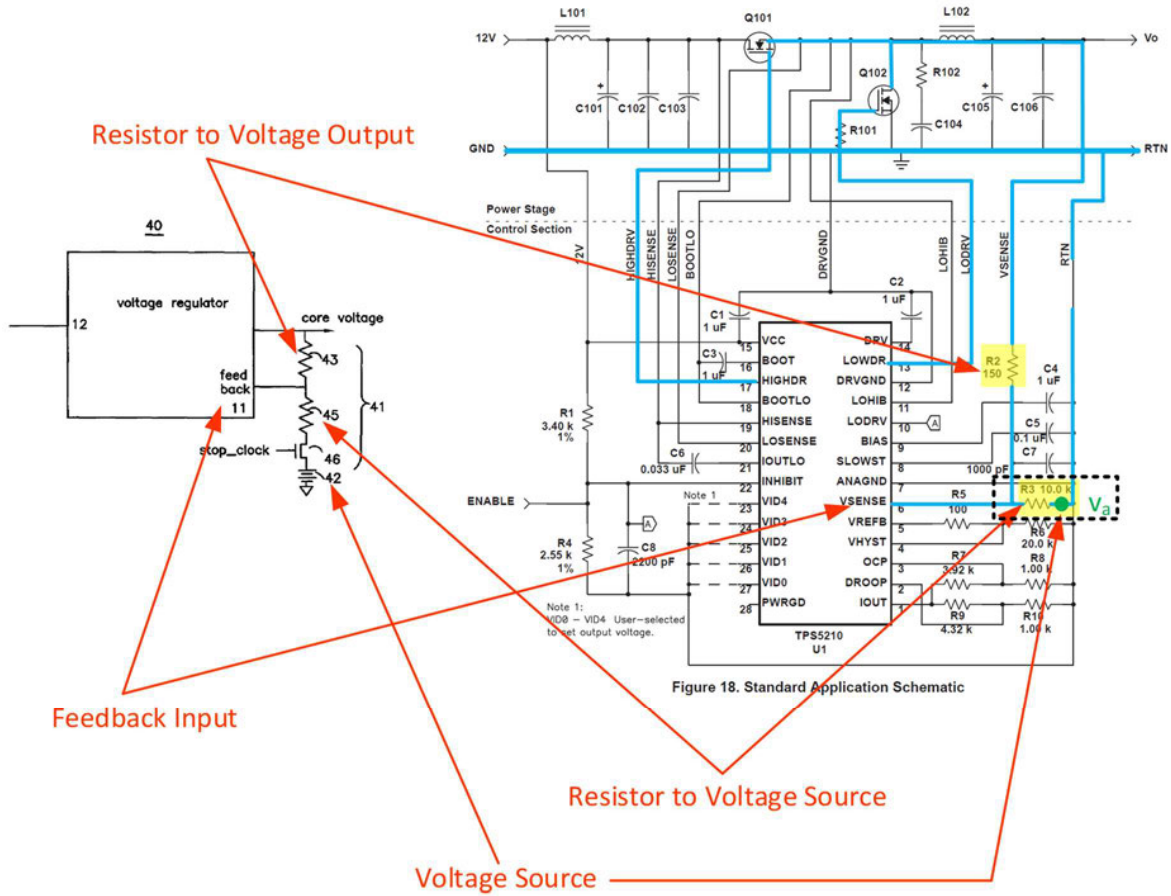U.S. Patent No. 7,260,731

The '731 Patent, FIG. 4

TI-TPS5210-DataSheet,
Figure 18 in View of
Knollman, Figure 3

(Ex.1001, FIG.4 (annotated); Ex.1008, at 19 (Figure 18).)  The dashed box in the

annotated figure above is zoomed in below, to show the voltage source $v_a$

connected between the resistor R3 and GROUND, as Nilsson teaches.

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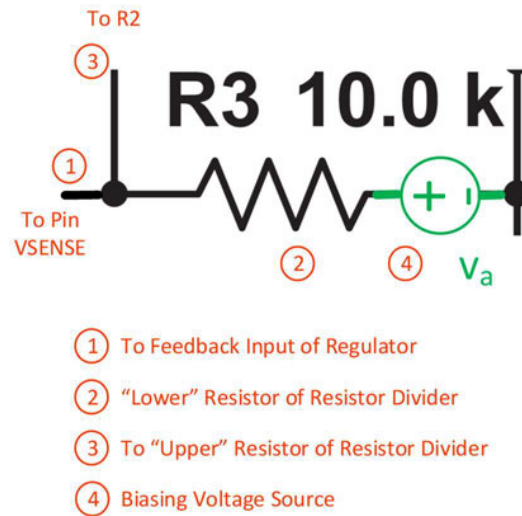


(Ex.1008, at 19 (Figure 18) (modified and zoomed in).)

607.    Even though Nilsson obtains the feedback directly from the op-amp

output while according to TI-TPS5210-Datasheet the output of the "Hysteresis

Comp" op-amp drives additional circuitry that ultimately provides $V_O$ (*see*

Ex.1008 at 2, "functional block diagram" and at 19 (Figure 18)), a POSITA would

have also understood that "Hysteresis Comp" op-amp and the additional circuitry

drive $V_O$ such that VSENSE is approximately equal to $V_{REF}$, so that $V_O =$

$V_{REF} \left(1 + \frac{R2}{R3}\right)$. (*See id.* at 21.)

608.    As such, as noted above, a POSITA would have further understood

that the "external resistor divider" having resistors R2 and R3 that TI-TPS5210-

Datasheet describes (*see id.* at 5), can be modified to include a "voltage source" $v_a$,

as Nilsson describes and depicts. (*See* Ex.1013 at 200 (Figure 6.14).)  In

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particular, Nilsson discloses a resistor-voltage-divider where the resistor Rb is

connected to the regulated output voltage and the resistor Ra is connected to the

voltage source $v_a$, which is connected to ground.

609. In the resistor-voltage-divider that TI-TPS5210-Datasheet discloses,

the resistor R2, which is coupled to the regulated output voltage $V_O$, is analogous

to Nilsson's resistor Rb, and the resistor R3 is analogous to Nilsson's resistor Ra.

A voltage source, such as $v_a$, can be included between the resistor R3 and ground,

as shown above.

610. A POSITA would have been motivated to make the above-described

modification for at least two reasons. First, prior to 2000, extending the output-

voltage range of a voltage regulator was a well-known objective. (*See, e.g.*,

Ex.1040 at 13 (stating that the "**output voltage [of TPS5210] can be extended**

**down to 0 V to 1.3 V** using the auxiliary circuitry described in this note");

Ex.1041, 1:15-18 (describing "a built-in voltage drop circuit for reducing power

source voltage so as to operate internal circuits such as a memory cell array at a

low voltage")). It was known that such lower regulated voltages can significantly

minimize static power consumption in the sleep state of a CPU and/or in other

circuitry that may be operated a slow speeds. Second, the modification as

described above requires nothing more than adding a voltage source between the

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resistor R3 and ground, and is therefore simple and inexpensive.

611. As such, the combination of TI-TPS5210-Datasheet and Nilsson

teaches this claim element.

612. In summary, Helms in view of TI-TPS5210-Datasheet, further in view

of Nilsson, teaches each and every element of claim 12 and renders it unpatentable,

as obvious.

### 3. Independent Claim 13

#### a. Elements 13[pre] through 13[a.2]

613. Elements 13[pre] through 13[a.2] are identical, respectively, to

Elements 8[pre] through 8[a.2], as set forth below:

| | |
|---|---|
| 8[pre] A circuit for providing a regulated voltage to a processor comprising: | 13[pre] A circuit for providing a regulated voltage to a processor comprising: |
| 8[a] a voltage regulator having: | 13[a] a voltage regulator having: |
| 8[a.1] an output terminal providing a selectable voltage, and | 13[a.1] an output terminal providing a selectable voltage; |

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| 8[a.2]  an input terminal for receiving signals indicating the selectable voltage level; | 13[a.2]  an input terminal for receiving signals indicating the selectable voltage level; and[10] |
|---|---|

614.   As such, for the reasons provided under Ground 4 for Elements 8[pre]

through 8[a.2], Helms teaches Elements 13[pre] through 13[a.2].

### b.   Element 13[a.3]: "a voltage regulator feedback circuit;"

615.   TI-TPS5210-Datasheet discloses "*a voltage regulator feedback*

*circuit*" because the TPS5210 regulator controller (voltage regulator) includes a

pin VSENSE that can be coupled via a resistor-voltage-divider to the output

voltage pin $V_O$, and because the voltage signal VSENSE received at the pin

VSENSE drives internal circuity that provides signals HIGHDR and LOWDR that

drive high-side and low-side FETs, that ultimately regulate the output voltage $V_O$,

thus forming a feedback loop, where the circuitry of the feedback loop is a

"*voltage regulator feedback circuit*."

616.   In particular, as discussed for Element 12[c], a resistor-voltage-divider

having the resistors R2 and R3 provides a signal VSENSE at the VSENSE pin, and

the VSENSE pin, the internal circuitry coupled to the VSENSE pin, and the

---

[10] This difference is insubstantial.

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external circuitry driven by the signals HIGHDR and LOWDR, together, constitute

feedback circuitry for the TPS5210 regulator controller.  Thus, TI-TPS5210-

Datasheet discloses "*a voltage regulator feedback circuit*."

### c.    Element 13[b]

617.   Element 13[b] is identical to Element 8[b.1], as set forth below.

| 8[b.1]  means for providing signals at the input terminal of the voltage regulator for selecting a voltage for operating the processor in a computing mode and a voltage of a level less than that for operating the processor in a computing mode, | 13[b]  means for providing signals at the input terminal of the voltage regulator for selecting a voltage for operating the processor in a computing mode and a voltage of a level less than that for operating the processor in a computing mode; and[11] |
|---|---|

618.   As such, for the reasons provided under Ground 4 for Element 8[b.1],

Helms teaches Element 13[b].

### d.    Element 13[c]

619.   Element 13[c], in substance, is the same as Element 12[c], as set forth

below:

| 12[c]  means for reducing the selectable voltage below a <u>lowest</u> level | 13[c]  means for reducing the selectable voltage below a level |
|---|---|

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[11] This difference is insubstantial.

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| the voltage regulator is specified to output | provided by the voltage regulator comprising |
|---|---|

620. Since "*a lowest level the voltage regulator is specified to output*" is "*a level provided by the voltage regulator*," for the reasons provided under this Ground for Element 12[c], TI-TPS5210-Datasheet in view of Nilsson teaches Element 13[f].

        e.        **Element 13[c.1]: "a voltage divider network joined between the output terminal and a voltage source furnishing a value higher than the selectable voltage, and"**

621. The combination of TI-TPS5210-Datasheet and Nilsson discloses "*a voltage divider network joined between the output terminal and a voltage source furnishing a value higher than the selectable voltage*" because, as discussed for Element 12[c], TI-TPS5210-Datasheet discloses a resistor-voltage-divider and Nilsson discloses a voltage source $v_a$.

622. In particular, as discussed for Element 12[c], TI-TPS5210-Datasheet discloses a resistor-voltage-divider having the resistors R2 and R3 provides a signal VSENSE at the VSENSE pin of the TPS5210 controller (*voltage regulator*). The resistor-voltage-divider is coupled to the output $V_O$ (*output terminal*) of the TPS5210 controller. (*See* Ex.1008 at 19 (Figure 18).)

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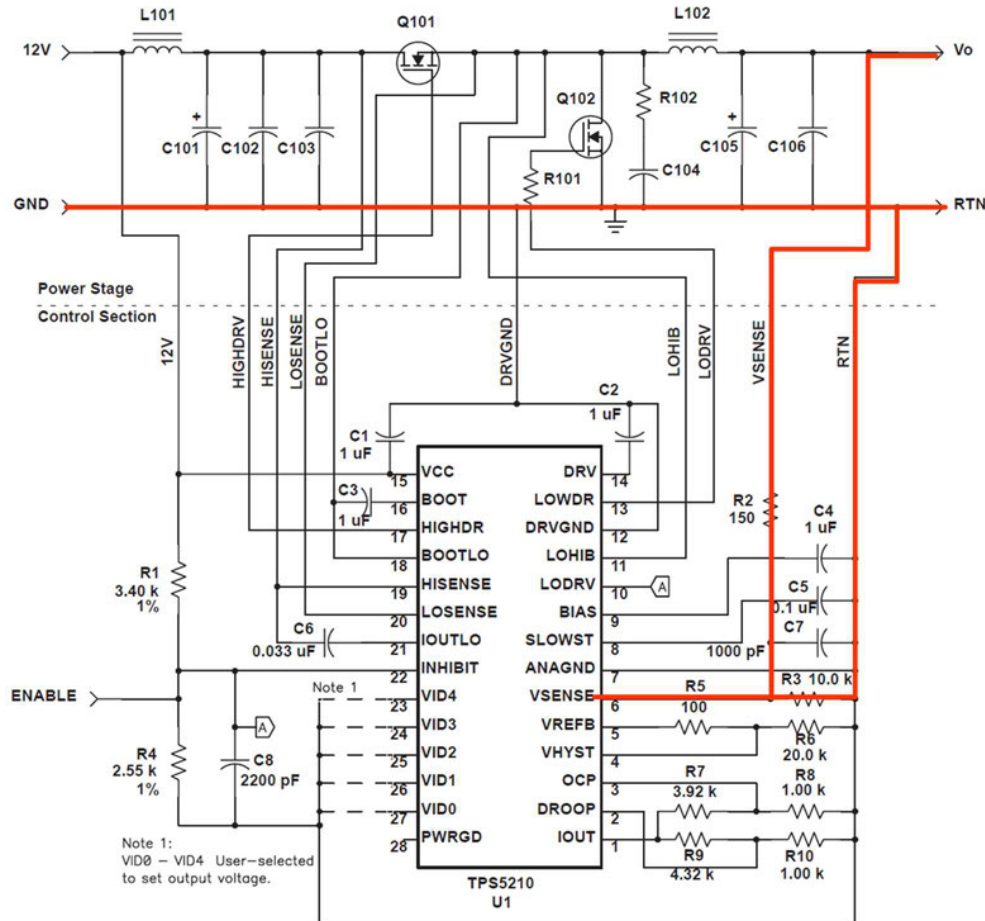


Figure 18. Standard Application Schematic

(*Id*. at 19 (Figure 18 (annotated)).)

623.   Per Ohm's law, the voltage VSENSE is a fraction of the voltage $V_O$

given by the expression $\text{VSENSE} = V_O\left(\frac{R3}{R2+R3}\right)$ and, hence, TI-TPS5210-

Datasheet's resistor-voltage-divider does function a *voltage divider*.

624.   Nilsson discloses a voltage source $v_a$ coupled between one of the

resistors of a resistor-voltage-divider and ground.  (*See* Ex.1013 at 200 (Figure

6.14).)

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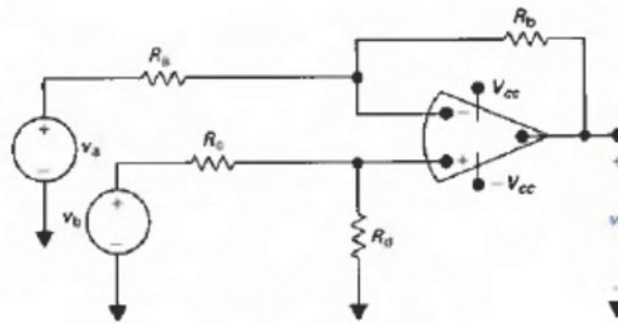U.S. Patent No. 7,260,731



**FIGURE 6.14** A difference amplifier.

(Ex.1013 at 200 (Figure 6.14).)

625.  As further discussed for Element 12[c], a POSITA would have

understood that the resistor-voltage-divider of the TPS5210 controller can be

readily modified as Nilsson discloses, so that the output voltage can finely tuned

by **either raising or lowering** it relative to a selected reference voltage.  As shown

below, in the resistor-voltage-divider of the TPS5210 controller so modified, the

resistor-voltage-divider is coupled between the output voltage pin $V_O$ and a voltage

source $v_a$, as Nilsson discloses.

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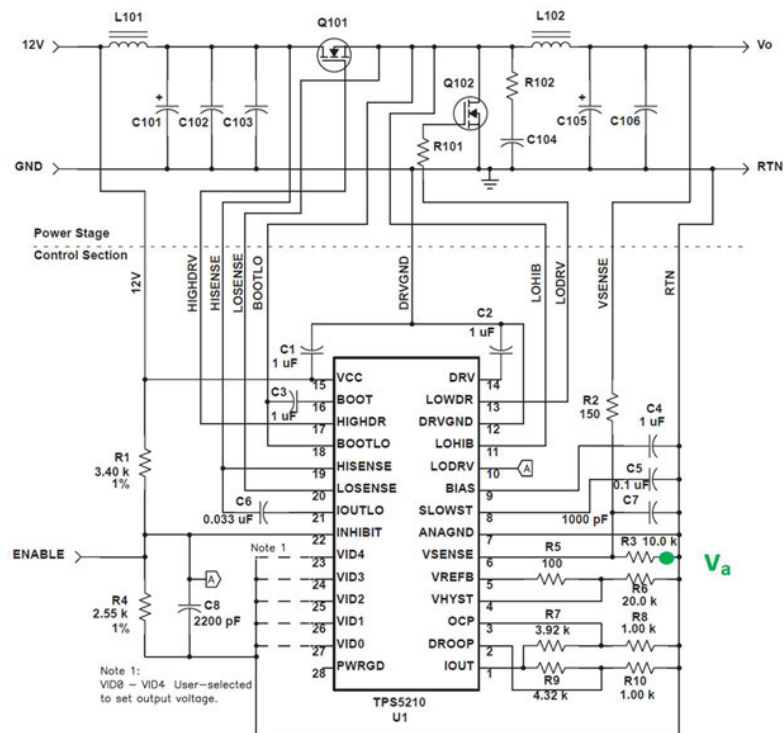U.S. Patent No. 7,260,731



Figure 18. Standard Application Schematic

(Ex.1008 at 19 (Figure 18 (modified)).)

626. As also discussed for Element 12[c], a POSITA would have

understood that to lower the output voltage $V_O$ relative to $V_{REF}$, the voltage source

$v_a$ must provide a voltage greater than $V_{REF}$. Since VID0-VID4 set as "01111"

specifies the lowest selectable $V_{REF}$ of 1.3 V, (*see* Ex.1008 at 6, Table 1), a

POSITA would have understood that providing $v_a$ **greater than the lowest**

**selectable $V_{REF}$** of 1.3 V, and by setting VID0-VID4 to "01111," the output

voltage $V_O$ of the TPS5210 controller would be **lowered** below 1.3 V, as Nilsson

suggests.

627. In particular, Nilsson's Equation 6.21 shows that while the output

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voltage is scaled up from a voltage $v_b$, it is scaled down from a voltage $v_a$ (*See*

Ex.1013 at 200; *id*. (Figure 6.14).)  As discussed above in connection with Element

12[c], in the voltage regulator of TI-TPS5219-Datasheet, modified according to

Nilsson's configuration, the output voltage is given by:

$$V_O = V_{REF} - (v_a - V_{REF}) \left(\frac{R2}{R3}\right)$$

628.   As also discussed in connection with Element 12[c], in one example,

if the inputs VID0-VID4 are set as "01111" according to Table 1 (Ex.1008 at 6),

$V_{REF}$ would be 1.3 V, the lowest voltage the TPS5219 controller/regulator is

specified to output.  If $v_a$ is selected to be 2 V, per the Equation above, $V_O$ would

be approximately equal to 1.29 V.  If $v_a$ is selected to be 4 V, per the Equation

above, $V_O$ would be approximately equal to 1.26 V.  In general, a POSITA would

have understood that as long as the voltage $v_a$ is **greater than $V_{REF}$** (1.3 V), the

output voltage $V_O$ would be "*below [the] lowest level [of 1.3 V] the voltage*

*regulator is specified to output*."

629.   Thus, the combination of TI-TPS5210-Datasheet and Nilsson

discloses "*a voltage divider network joined between the output terminal and a*

*voltage source furnishing a value higher than the selectable voltage*" and, thus,

teaches this Element.

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> **f.      Element 13[c.2]: "the voltage regulator feedback
> circuit receiving a value from the voltage divider
> network."**

630.   TI-TPS5210-Datasheet discloses "*the voltage regulator feedback
circuit receiving a value from the voltage divider network*" because the TPS5210
regulator controller (voltage regulator) includes a pin VSENSE that receives the
signal VSENSE via a resistor-voltage-divider (*the voltage divider network*).

631.   As discussed for Element 12[c], the TPS5210 controller has a pin
VSENSE that can coupled to the output voltage pin $V_O$ via a resistor-voltage-
divider having resistors R2 and R3.  Through the resistor-voltage-divider (voltage
divider) the pin VSENSE receives a signal VSENSE.  As also discussed for
Element 12[c], the VSENSE pin, the internal circuitry coupled to the VSENSE pin,
and the external circuitry driven by the signals HIGHDR and LOWDR, together,
constitute feedback circuitry for the TPS5210 regulator controller, *i.e.*, the "*voltage
regulator feedback circuit*."

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Figure 18. Standard Application Schematic

(Ex.1008 at 19 (Figure 18 (annotated)).)

632.    Thus, TI-TPS5210-Datasheet discloses "*the voltage regulator feedback circuit receiving a value*" VSENSE "*from the*" resistor-voltage-divider, *i.e.*, the "*voltage divider network*" and, hence, teaches this Element.

633.    In summary, Helms in view of TI-TPS5210-Datasheet, further in view of Nilsson, teaches each and every element of claim 13 and renders it unpatentable, as obvious.

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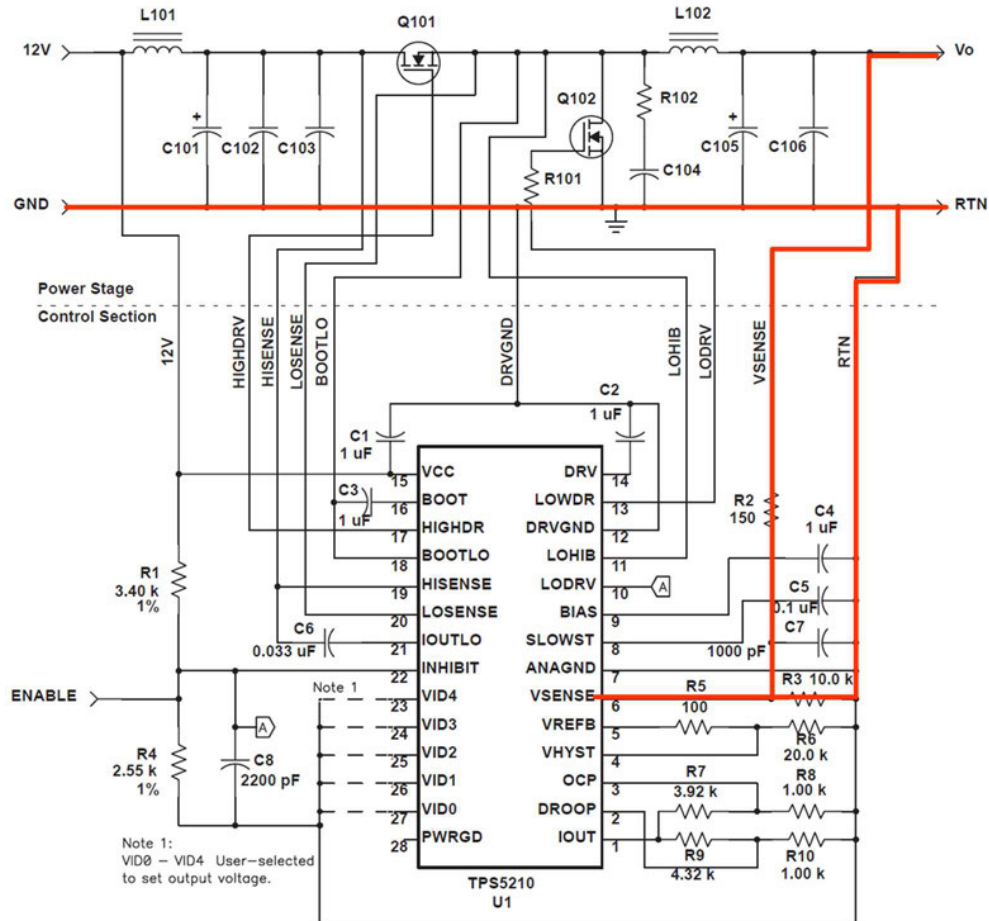Petition for *Inter Partes* Review of
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## 4. Independent Claim 15

### a. Elements 15[pre] through 15[a.2]

634. Elements 15[pre] through 15[a.2] are identical, respectively, to

Elements 8[pre] through 8[a.2], as set forth below:

| 8[pre]  A circuit for providing a regulated voltage to a processor comprising: | 15[pre]  A circuit for providing a regulated voltage to a processor comprising: |
|---|---|
| 8[a]  a voltage regulator having: | 15[a]  a voltage regulator having: |
| 8[a.1]  an output terminal providing a selectable voltage, and | 15[a.1]  an output terminal providing a selectable voltage, and |
| 8[a.2]  an input terminal for receiving signals indicating the selectable voltage level; | 15[a.2]  an input terminal for receiving signals indicating the selectable voltage level; and[12] |

635. As such, for the reasons provided under Ground 4 for Elements 8[pre]

through 8[a.2], Helms teaches Elements 15[pre] through 15[a.2].

### b. Element 15[a.3]: "a voltage regulator feedback circuit;"

636. This Element is identical to Element 13[a.3], which also recites "*a*

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[12] The different is insubstantial.

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*voltage regulator feedback circuit*." As such, for the reasons provided under this

Ground for Element 13[a.3] and under Ground 4 for Element 12[c], TI-TPS5210-

Datasheet discloses this Element.

c. **Element 15[b]**

637. Element 15[b] is substantially the same as Element 8[b.1], with the

difference therebetween underlined, as set forth below.

| 8[b.1] <u>means for providing signals at the input terminal of the voltage regulator</u> for selecting a voltage for operating the processor in a <u>computing</u> mode and a voltage of a level less than that for operating the processor in a computing mode, | 15[b] <u>circuitry coupled to said input terminal and configured to provide signals to the input terminal</u> for selecting a <u>first</u> voltage for operating the processor in a <u>first</u> mode and a <u>second</u> voltage for operating the processor in a <u>second</u> mode; |
|---|---|

638. As discussed under Ground 4 for Element 8[b.1], the "*means for*

*providing signals at the input terminal of the voltage regulator*" includes a

multiplexed VID MUX, which, a POSITA would have understood, constitutes

"<u>circuitry coupled to said input terminal and configured to provide signals to the</u>

<u>input terminal</u>."

639. As also discussed under Ground 4 for Element 8[b.1], the VID MUX

can select between OVID, "*a voltage for operating the processor in a <u>computing</u>*

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*mode,*" and SVID, "*a voltage of a level less than that for operating the processor*

*in a computing mode*" which is supplied to the processor when the processor is in

the sleep mode.  This is illustrated below.
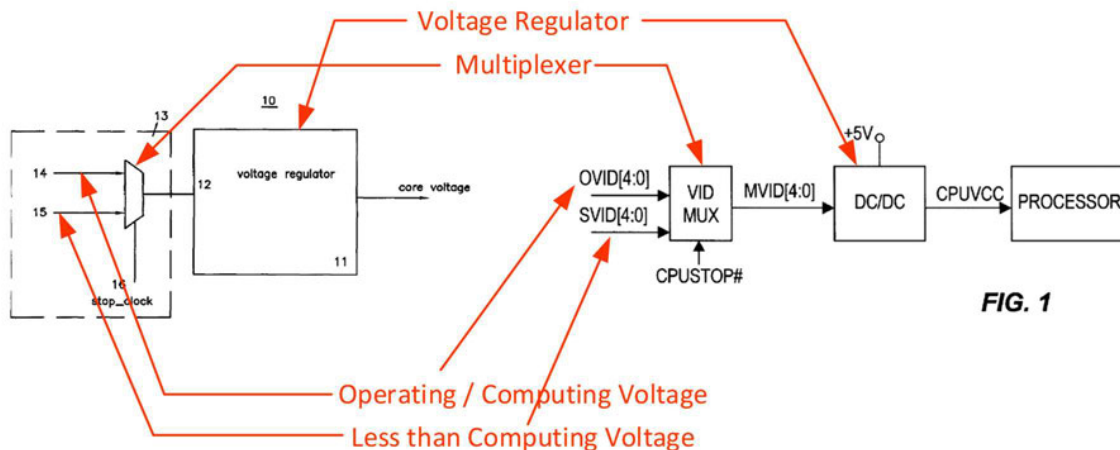


The '731 Patent, FIG. 3                          Helms, FIG. 1

(Ex.1001, FIG. 3 and Helms, FIG. 1 (annotated).)

640.   Thus, the "*computing mode*" is the "*first mode*" recited in Element

15[b] and the sleep mode is the "*second mode*" recited in Element 15[b].

641.   As such, for the reasons provided under Ground 4 for Element 8[b.1],

Helms teaches Element 15[b].

> **d.     Element 15[c]: "a voltage source furnishing a value
> higher than the selectable voltage; and**

642.   The combination of TI-TPS5210-Datasheet and Nilsson teaches a

voltage source $v_a$ providing a voltage greater than the voltage $V_{REF}$ selected using

inputs VID0-VID4 of the TPS5210 controller, where $v_a$ is "*a voltage source*

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*furnishing a value higher than the selectable voltage*.

643.   In particular, Element 13[c.1] recites in part "*a voltage source*

*furnishing a value higher than the selectable voltage*."  Therefore, for the reasons

provided under Element 13[c.1], which include reasons provided under Element

12[c], the combination of TI-TPS5210-Datasheet and Nilsson teaches this Element.

> **e.      Element 15[d]: "a feedback circuit coupled to the
> voltage source, the output terminal, and the voltage
> regulator feedback circuit."**

644.   The combination of TI-TPS5210-Datasheet and Nilsson discloses "*a*

*feedback circuit coupled to the voltage source, the output terminal, and the voltage*

*regulator feedback circuit*" because, as discussed for Element 12[c], TI-TPS5210-

Datasheet discloses a resistor-voltage-divider (*a feedback circuit*) and Nilsson

discloses a voltage source $v_a$.  Moreover, the resistor-voltage-divider is coupled

between the voltage source $v_a$ (*voltage source*) and the output terminal of the

TPS5210 controller supplying the regulated voltage $V_O$ (*output terminal*), and is

also coupled to the pin VSENSE to provide the voltage signal VSENSE to the

feedback circuit of the TPS5210 controller (*voltage regulator feedback circuit*).

645.   In particular, as discussed for Element 12[c], TI-TPS5210-Datasheet

discloses a resistor-voltage-divider having the resistors R2 and R3 provides a

signal VSENSE at the VSENSE pin of the TPS5210 controller (*voltage regulator*).

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The resistor-voltage-divider is coupled to the output $V_O$ of the TPS5210 controller.

(*See* Ex.1008 at 19, Figure 18.) As such, per Ohm's law, the voltage signal

VSENSE is a fraction of the output voltage $V_O$ given by: $VSENSE = V_O \left( \frac{R3}{R2+R3} \right)$.



Figure 18. Standard Application Schematic

(*Id.* at 19 (Figure 18 (annotated)).)

646. Since VSENSE is derived from $V_O$ and, as discussed under Ground 4

for Element 12[c], VSENSE controls $V_O$, the circuitry that generate VSENSE, i.e.,

the resistor-voltage-divider having the resistors R2 and R3, constitutes a "*feedback*

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*circuit*."

647. Nilsson discloses a voltage source $v_a$ coupled between one of the

resistors of a resistor-voltage-divider and ground. (*See* Ex.1013 at 200 (Figure
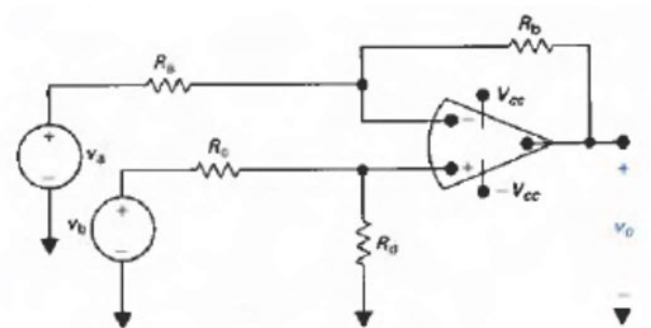
6.14).)



FIGURE 6.14 A difference amplifier.

(*Id.*)

648. As further discussed for Element 12[c], a POSITA would have

understood that the resistor-voltage-divider of the TPS5210 controller can be

readily modified as Nilsson discloses, so that the output voltage can finely tuned

by **either raising or lowering** it relative to a selected reference voltage. As shown

below, in the resistor-voltage-divider of the TPS5210 controller so modified, **the**

**resistor-voltage-divider (*feedback circuit*) is coupled between the output**

**voltage pin V$_O$ (*output terminal*) and a voltage source $v_a$ (*voltage source*)**, as

Nilsson discloses.

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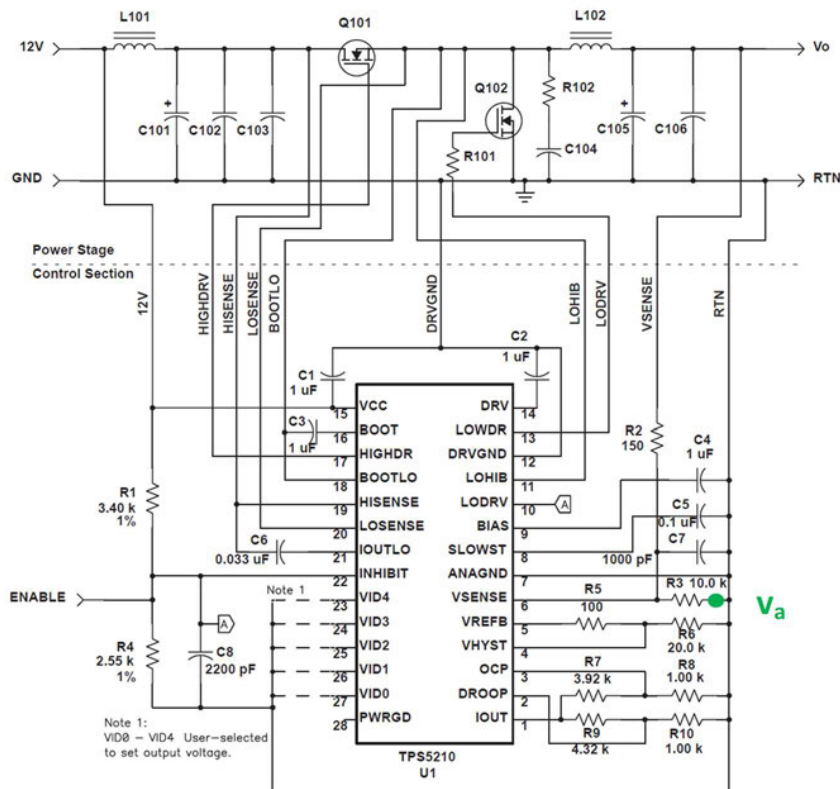U.S. Patent No. 7,260,731



Figure 18. Standard Application Schematic

(Ex.1008 at 19 (Figure 18 (modified)).)

649.  Additionally, as discussed for Element 12[c], the VSENSE pin, the

internal circuitry coupled to the VSENSE pin, and the external circuitry driven by

the signals HIGHDR and LOWDR, together, constitute feedback circuitry for the

TPS5210 regulator controller (the "*voltage regulator feedback circuit*").  Since the

resistor-voltage-divider provides the signal VSENSE, the resistor-voltage-divider

(*feedback circuit*) is coupled via the VSENSE pin to the feedback circuitry for the

TPS5210 regulator controller (the *voltage regulator feedback circuit*), as well, as

depicted in Figure 18 above.

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650. As such, the combination of TI-TPS5210-Datasheet and Nilsson

discloses this Element.

651. In summary, Helms in view of TI-TPS5210-Datasheet, further in view

of Nilsson, teaches each and every element of claim 15 and renders it unpatentable,

as obvious.

### 5. Claim 16

652. Claim 16 depends from claim 15, and further recites: "***wherein the

first voltage is for operating the processor in a computing mode and the second

voltage is a level less than that for operating the processor in the computing

mode.***"

653. Helms teaches these claim limitations because, as discussed under

Ground 4 for Element 8[b.1], Helms teaches a multiplexor VID MUX (*circuitry*,

recited in Element 15[b]) that may provide a voltage specified by OVID or SVID

to the voltage regulator. As discussed for Element 8[b], the voltage specified by

OVID is the "*first voltage*" and, as discussed under Ground 4 for Element 8[b.1],

the voltage specified by OVID is "*a voltage for operating the processor in a

computing mode.*"

654. Moreover, as discussed for Element 8[b], the voltage specified by

SVID is the "*second voltage*" and, as discussed under Ground 4 for Element

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8[b.1], the voltage specified by SVID is sleep voltage or a voltage at "*a level less than that for operating the processor in the computing mode*."

655.   Thus, Helms teaches the limitations that claim 16 recites.

### 6.   Claims 17 and 18

656.   Claim 17 depends from claim 16 (which depends from claim 15), and claim 18 depends from claim 15, and both claims 17 and 18 further recite:

"***wherein the feedback circuit comprises a voltage divider.***"

657.   TI-TPS5210-Datasheet discloses this limitation.  As discussed under this Ground for Element 15[d], and under Ground 4 for Element 12[c], TI-TPS5210-Datasheet discloses a resistor-voltage-divider having resistors R2 and R3 as a "*feedback circuit*" that derives a voltage signal VSENSE from the output voltage $V_O$.  As discussed under this Ground for Element 13[c.1], the resistor-voltage-divider is a *voltage divider*.  Thus, Helms discloses the limitation recited in claims 17 and 18.

658.   In summary, Helms in view of TI-TPS5210-Datasheet, further in view of Nilsson, teaches each and every element of each of claims 15-18 and renders these claims unpatentable, as obvious.

## VII.   NO SECONDARY CONSIDERATIONS OF NON-OBVIOUSNESS

659.   I understand from counsel that the Patent Owner in the underlying

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district court litigation has not yet identified any evidence with respect to

secondary considerations of non-obviousness.

660.   To the extent the Patent Owner cites any evidence of sales or any

praise or any industry recognition of products that the Patent Owner asserts to

implement the claimed invention, I am not aware of any information demonstrating

that any purported increased sales, commercial success, praise, or any other

secondary factor (that the Patent Owner may assert) was a result of *the particular*

*features recited in the '731 patent's claims*.   Since the Patent Owner has not yet

identified any evidence of secondary considerations, the Patent Owner cannot

demonstrate that the limitations of the claimed invention in particular, as opposed

to other features of the products at issue, were the factors that caused any increased

sales, praise, or any other asserted secondary considerations.

661.   Thus, based on my review of the evidence to date, I can summarize

my opinions regarding any alleged secondary considerations of non-obviousness

relating to the '731 patent, as follows:

662.   *No commercial success of the claimed invention*.   The Patent Owner

has not cited any evidence of particular commercial success of products

embodying the '731 patent as opposed to products that do not embody the '731

patent.   The Patent Owner has not cited any evidence that any commercial success

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of any products is particularly a result of the claimed inventions recited in the '731

patent's claims and not due to any other facts.

663.    *No long-felt but unsolved need*.  The Patent Owner has not cited any

evidence of any long-felt need that remained unsolved in the prior art before the

'731 patent.  To the contrary, as discussed above, the prior art solved the problems

that the '731 patent purported to address.

664.    *No failure of others*.  The Patent Owner has not cited any evidence of

anyone who tried, but failed, to solve the problems addressed by the '731 patent.

As shown by my analysis above, there existed prior art references that successfully

disclosed and rendered obvious the subject matter claimed by the '731 patent.

665.    *No copying of the claimed invention*.  The Patent Owner has not cited

any evidence that any other party (including Facebook or third parties) ever copied

from the '731 patent and its claimed invention.

666.    *No unexpected results of the claimed invention*.  The Patent Owner

has not cited any evidence of unexpected results achieved by the '731 patent's

claimed invention.  To the contrary, the prior art disclosed the predictable,

expected results that show why the '731 patent's claims are obvious as discussed in

my Declaration.

667.    *No praise for the claimed invention*.  The Patent Owner has not cited

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any evidence of praise for the claimed invention recited in the '731 patent.

668.  *No surprise or skepticism at the claimed invention*.  The Patent Owner has not cited any evidence that observers were surprised by, or skeptical of, the claimed invention recited in the '731 patent.

669.  *No departure from the wisdom of the prior art*.  The Patent Owner has not cited any evidence that the claimed inventions of the '731 patent departed from the wisdom of the prior art.  The '731 patent claims subject matter that was already present in the prior art, including in the references discussed in my analysis above.

670.  Moreover, with respect to the considerations discussed above, I also refer to and incorporate my opinions stated throughout this Declaration, including my analysis showing that the '731 patent is directed to techniques known in the prior art and does not provide any inventive technology.

671.  To the extent the Patent Owner at a later date cites or provides any other evidence regarding secondary considerations, including any expert opinions, I reserve the right to supplement my analysis and opinions to comment on it.

## VIII.  CONCLUSION

672.  In my opinion, based on my review of the '731 patent, the materials referenced herein, and my knowledge of what a POSITA would have known at and before the '731 patent's priority date about the technology at issue, a POSITA

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would have understood all of the claim elements and limitations of challenged

claims 1-18 to be present and described in the references cited under Grounds 1-6.

Accordingly, it is my opinion that challenged claims 1-18 should be found
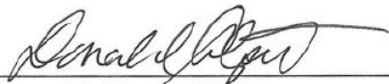
unpatentable.

673.   I reserve the right to supplement my opinions in the future to respond

to any arguments or positions that the Patent Owner may raise, taking account of

new information as it becomes available to me.

674.   I hereby declare that all statements made herein of my own

knowledge are true and that all statements made on information and belief are

believed to be true; and further that these statements were made with the

knowledge that willful false statements and the like so made are punishable by fine

or imprisonment, or both, under Section 1001 of Title 18 of the United States

Code.

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Respectfully submitted,

Dated: September 13, 2021

_____
Donald Alpert, Ph.D.