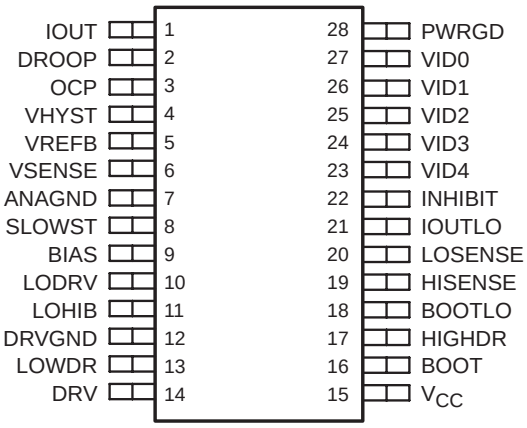
SLVS171A − SEPTEMBER 1998 − REVISED MAY 1999

- ±1% Reference Over Full Operating Temperature Range
- Synchronous Rectifier Driver for Greater Than 90% Efficiency
- Programmable Reference Voltage Range of 1.3 V to 3.5 V
- User−Selectable Hysteretic Type Control
- Droop Compensation for Improved Load Transient Regulation
- Adjustable Overcurrent Protection
- Programmable Softstart
- Overvoltage Protection
- Active Deadtime Control
- Power Good Output
- Internal Bootstrap Schottky Diode
- Low Supply Current . . . 3-mA Typ

DW OR PWP PACKAGE
(TOP VIEW)



description

The TPS5210 is a synchronous-buck regulator controller which provides an accurate, programmable supply voltage to microprocessors. An internal 5-bit DAC is used to program the reference voltage to within a range of 1.3 V to 3.5 V. The output voltage can be set to be equal to the reference voltage or to some multiple of the reference voltage. A hysteretic controller with user-selectable hysteresis and programmable droop compensation is used to dramatically reduce overshoot and undershoot caused by load transients. Propagation delay from the comparator inputs to the output drivers is less than 250 ns. Overcurrent shutdown and crossover protection for the output drivers combine to eliminate destructive faults in the output FETs. The softstart current source is proportional to the reference voltage, thereby eliminating variation of the softstart timing when changes are made to the output voltage. PWRGD monitors the output voltage and pulls the open-collector output low when the output drops 7% below the nominal output voltage. An overvoltage circuit disables the output drivers if the output voltage rises 15% above the nominal value. The inhibit pin can be used to control power sequencing. Inhibit and undervoltage lockout assures the 12-V supply voltage and system supply voltage (5 V or 3.3 V) are within proper operating limits before the controller starts. Single-supply (12 V) operation is easily accomplished using a low-current divider for the required 5-V signals. The output driver circuits include 2-A drivers with internal 8-V gate-voltage regulators. The high-side driver can be configured either as a ground-referenced driver or as a floating bootstrap driver. The TPS5210 is available in a 28-pin SOIC package and a 28-pin TSSOP PowerPAD™ package. It operates over a junction temperature range of 0°C to 125°C.

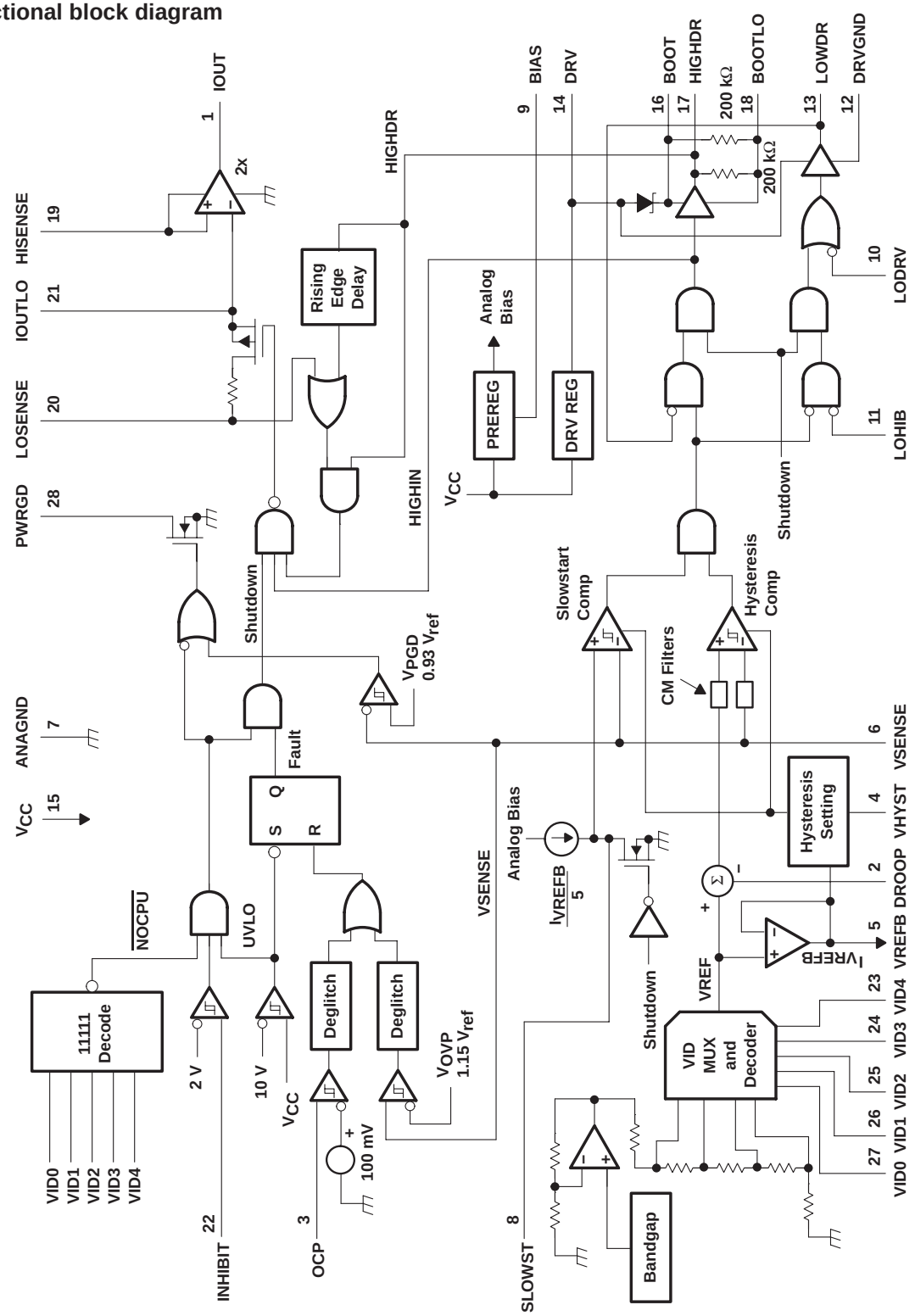
AVAILABLE OPTIONS

T_J	PACKAGES	
	SOIC (DW)	TSSOP (PWP)
0°C to 125°C	TPS5210DW	TPS5210PWPR

The DW package is available taped and reeled. Add R suffix to device type (e.g., TPS5210DWR).

Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

functional block diagram



Terminal Functions

TERMINAL NAME	TERMINAL NO.	I/O	DESCRIPTION
ANAGND	7		Analog ground
BIAS	9	O	Analog BIAS pin. A 1-μF ceramic capacitor should be connected from BIAS to ANAGND.
BOOT	16	I	Bootstrap. Connect a 1-μF low-ESR capacitor from BOOT to BOOTLO.
BOOTLO	18	O	Bootstrap low. Connect BOOTLO to the junction of the high-side and low-side FETs for floating drive configuration. Connect BOOTLO to PGND for ground reference drive configuration.
DROOP	2	I	Droop voltage. Voltage input used to set the amount of output-voltage set-point droop as a function of load current. The amount of droop compensation is set with a resistor divider between IOUT and ANAGND.
DRV	14	O	Drive regulator for the FET drivers. A 1-μF ceramic capacitor should be connected from DRV to DRVGND.
DRVGND	12		Drive ground. Ground for FET drivers. Connect to FET PWRGND.
HIGHDR	17	O	High drive. Output drive to high-side power switching FETs
HISENSE	19	I	High current sense. For current sensing across high-side FETs, connect to the drain of the high-side FETs; for optional resistor sensing scheme, connect to power supply side of current-sense resistor placed in series with high-side FET drain.
INHIBIT	22	I	Disables the drive signals to the MOSFET drivers. Can also serve as UVLO for system logic supply (either 3.3 V or 5 V).
IOUT	1	O	Current out. Output voltage on this pin is proportional to the load current as measured across the Rds(on) of the high-side FETs. The voltage on this pin equals $2 \times R_{ds(on)} \times IOUT$. In applications where very accurate current sensing is required, a sense resistor should be connected between the input supply and the drain of the high-side FETs.
IOUTLO	21	O	Current sense low output. This is the voltage on the LOSENSE pin when the high-side FETs are on. A ceramic capacitor should be connected from IOUTLO to HISENSE to hold the sensed voltage while the high-side FETs are off. Capacitance range should be between 0.033 μF and 0.1 μF.
LODRV	10	I	Low drive enable. Normally tied to 5 V. To activate the low-side FETs as a crowbar, pull LODRV low.
LOHIB	11	I	Low side inhibit. Connect to the junction of the high and low side FETs to control the anti-cross-conduction and eliminate shoot-through current. Disabled when configured in crowbar mode.
LOSENSE	20	I	Low current sense. For current sensing across high-side FETs, connect to the source of the high-side FETs; for optional resistor sensing scheme, connect to high-side FET drain side of current-sense resistor placed in series with high-side FET drain.
LOWDR	13	O	Low drive. Output drive to synchronous rectifier FETs
OCP	3	I	Over current protection. Current limit trip point is set with a resistor divider between IOUT and ANAGND.
PWRGD	28	O	Power good. Power Good signal goes high when output voltage is within 7% of voltage set by VID pins. Open-drain output.
SLOWST	8	O	Slow Start (soft start). A capacitor from SLOWST to ANAGND sets the slowstart time. Slowstart current = $I_{VREFB}/5$
V_{CC}	15		12-V supply. A 1-μF ceramic capacitor should be connected from V_{CC} to DRVGND.
VHYST	4	I	HYSTERESIS set pin. The hysteresis is set with a resistor divider from V_{REFB} to ANAGND. The hysteresis window = $2 \times (V_{REFB} - V_{HYST})$
VID0	27	I	Voltage Identification input 0
VID1	26	I	Voltage Identification input 1
VID2	25	I	Voltage Identification input 2
VID3	24	I	Voltage Identification input 3
VID4	23	I	Voltage Identification input 4. Digital inputs that set the output voltage of the converter. The code pattern for setting the output voltage is located in Table 1. Internally pulled up to 5 V with a resistor divider biased from V_{CC}.
VREFB	5	O	Buffered reference voltage from VID network
VSENSE	6	I	Voltage sense Input. To be connected to converter output voltage bus to sense and control output voltage. It is recommended an RC low pass filter be connected at this pin to filter noise.

detailed description

V_{REF}

The reference/voltage identification (VID) section consists of a temperature-compensated bandgap reference and a 5-bit voltage selection network. The 5 VID terminals are inputs to the VID selection network and are TTL-compatible inputs internally pulled up to 5 V by a resistor divider connected to V_{CC}. The VID codes conform to the Intel *VRM 8.3 DC-DC Converter Specification* for voltage settings between 1.8 V and 3.5 V, and they are decremented by 50 mV, down to 1.3 V, for the lower VID settings. Voltages higher than V_{REF} can be implemented using an external divider. Refer to Table 1 for the VID code settings. The output voltage of the VID network, V_{REF}, is within ±1% of the nominal setting over the VID range of 1.3 V to *2*.5 V, including a junction temperature range of 5°C to +125°C, and a V_{CC} supply voltage range of 11.4 V to 12.6 V. The output of the reference/VID network is indirectly brought out through a buffer to the V_{REFB} pin. The voltage on this pin will be within 2% of V_{REF}. It is not recommended to drive loads with V_{REFB}, other than setting the hysteresis of the hysteretic comparator, because the current drawn from V_{REFB} sets the charging current for the slowstart capacitor. Refer to the slowstart section for additional information.

hysteretic comparator

The hysteretic comparator regulates the output voltage of the synchronous-buck converter. The hysteresis is set by 2 external resistors and is centered on V_{REF}. The 2 external resistors form a resistor divider from V_{REFB} to ANAGND, with the output voltage connecting to the V_{HYST} pin. The hysteresis of the comparator will be equal to twice the voltage *difference* between the V_{REFB} and V_{HYST} pins. The propagation delay from the comparator inputs to the driver outputs is 250 ns (maximum). The maximum hysteresis setting is 60 mV.

low-side driver

The low-side driver is designed to drive low-Rds(on) n-channel MOSFETs. The current rating of the driver is 2 A, source and sink. The bias to the low-side driver is internally connected to the DRV regulator.

high-side driver

The high-side driver is designed to drive low-Rds(on) n-channel MOSFETs. The current rating of the driver is 2 A, source and sink. The high-side driver can be configured either as a ground-referenced driver or as a floating bootstrap driver. When configured as a floating driver, the bias voltage to the driver is developed from the DRV regulator. The internal bootstrap diode, connected between the DRV and BOOT pins, is a Schottky for improved drive efficiency. The maximum voltage that can be applied between BOOT and DRVGND is 30 V. The driver can be referenced to ground by connecting BOOTLO to DRVGND, and connecting BOOT to either DRV or V_{CC}.

deadtime control

Deadtime control prevents shoot-through current from flowing through the main power FETs during switching transitions by actively controlling the turn-on times of the MOSFET drivers. The high-side driver is not allowed to turn on until the gate-drive voltage to the low-side FETs is below 2 V; the low-side driver is not allowed to turn on until the voltage at the junction of the high-side and low-side FETs (Vphase) is below 2 V.

current sensing

Current sensing is achieved by sampling and holding the voltage across the high-side power FETs while the high-side FETs are on. The sampling network consists of an internal 60-Ω switch and an external ceramic hold capacitor. Recommended value of the hold capacitor is between 0.033 µF and 0.1 µF. Internal logic controls the turn-on and turn-off of the sample/hold switch such that the switch does not turn on until the Vphase voltage transitions high, and the switch turns off when the input to the high-side driver goes low. The sampling will occur only when the high-side FETs are conducting current. The voltage on the IOUT pin equals 2 times the sensed high-side voltage. In applications where a higher accuracy in current sensing is required, a sense resistor can be placed in series with the high-side FETs, and the voltage across the sense resistor can be sampled by the current sensing circuit.

detailed description (continued)

droop compensation

The droop compensation network reduces the load transient overshoot/undershoot on V_O, relative to V_{REF}. V_O is programmed to a voltage greater than V_{REF} by an external resistor divider from V_O to VSENSE to reduce the undershoot on V_O during a low-to-high load transient. The overshoot during a high-to-low load transient is reduced by subtracting the voltage on DROOP from V_{REF}. The voltage on IOUT is divided with an external resistor divider, and connected to DROOP.

inhibit

INHIBIT is a TTL-compatible digital input used to enable the controller. When INHIBIT is low, the output drivers are low and the slowstart capacitor is discharged. When INHIBIT goes high, the short across the slowstart capacitor is released and normal converter operation begins. When the system-logic supply is connected to INHIBIT, it also controls power sequencing by locking out controller operation until the system-logic supply exceeds the input threshold voltage of the inhibit circuit. The 12-V supply and the system logic supply (either 5 V or 3.3 V) must be above UVLO thresholds before the controller is allowed to start up. The start threshold is 2.1 V and the hysteresis is 100 mV for the INHIBIT comparator.

V_{CC} undervoltage lockout (UVLO)

The undervoltage lockout circuit disables the controller while the V_{CC} supply is below the 10-V start threshold during power up. When the controller is disabled, the output drivers will be low and the slowstart capacitor is discharged. When V_{CC} exceeds the start threshold, the short across the slowstart capacitor is released and normal converter operation begins. There is a 2-V hysteresis in the undervoltage lockout circuit for noise immunity.

slowstart

The slowstart circuit controls the rate at which V_O powers up. A capacitor is connected between SLOWST and ANAGND and is charged by an internal current source. The current source is proportional to the reference voltage, so that the charging rate of C_{slowst} is proportional to the reference voltage. By making the charging current proportional to V_{REF}, the power-up time for V_O will be independent of V_{REF}. Thus, C_{SLOWST} can remain the same value for all VID settings. The slowstart charging current is determined by the following equation:

$$I_{slowstart} = I(V_{REFB}) / 5 \quad \text{(amps)}$$

Where $I(V_{REFB})$ is the current flowing out of V_{REFB}.

It is recommended that no additional loads be connected to V_{REFB}, other than the resistor divider for setting the hysteresis voltage. The maximum current that can be sourced by the V_{REFB} circuit is 500 µA. The equation for setting the slowstart time is:

$$t_{SLOWST} = 5 \times C_{SLOWST} \times R_{VREFB} \quad \text{(seconds)}$$

Where R_{VREFB} is the total external resistance from V_{REFB} to ANAGND.

power good

The power-good circuit monitors for an undervoltage condition on V_O. If V_O is 7% below V_{REF}, then the PWRGD pin is pulled low. PWRGD is an open-drain output.

overvoltage protection

The overvoltage protection (OVP) circuit monitors V_O for an overvoltage condition. If V_O is 15% above V_{REF}, then a fault latch is set and both output drivers are turned off. The latch will remain set until V_{CC} goes below the undervoltage lockout value. A 3-µs deglitch timer is included for noise immunity. Refer to the LODRV section for information on how to protect the microprocessor against overvoltages due to a shorted fault across the high-side power FET.

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