



[54] **APPARATUS AND METHOD FOR PREVENTING THEFT OF COMPUTER DEVICES**

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 Attorney, Agent, or Firm—Pollock, Vande Sande & Amernick

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 [51] Int. Cl.⁶ **G06F 7/00**
 [52] U.S. Cl. **395/188.01; 395/652**
 [58] Field of Search 395/186, 188.01, 395/187.01, 183.12, 652; 380/3, 4, 23, 25

[57] **ABSTRACT**

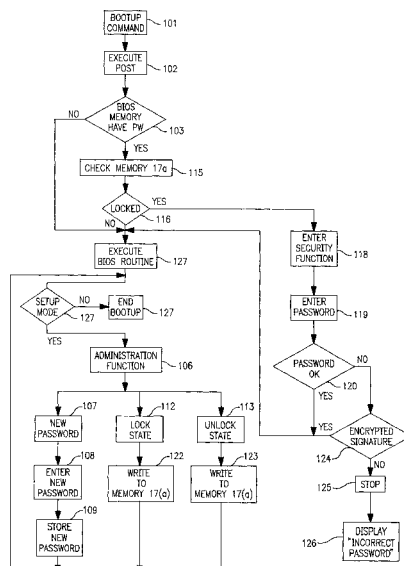
Apparatus and method for discouraging computer theft. The apparatus and method requires that a password or other unique information be supplied to the computer before the computer BIOS routines can be completely executed. A BIOS memory storing the BIOS routines includes a security routine which will determine whether or not the required password entered by the user, or a known quantity read from an externally connected memory device is present. The security function stored within the BIOS memory also includes an administration function which permits the computer to be either placed in a locked state, thereby requiring password or the known quantity read from an externally connected memory device to be present each time the computer is booted up. The administration function also permits an unlock state which permits the computer boot up process to complete without entering any password or externally supplied quantity. The external memory location is consulted during each boot up sequence, to determine whether the computer has been placed in the locked or in the unlocked state. If the security depends upon the supply of the known quantity from an externally connected memory device, the computer will be inoperable to anyone not in possession of the external memory device. In the event that the external memory location bearing the locked or unlocked code is removed, the security function assumes the computer to be in the locked state, thus frustrating avoidance of the locked state by tampering with the external memory.

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16 Claims, 5 Drawing Sheets



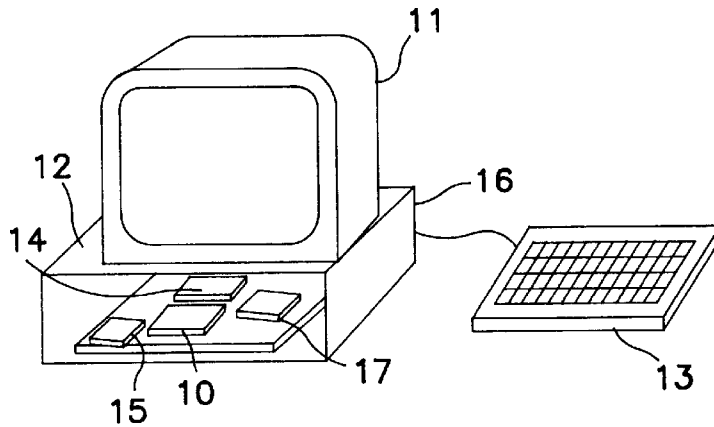


FIG. 1

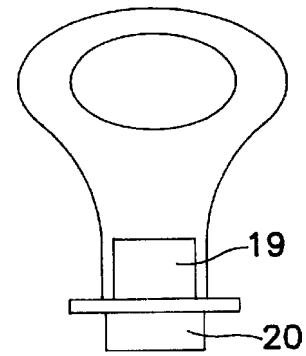
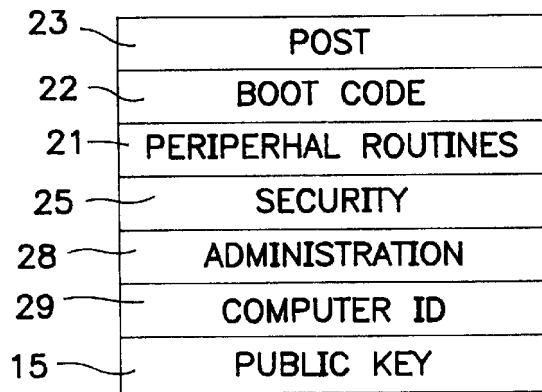
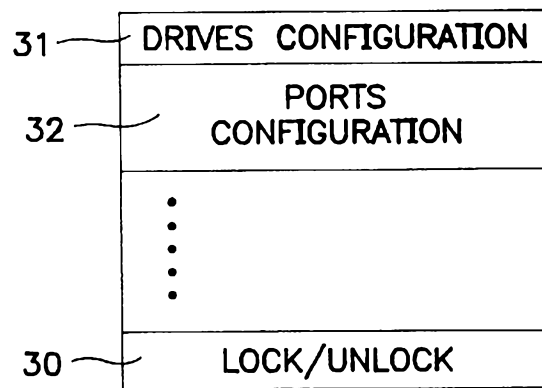


FIG. 2



BIOS
MEMORY

FIG. 3



CMOS RAM

FIG. 4

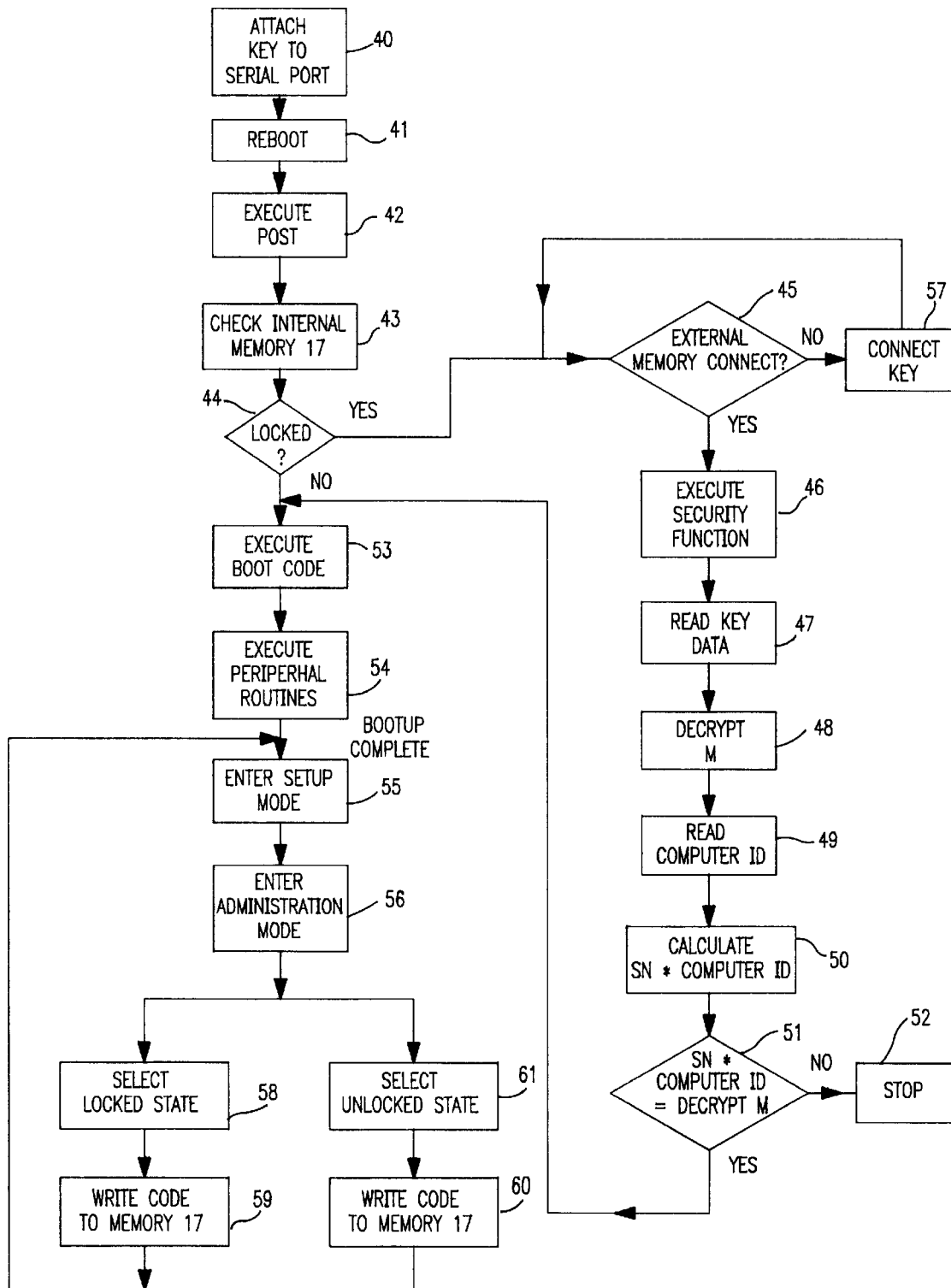


FIG. 5

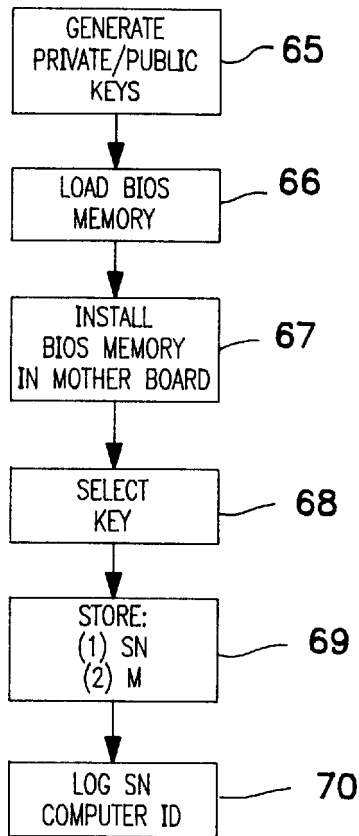


FIG. 6

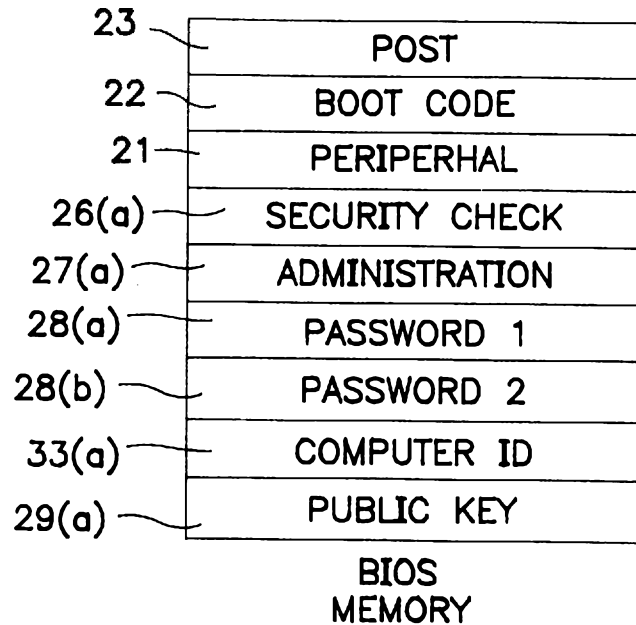
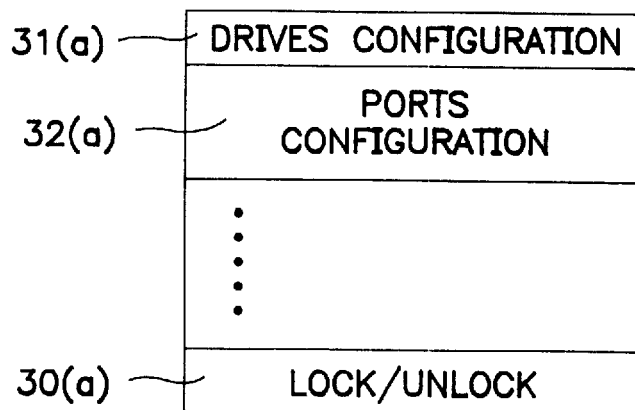


FIG. 7



CMOS RAM

FIG. 8

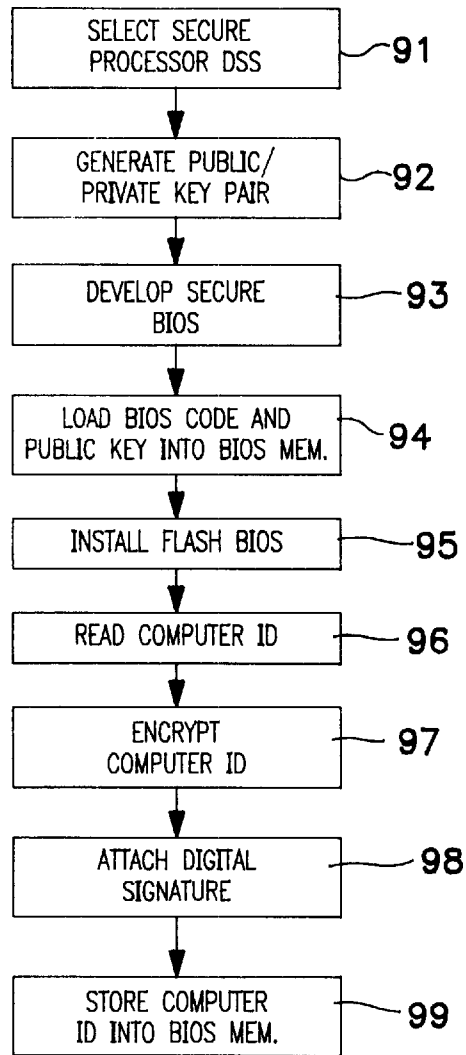


FIG. 9

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