10-Bit, 105 MSPS/125 MSPS/150 MSPS, 1.8 V Dual Analog-to-Digital Converter

AD9600

FEATURES

SNR = 60.6 dBc (61.6 dBFS) to 70 MHz at 150 MSPS
SFDR = 81 dBc to 70 MHz at 150 MSPS
Low power: 825 mW at 150 MSPS
1.8 V analog supply operation
1.8 V to 3.3 V CMOS output supply or 1.8 V LVDS supply
Integer 1 to 8 input clock divider
Intermediate frequency (IF) sampling frequencies up to 450 MHz
Internal analog-to-digital converter (ADC) voltage reference
Integrated ADC sample-and-hold inputs
Flexible analog input: 1 V p-p to 2 V p-p range
Differential analog inputs with 650 MHz bandwidth
ADC clock duty cycle stabilizer
95 dB channel isolation/crosstalk
Serial port control
User-configurable built-in self-test (BIST) capability
Energy-saving power-down modes
Integrated receive features
- **Fast detect/threshold bits**
- **Composite signal monitor**

APPLICATIONS

Point-to-point radio receivers (GPSK, QAM)
Diversity radio systems
I/Q demodulation systems
Smart antenna systems
Digital predistortion
General-purpose software radios
Broadband data applications
Data acquisition
Nondestructive testing

PRODUCT HIGHLIGHTS

1. Integrated dual, 10-bit, 150 MSPS/125 MSPS/105 MSPS ADC.
2. Fast overrange detect and signal monitor with serial output.
3. Signal monitor block with dedicated serial output mode.
4. Proprietary differential input maintains excellent SNR performance for input frequencies up to 450 MHz.
5. The AD9600 operates from a single 1.8 V supply and features a separate digital output driver supply to accommodate 1.8 V to 3.3 V logic families.
6. A standard serial port interface supports various product features and functions, such as data formatting (offset binary, twos complement, or gray coding), enabling the clock DCS, power-down mode, and voltage reference mode.
7. The AD9600 is pin compatible with the AD9627-11, AD9627, and AD9640, allowing a simple migration from 10 bits to 11 bits, 12 bits, or 14 bits.

FUNCTIONAL BLOCK DIAGRAM

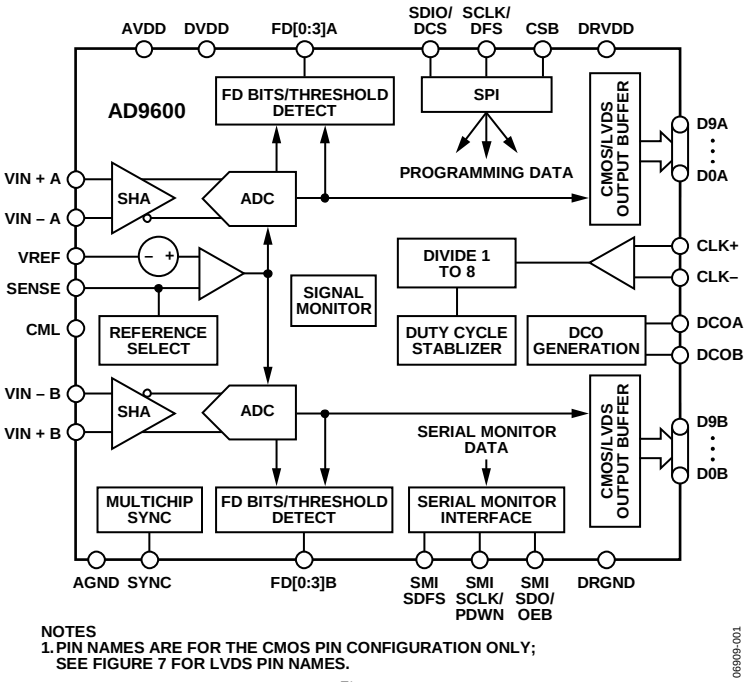

Figure 1.

Rev. B

TABLE OF CONTENTS

REVISION HISTORY

12/09—Rev. A to Rev. B

Added new models to Specifications Section 5
Changes to Table 7 12
Updated Outline Dimensions 71
Changes to Ordering Guide 72

6/09—Rev. 0 to Rev. A

Changes to Specifications Section 4
Changes to Figure 3 10
Changes to Figure 11, Figure 12, and Figure 14 16
Changes to Table 12 28
Changes to Configuration Using the SPI Section 37
Changes to Table 22 40
Changes to Signal Monitor Period (Register 0x113 to Register 0x115) Section 45
Added Exposed Pad Notation to Outline Dimensions 70

11/07—Revision 0: Initial Version

GENERAL DESCRIPTION

The AD9600 is a dual, 10-bit, 105 MSPS/125 MSPS/150 MSPS ADC. It is designed to support communications applications where low cost, small size, and versatility are desired.

The dual ADC core features a multistage, differential pipelined architecture with integrated output error correction logic. Each ADC features wide bandwidth, differential sample-and-hold analog input amplifiers supporting a variety of user-selectable input ranges. An integrated voltage reference eases design considerations. A duty cycle stabilizer is provided to compensate for variations in the ADC clock duty cycle, allowing the converters to maintain excellent performance.

The AD9600 has several functions that simplify the automated gain control (AGC) function in a communications receiver. For example, the fast detect feature allows fast overrange detection by outputting four bits of input level information with very short latency.

In addition, the programmable threshold detector allows monitoring the amplitude of the incoming signal with short latency, using the four fast detect bits of the ADC. If the input signal level exceeds the programmable threshold, the fine upper threshold indicator goes high. Because this threshold is set from the four MSBs, the user can quickly adjust the system gain to avoid an overrange condition.

Another AGC-related function of the AD9600 is the signal monitor. This block allows the user to monitor the composite magnitude of the incoming signal, which aids in setting the gain to optimize the dynamic range of the overall system.

The ADC output data can be routed directly to the two external 10-bit output ports. These outputs can be set from 1.8 V to 3.3 V CMOS or 1.8 V LVDS. In addition, flexible power-down options allow significant power savings.

SPECIFICATIONS

DC SPECIFICATIONS

AVDD = 1.8 V, DVDD = 1.8 V, DRVDD = 3.3 V, maximum sample rate, VIN = −1.0 dBFS differential input, 1.0 V internal reference, DCS enabled, fast detect output pins disabled, signal monitor disabled, unless otherwise noted.

Table 1.

		AD9600ABCPZ-105/ AD9600BCPZ-105			AD9600ABCPZ-125/ AD9600BCPZ-125			AD9600ABCPZ-150/ AD9600BCPZ-150			
Parameter	**Temp**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Unit**
RESOLUTION	Full	10			10			10			Bits
ACCURACY											
No Missing Codes	Full		Guaranteed			Guaranteed			Guaranteed		
Offset Error	Full		±0.3	±0.7		±0.3	±0.7		±0.3	±0.7	% FSR
Gain Error	Full	−3.6	−2.2	−1.0	−4.0	−2.5	−1.3	−4.3	−3.0	−1.6	% FSR
Differential Nonlinearity (DNL)[1]	Full			±0.2			±0.2			±0.2	LSB
	25°C		±0.1			±0.1			±0.1		LSB
Integral Nonlinearity (INL)[1]	Full			±0.3			±0.3			±0.4	LSB
	25°C		±0.1			±0.1			±0.1		LSB
MATCHING CHARACTERISTICS											
Offset Error	Full		±0.3	±0.7		±0.3	±0.7		±0.2	±0.7	% FSR
Gain Error	Full		±0.2	±0.8		±0.3	±0.8		±0.2	±0.8	% FSR
TEMPERATURE DRIFT											
Offset Error	Full		±15			±15			±15		ppm/°C
Gain Error	Full		±95			±95			±95		ppm/°C
INTERNAL VOLTAGE REFERENCE											
Output Voltage Error (1 V Mode)	Full		±5	±16		±5	±16		±5	±16	mV
Load Regulation @ 1.0 mA	Full		7			7			7		mV
INPUT-REFERRED NOISE											
VREF = 1.0 V	25°C		0.1			0.1			0.1		LSB rms
ANALOG INPUT											
Input Span, VREF = 1.0 V	Full		2			2			2		V p-p
Input Capacitance[2]	Full		8			8			8		pF
VREF INPUT RESISTANCE	Full		6			6			6		kΩ
POWER SUPPLIES											
Supply Voltage											
AVDD, DVDD	Full	1.7	1.8	1.9	1.7	1.8	1.9	1.7	1.8	1.9	V
DRVDD (CMOS Mode)	Full	1.7	3.3	3.6	1.7	3.3	3.6	1.7	3.3	3.6	V
Supply Current											
I_{AVDD}[1]	Full		310			385			419		mA
I_{DVDD}[1]	Full		34			42			50		mA
I_{AVDD} and I_{DVDD}[1, 3]				365			455			495	
I_{DRVDD} (3.3 V CMOS)	Full		35			36			42		mA
I_{DRVDD} (1.8 V CMOS)	Full		15			18			22		mA
I_{DRVDD} (1.8 V LVDS)			42			44			46		mA
POWER CONSUMPTION											
DC Input	Full		600	650		750	800		825	890	mW
Sine Wave Input[1]											
DRVDD = 1.8 V	Full		645			813			892		mW
DRVDD = 3.3 V	Full		740			900			990		mW
Standby Power[3]	Full		68			77			77		mW
Power-Down Power	Full		2.5	6		2.5	6		2.5	6	mW

[1] Measured with a low input frequency, full-scale sine wave, with approximately 5 pF loading on each output bit.
[2] Input capacitance refers to the effective capacitance between one differential input pin and AGND. Refer to Figure 8 for the equivalent analog input structure.
[3] Standby power is measured with a dc input and the CLK+ and CLK– pins inactive)set to AVDD or AGND.

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