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Integrated applications of inspection data in the semiconductor manufacturing environment

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ABSTRACT

As integrated circuit fabrication processes continue to increase in complexity, it has been determined that data collection, retention, and retrieval rates will continue to increase at an alarming rate. At future technology nodes, the time required to source manufacturing problems must at least remain constant to maintain anticipated productivity as suggested in the International Technology Roadmap for Semiconductors (ITRS). Strategies and software methods for integrated yield management have been identified as critical for maintaining this productivity. Integrated yield management must use circuit design, visible defect, parametric, and functional test data to recognize process trends and excursions so that yield-detracting mechanisms can be rapidly identified and corrected. This will require the intelligent merging of the various data sources that are collected and maintained throughout the fabrication environment. The availability of multiple data sources and the evolution of automated analysis techniques are providing mechanisms to convert basic defect, parametric, and electrical data into useful prediction and control information. Oak Ridge National Laboratory and International SEMATECH have been working to develop new strategies and capabilities in integrated yield management based on technologies such as Automatic Defect Classification (ADC), Spatial Signature Analysis (SSA), and Automated Image Retrieval (AIR). In this paper we will discuss a survey of these image-based technologies and their application to the ITRS issues that are driving the need for integration and data reduction.

Keywords: semiconductor manufacturing, integrated yield management, automatic defect classification, spatial signature analysis, content-based image retrieval

1. INTRODUCTION

Semiconductor manufacturers invest billions of dollars in process equipment, and they are interested in obtaining as rapid a return on their investment as can be achieved. Rapid yield learning is thus becoming an increasingly important source of competitive advantage in the complex environment of semiconductor device fabrication. The sooner an integrated circuit device yields, the sooner the manufacturer can generate a revenue stream. Conversely, rapid identification of the source of yield loss can restore a revenue stream and prevent the destruction of material in process [1]. The 1999 International Technology Roadmap for Semiconductors (ITRS) states that: *in the face of this increased complexity, strategies and software methods for integrated yield management (IYM) have been identified as critical for maintaining productivity* [2]. Figure 1 represents this statement as a function of two critical parameters that are highlighted in the ITRS: *critical particle size*, and *defect sourcing complexity*. Critical particle size refers to the minimum size of

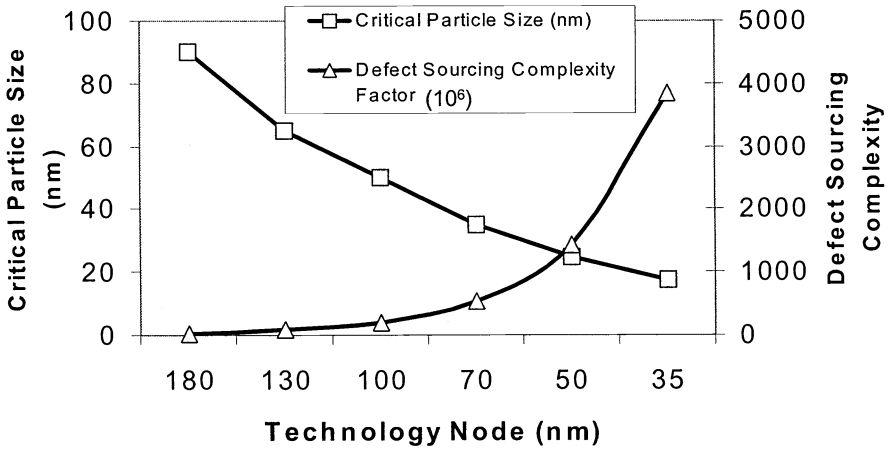

Figure 1 – Graphical representation of the "needle in the haystack" regarding the detection of small defects on complex semiconductor devices.

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particles that can cause electrical faults in an integrated circuit, whereas the complexity factor is the product of the number of transistors in a micro-processor by the number of process steps required to manufacture the device. These two parameters work against each other as manufacturers strive to meet future productivity goals in the industry. The challenge has been described as looking for a "needle in a haystack" [3].

Figure 2 demonstrates the current financial impact of the need to develop higher accuracy metrology capabilities and to reduce metrology information rapidly for the purpose of making accurate assessments and predictions of the causes of yield loss. Revenue spending for test and metrology (the bulk of which is wafer inspection) approached $10B in 2000 and is projected to increase. This corresponds to an increase in defect inspection expenditures for equipment, software, and support from around 1% of revenues in the early 1990's to over 3% in 2000. The issues driving these trends are the direct result of decreasing line widths (and therefore increased sensitivity to smaller particles), increasing device complexities, and increasing wafer dimensions.

To address these complex manufacturing issues, the Image Science and Machine Vision (ISMV) Group of the Oak Ridge National Laboratory (ORNL), and the Yield Management Tools (YMT) Program of International SEMATECH (ISMT) have been developing new technologies for automating the analysis of defects found in semiconductors. In this paper we will survey our work in this area over the past decade covering the topics of Automatic Defect Classification (ADC), Spatial Signature Analysis (SSA), Automated Image Retrieval (AIR), and the integration of these methods in the manufacturing environment, both as independent methods and in support of each other in the process of data reduction and yield learning.

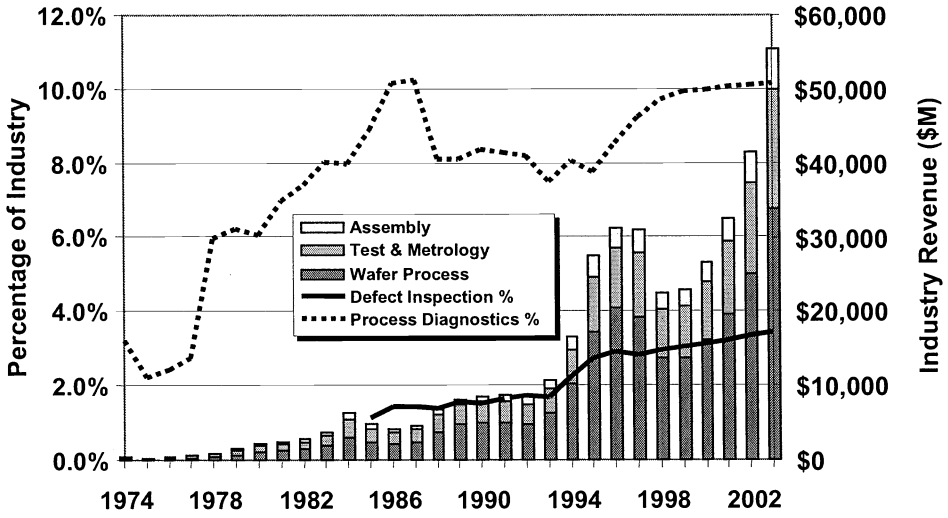

Figure 2 – Semiconductor industry expenditures of revenues for various components of manufacturing. Note the increase in spending on test and metrology and in particular, defect inspection.

2. YIELD MANAGEMENT

Semiconductor device yield can be defined as the ratio of functioning chips shipped versus the total number of chips manufactured. Yield management can be defined as the management and analysis of data and information from semiconductor process and inspection equipment for the purpose of rapid yield learning coupled with the identification and isolation of the sources of yield loss. The worldwide semiconductor market experienced chip sales of $144 billion in 1999 increasing to $234 billion in 2002 [4]. Small improvements in semiconductor device yield of tenths of a percent can save the industry hundreds of millions of dollars annually in lost products, product re-work, energy consumption, and by the reduction of waste streams.

It is in the area of yield management that ORNL and ISMT have been developing technologies that are impacting the manufacturers ability to rapidly isolate yield loss mechanisms and learn about yield issues for predictive and management purposes. Figure 3 depicts a simplified fabrication flow diagram. This diagram of production (including front-end and back-end processing), data management, and yield analysis, in Fig. 3a-d respectively, encapsulates the major components of the manufacturing environment where process and product data are generated, maintained, and accessed for yield management.

For our discussion we will focus on data that is generated from the wafer product itself, i.e., as opposed to process information such as tool condition data, temperature, pressure, etc. Figure 3a and 3b shows the process area in the fab where bare wafers enter the process, are printed and tested in-line, producing integrated circuits ready for packaging and sale. Metrology and defect data that are generated from the wafer are maintained in a variety of databases within the data

management system (DMS). Wafer defect, parametric, and electrical measurement data are typically maintained in a small group of databases (DBs) that are accessed as a virtual repository to facilitate data correlation between what is sensed on the wafer in terms of defectivity (e.g., optical or laser scanned images), parametric data (e.g., line widths and film thickness), electrical function (e.g., binmap and bitmap), and device yield. This data is accessed and analyzed by the failure analysis laboratory during off-line review and by the yield management team - i.e., engineers whose job is to improve current and future yield through yield learning and process improvement. During failure analysis, the wafer can undergo additional physical testing off-line to gain a better understanding of pattern, particle, or parametric fault mechanisms by high-resolution optical imaging, scanning electron microscopy (SEM), focused ion beam (FIB) cross-section analysis, atomic force microscopy (AFM), etc. (Fig. 3d). This image-based information augments the product-based DB therefore providing a historical record for current and future learning and yield prediction. It is the accumulation and manipulation of this in-line and off-line image data that is the basis for our work in yield management automation and the subject of the remainder of this paper. Further discussion of the semiconductor fabrication DMS architecture, function, and future needs can be found in references [5, 6].

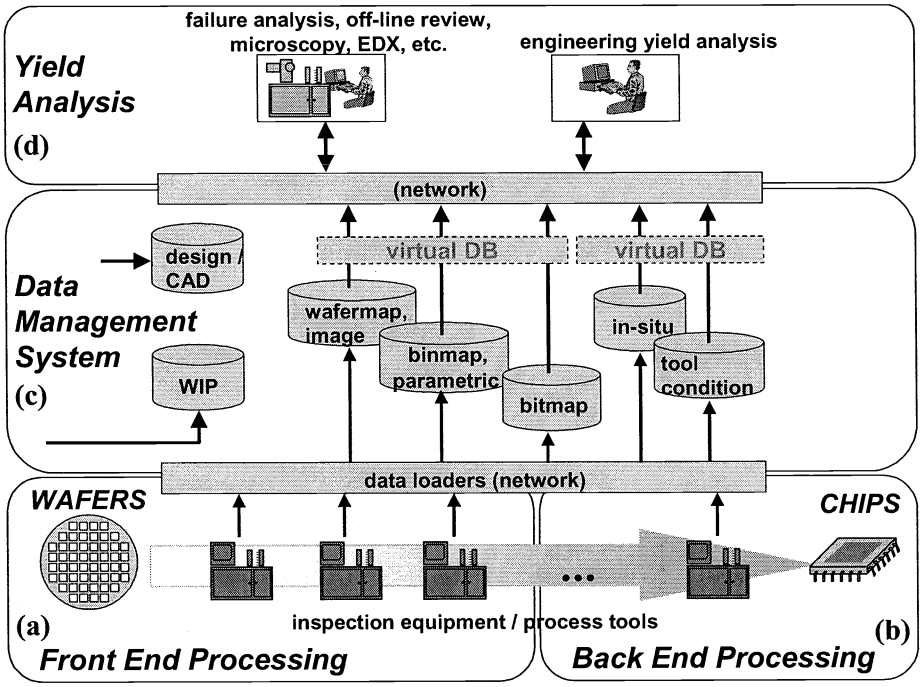

Figure 3 – Stylized representation of the three major components of the semiconductor fabrication environment: (a) and (b) front-end and back-end processing, (c) data management, and (d) yield analysis.

3. WAFER DATA ANALYSIS AUTOMATION

It has been estimated that up to 80% of yield loss in the mature production of high volume integrated circuits can be attributed to visually detectable random, process-induced defects (PIDs) such as particulates in process equipment [7, 8]. Yield learning can therefore be closely associated with the process of defect detection and reduction. In this section we will review our work in the automatic analysis of defect image data from in-line inspection and off-line review spanning the topics of ADC for individual defect classification, SSA for the classification of populations of defects, and AIR for the management of very large image repositories. Fig. 4 gives an example of the level of information reduction that is to be achieved in yield management through automation. This flow diagram is based on ITRS specifications for inspection equipment at the current technology node (i.e., 180 nm features) and

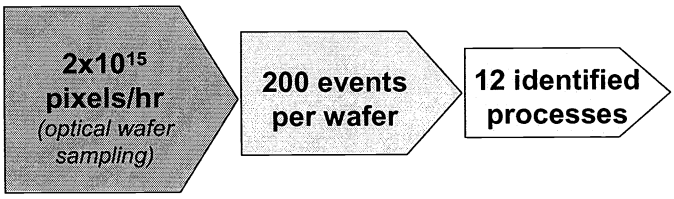

Figure 4 – Typical information reduction target based on ITRS specifications for yield learning.

200 mm diameter wafers at 150 wafers per hour per tool. In essence, the need is to reduce on the order of 10^{15} data samples per hour to around one dozen potential process sources. ADC, SSA, and AIR provide automation capabilities that support this goal.

1. Automatic Defect Classification

ADC was initially developed in the early '90s to automate the manual classification of defects during off-line optical microscopy review [9, 10, 11]. Since this time, ADC technologies have been extended to include optical in-line defect analysis and SEM off-line review [12]. For in-line ADC, a defect may be classified "on-the-fly", i.e., during the initial wafer scan of the inspection tool, or during a re-visit of the defect after the initial wafer scan, usually at higher resolution. During in-line detection the defect is segmented from the image using a die-to-die comparison or a method as shown in Fig. 5 [13, 8]. This figure shows an approach to defect detection based on a serpentine scan of the wafer using a die-to-die comparison; first showing A compared to B, B compared to C, etc., ultimately building a map of the entire wafer as shown in Fig. 5c. This electronic wafermap forms the primary data record that is maintained in the DMS and provides defect information for off-line review and spatial analysis. During off-line review the defect is re-detected using the specified electronic wafermap coordinates and die-to-die methods. The classification decision derived from the ADC process is maintained in the electronic wafermap for the wafer under test and will be used to assist in the rapid sourcing of yield impacting events and for predicting device yield through correlation with binmap and bitmap data if available.

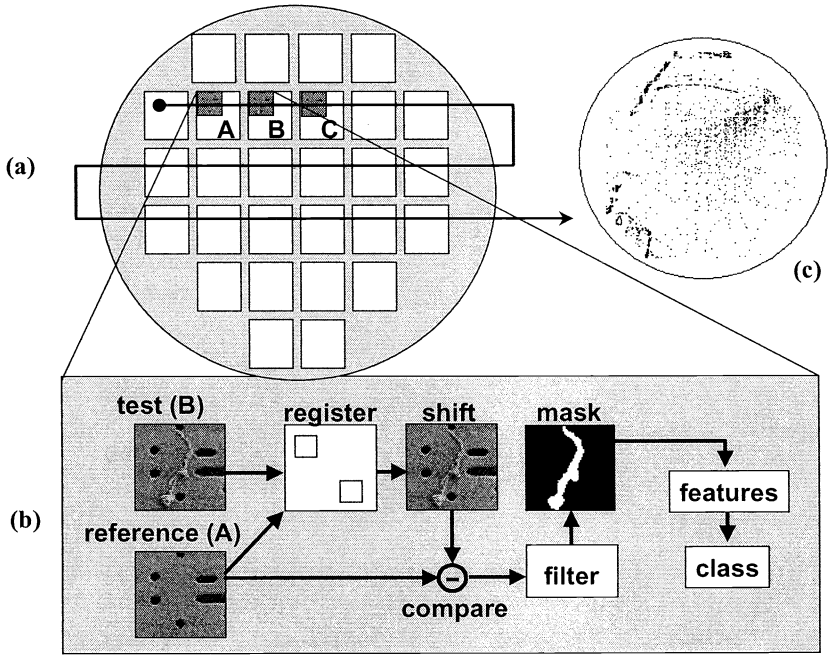

Figure 5 – Schematic representation of the typical serpentine defect scanning process in (a) resulting in the detection of defects (b), and ultimately in the generation of the wafermap in (c), an electronic record of wafer defectivity that is maintained in the DMS.

In semiconductor applications, the methods used for classifying defects vary greatly, although they are primarily feature-based. There are two broad categories of classifier in use: rule-based classifiers with a fixed number of pre-defined classes (pre-defined by the system developer), and trainable classifiers that are trained in the field by the end-user. Fixed-class systems have come into popularity for in-line applications since the resolution of these systems is generally less than off-line review microscopes. The reduced sensitivity of the in-line systems results in simple classification schemes that classify defects, for example, by size or brightness. There is no user training of a fixed-class system. The result is ease-of-use. The down side of this approach is that the system cannot easily be trained to accommodate new defect classes that are manufacturer-specific. A trainable system (e.g., based on distance-based classifiers such k-nearest neighbor or neural networks) can accommodate the wide range of defect types associated with different inspection points in the process, various process layers, or products, but can be cumbersome to train and maintain. The concept of having a classifier system that is ready to use has prompted the extension of the fixed-classifier concept to some off-line review systems but the lack of

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