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Tutorial paper

New tools for yield improvement in integrated circuit manufacturing: can they be applied to reliability?

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Abstract

This paper will start with a discussion of why probe yield (the number of good chips per silicon wafer) is so important to financial success in integrated circuit manufacturing. Actual data will be quoted and a numerical example shown. A simple model will be given to demonstrate the main factors influencing yield and the relationship between yield and reliability of the final product. In the last few years a range of new tools have been deployed in manufacturing, and these have accelerated the pace of yield improvement, thus increasing competitive pressures. These tools will be described, along with examples of their use. Topics will include in-line inspection and control, automatic defect classification and data mining techniques. A proposal is made to extend these tools to the improvement of reliability of products already in manufacturing by maintaining absolute chip identity throughout the entire wafer fabrication, packaging and final testing steps.

1. The importance of probe yields in financial success

Probe yield is obviously a very important and direct factor, and a few calculations show just how important. Fig. 1 shows a graph of capital equipment required by a company to manufacture ten million integrated circuits per year, as a function of die size and defect density. (Yield is inversely dependent on defect density.) Since the industry is generally in a growth mode, this is usually a very important question. For a die size of 200 mm^2 on a side, the difference between 50 and 150 defects per wafer comes out to $400M. The company with the highest yield will be able to plow this extra profit back into R&D and capacity expansion.

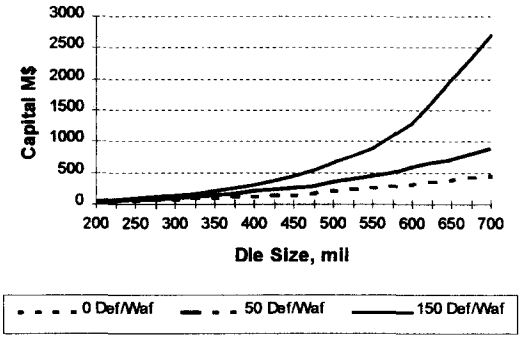

Figure 1. Capital needed for 10M units/year

Data from Leachman [1] can be used to calculate typical yields for various product types and technology generation. For example, in 1993, two different companies manufacturing 4M DRAM ran defect densities of 1.0 and 0.30 defects per cm^2, corresponding to yields of 49% and 80% respectively, which gave vastly different levels of profitability. Success in DRAM today requires yield in the mid-nineties.

Stock market analysts understand these economics very well, and generally have fairly good yield estimates especially when a few product types dominate a company's business. An example [2] from 1995 will illustrate: "We estimate that Intel's 0.6 micron line width fabs are now yielding 65% probe yield out of 154 potential die. As these yields improve over the months ahead, we believe that there is room for upside surprise to the gross margin estimate that we are projecting for Q3." In the last few years, stock prices have become more volatile, and good or bad news in yields can cause big swings in the market.

2. Yield models

A yield model, for example [3,4] is an equation, or increasingly a computer program, used to predict

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the die yield in terms of defect density, die area and other parameters. The purposes of a yield model are to:

(a) Predict the yield and therefore manufacturing cost during the design phase.

(b) Compare actual yield vs. the model, allowing product-specific problems to be identified and corrected.

(c) Determine the optimal level of integration, i.e., the number of transistors per chip.

(d) Set priorities for process improvement work.

(e) Allow extrapolations to future technologies with smaller line widths.

Designers usually want to fit the maximum number of electronic functions onto the chip, however, this will increase the die size and cost, so obviously a trade-off has to be made. Generally a new product will have a target market segment, which in turn will have a target price customers are willing to pay for the final product.

It is convenient to divide the yield loss mechanisms into three broad categories:

(a) Y_S is defined as the structural limited yield from dice that fail as a result of internal shorts or opens, due to systematic non-random failure mechanisms, which affect entire wafers or regions on the wafers.

(b) Y_E is defined as the electrical parameter limited yield, from dice that fail for out-of-tolerance electrical parameters such as threshold voltage or sheet resistance. Generally there are two categories. "Hard failures," where the circuit fails to function under any conditions because one or more internal logic levels are incorrect, and "soft failures," where the circuit does function, but fails to meet a specified product parameter, such as standby power or maximum clock frequency.

(c) Y_D is defined as the defect limited yield, from die which fail due to spot defects, such as those caused by particles. Sometimes these are erroneously referred to as "random" defects, although the types of particles found in semiconductor processing are seldom random, but clustered.

These definitions are somewhat arbitrary, since some failure mechanisms could fall under more than one category. For example, plasma etching processes can leave "residue," a dense pattern of very small point defects. In these definitions, this would be considered a structural yield loss mechanism. Structural problems generally come from limitations in the basic process technology from either poor capability, poor control or faults in the way the process steps are integrated together. This is the realm of the technologist or process integration engineer. Electrical limited yield is generally the province of the design engineer, but there are two ways to look at the problem. From the designer's standpoint, the process

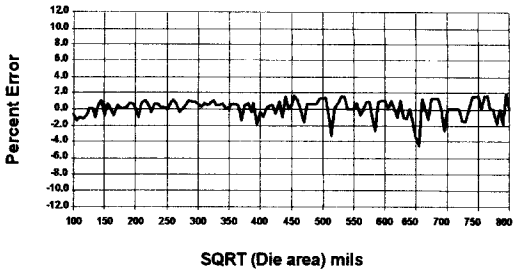

Fig. 2. Error between the actual available die and the equation

parameter distributions are fixed, and it's the designer's job to make sure the circuit functions over the full range. From the process engineer's view, the circuit is fixed but process controls need to be improved to ensure the product always has maximum yield. Defects are generally the realm of the manufacturing department and the manufacturing and process engineers that support them. Mallory et. al. [5] has some good examples of these distinctions.

3. Simple yield model

One simple yield model for the number of good dice per wafer is given by,

$$Y = NY_S Y_E Y_D$$

and

$$Y = \frac{Y_S Y_E \pi (D-2E)^2}{4A}\left[1 - \frac{0.725\sqrt{8A}}{D-2E}\right]\exp(-Ad_E)$$

Where N is the number of dice available per wafer. D is the diameter of the wafer. E is the width of an exclusion ring at the edge of the wafer where the yield is zero. A is the area of the die and d_E is an effective defect density. This calculation of the number of available die is approximate, but has been found to agree within one or two percent with the actual number counted on a range of products. See Fig. 2.

This model is based on the Poisson distribution, which is usually only a good approximation over a small range of die sizes. However, it does serve to demonstrate the strong dependence of the yield on die area and defect density. In this case d_E is not an actual defect density as you might estimate by inspection and counting, but rather an effective, "curve-fit" value that would give the predicted yield if the defects were actually random in nature. Other workers have refined the Poisson model using various distribution functions

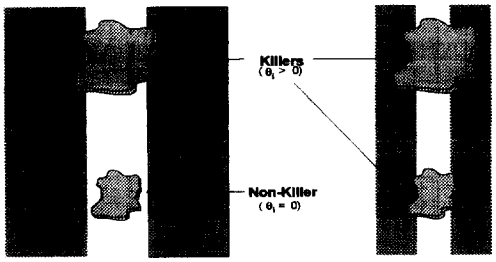

Fig. 3. The Effect of Particle Size on Yield at Different Line/Space Widths

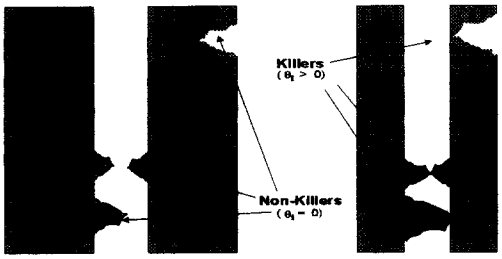

Fig. 4. The Effect of Pattern Defect Size on Yield at Different line/space widths

for the defect density, rather than a single value. For example, Stapper [4], Murphy [6] and Seeds [7].

In semiconductor manufacturing, wafers are inspected at various sample points during the process and the number of defects is counted. This actual defect density will be related to d_E as follows,

$$d_E = \theta d$$

Where d is the actual defect density and θ is the probability that a given defect will result in an actual circuit fault. The value of θ will depend on the defect size, composition (conducting or non-conducting) and permanence (is it cleaned off during processing before it can result in an electrical fault). The probability of failure is illustrated in Figs. 3 and 4.

Different types of circuitry tend to have different effective defect densities. For example, in DRAM the transistor elements form a tightly packed array with minimum feature sizes with minimum spacing. In contrast, a logic circuit will contain a greater amount of open space due to inefficiencies in close packing the "random logic." ROM and gate array devices might contain unused circuits and some defects become "non-killer" since they might cause a circuit node to become "stuck" at the logic level for which it

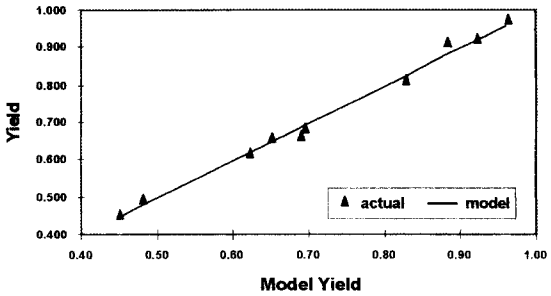

Fig. 5. Yields: actual vs. model

has already been programmed. This becomes a problem for complex microprocessors and other devices that contain more than one type of circuit. Stapper [9] proposes one way to deal with this. Alternatively, the term Ad_E can be modified as follows

$$Ad_E \rightarrow A(m_1 d_1 + m_2 d_2 + m_3 d_3 + ...)$$

Where the terms m and d represent the fractions of the chip area used by each circuit type and the corresponding effective defect density curve fit parameters. The values of m are known from the circuit design and the d values can be estimated either by regression analysis of a family of products or by comparing critical areas. (The critical area of a circuit is the area of an equivalent circuit with θ of 1.) Fig. 5 demonstrates that this relationship is a reasonable approximation in practice.

4. The relationship between yield and reliability

Small defects which locally reduce the line width or spacing, contact/via size or other feature size, but which do not cause a circuit failure on initial testing, can become "latent" defects. These can cause failures during device operation in the field. A narrow spot in a metal line can result in localized heating and electro-migration or can behave like a fuse. A location where two conductors are almost but not quite bridged, can fail in time due to leakage, dielectric wear out or breakdown. Particles left within the structure can react chemically with the circuit elements, for example, by causing corrosion of a metal line. Fig. 6 from Riordan et. al. [8] illustrates this relationship. In this paper the authors demonstrated the relationship by comparing probe yield and burn-in yield at a lot level, wafer level and location (x/y coordinates) within the wafer. Burn-in yield is known to correlate well with field failures over time. Fig. 7 shows an example for wafer level

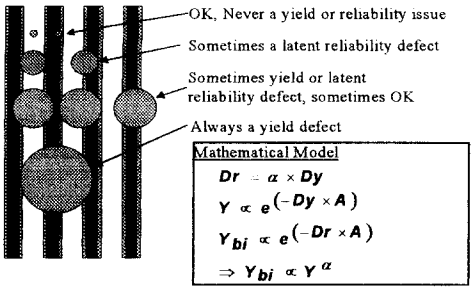

Fig 6. Model for reliability vs. yield [8]

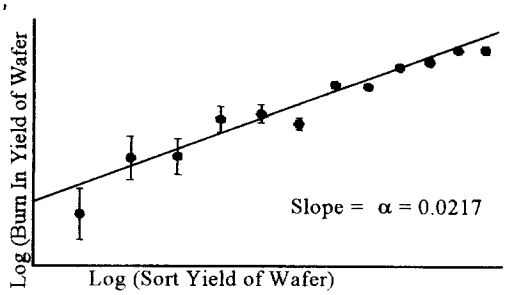

Fig 7. Reliability vs. Yield on a 1 million unit sample at the wafer level [8]

data. The burn-in yield is given by

$$Y_{bi} = kY^{\alpha}$$

$$\alpha = \frac{d_R}{d_E}$$

Where Y_{bi} is the burn-in yield, k is a constant and d_R is an effective density of defects causing burn-in failures.

5. Automated in-line defect inspection

The topic of "yield management" has recently started to be studied by academia, for example, by Nag et. al. [10]. They demonstrated that the rate of yield improvement and, therefore, overall profit is strongly tied to the ability of the wafer fab organization to quickly analyze yield loss mechanisms and take corrective or improvement action at the process step level. Obviously the closer the point of detection to the actual process step that is the source of a given defect, the more effective the yield management will be.

In recent years, automated in-line defect detection equipment has been widely deployed for product wafer inspection. There are two main types. The first basically uses polarized light scattering with very complex schemes to filter the periodicity of the circuit features and process the image data. These instruments are very good at detecting defects with topology, such as particles on the wafer surface. However, they are also able to pick up pattern type defects. The second type captures the image of an area on a die and converts it to pixels with a gray scale value applied to each. The identical area on another separate die is then imaged and compared to the first. If a difference is detected, then a defect is present.

This type of instrument is generally more sensitive, but usually slower. These tools are used for process control purposes, to detect an increase in defect density in-line, and also for improvement purposes by allowing the generation of Pareto charts of the baseline defect levels and types. Generally the key inspection points in the process are identified and sample of die on a sample of wafers measured. A sample of the defects found is then verified and classified by type. There are many technical papers published each year at several conferences. Radin [11] and Strathman and Lotz [12] are early examples. Once these tools became widely available they made a major contribution to yield improvement efforts. The equipment continues to improve in terms of speed and accuracy as better algorithms, electronics and optical techniques are developed.

6. Automated defect classification

A similar breakthrough is about to happen with "automated defect classification" (ADC). Inspection of a partially processed product wafer will reveal multiple types of defects, some freshly generated at the process step immediately preceding the inspection, but many from previous steps. Often, subsequent processing will modify the appearance of a defect. Plotting the total defect density on an SPC control chart will be useful, but an important trend for a particular defect mechanism might be missed in the overall noise, and similarly, for correlation between process conditions and total defect density. Also estimates of "kill ratio" or "probability of failure" will be estimates of the overall average of multiple defect mechanisms. The signal-to-noise ratio can be improved by reviewing the defects detected by the automated inspection, classifying them by type and applying data analysis to each type. Unfortunately this work takes great skill, is time consuming and suffers

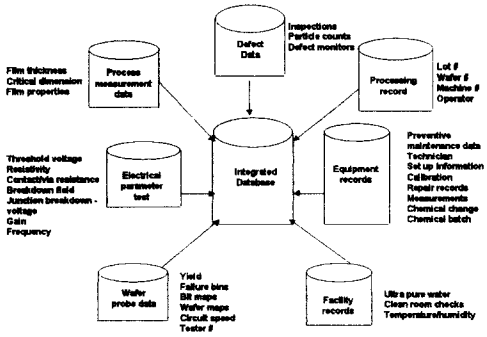

Fig. 8.Typical Wafer Fab Database

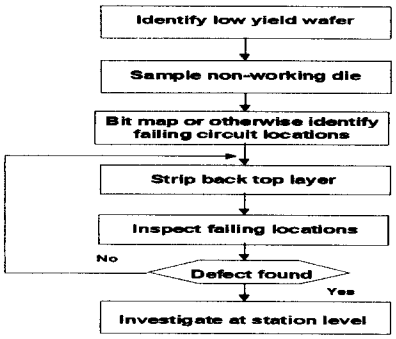

Fig. 9. Traditional Low Yield Analysis

from the imprecision of human judgement. In addition, the number of distinct defect type multiplies the amount of information generated. This defect review step is typically the bottleneck operation in defect management.

Automated defect classification has been under development for the last few years and has now reached the stage of maturity where useful information is generated. The technology is very complex and uses such techniques as neural net processing, fuzzy logic and machine learning made possible by the availability of cheap high performance computing. Accuracy and repeatability are far from perfect, but results are improving and are probably now as good as the average human inspector. Pilot and full manufacturing lines are now using ADC. For example, [13,14,15,16].

ADC tools are continuing to improve as evidenced by improved accuracy and repeatability and faster algorithms.

7. Automated in-line defect inspection using SEM

The next important technique on the horizon is automated defect detection using SEM. As device features continue to shrink, the problems of defect imaging become more acute. For an optical microscope, the resolution, R and depth of focus, d are given by, [17]

$$R = k_1 \frac{\lambda}{NA}$$

$$d = k_2 \frac{\lambda}{NA^2}$$

Where NA is the numerical aperture and k_1 and k_2 are constants. Combining these equations gives,

$$\lambda = \frac{k_2}{k_1^2} \frac{R^2}{d}$$

So for a given depth of focus the inspection wavelength must decrease with the desired resolution, i.e., minimum feature size or size of defect to be detected. This limit has forced the development of automated SEM-based defect detection [18], where the electron wavelength, of the order 0.042nm at 800eV, is much smaller than the defects of interest. In addition to their superior resolution, SEM-based inspection systems are also detecting additional defect types as a result of the charged particle nature of the electron beam. For example:

(a) Small defects hidden in dense features such as sub-quarter micron lines which cannot be resolved optically with thin small defects at the bottom.

(b) Unopened contacts and vias with residual material in the bottom for example due to incomplete etching.

(c) Defects in or on films with grain or surface roughness. SEM images of such materials appear smooth allowing higher sensitivity settings.

(d) Electrical defects exhibiting voltage contrast. Electrically floating structures charge differently, allowing detection of defects such as gate electrode shorted to substrate and metal line not connected through a via.

8. Software techniques for yield improvement

8.1 Introduction

This topic is very much an emerging area in the semiconductor industry. The availability of relatively

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