Benchmarking Semiconductor Manufacturing

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Abstract— **We are studying the manufacturing performance of semiconductor wafer fabrication plants in the US, Asia, and Europe. There are great similarities in production equipment, manufacturing processes, and products produced at these plants. Nevertheless, data reported here show that important quantitative measures of productivity vary by factors of 3 to as much as 5 across an international sample of 16 plants.**

We conducted on-site interviews with manufacturing personnel to better understand reasons for the observed wide variations in productivity. We have identified factors in the areas of information systems, organizational practices, process and technology improvements, and production control that correlate strongly with productivity.

I. Introduction

THE Competitive Semiconductor Manufacturing (CSM) Program at the University of California, Berkeley, since April 1991, has been conducting a detailed study of quality, productivity, and competitiveness in semiconductor manufacturing worldwide. The program is a joint activity of the College of Engineering, the Haas School of Business, and the Berkeley Roundtable on the International Economy at Berkeley, under sponsorship of the Alfred P. Sloan Foundation, and with the cooperation of semiconductor producers from Asia, Europe and the United States. The authors of this paper are the project's Co-Directors. Other contributors are named in the Acknowledgments. This article is based on data and analysis drawn from the continuing program [1].

The CSM program is being conducted by faculty, graduate students and research staff from UC Berkeley's schools of Engineering and Business, and Department of Economics. Many of the participating firms are represented on the program's Industry Advisory Board. The Board played an important role in defining the research agenda. A pilot study was conducted in 1991 with the cooperation of three semiconductor plants. The research plan and survey documents were thereby refined. The main phase of the CSM benchmarking study began in mid-1992 and will continue at least through 1997.

II. Focus of this Study

Our study focuses on semiconductor wafer processing as needed to produce VLSI chips including memories, microprocessors, signal processors, other logic, and mixed-signal products. Wafer processing takes place in manufacturing plants known as "fabs". Modern fabs require capital investment in plant and equipment of $500M to $1B each. They are the most costly manufacturing plants found in any industry today. The knowledge and skills required for efficient wafer fabrication require further large, ongoing investments. Manufacturing process sequences are exceedingly complex, with 400 or more sequential operations on a wafer over a span of 20 to 60 24-h days. A gross failure at any step can render a wafer worthless. The salable fraction of the total number of chips on a finished wafer, known as the "chip yield," varies from zero to 100%, depending on the effectiveness of quality control in avoiding localized defects on chips.

Today's principal VLSI products including memories, microprocessors, digital signal processors, application-specific logic, etc. are manufactured worldwide using very similar manufacturing equipment and processes. In many cases, 5 to 15 firms world-wide compete in selling interchangeable final products to hundreds of customers. Economic success in wafer fabrication clearly requires maximizing the output of salable products from a large fixed investment. Despite these obvious facts, there is an amazingly large variation in the manufacturing performance of semiconductor firms. The present study is intended to quantify and benchmark manufacturing performance and to identify superior practices in manufacturing technology, factory operation, organization, and management.

Our study has addressed only the wafer fabrication element of the total semiconductor manufacturing cycle. This is the most complex and capital-intensive element. The technologies and processes of packaging semiconductor chips are, however, growing in significance. Semiconductor packaging is the subject of a forthcoming report from another group [2].

III. Sources of Data and Limitations on Its Disclosure

The data and analysis summarized in this report derive from measurements of manufacturing performance and investigation of underlying determinants of performance at 16 wafer fabrication facilities in the United States, Europe, Japan and Taiwan. The companies operating these manufacturing facilities are listed in Table I. In selecting participants, we sought access to plants representing a cross-section of the industry, both internationally and in terms of business models and product mix. We asked for access to plants that had been in operation for at least three years. Substantial effort is required on the part of each participant. Some of those approached declined to participate. Participants who operate several semiconductor manufacturing lines generally opened one of their best lines to this study. Firms participate based on written agreement that we mask the relationship between individual firms and plants. We report results only in anonymous or aggregated forms.

Manuscript received March 3, 1995; revised December 9, 1995. This work was supported by a grant from the Alfred P. Sloan Foundation, New York, as a part of the Foundation's program of Manufacturing Industry Studies.

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Publisher Item Identifier S 0894-6507(96)03273-3.

TABLE I
COMPANIES PARTICIPATING IN THE MAIN PHASE OF THE COMPETITIVE SEMICONDUCTOR MANUFACTURING SURVEY (FIRST 18 MONTHS)

Advanced Micro Devices, Inc.	Nihon Semiconductor, Inc.
Cypress Semiconductor, Inc.	NEC Corp.
Delco Electronics, Inc.	Oki Electric Industry, Ltd.
Digital Equipment Corp. (2 sites)	Silicon Systems, Inc.
Intel Corporation	Taiwan Semiconductor Mfg.
International Business Machines, Inc.	Texas Instruments, Inc.
ITT Intermetall	Toshiba Corp.
LSI Logic. Corp	

The Berkeley team signs nondisclosure agreements with all participating firms.

As the first step, participants complete a 70–page mail-out questionnaire (MOQ), reporting data concerning clean room size and class, staffing levels, equipment counts, wafer starts, die yields, line yields, cycle times, manufacturing systems, etc. over the last four years. From the completed MOQ's, we calculate technical metrics of manufacturing performance for each participant. We then rank the participants for each of the metrics.

We observed a great variation in the scores. In an attempt to understand the factors that account for performance differences, we conduct a two-day visit at each participating site. We tour the manufacturing line, interview a cross-section of the staff, and hold a series of sessions to determine the fab's strategies for improving manufacturing performance. We assess each fab's resources for improvement including computer integrated manufacturing (CIM) and information systems, human resources development, deployment of work groups and teams, etc. These more qualitative evaluations of participants' operational practices are then correlated with the performance metrics to identify those practices that underlie top performance.

IV. METRICS OF MANUFACTURING PERFORMANCE

The technical metrics we use to measure manufacturing performance of the participants are defined as follows:

1) *Cycle time per wafer layer* measures the duration, expressed in fractional working days, consumed by production lots of wafers from the time of release into the fab until time of exit from the fab, divided by the number of masking layers. The participants report cycle times for each of several process flows they may operate; we compute a weighted average cycle time per layer for the fab, where the weights are the number of wafer starts in each process flow.
2) *Line yield* measures the fraction of wafers started that emerge from the fab as completed wafers ready for electrical testing of the individual circuits on the wafer. In monthly periods, the participants report line yield for each of their process flows, calculated as

$$(\mathrm{WO})/[(\mathrm{WO}) + (\mathrm{SC})]$$

where WO is the number of wafers completed during the month and SC is the number of wafers scrapped during the month. We normalize the reported line yields into scores expressing the line yield per ten wafer layers using the formula

$$\mathrm{LY10} = \mathrm{LY}^{(10/\mathrm{ML})}$$

where LY is the reported line yield, ML is the number of masking layers, and LY10 is the calculated line yield per ten layers. We then compute a weighted average line yield per ten layers for the fab, where the weight for each process flow is the number of wafer starts of the flow.
3) *Die yield* expresses the fraction of the total whole die on a completed wafer that pass the electrical probe test. The participants report their die yields for the highest volume product in each of their process flows. For memory products, the reported die yield is that after laser repair. We convert the reported die yield into a defect density using the Murphy model

$$Y = \{(1 - e^{-AD})/AD\}^2$$

where Y is the reported die yield, A is the die area in square centimeters, and D is the calculated defect density, expressed as defects per square centimeter. The calculated defect densities account for all yield losses remaining after repair, including spot defects, parametric problems, and any other losses. We compare defect density scores of the participants only after sorting process flows into memory and logic groups that are further categorized by the minimum geometry achievable with the flow.
4) *Stepper productivity* expresses the number of wafer layers completed per 5X stepper per calendar day (considering only layers exposed using 5X steppers). We estimate the number of wafer operations in a process flow performed per calendar day by 5X steppers using the formula

$$\mathrm{SL} = (\mathrm{WS}/7)(\mathrm{NL})(\mathrm{LY}')$$

where SL is the calculated number of 5X stepper operations per day, WS is the reported average number of wafer starts per week in the process flow, NL is the number of masking layers in the process flow performed on 5X steppers, and LY′ is an inflated line yield computed as

$$\mathrm{LY}' = (1.0 + \mathrm{LY})/2$$

where LY is the reported line yield for the process flow. (This inflated line yield allows for half of the total line yield loss to load 5X steppers, or equivalently, it assumes the average wafer that is scrapped makes it through half the 5X layers before being discarded.) The calculated 5X stepper operations per day for all process flows are summed, then divided by the number of 5X steppers present in the fab to obtain the value of the metric.
While participants processing a wide variety of products must change reticles more frequently than those producing only a few products, we observed that some participants have automated reticle changes to the point that there is almost no lost time on their 5X steppers when they change reticles. We therefore make no al-

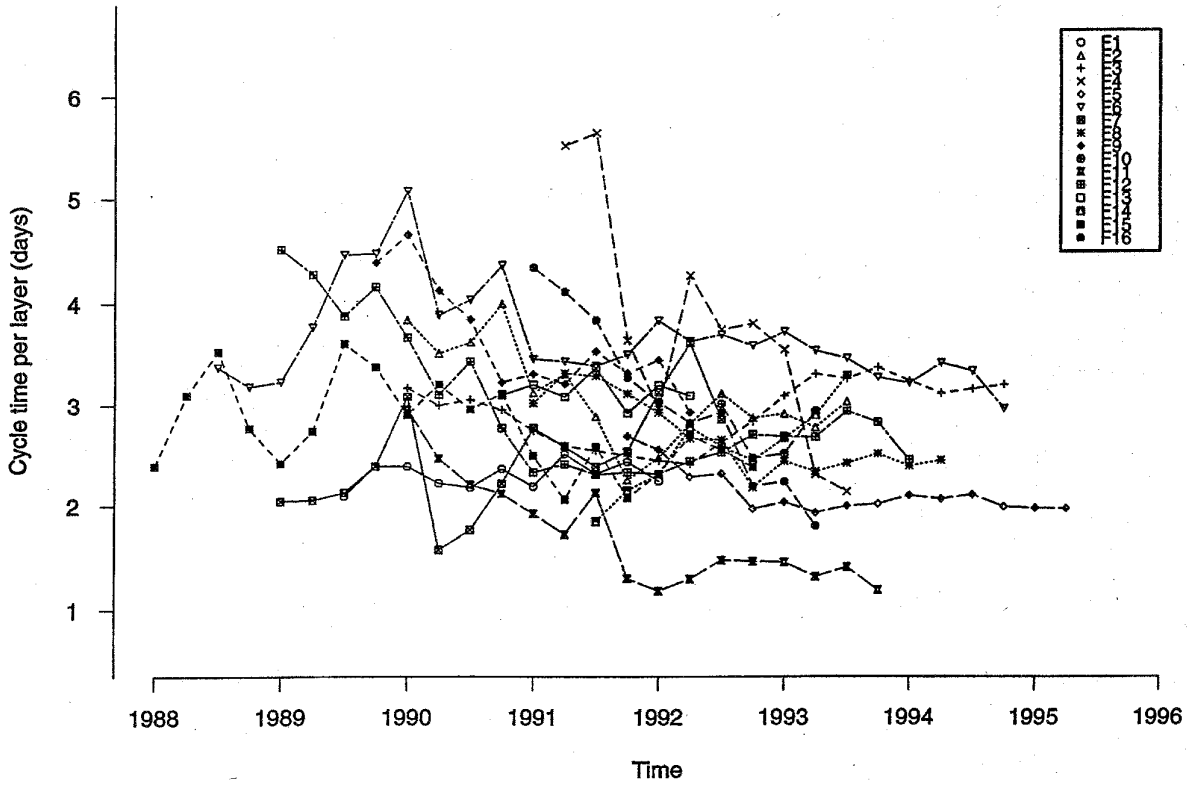


Fig. 1. Cycle time per layer.

lowance for product mix in computing this metric. We also did not make any allowances for differences in average die sizes among the participants.

5) *Direct labor productivity* expresses the total number of wafer layers completed per operator per working day. To compute this metric, we first estimate for each process flow the total number of wafer layers completed per working day using the formula

$$\mathrm{WL} = (\mathrm{WS}/\mathrm{WD})(\mathrm{TL})(\mathrm{LY}')$$

where WS is the average number of wafer starts per week, WD is the number of working days per week, TL is the total number of wafer layers in the process flow, and LY′ is the inflated line yield defined as above. We then compute the metric by summing the WL figures for each process flow and dividing by the reported number of production operators.

6) *Total labor productivity* expresses the total number of wafer layers completed per working day divided by the total head count. This metric is computed similarly, except the divisor is the reported total number of fab employees, including dedicated staff from equipment vendors.

7) *On-time delivery* measures the ability of the participants to meet production schedules. It expresses the percentage of items scheduled for output in a week whose actual output quantity by the end of the week is greater than or equal to the scheduled quantity. Some participants report on-time delivery at the die level, some at the finished goods level, some at both levels, while others declined to state their performance or simply did not know.

We encountered a wide range in scores for each metric, even though the basic process technology and the major manufacturing equipment in use at the participants were generally similar. Table II summarizes the best, average, and worst scores for each metric, considering the latest data points we received from each of the sixteen participants, and provides an estimate of the relative ranking of Japanese and US firms in each metric. These data points represent measurements of manufacturing performance in some quarter between the middle of 1992 and the end of 1993, depending upon the participant.

Rates of improvement also are studied for each participant. Figs. 1–6 graph the first six metric scores over time for the participants. To protect confidentiality, a coding scheme is used whereby the participating fabs are labeled $F1$–$F16$. The scheme is uniform across the graphs, e.g., $F1$ refers to the same fab on all graphs. Scores for each technical metric are computed for each quarter over a period of three to four years. In graphs of defect densities, multiple curves are sometimes displayed for the same fab, indicating the fab operated more than one process flow in the category of flow that is graphed. For most metrics, the ranking of participants does not change quickly. We did not find many cases where a last-place participant overtook the leader for a particular metric, although a few participants improved their rankings considerably over the period.

Perhaps the most striking phenomenon observed in our measurements concerns the initial defect densities for process

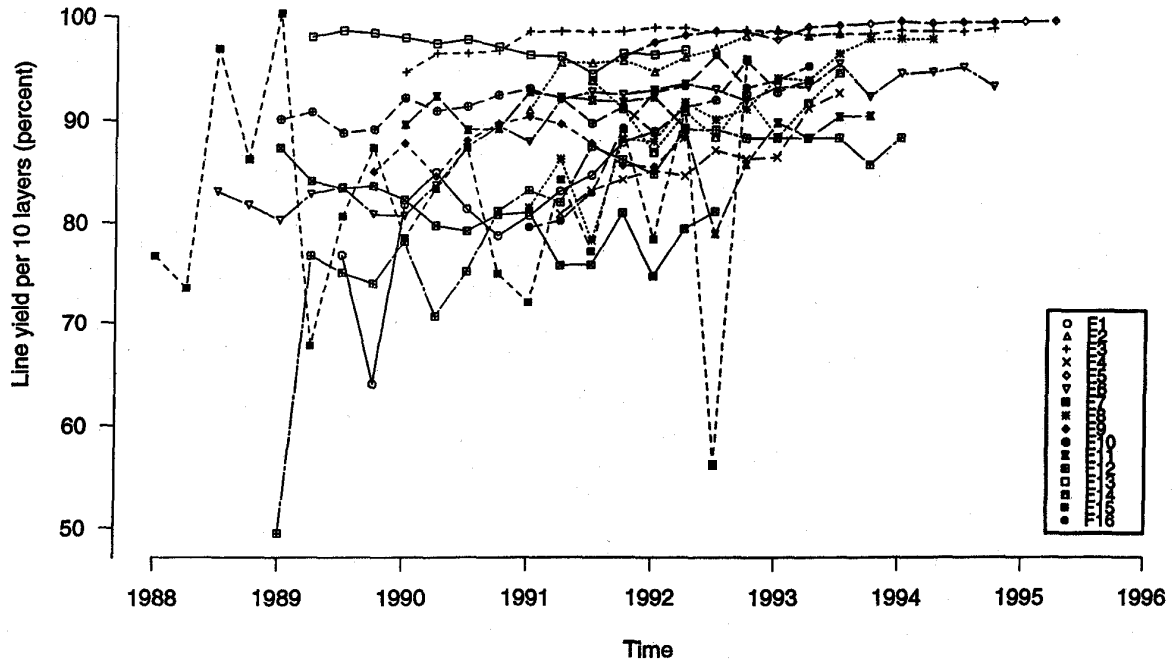


Fig. 2. Line yield.

flows, that is, the defect densities realized in the first quarter after transfer of the process flow into manufacturing. We recorded a factor-of-ten range in initial defect densities. Those fabs with poor starting points tend to have faster rates of improvement, but not nearly fast enough to overtake those with good starting points, at least not for several years, as those with good starting points also make steady if somewhat slower progress reducing defect densities.

V. Analysis of Practices Underlying Manufacturing Performance

Our main objective in the CSM survey is to identify those operational practices that underlie leading-edge manufacturing performance. Summarized below are the operational practices that distinguish those fabs achieving best or near-best scores in one or several of the metrics described above. (For the sake of brevity, we refer to such fabs as the "leading" fabs.) But before summarizing our findings in that regard, it is only fair to acknowledge that our analysis does not account for several strategic factors concerning product design and fab design that may strongly influence manufacturing performance.

First, the restrictiveness of product design rules can have a strong influence on observed die yields and hence on our calculated defect densities. Issues of overall business strategy influence the choice of design rules and affect the priority attached to the different metrics of manufacturing performance. We made no attempt to normalize defect density scores for differences in design rules and/or overall business strategy among the participants.

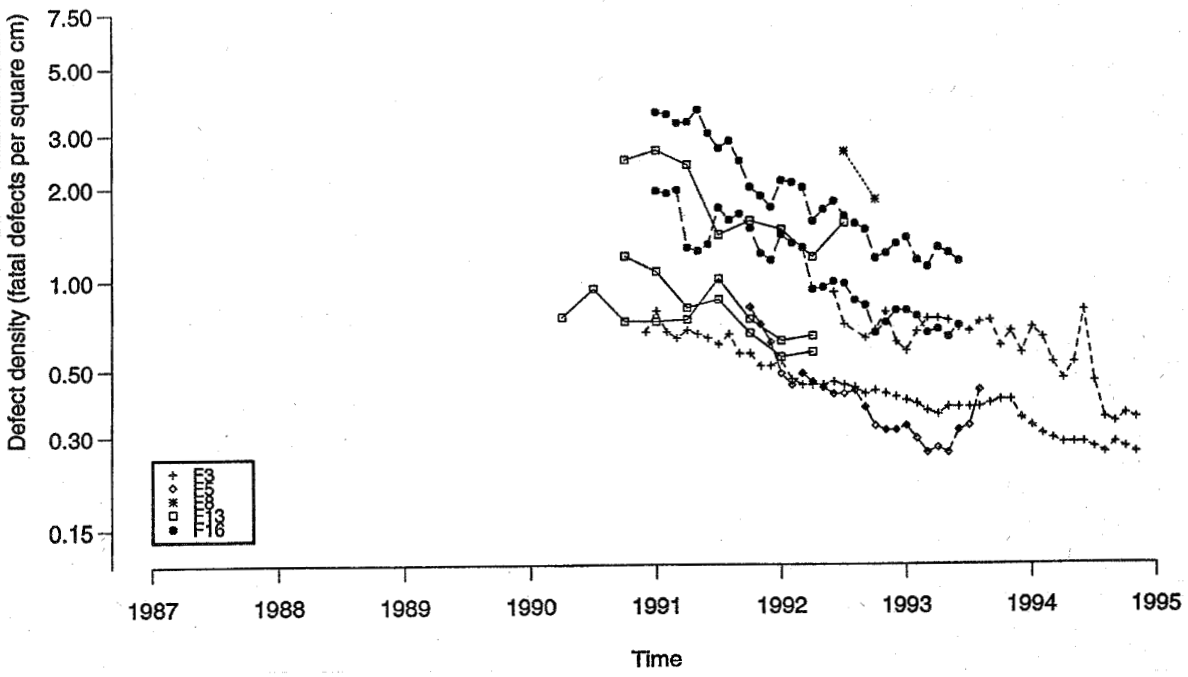
Second, the range of sizes of fabs in our survey, in terms of wafer starts, spans a factor of almost fifty. Small fabs generally have inferior labor and equipment productivity scores, because of the indivisibility of machines and operators, and because of the tendency to install extra equipment to avoid situations in which a particular process step must be performed by a one-of-a-kind equipment type. We made no attempt to normalize productivity scores to account for fab size.

Third, the assignment of older-generation of processing equipment to newer-generation process flows may result in lower values for several metrics than would be possible with newer equipment. While yields may be lower for the strategy to employ older processing equipment, capital costs are lower

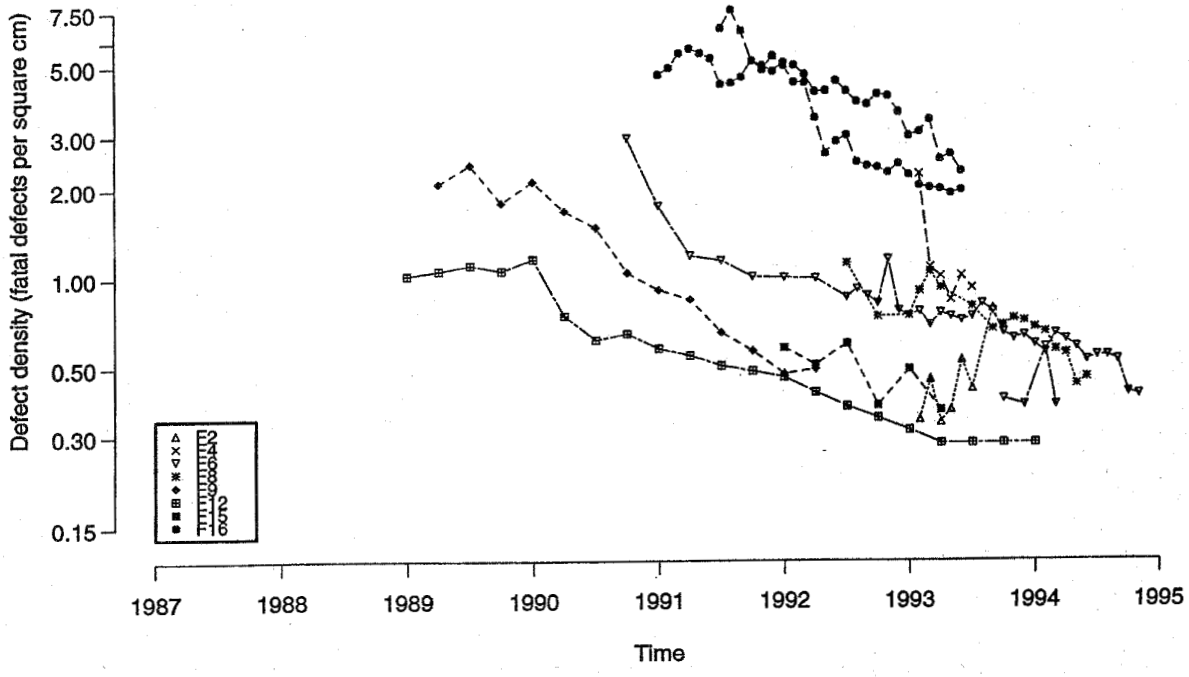
TABLE II
Summary of Technical Metric Scores, Competitive Semiconductor Manufacturing Survey (First 18 Months)

Metric	Best score	Average score	Worst score	Japan vs. US
Cycle time per layer (days)	1.2	2.6	3.3	–
Line yield per ten layers (%)	98.9	92.8	88.2	++
Murphy defect density - (defects/cm^2)				Overall: ++
0.7 - 0.9 micron CMOS memory	0.28	0.74	1.52	
0.7 - 0.9 micron CMOS logic	0.28	0.79	1.94	
1.0 - 1.25 micron CMOS logic	0.23	0.47	0.96	
1.3 - 1.5 micron CMOS logic	0.21	0.61	1.15	
5X stepper throughput (5X layers completed per machine-day)	724	382	140	+
Direct labor productivity (wafer layers completed/operator-day)	63.0	29.6	8.0	+
Total labor productivity (wafer layers completed/total staff-day)	37.7	17.6	3.3	++
On-time Delivery (% of line items with 95% of die output on time)	100%	89%	76%	–

Average and worst scores are calculated after discarding the worst data sample for each metric. Legend:
++ Japanese fabs are almost uniformly superior
+ Japanese fabs are generally superior
0 Superior/inferior fabs are not distinguished by region
– US fabs are generally superior
— US fabs are almost uniformly superior



(a)



(b)

Fig. 3. (a) Memory defect density 0.7–0.9μ CMOS process flows. (b) Memory defect density 0.7–0.9μ CMOS process flows. (c) Logic defect density 0.7–0.9μ CMOS process flows. (d) Logic defect density 1.3–1.5μ CMOS process flows.

as well, and so the strategy might turn out to be economically competitive or even superior to the strategy that employs solely new processing equipment. We made no attempt to normalize metric scores for the generations of equipment applied.

With these strategic factors aside, we now turn to the various operational practices we found to be correlated with good manufacturing performance (in terms of the manufacturing metrics we have defined). These practices may be categorized into four basic types of practices at which a fab must excel in order to realize excellent manufacturing performance.

First, a fab must have computer systems providing strong process control, excellent data collection and excellent data

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