Metrology needs for the semiconductor industry over the next decade

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Metrology Needs for the Semiconductor Industry Over the Next Decade

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Metrology will continue to be a key enabler for the development and manufacture of future generations of integrated circuits. During 1997, the Semiconductor Industry Association renewed the National Technology Roadmap for Semiconductors (NTRS) through the 50 nm technology generation and for the first time included a Metrology Roadmap (1). Meeting the needs described in the Metrology Roadmap will be both a technological and financial challenge. In an ideal world, metrology capability would be available at the start of process and tool development, and silicon suppliers would have 450 mm wafer capable metrology tools in time for development of that wafer size. Unfortunately, a majority of the metrology suppliers are small companies that typically can't afford the additional two to three year wait for return on R&D investment. Therefore, the success of the semiconductor industry demands that we expand cooperation between NIST, SEMATECH, the National Labs, SRC, and the entire community.

In this paper, we will discuss several critical metrology topics including the role of sensor-based process control, in-line microscopy, focused measurements for transistor and interconnect fabrication, and development needs. Improvements in in-line microscopy must extend existing critical dimension measurements up to 100 nm generations and new methods may be required for sub 100 nm generations. Through development, existing metrology dielectric thickness and dopant dose and junction methods can be extended to 100 nm, but new and possibly in-situ methods are needed beyond 100 nm. Interconnect process control will undergo change before 100 nm due to the introduction of copper metallization, low dielectric constant interlevel dielectrics, and Damascene process flows.

INTRODUCTION

Integrated circuits (ICs) are the cornerstone of a multi-billion dollar electronics industry that is leading civilization into the 21st century. IC technology is being driven by consumer demands for improved applications, such as information processing and communications, with greater capability at a constant cost. Thus, consumers have forced the historical trend of a 25 to 30% cost reduction per unit function per year. More than 30 years ago, Gordon Moore observed that the number of transistors in a manufactured die increased by a factor of two every year (2). From this observation, it was postulated that the number of bits in memory chips would increase by a factor of four every three years. A 30% decrease in feature size every three years and a 1.5x increase in chip size are two of the factors that enable the continuation of Moore's law. The other factors that have kept the industry on the historical cost reduction trend are yield improvement, wafer size increase, and overall equipment effectiveness. The cost productivity curve is shown in Fig. 1.

The overwhelming cost of research and development including product development for each new technology generation has forced international cooperation for the semiconductor industry. For example, the total cost of developing 300 mm-wafer-capable manufacturing is estimated to be more than $10 billion, and the development of 193 nm lithography

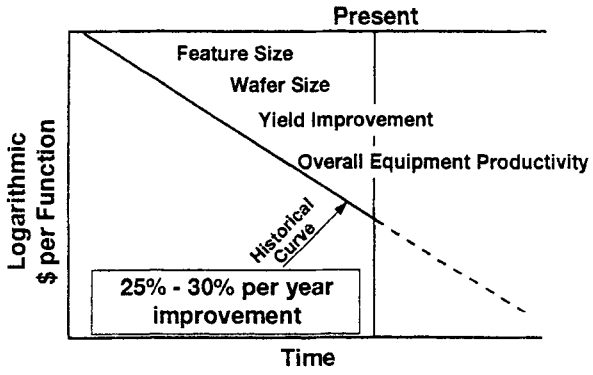

FIGURE 1. *Historical Trend of 25-30% Annual Cost Reduction per Unit Function for the Semiconductor Industry.*

is estimated at around $1 billion (3). One example of cooperation is the National Technology Roadmap for Semiconductors (1). The 1992, 1994, and 1997 Roadmaps provide a consensus view of the most critical technology requirements for IC manufacture with a 15 year horizon. The 1997 NTRS projects these technology needs to the 50 nm technology generation. The NTRS allows R&D organizations such as SEMATECH, SRC, MARCO, and interested national labo-

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ratories to focus their resources on the most critical requirements and plan activities according to the industry's implementation timeline (1).

Metrology enables the lithography, wafer size, yield, and equipment effectiveness drivers of cost reduction, and therefore metrology technology needs to keep pace with process technology. In addition, metrology must also enable the rapid introduction of new products which require the "ramping within ramps" such as the manufacture of higher speed versions of a generation of microprocessor (4). For the first time, the 1997 version of the NTRS contains a Metrology Roadmap. In this paper, we will describe the industry's metrology needs over the next ten years using the 1997 NTRS for technical guidance.

The 1997 NTRS describes the key challenges that the industry faces if it is to keep on the historical cost-productivity curve (1). These critical industry challenges provide a means of prioritizing metrology requirements. The overall challenges are listed below with a brief description (1):

- *The ability to continue affordable scaling*
  Continue the roadmapped timeline for new technology generations

- *Affordable lithography at and below 100 nm*
  Move to 193 nm optical lithography and find affordable replacements for optical lithography

- *New materials and structures*
  Short term: replace aluminum/silicon dioxide interconnect materials with copper and low dielectric constant materials including appropriate cost saving Damascene processes; Long Term: find a solution for transistor design and materials for sub 100 nm technology generations

- *GHz frequency operation on- and off-chip*
  High-frequency on-chip interconnects and off-chip packaging based interconnects must allow full utilization of increases in chip speed

- *Metrology and test*
  This paper describes the required metrology, and electrical testing of chip functionality must remain cost-effective as chip functionality increases

- *The research and development challenge*
  Provide an affordable infrastructure that moves technology from basic research into manufacturing

Metrology needs must be prioritized and developments driven to enable the key processing technology that will allow us to maintain the cost reduction trend and profit margins that maintain an economically healthy industry. In a perfect world, metrology capability would be available when process tool suppliers initiate tool development for the next technology generation (1). Unfortunately, this forces the metrology suppliers to wait three years longer than process tool suppliers for a return on their investment in new tool development. The same principle applies to changing wafer size, and time for return on investment will be longer than three years for 300 mm wafer metrology tools. The entire community must cooperate to overcome this challenge.

The Metrology Roadmap describes the requirements and potential solutions for the off-line, in-line, and in-situ measurements. Other metrology needs are found in the Defect Reduction Technologies Roadmap. In Fig. 2, an overview of the multiple measurement requirements is depicted in terms of the fab process flow.

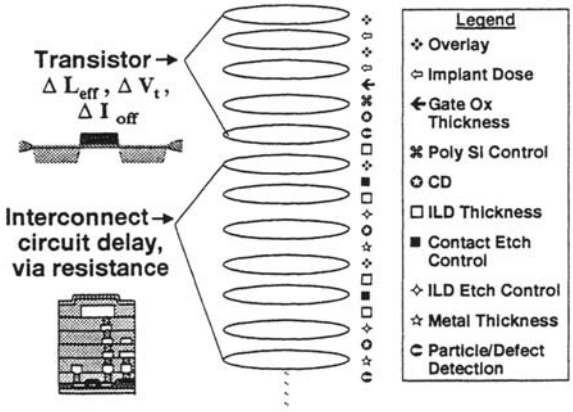

FIGURE 2. *In-FAB Metrology*
Metrology is used to control fabrication processes so that integrated circuit electrical performance falls within product specifications. At the 150 nm technology generation, there will be approximately 500 process steps requiring more than 20 overlay and 35 CD measurements.

In addition to fab process metrology, packaging metrology is covered in the 1997 NTRS. Metrology is expected to continue to migrate from off-line toward in-line and in-situ application. However, off-line measurements will continue to provide highly detailed information that requires special capabilities. For example, transmission electron microscopy (TEM) is often the only means of analyzing small features found in modern IC's. Evolutionary improvements of current in-line metrology methods are expected to enable control of implant and thin film processes. Currently, many transistor and interconnect processes are controlled using physical measurements on unpatterned (test) wafers. The need for nondestructive measurements on product wafers is an additional challenge for in-line metrology. Initial implementation of in-situ sensor-based process control has proven the usefulness of this approach through improved tool throughput and reduced wafer scrap. Many of these sensors measure something that allows control of wafer level properties, often indirectly. In addition to increasing their range of applications, sensors are expected to evolve to provide more de-

tailed information on the wafer with increased spatial resolution (i.e., die to die uniformity). Micro-electromechanical systems (MEMS) are expected to become the smart sensors of the future (1). One visionary example is an etch chamber with a strategically located mass spectrometer on a chip with built-in circuitry for real time process control. Packaging metrology is not as mature as wafer fab metrology, and thus there are many opportunities to implement existing technology as well as to develop appropriate new methods.

The advantages of in-line measurements, such as improved analysis cycle time, have resulted in the "FAB-LAB" concept (5,6). The laboratories contain tools and data management/analysis systems capable of characterizing product wafers using information such as particle/defect location maps (5). The FAB-LAB is an integral part of pilot line as well as fab start-up and operation, and there are examples of FAB-LABs both inside and next to the clean room. It is interesting to note that some IC manufacturers have located traditionally out of the fab tools such as TEM inside clean rooms. This is one example of how the need to reduce the cycle time for product development and yield learning has driven the industry. The relationship between analysis cycle time requirements and the proximity of analysis tools to the fabrication line has been described elsewhere (5).

THE MEASUREMENT REQUIREMENTS AND FUTURE OF STATISTICAL PROCESS CONTROL

Statistical Process Control (SPC) methodology is used to control each IC manufacturing process so that a majority of the final product has a narrow range of electrical characteristics. In this section, we emphasize the need for process application based evaluation of metrology tools capability for use in SPC. Automated in-line and appropriate off-line metrology tools are evaluated for SPC by the measurement precision to process tolerance (process specification range) ratio criterion, P/T. The P/T should be < 10%, but 30% is often tolerated. $P/T = 6\sigma/(UL-LL)$ where the measurement precision (variation), σ, includes the short-term repeatability and long-term reproducibility, and UL and LL are the upper and lower process limits, respectively. The P/T metric is well accepted by the semiconductor industry.

Determination of the true P/T ratio for the process range of interest requires careful implementation of the P/T methodology and reference materials with identical feature size, shape, and composition to the processed wafer being measured. Often, there are no certified reference materials that meet this requirement, and P/T ratio and measurement accuracy are determined using best available reference materials. One key example is the lack of an oxide thickness standard for sub 5 nm SiO_2 and nitrided oxides.

Another aspect of true determination of P/T capability is measurement linearity. If one determines the P/T ratio for a thickness or width measurement using a reference material that has larger (or smaller) dimensions than the features being measured during IC manufacture, lack of measurement linearity could result in insufficient resolution to distinguish changes over the entire process range of interest. For the sake of argument, we will call tool precision determined using inadequate reference materials as "estimated tool precision."

Often, the concept of measurement resolution is confused with "estimated tool precision." It is possible for a tool to appear to have small (i.e., good) precision and still have poor resolution. As transistor and interconnect features shrink, greater resolution is becoming more critical. The criteria for metrology tool applicability to SPC need to include both P/T and resolution.

For example, we need to be able to distinguish a 2.0 nm thick transistor gate dielectric from a film having 2.1 nm or 2.2 nm thickness. Another example is distinguishing a 100 nm gate electrode width (critical dimension, CD) from a 102 nm CD. SPC criteria are usually applied to physical measurements, but electrical measurement variability also needs to be suitably small.

Another example of the varied and thus confusing usage of the term resolution is in critical dimension (CD) measurement by scanning electron microscopy (SEM). The microscopy community has used two different methods to determine the resolution of a scanning electron microscope (SEM). One is the width of the electron beam, and the other is the ability to distinguish two closely spaced features in an image of a well characterized test sample. Fine gold particles on a carbon background is a well accepted test sample.

Despite the long history of these methods, there do not seem to be standardized (SEMI, ASTM, etc.) resolution procedures. Another measure of the resolution of an SEM dedicated to CD measurement is its ability to distinguish repeatedly differences in transistor gate linewidth (e.g., 100 nm from 102 nm). This process application based metric for resolution would facilitate evaluation of true SPC capability.

One way to assure that the metrology tool has adequate resolution is to determine the true P/T capability by using a series of standardized, accurate reference materials over the measurement range specified by the upper and lower process limits. In Fig. 3, we depict how the multiple reference materials approach might work. We note that some measurements may require one suitable reference material for P/T determination.

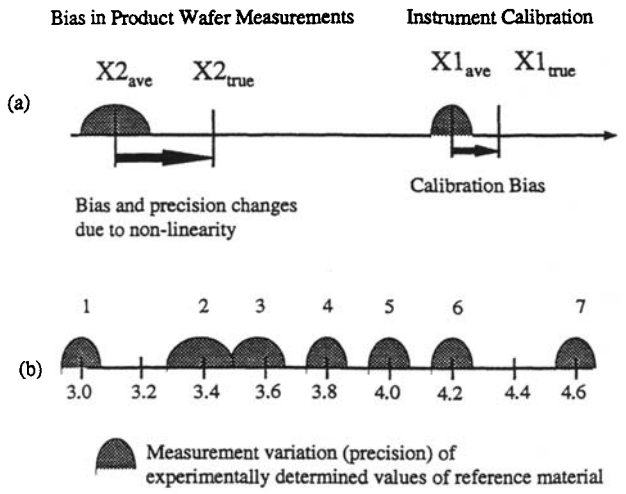

FIGURE 3. *Relationship between Measurement Resolution and Precision*

(a) Measurement non-linearities can result in bias (difference between true and measured value) changes between the calibrated value and values within the range of interest.

(b) For this example let us assume that the process tolerance (also called process specifications) is from 3.0 nm to 4.6 nm. The measurement precision at 3σ (variation) is shown for reference materials inside the process range. The experimental P/T capability observed using reference materials 4, 5, and 6 indicates that a single measurement of a 4.0 nm is different from one at 3.8 nm or 4.2 nm. Thus this fictitious metrology tool can resolve those values. The tool is not able to resolve 3.4 nm from 3.6 nm at 3σ.

A SEMI task force will be standardizing the implementation of P/T over the next several years. This type of activity can greatly improve the usefulness of the P/T metric, and perhaps it could be called the "Resolution P/T." Implementation of this methodology is hampered by the lack of reference materials with features (size, composition, etc.) inside the measurement range of interest.

The goal of sensor-based process control is to become real time. In-line measurement tools are (when appropriate) used for run to run control. The concept of P/T must be extended to allow evaluation of sensors. Sensors appear to have the interesting challenge of being required to measure process variation without the luxury of averaging over multiple measurements to improve precision.

One revolutionary improvement in SPC has been the use of cumulative data sets (from the same sample, across a wafer, and previous samples) to greatly improve estimation of measurement precision (6,7). A smaller estimated precision may mean that a metrology tool is capable of meeting P/T criteria for SPC without hardware improvements or it can allow reduction of process tolerances while maintaining P/T. Since this improvement was not associated with the measurement tool itself, it raises questions about how to evaluate improvements in metrology tools.

CORRELATION OF PHYSICAL AND ELECTRICAL MEASUREMENTS

IC performance and yield are ultimately evaluated by the electrical parametric and functional testing. It is possible to measure the relevant electrical properties of transistor and interconnect structures on product wafers during IC manufacture. Clearly, this requires that the wafers have been processed to the point where a complete transistor (or interconnect structure) is fabricated. When the manufacturing process is mature and robust and a majority of the process flow is transferred to the next product or technology generation, electrical metrology may provide a majority of process control needs. However, when excursions in process tool performance or process material quality occur, they need to be observed and controlled long before an electrical test can be performed. In this section, we describe several levels of correlating physical and electrical measurements. These levels can be described as follows: correlation of electrical and physical measurements of a specific physical feature such as gate dielectric thickness; correlation of a set of physical parameters with the electrical properties of the transistor or interconnect structure; and correlation of die, wafer, or lot level data with yield.

Since scrap prevention is one of the goals of physical, in-line metrology, physical measurement must correlate with electrical performance. The gate dielectric thickness, gate electrode critical dimension, and implant dose and profile all influence transistor electrical parameters such as threshold voltage, off current, and gate delay. Modeling of transistors provides insight into the nature of the correlation of physical parameters with electrical performance, including manufacturing sensitivities (8).One can model the change in variation of electrical parameters using device simulation and selected ranges of physical parameter variation. The variation of threshold voltage range with range of gate length and channel implant is shown for a fixed range of gate dielectric thickness and other physical parameters in Fig. 4. Zeitzoff and Tasch discuss manufacturing sensitivity in these proceedings (8).

Another issue is that integrated circuit development requires statistically significant information which can only come from electrical test. The need for early measurement capability during process tool development is highlighted by the push for more rapid ramping of pilot line yield. Delivery of well characterized process tools greatly facilitates rapid pilot line yield ramping. Bartelink is credited with initiating the field of Statistical Metrology which utilizes electrical test structures to determine across the die and across the wafer properties (9, 10). Statistical Metrology is a set of procedures designed to deconfound measurement error from true process variation. Statistical Metrology is discussed in the Process Integration, Devices, and Structures Roadmap and the Metrology Roadmap's one page contribution to that roadmap (1).

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