Benchmarking Semiconductor Manufacturing

Robert C. Leachman and David A. Hodges

Competitive Semiconductor Manufacturing Program
Engineering Systems Research Center
University of California at Berkeley
Berkeley, CA 94720

Abstract

We are studying the manufacturing performance of semiconductor wafer fabrication plants in the US, Asia, and Europe. There are great similarities in production equipment, manufacturing processes, and products produced at semiconductor fabs around the world. However, detailed comparisons over multi-year intervals show that important quantitative indicators of productivity, including defect density (yield), major equipment production rates, wafer throughput time, and effective new process introduction to manufacturing, vary by factors of 3 to as much as 5 across an international sample of 28 fabs.

We conduct on-site observations, and interviews with manufacturing personnel at all levels from operator to general manager, to better understand reasons for the observed wide variations in performance. We have identified important factors in the areas of information systems, organizational practices, process and technology improvements, and production control that correlate strongly with high productivity. Optimum manufacturing strategy is different for commodity products, high-value proprietary products, and foundry business.

Introduction

This comparative study involved the measurement of manufacturing performance and investigation of underlying determinants of performance at 28 wafer fabrication facilities in the United States, the United Kingdom, Germany, Spain, Japan, Korea and Taiwan. The companies operating these facilities are displayed in Table 1.

Companies Participating in the Main Phase of the Competitive Semiconductor Manufacturing Survey	
Advanced Micro Devices, Inc. (AMD)	National Semiconductor Corp. (2 fabs)
Cypress Semiconductor, Inc.	NEC Corp.
Delco Electronics Corp.	Oki Electric Industry, Ltd.
Digital Equipment Corp. (2 fabs)	Samsung Electronics Co., Ltd.
Harris Corporation	Silicon Systems, Inc. (SSI)
Hyundai Electronics Industries, Ltd.	Sony Microelectronics Corp. (2 fabs)
Intel Corporation	Taiwan Semiconductor Mfg. Corp. (TSMC)
Int'l Business Machines, Inc. (IBM)	Texas Instruments, Inc.
ITT Intermetall	Tohoku Semiconductor Corp. (TSC)
LSI Logic Corp. (2 fabs)	Toshiba Corp.
Lucent Technologies (2 fabs)	United Microelectronics Corp. (UMC)
Motorola, Inc.	

Table 1

Each participant completes a 100-page questionnaire covering objective data including clean room size and class, head counts, equipment counts, wafer starts, die yields, line yields, cycle times, computer systems, etc. over the preceding four years. From this data we calculate technical metrics of manufacturing performance for each participant. We then compare performances on each of the metrics.

We observe great variations in the scores of the various participants. To understand what practices account for such performance differences, we conduct a two-day site visit with each participant. We tour the manufacturing line, interview a cross-section of the entire fab staff, and hold discussions concerning strategies for improving yields, increasing wafer throughput, reducing cycle times, etc. We survey each firm's activities to improve computer integrated manufacturing (CIM) and information systems, human resources development, effectiveness of work groups and teams, etc. These more qualitative indicators of participants' operational practices are then correlated with the performance scores to identify those practices that underlie good or bad performance. Performance and practice comparisons are separated into VLSI memory, VLSI logic, and MSI categories, according to the type and sophistication of devices that are fabricated. The individual identities of the participating fabs are coded. Each participant receives all the comparative data but knows only its own code identifier.

Metrics of manufacturing performance

We use the following technical metrics to measure manufacturing performance:

- Average line yield, the percentage of wafers started that are completed properly, normalized to twenty mask layers.

- Defect densities, calculated for major process flows in each fab by using reported die yields and die sizes in the Murphy model of defect density. The reported defect densities account for all yield losses, including both spot defects and parametric problems. For memory products, the die yields applied to the defect density formula are final die yields after laser repair.

- Integrated fab and die sort yield, calculated as the product of line yield per twenty masking layers and the estimated die yield for a 0.5 sq cm die. This die yield is estimated using the Murphy defect density calculated from reported die yields as described above.

- Wafer masking layers completed per 5X stepper per calendar day (considering only layers exposed using 5X steppers).

- Wafer implant layers completed per ion implanter per calendar day.

- Wafer metal layers completed per metallization machine per calendar day.

- Integrated 5X stepper throughput, the equivalent number of full-wafer operations per 5X stepper per day, calculated as the number of 5X wafer operations per day times the integrated yield defined above.

- Average cycle time per mask layer.

- Wafer masking layers completed per operator per working day (considering all masking layers, regardless of type of lithography equipment).

- Wafer masking layers completed per working day divided by the total head count.

For all of these metrics, we encountered a wide range in scores, even though the basic process technology in use at the participants was generally similar. Table 2 summarizes scores for each metric for the CMOS memory category, considering the latest data points we received from each

of the 28 participants. Similar spreads in the data were found also for CMOS logic fabs. The time interval covered is from the middle of 1992 to the middle of 1995.

Rates of improvement were studied for each participant. Scores for each technical metric were computed for each quarter over a period of three to four years. For most metrics, the ranking of participants changes slowly, i.e., we found few cases where a last-place participant overtook the leader for a particular metric, although some participants improved their rankings considerably over the period.

One of the most striking trends we observed in our measurements concerns the initial defect densities for process flows, i.e., the defect densities realized in the first calendar quarter after transfer of the process flow into manufacturing. We recorded a factor-of-ten range in initial defect densities. Those fabs with poor starting points tend to have faster rates of improvement, but not nearly fast enough to overtake those with good starting points, at least not for several years, as those with good starting points also make steady if somewhat slower progress reducing defect densities.

The integrated stepper throughput metric is perhaps our best indicator of overall fab productivity, at least for submicron fabs dependent on this technology for photolithography. The varying strengths and weaknesses in line yield, die yield (defect density) and stepper throughput among our participants are integrated to see the overall throughput of good silicon per machine. Even for such an integrated metric, we find a remarkable factor-of-seven range in performance.

Technical Metric Scores: Memory Fabs

Metric	Best	Avg	Wrst
Line yield per twenty layers (%)	98.8	93	87.1
Murphy defect density - 0.45 - 0.6 micron CMOS memory (defects per sq cm after repair)	0.03	0.59	1.34
Murphy defect density - 0.7 - 0.9 micron CMOS memory (defects per sq cm after repair)	0.01	0.51	1.81
Murphy defect density - 1.0 - 1.25 micron CMOS memory (defects per sq cm after repair)	0.31	0.59	1.08
Integrated fab and sort yield (%) 0.45 - 0.6 micron CMOS memory (0.5 sq cm device)	91.7	72.1	46
Integrated fab and sort yield (%) 0.7 - 0.9 micron CMOS memory (0.5 sq cm device)	92.9	73.9	35.9
Integrated fab and sort yield (%) 1.0 - 1.25 micron CMOS memory (0.5 sq cm device)	77	66.7	48.3
5X Stepper throughput (wafer operations per 5X stepper per day)	606	463	281
Ion implanter throughput (wafer operations per implanter per day)	1360	855	339
Metallization throughput (wafer operations per machine per day)	273	147	53
Integrated 5X stepper throughput (Full-wafer ops/stepper-day)	479	344	160
Cycle time per mask layer (days)	1.8	2.9	4.1
Direct labor productivity (mask layers completed/operator-day)	71.7	42.6	18.4
Total labor prod. (mask layers/p-d)	51.6	27.3	15.1

Table 2

Practices underlying manufacturing performance

Our main objective is to identify those operational practices that underlie leading-edge manufacturing performance. Summarized below are the operational practices that distinguish those fabs achieving best or near-best scores in one or several of the metrics described above. (For the sake of brevity, we refer to such fabs as the "leading" fabs.) But before summarizing our findings in that regard, it is only fair to acknowledge that our analysis does not account for several strategic factors concerning product design and fab design that may strongly influence manufacturing performance.

First, the restrictiveness of product design rules can have a strong influence on observed die yields and hence on our calculated defect densities. We made no attempt to normalize defect density scores for potential differences in design rules among the participants.

Second, the range of sizes of fabs in our survey, in terms of wafer starts, spans a factor of almost fifty. Small fabs generally have inferior labor and equipment productivity scores, because of the indivisibility of machines and personnel, and because of the tendency to install extra equipment to avoid situations in which a particular process step must be performed by a one-of-a-kind equipment type. In the tables of metric scores, we do not adjust productivity scores to account for fab size. For a general assessment, we define as large fabs those that make more than 7,000 wafer starts per week, medium fabs that make 2,500 - 7,000 wafer starts per week, and small fabs at less than 2,500 wafer starts per week. Large fabs lead almost every one of our labor and equipment productivity metrics, although fab size above 7,000 wafer starts per week does not improve performance. In the yield and defect density metrics, small and medium fabs are competitive with the large fabs.

Third, using older-generation processing equipment on newer process flows may make the achievement of world-class defect densities much more difficult than if newer equipment is used. While yields may be lower when employing older processing equipment, capital costs are lower as well, and so the strategy might turn out to be economically competitive or even superior to the strategy that employs solely new processing equipment. We made no attempt to adjust defect density scores for the generations of equipment applied.

With these strategic factors aside, we now summarize the various operational practices we found to be correlated with good manufacturing performance (in terms of the manufacturing metrics we have defined). We define eight basic themes for key practices that underlie leading performance. In short, these themes are:

1. Make manufacturing mistake-proof

2. Integrate process, equipment and product data, and analyze it statistically

3. Automate information handling and step-level material handling

4. Develop a problem-solving organization

5. Reduce the division of labor

6. Secure the requisite technical talent

7. Manage new process introductions

8. Schedule manufacturing activity

Proper execution of the very complex manufacturing process is essential. Some participants with a narrow product mix and very disciplined, well-trained operators achieve high line yields with little or no automation. But other leading participants have applied very effective forms of information automation that make manufacturing very mistake-proof. Such automation includes procedural checks that require the right production lot and the right machine to be selected before processing activity may be initiated, and automated download of the machine recipe (i.e., the processing parameters) to the processing machines.

Good process control systems do not make manufacturing strictly mistake-proof, but they serve to contain losses to minimal levels. All fabs in our survey apply SPC to their processes and equipment. The leading fabs make considerable use of sensors and computers to monitor equipment performance, and provide automated notification of out-of-control conditions and on-line assistance for trouble-shooting.

The leading fabs utilize computerized tracking systems to achieve excellent data collection and excellent data analysis capabilities. They collect large amounts of data concerning process and product conditions (an activity termed engineering data collection, or "EDC"), equipment maintenance and operation history, lot production history, and yield results. They integrate these data in a single relational database. Statistical tools are routinely applied to these data by process engineers, enabling them to expeditiously pinpoint causes of low die yields and make rapid deployment of counter-measures to contain losses.

The leading fabs rigorously measure the overall equipment efficiency (OEE) of their key processing equipment, identifying losses in throughput and prioritizing needed improvements. In the best fabs, equipment status is automatically captured from machine logs using SECS-II interfaces. Actual processing time is automatically monitored and compared against engineering standards; alarms are triggered when elapsed times are excessive.

Automation of information handling and step-level material reduces the overhead surrounding the performance of processing steps. Automation of information handling includes procedural checks and auto-recipe download as described above. It also includes automated capture of engineering data and equipment tracking data using bar codes and sensors, as well as automated notification of operators or technicians when machines are about to become idle or when they require maintenance or attention.

Material handling automation efforts may be divided into three types: interbay automation, intrabay automation, and step-level automation. Interbay automation concerns the movement of production lots between equipment bays using automated guided vehicles (AGVs) or overhead tracks to transport lots between stockers serving the bays. Intrabay automation concerns the movement of lots between stockers and processing machines in the bay using AGVs or traveling robot arms. Step-level automation involves the use of robot arms or tracks to handle wafers or cassettes of wafers between lot box and processing chamber, or between consecutive processing chambers. We find that step-level automation has the greatest positive impact on fab performance among our participants. For instance, fabs that have linked up coat, expose and develop steps in photolithography into a single automated sequence achieve higher yields and lower cycle times with no reduction of equipment throughput.

Fabs that have developed a strong problem-solving organization are very good at problem recognition, problem solving, and elimination of repetitive problems. Semiconductor manufacturing is characterized by immature processes and immature equipment, and by

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