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A REVIEW OF PRODUCTION PLANNING AND SCHEDULING MODELS IN THE SEMICONDUCTOR INDUSTRY PART I: SYSTEM CHARACTERISTICS, PERFORMANCE EVALUATION AND PRODUCTION PLANNING

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Although the national importance of the semiconductor industry is widely acknowledged, it is only recently that the production planning and scheduling problems encountered in this environment have begun to be addressed using industrial engineering and operations research techniques. These problems have several features that make them difficult and challenging: random yields and rework, complex product flows, and rapidly changing products and technologies. Hence their solution will contribute considerably to the theory and practice of production planning and control. In a two-part project we present a review of research in this area to date, discuss the applicability of the various approaches and suggest directions for future research. In this paper, Part I, we describe the characteristics of the semiconductor manufacturing environment and review models related to performance evaluation and production planning. Part II will review research on shop-floor control in this industry to date.

■ The miniaturization of electronic components by means of Very Large Scale Integration (VLSI) technologies has been one of the most significant technological developments of the last fifty years. Improving technologies and decreasing prices have led to integrated circuits appearing in all walks of life. The computer revolution of the past two decades is a direct result of the ability to develop and fabricate these components economically. The development of Computer-Integrated Manufacturing (CIM) systems, essential to the maintenance of competitive edge in today's highly competitive global markets, is directly linked to the availability of the integrated circuits necessary for their implementation. Integrated circuits are also used in a wide range of industries such as domestic appliances, cars and avionics. Although the industry is facing heavy competition from overseas, especially from the Pacific Rim countries, it is only recently that the operational aspects of semiconductor manufacturing have been addressed and attempts made to apply industrial engineering and operations research techniques to these problems.

The goal of this paper is to provide an overview of the semiconductor manufacturing process, its characteristics and management objectives and review research efforts in production planning and scheduling in this industry to date. We classify this work based on the problems addressed. The problem areas we consider are the following:

1. *Performance evaluation*. Models whose objective is descriptive rather than prescriptive in nature, used for understanding the behavior of a given system;

2. *Production planning*. Long-term, more aggregate production planning with a time horizon of months or weeks;

3. *Shop-floor control*, which addresses the questions of how much material to start into the facility and how to control the material once started.

Clearly, there are several applications that fit more than one of these categories. The literature on shop-floor control is further subclassified by the approaches used as input regulation and dispatching rules, deterministic scheduling algorithms, control-theoretic approaches and knowledge-based systems. The structure of this classification is shown in Figure 1. In this paper we discuss the manufacturing process and management objectives, and review performance evaluation and pro-

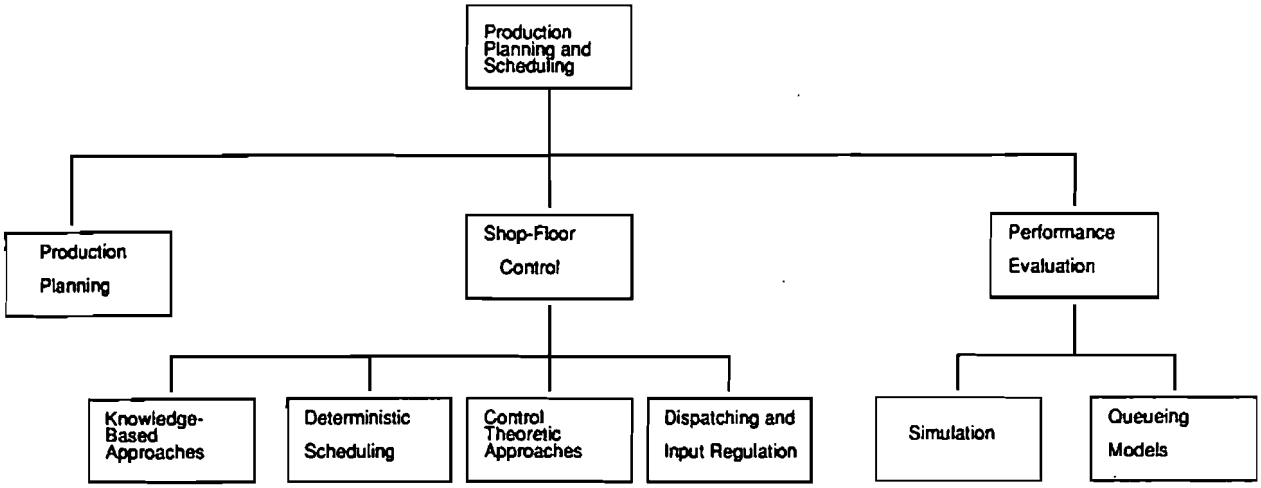

Figure 1. Classification of production planning and scheduling research

duction planning models. Research on shop-floor control problems is reviewed in Part II [69].

We have focused on production planning and scheduling applications in the semiconductor industry at the expense of other important areas such as product design and chip allocation [3], [35], [62], process modeling and improvement (e.g., [52]) and implementation of Just-in-Time manufacturing [49]. We have also not included the extensive literature on lot-sizing in the presence of random yields since a survey of this literature has already been carried out by Yano and Lee [76]. There is also a large body of industrial engineering and operations research literature which is relevant to the problems encountered in the semiconductor industry. In order to avoid diversifying into a survey of the entire area of production planning and scheduling, we shall not review this literature in detail but instead give references and discuss its relevance to problems in the semiconductor industry, with the hope of bringing them to the attention of practitioners and researchers. While we have made every effort to make this survey as comprehensive as possible within the above-mentioned limitations, it is highly likely that some contributions have been inadvertently omitted, for which we apologize in advance.

The Semiconductor Manufacturing Process

The process by which very large-scale integrated circuits are manufactured can be divided into four basic steps: wafer fabrication, wafer probe, assembly or packaging and final testing (Figure 2).

Wafer fabrication is the most technologically complex and capital intensive of all four phases. It involves the processing of wafers of silicon or gallium arsenide in order to build up the layers and patterns of metal and wafer material to produce the required circuitry. The number of operations can be well into the hundreds for a complex component such as a microprocessor. Many of these operations have to be performed in a clean-room environment to prevent particulate contamination of the wafers. The facility in which wafer fabrication takes place is referred to as a *wafer fab*. Product moves through the fab in lots, often of a constant size

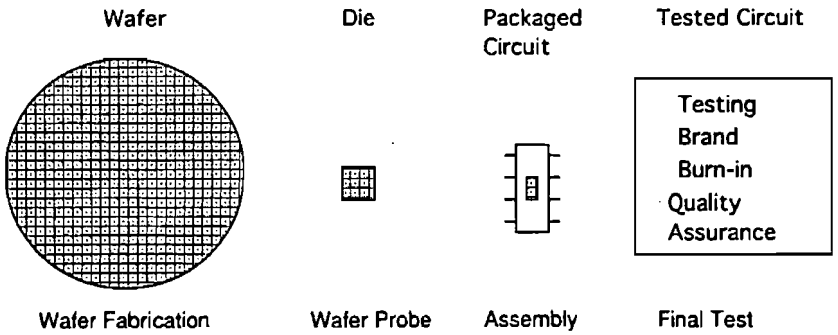

Figure 2. Basic steps of the semiconductor manufacturing process

based on standard containers used to transport wafers. While the specific operations may vary widely depending on the product and the technology in use, an idea of the processes in wafer fabrication can be seen in Figure 3 [14]. Brief descriptions of the various operations are given in the Appendix. This sequence of operations is repeated for each layer of circuitry on the wafer. Detailed descriptions of the technologies used in wafer fabrication can be found in texts on this subject such as Sze [68] and Runyan and Bean [60].

In wafer probe, the individual circuits, of which there may be hundreds on each wafer, are tested electrically by means of thin probes. Circuits that fail to meet specifications are marked with an ink dot. The wafers are then cut up into individual circuits and the defective circuits discarded.

Wafer fabrication and probe are generally referred to as "front-end" operations. The following stages, assembly and final test, are referred to as the "back-end."

In the back-end operations, lots may vary in size from several individual circuits to several thousand. The actual sequence of operations a lot will go through depends on the product and on customer specification. These characteristics are due to the fact that a lot is generally more closely associated with a particular order and customer than is the case in wafer fab or probe.

In assembly the circuits are placed in plastic or ceramic packages that protect them from the environment. There are many different types of packages, such as plastic or ceramic dual in-line packages, leadless chip carriers, and pin-grid arrays. Since it is possible for a given circuit to be packaged in many different ways, there is a great proliferation of product types at this stage. Once the leads have been attached and the package sealed and tested for leaks and other defects, the product is sent to final test.

The goal of the testing process is to ensure that customers receive a defect free product by using automated testing equipment to interrogate each integrated circuit and determine whether it is operating at the required specifications. While the specific product flow varies considerably, a broad idea can be formed from Figure 4. Brief descriptions of the main operations taking place in the testing area are given in the Appendix.

An important characteristic of the testing process from a production planning standpoint is the downgrading or binning that takes place here. A circuit, when tested, may not meet the specification it was originally built for, but may meet another less rigorous one. For example, a microprocessor intended to operate at 20MHz may fail at that frequency but may pass tests at 16MHz. Thus when a lot is tested a number of different grades of product may emerge, resulting in not enough of the desired product being available and unwanted inventory of the lower grade product. It is also possible to use inventory of higher-grade product to meet demand of a lower-grade product.

We can highlight the following factors that make production planning and scheduling in the semiconductor industry particularly difficult. Similar discussions can be found in Bai and Gershwin [4] and Hughes and Shott [36].

1. *Complex Product Flows*: The number of process steps is high, and a number of these steps take place on the same production equipment. For example, a wafer may have to visit the photolithography workstation eight or nine times to have all layers of circuitry fabricated. These product flows, where a lot visits a workcenter more than once, are known as reentrant product flows.

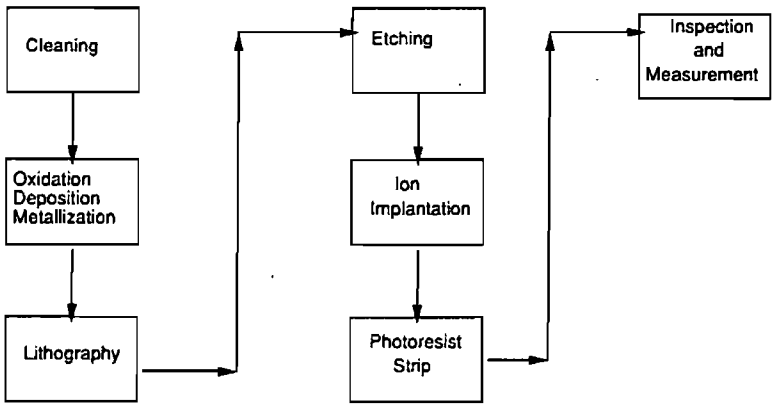

Figure 3. Basic operation sequence for wafer fabrication

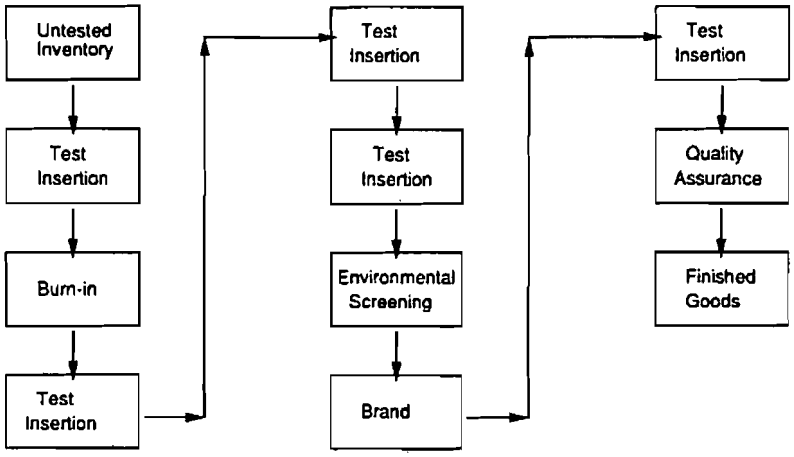

Figure 4. Example product flow through final testing facility

2. *Random Yields*: Process yields are uncertain and vary due to environmental conditions, problems with production equipment or material. In the testing stage there is also the issue of downgrading described above. Yields for well-established products may be predicted using historical data, but the constant introduction of new products and technologies makes yield estimation a major problem. Cunningham [18] provides a survey and comparison of statistical yield estimation models in use in industry. Another detrimental effect of yield problems is the large amount of engineering hold time on both lots and equipment while troubleshooting is in progress.

3. *Diverse Equipment Characteristics*: The characteristics of the equipment used in semiconductor manufacturing vary widely. Some machines have significant sequence-dependent setup times, while others do not. Some workcenters such as etching and burn-in consist of batch processing machines, where a number of lots are processed simultaneously as a batch. There are critical time windows between several processes, such as between burn-in and test where a lot has to be tested within 96 hours of leaving burn-in or repeat the entire burn-in sequence.

4. *Equipment Downtime*: The production equipment used in semiconductor manufacturing is technologically extremely sophisticated. It requires extensive preventive maintenance and calibration, and is still subject to unpredictable failures. It is estimated that the main cause of uncertainty in semiconductor manufacturing operations is due to unpredictable equipment downtime [34], [45], which is also cited as a major contributor to the cost advantage of overseas manufacturers.

5. *Production and Development in Shared Facilities*: Due to the constant development of new products and processes, very often the same equipment is used for both production lots and engineering test and qualification lots. The conflicting goals of the manufacturing and the engineering organizations add to the confusion.

6. *Data Availability and Maintenance*: The sheer volume of data in a semiconductor manufacturing facility makes data acquisition and maintenance an extremely time-consuming and difficult task. Sullivan and Fordyce [67] give the transaction volume in an IBM wafer fab as 240,000 per day. For each operation a product undergoes, information like processing times and yields has to be stored. The constant introduction of new product types to keep up with the changing markets further complicates this problem, which is also compounded as one moves from the front-end towards the final testing stages due to multiple packaging and co-production possibilities.

The main focus of manufacturing strategies in the semiconductor industry is on minimizing production costs and increasing productivity while improving both quality and delivery time performance. Major factors affecting costs are yield, labor, materials, inventory, equipment and facility depreciation and number of starts per week [36]. The major forces in the industry to date have been the manufacturers of standard products in fairly high volumes. In these operations, a common approach has been to buffer the wafer fabs against fluctuations in the external demand by holding inventories of probed die, referred to as die-bank inventories, between the front-end and back-end operations. Hence

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