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Paper 10
Entered: September 2, 2022

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

STMICROELECTRONICS, INC.
Petitioner,

v.

OCEAN SEMICONDUCTOR LLC,
Patent Owner.

IPR2022-00681
Patent 6,968,248 B1

Before MIRIAM L. QUINN, JOHN D. HAMANN, and DAVID COTTA, *Administrative Patent Judges.*

QUINN, *Administrative Patent Judge.*

DECISION
Granting Institution of *Inter Partes* Review
35 U.S.C. § 314
Granting Motion for Joinder
35 U.S.C § 315(c); 37 C.F.R. § 42.122

I. INTRODUCTION

Petitioner STMicroelectronics, Inc. ("Petitioner") filed a Petition requesting *inter partes* review of claims 1–22 of U.S. Patent No. 6,968,248 B1 ("the '248 patent"). Paper 1 ("Pet."). Petitioner also filed a Motion for Joinder seeking joinder as a petitioner with Applied Materials, Inc. in *Applied Materials, Inc v. Ocean Semiconductor LLC*, IPR2021-01342 (the "Applied Materials IPR"). Paper 3 ("Joinder Motion"). Ocean Semiconductor ("Patent Owner") filed a Preliminary Response. Paper 7 ("Prelim. Resp."). With authorization of the Board, Petitioner filed a Reply to Patent Owner's Preliminary Response. Paper 8 ("Reply"). And Patent Owner filed a Sur-Reply to Petitioner's Reply. Paper 9 ("Sur-Reply"). Patent Owner did not file an opposition to the Motion for Joinder.

We have authority under 35 U.S.C. § 314. Upon considering the information presented in the parties' papers, for reasons discussed below, we institute *inter partes* review of claims 1–22 of the '248 patent and grant Petitioner's Motion for Joinder.

A. Related Matters

The parties indicate that the '248 patent has been asserted in ten pending litigations: *Ocean Semiconductor LLC v. Analog Devices, Inc.*, No. 1:20-cv-12310 (D. Mass.); *Ocean Semiconductor LLC v. Infineon Techs. AG*, No. 1:20-cv-12311 (D. Mass.); *Ocean Semiconductor LLC v. Huawei Devices USA, Inc.*, No. 4:20-cv-991 (E.D. Tex.); *Ocean Semiconductor LLC v. MediaTek Inc.*, No. 6:20-cv-1210 (W.D. Tex.); *Ocean Semiconductor LLC v. NVIDIA Corp.*, No. 6:20-cv-1211 (W.D. Tex.); *Ocean Semiconductor LLC v. NXP Semiconductors N.V.*, No. 6:20-cv-1212 (W.D. Tex.); *Ocean Semiconductor LLC v. Renesas Electronics Corp.*, No. 6:20-cv-1213 (W.D. Tex.); *Ocean Semiconductor LLC v. Silicon*

Labs. Inc., No. 6:20-cv-1214 (W.D. Tex.); *Ocean Semiconductor LLC v. STMicroelectronics, Inc.*, No. 6:20-cv-1215 (W.D. Tex.); and *Ocean Semiconductor LLC v. Western Digital Techs., Inc.*, No. 6:20-cv-1216 (W.D. Tex.). Pet. 1–2; Paper 5 (Patent Owner's Mandatory Notices), 2. In addition, Petitioner has filed another petition for *inter partes* review (IPR2022-00680) of related patent U.S. Patent No. 6,907,305 B2. Pet 2.

B. The '248 Patent

The '248 patent relates to "scheduling in an automated manufacturing environment." Ex. 1001, 1:20–21. The '248 patent describes the manufacture of integrated circuits for modern semiconductor devices containing numerous structures or features, typically the size of a few micrometers. *Id.* at 1:38–41. The '248 patent further describes that the fabrication of integrated circuits generally involves processing a number of wafers through a series of fabrication tools, where layers of material are added to, removed from, and/or treated on a semiconducting substrate. *Id.* at 1:41–45. According to the '248 patent, controlling a semiconductor factory ("fab") that fabricates such integrated circuits is a challenging task, where the fab is a complex environment where numerous parts (typically 40,000 wafers or more) and numerous part types (typically 100 part types or more) are simultaneously being manufactured. *Id.* at 1:65–2:3. As each wafer moves through the fab, it may undergo more than 300 processing steps, many of which use the same machines, where a large factory may contain approximately 500 computer-controlled machines to perform this wafer processing. *Id.* at 2:3–8. As described in the '248 patent, routing, scheduling, and tracking material through the fab is a difficult and complicated task, even with the assistance of a computerized factory control system. *Id.* at 2:8–11.

Figure 3 illustrates an implementation of reactive scheduling of activities of a process flow for a semiconductor fabrication facility and is reproduced below.

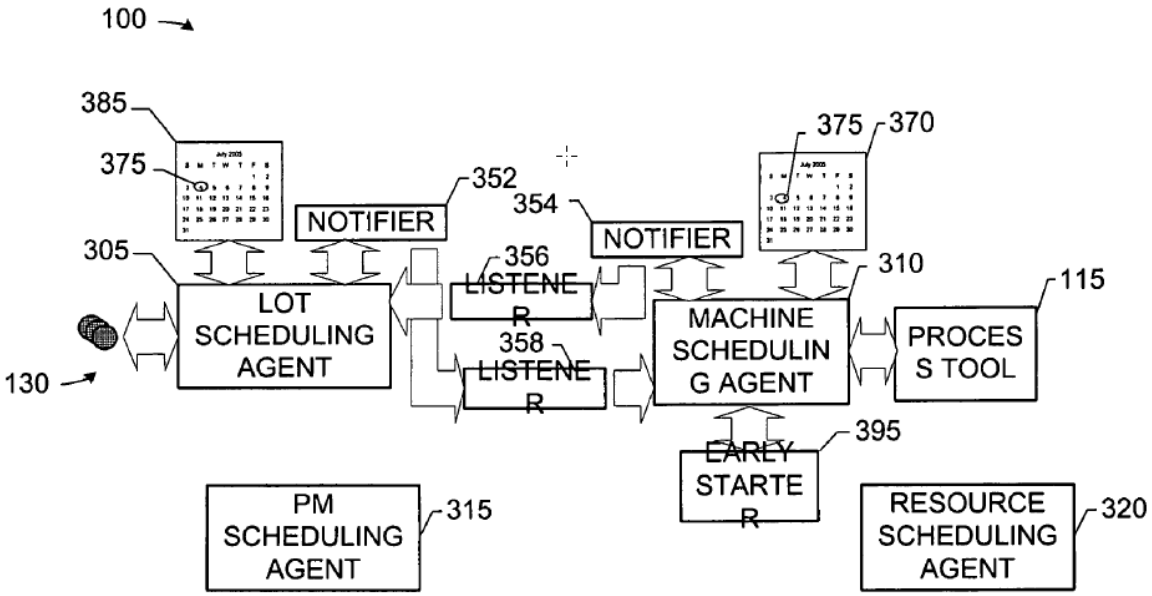

FIG. 3

Figure 3 shows a portion of process flow 100 from a semiconductor fabrication facility, and the manner in which it schedules appointments for the consumption of resources. *Id.* at 4:28–32. Process flow 100 includes stations 105, each station 105 including computing device 110 communicating with process tool 115. *Id.* at 5:17–19. Process tools 115 are processing lots 130 of wafers 135 that will eventually become integrated circuit devices, where process tool 115 may be a fabrication tool used to fabricate some portion of wafers 135. *Id.* at 5:24–26, 6:43–45.

Each computing device 110 includes software agent 265, where software agents 265, collectively, are responsible for efficiently scheduling and controlling lots 130 of wafers 135 through the fabrication process. *Id.* at 6:24–26, 47–50. Collectively, software agents 265 reactively and

proactively schedule activities for each lot 130 for operations on a specific qualified process tool 115. *Id.* at 6:63–7:3. More specifically, the software agents (or scheduling agents) 265 include: Lot Scheduling Agent ("LSA") 305 that schedules activities on behalf of lots 130 of wafers 135; Machine Scheduling Agent ("MSA") 310 that schedules activities on behalf of process tools 115; PM Scheduling Agent ("PMSA") 315 that schedules activities on behalf of preventative maintenance ("PMs") and equipment qualification ("Quals") (not shown in Figure 3); and Resource Scheduling Agent ("RSA") that schedules activities on behalf of resources (not shown in Figure 3). *Id.* at 7:20–30. Some of these activities are scheduled reactively (i.e., in response to events occurring in process flow 100). *Id.* at 7:36–37. For example, the '248 patent describes the process as detecting an occurrence of a predetermined event in the process flow 100; notifying a subscribing software scheduling agent (e.g., LSA 305, MSA 310, PMAS 315, or RSA 320) of the occurrence; and reactively scheduling an action responsive to the detection of the predetermined event. *Id.* at 7:38–46.

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