United States District Court
EASTERN DISTRICT OF TEXAS
SHERMAN DIVISION

OCEAN SEMICONDUCTOR LLC, *Plaintiff,* v. HUAWEI DEVICE USA, INC., HUAWEI DEVICE CO., LTD., AND HISILICON TECHNOLOGIES CO., LTD., *Defendants*.	§ § § § § § § § § § §	Civil Action No. 4:20-CV-00991-ALM

CLAIM CONSTRUCTION MEMORANDUM AND ORDER

Before the Court are Plaintiff Ocean Semiconductor LLC's ("Plaintiff" or "Ocean") Opening Claim Construction Brief (Dkt. #26), Defendants Huawei Device USA, Inc., Huawei Device Co., Ltd., and HiSilicon Technologies Co., Ltd's ("Defendants" or collectively "Huawei") Responsive Claim Construction Brief (Dkt. #33), and Plaintiff's Reply Claim Construction Brief (Dkt. #34).[1] Also before the Court is the parties' December 23, 2021 Joint Claim Construction and Prehearing Statement (Dkt. #36). The Court held a claim construction hearing on January 14, 2022, to determine the proper construction of the disputed claim terms in U.S. Pat. No. 6,660,651 ("the '651 Patent"), U.S. Pat. No. 7,080,330 ("the '330 Patent"), U.S. Pat. No. 6,725,402 ("the '402 Patent"), U.S. Pat. No. 8,676,538 ("the '538 Patent"), U.S. Pat. No. 6,836,691 ("the '691 Patent"), U.S. Pat. No. 6,907,305 ("the '305 Patent"), and U.S. Pat. No. 6,968,248 ("the '248 Patent") (collectively, "the Asserted Patents").

The Court issues this Claim Construction Memorandum Opinion and Order and hereby

[1] Citations to the parties' filings are to the filing's number in the docket (Dkt. #) and pin cites are to the page numbers assigned through ECF.

incorporates-by-reference the claim construction hearing and transcript. For the following reasons, the Court provides the constructions set forth below.

I. BACKGROUND

Plaintiff asserts seven patents against Defendants. In general, the Asserted Patents relate to technologies supporting semiconductor manufacturing operations. Shortly before the start of the January 14, 2022 hearing, the Court provided the parties with preliminary constructions with the aim of focusing the parties' arguments and facilitating discussion.

The '651 Patent, titled "Adjustable Wafer Stage, and a Method and System for Performing Process Operations Using Same," issued on December 9, 2003, and was filed on November 8, 2001. The '651 Patent generally relates "to semiconductor fabrication technology, and, more particularly, to an adjustable wafer stage, and a method and system for performing process operations using same." '651 Patent at 1:8–11. The Abstract of the '651 Patent states:

> A process tool comprised of an adjustable wafer stage and various methods and systems for performing process operations using same is disclosed herein. In one illustrative embodiment, the process tool is comprised of a process chamber, and an adjustable wafer stage in the process chamber to receive a wafer positioned thereabove, the wafer stage having a surface that is adapted to be raised, lowered or tilted. In further embodiments, the process tool further comprises at least three pneumatic cylinders or at least three rack and pinion combinations, each of which are operatively coupled to the wafer stage by a ball and socket connection. A system disclosed herein is comprised of a metrology tool for measuring a plurality of wafers processed in a process tool to determine across-wafer variations produced by the process tool, a process tool comprised of an adjustable wafer stage that has a surface adapted to receive a wafer to be processed in the tool, and a controller for adjusting a plane of the surface of the wafer stage based upon the determined across-wafer variations produced by the tool, whereby the process tool processes at least one subsequently processed wafer positioned on the wafer stage after the plane of the surface of the wafer stage has been adjusted.

Claim 19 of the '651 Patent is an illustrative claim and recites the following elements (disputed terms in italics):

19. A method, comprising:
providing a *process chamber* comprised of a wafer stage, said wafer stage having a surface that is adjustable;
adjusting said surface of said wafer stage by actuating at least one of a plurality of *pneumatic cylinders* that are operatively coupled to said wafer stage to accomplish at least one of raising, lowering and varying a tilt of said surface of said wafer stage;
positioning a wafer on said wafer stage; and
performing a process operation on said wafer positioned on said wafer stage.

The '330 Patent, titled "Concurrent Measurement of Critical Dimension and Overlay in Semiconductor Manufacturing," issued on July 18, 2006, and was filed on March 5, 2003. The '330 Patent generally relates "to monitoring and/or controlling a semiconductor fabrication process, and in particular to a system and methodology for concurrently measuring critical dimensions and overlay during the fabrication process and controlling operating parameters to refine the process in response to the measurements." '330 Patent at 1:6–12. The Abstract of the '330 Patent states:

> A system and methodology are disclosed for monitoring and controlling a semiconductor fabrication process. One or more structures formed on a wafer matriculating through the process facilitate concurrent measurement of critical dimensions and overlay via scatterometry or a scanning electron microscope (SEM). The concurrent measurements mitigate fabrication inefficiencies, thereby reducing time and real estate required for the fabrication process. The measurements can be utilized to generate feedback and/or feed-forward data to selectively control one or more fabrication components and/or operating parameters associated therewith to achieve desired critical dimensions and to mitigate overlay error.

Claim 19 of the '330 Patent is an illustrative claim and recites the following elements (disputed term in italics):

19. A method for monitoring and controlling a semiconductor fabrication process comprising:
providing a plurality of wafers undergoing the fabrication process;

mapping the plurality of wafers into one or more logical grids comprising one or more portions in which a grating structure for use in concurrent measurements is formed;

concurrently measuring one or more critical dimensions and overlay in a wafer undergoing the fabrication process; determining if one or more of the critical dimensions are outside of acceptable tolerances;

determining whether an overlay error is occurring;

developing control data based upon one or more concurrent measurements when at least one of an overlay error is occurring and one or more of the critical dimensions fall outside of acceptable tolerances; and

feeding forward or backward the control data to adjust one or more fabrication components or one or more operating parameters associated with the fabrication components when at least one of an overlay error is occurring and one or more of the critical dimensions fall outside of acceptable tolerances to mitigate overlay error and/or to bring critical dimension within acceptable tolerances.

The '402 Patent, titled "Method and Apparatus for Fault Detection of a Processing Tool and Control Thereof Using an Advanced Process Control (APC) Framework," issued on April 20, 2004, and was filed on July 31, 2000. The '402 Patent generally relates "to semiconductor fabrication technology, and, more particularly, to a method and apparatus for fault detection and control of a processing tool using an Advanced Process Control (APC) framework." '402 Patent at 1:9–12. The Abstract of the '402 Patent states:

> A method and apparatus for providing fault detection in an Advanced Process Control (APC) framework. A first interface receives operational state data of a processing tool related to the manufacture of a processing piece. The state data is sent from the first interface to a fault detection unit. A fault detection unit determines if a fault condition exists with the processing tool based upon the state data. A predetermined action is performed on the processing tool in response to the presence of a fault condition. In accordance with one embodiment, the predetermined action is to shutdown the processing tool so as to prevent further production of faulty wafers.

Claim 1 of the '402 Patent is an illustrative claim and recites the following elements (disputed term in italics):

1.A method comprising:

receiving at a first interface operational state data of a processing tool related to the manufacture of a processing piece;
sending the state data from the first interface to a fault detection unit, wherein the act of sending comprises: sending the state data from the first interface to a data collection unit;
accumulating the state data at the data collection unit; translating the state data from a first communications protocol to a second communications protocol compatible with the fault detection unit; and sending the translated state data from the data collection unit to the fault detection unit; determining if a fault condition exists with the processing tool based upon the state data received by the fault detection unit;
performing a predetermined action on the processing tool in response to the presence of a fault condition; and
sending an alarm signal indicative of the fault condition to an *advanced process control framework* from the fault detection unit providing that a fault condition of the processing tool was determined by the fault detection unit,
wherein performing a predetermined action further comprises sending a signal by the framework to the first interface reflective of the predetermined action.

The '538 Patent, titled "Adjusting Weighting of a Parameter Relating to Fault Detection Based on a Detected Fault," issued on March 18, 2014, and was filed on November 2, 2004. The '538 Patent generally relates "to semiconductor manufacturing, and, more particularly, to a method, system, and apparatus for performing a process to improve fault detection reliability through feedback." '538 Patent at 1:9–12. The Abstract of the '538 Patent states:

> A method, apparatus and a system, for provided for performing a dynamic weighting technique for performing fault detection. The method comprises processing a workpiece and performing a fault detection analysis relating to the processing of the workpiece. The method further comprises determining a relationship of a parameter relating to the fault detection analysis to a detected fault and adjusting a weighting associated with the parameter based upon the relationship of the parameter to the detected fault.

Claims 1 and 5 of the '538 Patent is an illustrative claim and recites the following elements (disputed term in italics):

1.A method, comprising:
performing in a computer a fault detection analysis relating to processing of a workpiece;

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