UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

APPLIED MATERIALS, INC.,

Petitioner

v.

OCEAN SEMICONDUCTOR LLC,

Patent Owner

IPR2021-01342
U.S. Patent No. 6,968,248

DECLARATION OF KURT D. HUMPHREY

Mail Stop PATENT BOARD
Patent Trial and Appeal Board
US Patent and Trademark Office
P.O. Box 1450
Alexandria, VA 22313-1450

I. INTRODUCTION

1. My name is Kurt D. Humphrey and I have been retained by Plaintiff Ocean Semiconductor LLC ("Ocean" or "Plaintiff") as an expert witness in the above- IPR2021-01342 brought by Applied Materials, Inc. ("Applied Materials" or "Petitioner") before the Patent Trial and Appeals Board ("PTAB") of the United States Patent and Trademark Office.

2. I make this declaration in support of Patent Owner Ocean Semiconductor LLC's ("Ocean") Patent Owner's Response to the Petition in IPR2021-01342.

3. This report contains statements of my opinions formed to date regarding U.S. Patent No. 6,968,248 ("'248 patent") and the bases and reasons for those opinions. I may offer additional opinions based on further review of materials in this case, including opinions and/or testimony of other expert witnesses.

4. I reserve the right to revise, supplement, and/or amend my opinions in this declaration based on future positions taken by Petitioner and/or their experts, additional documents, testimony, or other information provided by Petitioner or its witnesses, any orders from the Board, or as I may otherwise find necessary and to offer rebuttal analyses and/or opinions to any such positions of the Petitioner.

5. My educational and professional background, patents, and professional association memberships are listed in my curriculum vitae. (Ex. 2042.)

II. QUALIFICATIONS

6. Based on the following qualifications and experience, I believe I am qualified to offer opinions as to whether or not the challenged claims of the ’248 patent would have been obvious to one of ordinary skill in the art at the filing date of the ’248 patent.

7. I have more than 40 years of experience in all phases of design and implementation of electronic devices, including over 30 years of experience in the design and implementation of computer semiconductor devices. My work has focused on the development, integration, and optimization of new processes and circuits into one final work product and introducing it to production.

8. I received a Bachelor of Science degree in Ceramic Engineering from the University of Missouri. I then accepted a Product Development engineering position with General Motors’ AC Spark Plug division in 1978, where I received the General Motors Graduate Study Fellowship. I received my Master of Science degree in Ceramic Engineering from the University of Missouri in 1980.

9. Between 1980 and 1983, I was a Process Development Engineer at Delco Electronics Div. General Motors. During that time, I evaluated external silicon wafer suppliers while also introducing intrinsic-gettered substrates into MOS fabrication, resulting in an average 7% increase in die yield across all devices.

10. I worked for AT&T Technologies from 1983 through 1986 as a Process Engineering and Yield Enhancement Manager. During that time, I contributed to

the successful start up of new 125 mm high volume memory fabrication facility. I also coordinated DRAM process transfer from research and development to fab, and directed yield enhancement activities for 256k DRAM production for a new 125mm line.

11. After leaving AT&T in 1986, I worked for Philips Research Labs in Eindhoven, The Netherlands from 1986 through 1989 as a Process Integration Manager for CMOS processes. During my employment at Philips Research Labs, I served as Sub-micron Process Integration Manager and directed the development of a state of the art 0.7µ CMOS process from research and development through final product qualification. I also developed the first sub-micron CMOS process utilizing retro-wells, suppressed-BB LOCOS, salicide with TiSi2 local interconnect, W plugs, and I-line lithography.

12. My work with CMOS processes continued after leaving Philips Research Labs, when I became the Process Integration Manger at United Technologies Microelectronics Center, United Technologies Corp. from 1989 through 1995. There, I directed next-generation CMOS and bipolar process technology development projects, incluging ACUTE (advanced dielectrically-isolated, complementary bipolar linear array process on SOI), UTERPROG (radiation-hardened 1.0µ CMOS process technology utilizing vertical amorphous Si antifuses), and UTERTLM (1.0µ triple-level metal, rad-hard CMOS). I also developed advanced amorphous silicon metal-to-metal antifuse technology to

support 256k RHPROM and RHPAL field programmable products, and developed novel deep trench-isolated, complementary bipolar SOI process.

13. I next worked for Rockwell Semiconductor Systems (a.k.a. Conexant Systems) in multiple areas between 1995 and 1999. While at Rockwell, I managed process integration and advanced process development. I demonstrated first fully-functional Trench IGBTs and silicon MEMS gyros using 125mm substrates and authored 3 MEMS and 1 SAW filter disclosures. I also successfully completed comprehensive STI and 90nm CMOS process development test chips in record time to support an aggressive 90nm qualification schedule. As the Advanced Process Development Manager, my primary focus was state-of-the-art semiconductor products. I coordinated design rules, mask/reticle specifications, test chip design/layout, process qualification and transfer to production for 90nm CMOS process development in Rockwell's Advanced Process Technology (APT) department in Newport Beach.

14. After leaving Rockwell, I worked for TAEUS International Corp. as the Director for Engineering Services between 1999 and 2005. During this time, I managed patent evaluation and reverse engineering projects from the initial proposal through project completion and final review stages. I served as a primary technical contributor/SME on wireless telecom/networking standards, including 802.11, Bluetooth and 3G/4G cellular and associated SEPs, optical networking and opto-electronic/photonics components, e.g. solid state DFB/quantum well lasers,

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