intel

Intel486™ FAMILY OF MICROPROCESSORS
LOW POWER VERSION
DATA SHEET

Low Power Intel486™ SX CPU/Intel487™ SX MCP
Low Power Intel486 DX CPU

- **Lower Power Dissipation**
  - **— Dynamic Frequency Scalability**
  - **— I_{CC}(max) Reduced to 150 mA at 2 MHz**
  - **— Improved V_{CC} Rating (± 10%)**
- **Binary Compatible with Large Software Base**
  - **— MS-DOS*, OS/2**, Windows***
  - **— UNIX*** System V/386**
  - **— iRMX®, iRMK Kernels**
- **High Integration Enables On-Chip**
  - **— 8 KByte Code and Data Cache**
  - **— Floating Point Unit on the Intel486 DX CPU and Intel487™ SX Math CoProcessor**
  - **— Paged, Virtual Memory Management**
- **Easy to Use**
  - **— Built-In Self Test**
  - **— Hardware Debugging Support**
  - **— Intel Software Support**
  - **— Extensive Third Party Software Support**
- **168-Lead Pin Grid Array Package for Intel486 DX Microprocessor**
- **168-Lead Pin Grid Array for Intel486™ SX Microprocessor**
- **196-Lead Plastic Quad Flat Package for Intel486™ SX Microprocessor**
- **169-Pin Grid Array Package for Intel487™ SX Math CoProcessor**
- **High Performance Design**
  - **— Intel486™ One Clock Instruction Core**
  - **— 16/20/25 MHz Operation for Intel486™ SX**
  - **— 25 MHz Operation for Intel486™ DX**
  - **— 64 MByte/Sec Burst Bus**
  - **— CHMOS IV Process Technology**
  - **— Dynamic Bus Sizing for 8-, 16- and 32-Bit Buses**
- **Complete 32-Bit Architecture**
  - **— Address and Data Buses**
  - **— Registers**
  - **— 8-, 16- and 32-Bit Data Types**
- **Multiprocessor Support**
  - **— Multiprocessor Instructions**
  - **— Cache Consistency Protocols**
  - **— Support for Second Level Cache**

The data sheet describes both the Low Power Intel486 SX and the Low Power Intel486 DX microprocessors. The Intel487 SX Math CoProcessor will support the low power Intel486 SX microprocessor as an optional upgrade available through the retail channel.

The Low Power Intel486 family microprocessors meet today's need for high performance portables. Their combination of special features like dynamic frequency scaling, lower minimum frequency, improved V_{CC} operation and high integration contribute significantly to lower power dissipation and meet the needs of portable computing.

The Low Power capability is achieved by operating the Intel486 microprocessor in the 2X mode. The frequency can be varied dynamically between maximum to minimum as needed. The frequency change does not affect contents of the registers and data integrity is maintained. Power dissipation is reduced significantly at 2 MHz where I_{CC} is only 150 mA compared to 600 mA at 20 MHz. Low power versions are offered for both the Intel486 SX and the Intel486 DX microprocessors.

The Low Power Intel486 microprocessors are 100-percent compatible with all versions of the Intel386™ microprocessor family, assuring compatibility with the more than $40 billion software base of MS-DOS, Windows, OS/2 and UNIX/System operating system applications. The Low Power Intel486 microprocessor integrates the same RISC-technology, one clock per instruction integer core, on-chip cache, and memory management unit as the standard Intel486 microprocessor.

The Intel487 SX Math CoProcessor provides optional math upgrade capability for the Intel486 SX microprocessor and supports low power operation; providing end-users increased floating point performance for more than 2100 software packages that were designed to use Intel Math CoProcessors. Note that the Intel OverDrive™ Processor does not work in systems based on the Low Power Intel486 CPU.

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**OS/2 is a trademark of International Business Machines.
***UNIX is a trademark of UNIX Systems Laboratories.

December 1992
Order Number: 241199-002

Intel486™ Family of Microprocessors
Low Power Version
Data Sheet

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This document should be used in conjunction with the Intel486™ DX Microprocessor data sheet (order number 240440-004, June 1991) and the Intel486™ SX Microprocessor data sheet (order number 240950-002, October 1991).

1.0 INTRODUCTION

The Low Power Intel486 microprocessor brings Intel486 technology and performance to the portable computer market. The low power capability is achieved by a frequency scalability feature during normal operation. The operating frequency can be brought down dynamically resulting in lower power supply current (I_{CC}). This results in minimal power dissipation which ensures a longer battery life.

The Low Power Intel486 microprocessor integrates the same RISC-technology, one clock per instruction integer core, on-chip cache, and memory management unit as the standard Intel486 microprocessor.

The Low Power Intel486 microprocessor has the following special features:

- **Frequency Scalability**—This is achieved by operating the Intel486 microprocessor in the 2X clock mode. The frequency can be varied dynamically from maximum back to minimum or vice versa. The frequency change does not affect the register content of the CPU, thus data integrity is maintained.
- **Lower Minimum Frequency**—The Low Power Intel486 microprocessor can be operated at a minimum frequency of 2 MHz, at which I_{CC}(max) is only 150 mA, compared to an I_{CC}(max) of 600 mA at 20 MHz operation. The power dissipation is thus drastically reduced ensuring a longer battery life.
- **Improved V_{CC} Operation**—The Low Power Intel486 microprocessor has an improved V_{CC} rating of ±10%. Again this feature makes it extremely attractive to portable battery powered applications.

The above three features ensure power savings for portable computer systems resulting in prolonged battery life.

Besides the above special features, the Low Power Intel486 microprocessor has an identical feature set to the standard Intel486 CPU. This includes:

- **Binary Compatibility**—The Low Power Intel486 CPU is binary compatible with the 8086, 8088, 80186, 80286, i386™ SX, i386™ DX, Intel486™ SX and Intel486™ DX CPUs.
- **Full 32-Bit Integer Processor**—The Low Power Intel486 CPU performs a complete set of arithmetic and logical operations on 8-, 16-, and 32-bit data types using a full-width ALU and eight general-purpose registers.
- **Separate 32-Bit Address and Data Paths**—Four gigabytes of physical memory can be addressed directly.
- **Single-Cycle Execution**—Many instructions execute in a single clock cycle.
- **On-Chip Floating Point Unit**—This is available on the Intel486 DX CPU. The 32-, 64-, and 80-bit formats specified in IEEE standard 754 are supported. The unit is binary compatible with the 8087, 80287, i387™, i387™ SX, and Intel487™ math coprocessors and the Intel486™ CPU.
- **On-Chip Memory Management Unit**—Address-management and memory-space protection mechanisms maintain the integrity of memory. This is necessary in multitasking and virtual-memory environments, like those implemented by the UNIX and OS/2 operating systems. Both memory segmentation and paging are supported.
- **On-Chip Cache with Cache Consistency Support**—The internal write-through cache can hold 8 KBytes of data or instructions. Cache hits are as fast as read accesses to a processor register. Bus activity is tracked to detect alterations in the memory which internal cache represents. The internal cache can be invalidated or flushed, so that an external cache controller can maintain cache consistency in multi-processor environments.
- **External Cache Control**—Write-back and flush controls over an external cache are provided so that the processor can maintain cache consistency in multi-processor environments.
- **Instruction Pipelining**—The fetching, decoding, execution and address translation of instructions are overlaped within the Low Power Intel486 microprocessor. This results in a continuous execution rate of one clock cycle per instruction, for most instructions.
- **Burst Cycles**—Burst transfers allow a new doubleword to be read from memory each clock cycle. With this capability the internal cache and instruction prefetch buffer can be filled very rapidly.
- **Write Buffers**—The processor contains write buffers to enhance the performance of consecutive writes to memory. The Low Power Intel486 CPU can continue operations internally after a write, without waiting for the write to be executed on the external bus.
- **Bus Backoff**—If another bus master needs control of the bus during a Low Power Intel486 microprocessor initiated bus cycle, the Low Power

Intel486 microprocessor will float its bus signals, then restart its cycle when the bus becomes available again.

- **Instruction Restart**—Programs can continue execution following an exception generated by an unsuccessful attempt to access memory. This feature is important for supporting demand-paged virtual memory applications.
- **Dynamic Bus Sizing**—External controllers can dynamically alter the effective width of the data bus. Bus widths of 8, 16 or 32 bits can be used.

1.1 Pinout

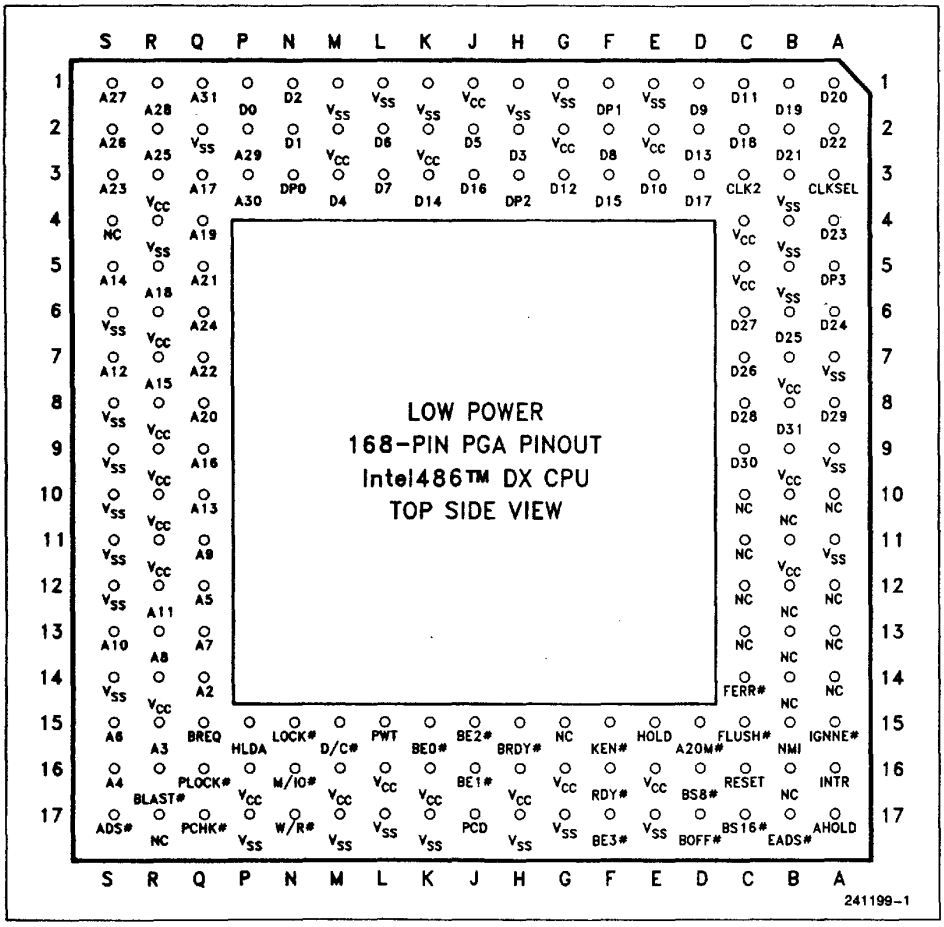

Figure 1-1. Low Power Intel486™ DX CPU Pinout (Top Side View)

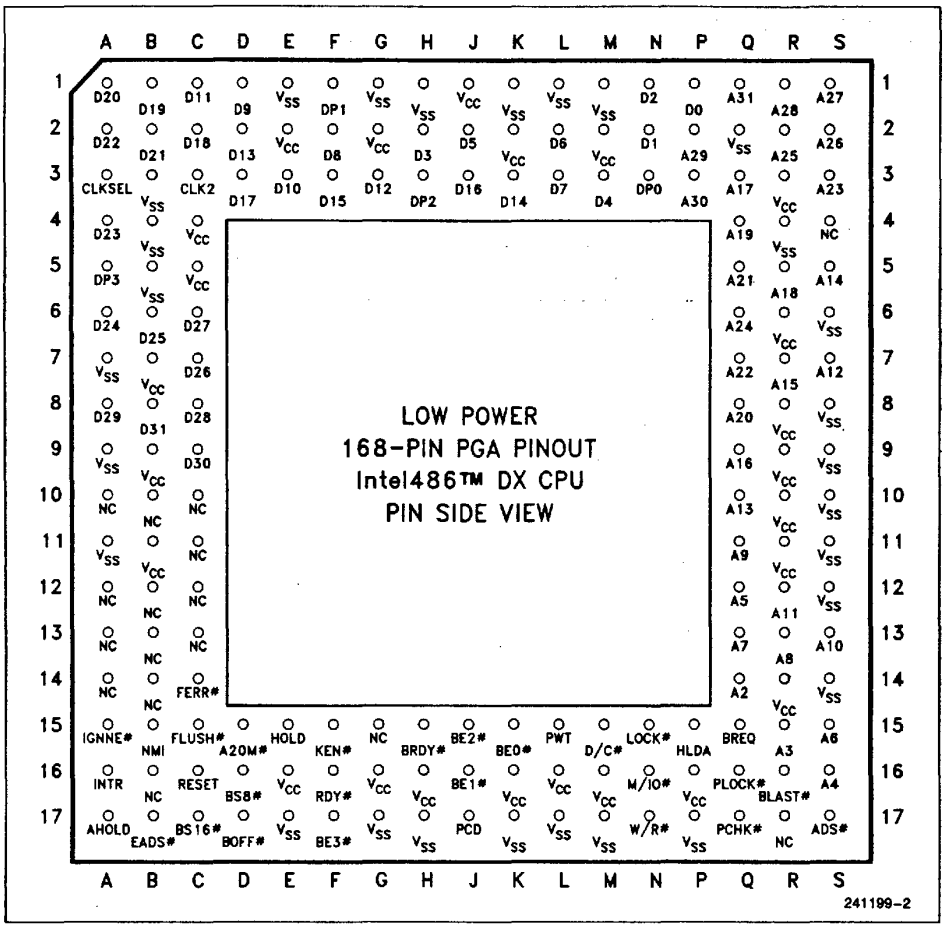

Figure 1-2. Low Power Intel486™ DX CPU Pinout (Pin Side View)

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