18351 U.S. PTO

082107

U.S. PTO
11/894991
08/21/2007

Attorney Docket No.: TRAN-P470

# IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

| I hereby certify that this transmittal of the below described documents is being deposited with the United States Postal Service in an envelope bearing Express Mail Postage and an Express Mail label, with the below serial number, addressed to the Commissioner for Patents P.O. Box 1450 Alexandria, VA 22313-1450, on the below date of deposit. | | | |
|---|---|---|---|
| Express Mail Label No.: | EM061752383US | Name of Person Making the Deposit: | Anthony Chou |
| Date of Deposit: | 08/21/2007 | Signature of the Person Making the Deposit: | Anthony Chou |

Inventor(s): Andrew Read, Sameer Halapete, Keith Klayman

Title: SAVING POWER WHEN IN OR TRANSITIONING TO A STATIC MODE OF A PROCESSOR

This is a request for filing a Divisional application under 37 CFR 1.53(b), of pending prior application Application No. 09/694,433 filed on 10/23/2000

of Andrew Read, Sameer Halapete, Keith Klayman
*Inventor(s)*

for SAVING POWER WHEN IN OR TRANSITIONING TO A STATIC MODE OF A PROCESSOR
*Title of invention*

Examiner: Art Unit:

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

## TRANSMITTAL OF FILING UNDER 37 CFR 1.53(b) APPLICATION ELEMENTS

[ ] Application claims small entity status (if applicable) *37 CFR 1.27.*

[ X ] Specification [Total Pages 21 ]

[ X ] Drawings *(35 U.S.C. 113)* [Total Sheets 2 ]

[ X ] Oath or Declaration [Total Sheets 2 ]

[ ] Newly executed (original or copy)
[ X ] A copy from a prior application *(37 CFR 1.63 (d))*

[ ] DELETION OF INVENTOR(S)
Signed statement attached deleting inventor(s) name in the prior application, *see 37 CFR 1.63 (d)(2) and 1.33(b)*

[ X ] Power of Attorney

## ACCOMPANYING APPLICATION PARTS

[ ] Assignment Papers (cover sheet & document(s))

Name of Assignee Transmeta Corporation

[ ] 37 CFR 3.73 (b) Statement (when there is an assignee)

[ ] English Translation Document (if applicable)

[ ] Information Disclosure Statement (PTO/SB/08 or PTO-1449)
[ ] Copies of citations attached

[ ] Preliminary Amendment

[ X ] Return Receipt Postcard (MPEP 503)
(Should be specifically itemized)

[ ] Certified Copy of Priority Document(s)
(if foreign priority is claimed)

[ X ] Nonpublication Request under 35 U.S.C. 122 (b)(2)(B)(i).
Applicant must attach form PTO/SB/35 or equivalent.

[ X ] Other: Power of Attorney by Assignee of Entire Interest (Revocation of Prior Powers) documents are included.

**Petition for Suspension of Prosecution for the Time Necessary to File an Amendment**

[ ] There is provided herewith a Petition To Suspend Prosecution For The Time Necessary to File An Amendment (New Application Filed Concurrently).

**Priority Claim**

**35 U.S.C. 119**

[ ] Priority of Application Number _____ filed on _____ in _____ is claimed under 35 U.S.C. 119.

[ ] The certified copy has been filed in prior U.S. Application No. _____ in _____

[ ] The certified copy will follow.

**35 U.S.C. 120, 121 and 365(c)**

"This application is a divisional and claims the benefit of copending application(s)

[X] application number 09/694,433 filed on 10/23/2000

[ ] International Application _____ filed on _____

which designated the U.S."

**Inventorship Statement**

(a) With respect to prior copending U.S. application from which this application claims benefit under 35 USC 120 the inventor(s) in this application are:

[X] the same.

[ ] less than those named in the prior application. It is requested that the following inventor(s) identified above for the prior application be deleted:

_____
*Type names of inventors to be deleted*

(b) The inventorship for all the claims in this application are

[X] the same.
[ ] not the same. And an explanation, including the ownership of the various claims at the time the last claimed invention was made, is submitted.

### Maintenance of Codependency of Prior Application

[ ] A petition, fee and response has been filed to extend the term pending prior application until .....
[ ] A copy of the petition for extension of time in the prior application is attached.

### Conditional Petition for Extension of Time in Prior Application

[X] A conditional petition for extension of time is being filed in the pending parent application.
[X] A copy of the conditional petition for extension of time in the prior application is attached

### Abandonment of Prior Application *(if applicable)*

[ ] Please abandon the prior application at a time while the prior application is pending or when the petition for extension of time or to revive in that application is granted and when this application is granted a filing date so as to make this application copending with said prior application.

### Notification in Parent Application of the Filing of This Divisional Application

[X] A notification of the filing of this divisional is being filed in the parent application from which this application claims priority under 35 USC § 120.

**FEE CALCULATION**

**1. BASIC FILING, SEARCH, AND EXAMINATION FEES**

| | Filing Fees | Search Fees | | Examination Fees | | | |
|---|---|---|---|---|---|---|---|
| | | Small Entity | | Small Entity | | Small Entity | |
| Application Type | Fee ($) | Fee ($) | Fee ($) | Fee ($) | Fee ($) | Fee ($) | Fees Paid ($) |
| Utility | 300 | 150 | 500 | 250 | 200 | 100 | $1,000.00 |
| Design | 200 | 100 | 100 | 50 | 130 | 65 | $ |
| Plant | 200 | 100 | 300 | 150 | 160 | 80 | $ |
| Reissue | 300 | 150 | 500 | 250 | 600 | 300 | $ |
| Provisional | 200 | 100 | | | | | $ |

**2. EXCESS CLAIM FEES**

| Fee Description | Small Entity Fee ($) | Fee ($) |
|---|---|---|
| Each claim over 20 or, for Reissues, each claim over 20 and more than in the original patent | 50 | 25 |
| Each independent claim over 3 or, for reissues, each independent claim more than in the original patent | 200 | 100 |

Multiple dependent claims 360 180

| Total Claims | | Extra Claims | Fee ($) | Fee Paid ($) | Multiple Dependent Claims | |
|---|---|---|---|---|---|---|
| 19 | minus 20 | 0 | x $50.00 | $0.00 | | |
| | HP = highest number of Independent Claims Paid for, if greater than 3 | | | | | |
| | | | | | | |
| **Indep. Claims** | | **Extra Claims** | **Fee ($)** | **Fee Paid ($)** | | |
| 4 | minus 3 | 1 | x $200.00 | $200.00 | | |
| | HP = highest number of Independent Claims Paid for, if greater than 3 | | | | | |

**3. APPLICATION SIZE FEE**

If the specification and drawings exceed 100 sheets of paper, the application size fee due is &250 ($125 for small entity) for each additional 50 sheets or fraction thereof. See U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).

Total Sheets

| Total Sheets | | Extra Sheets | | Number of each additional 50 or fraction thereof | Fee $ | | Fee Paid $ |
|---|---|---|---|---|---|---|---|
| 23 | -100 | 0 | /50 | | | = | $0.00 |

**4. OTHER FEE(S)**

Non-English specification, $130 fee (no small entity discount)
Other:

**Total Fees Due ($)**
$1,200.00

**5. PAYMENT OF FEES**

The full fee due in connection with this communication is provided as follows:

1. Not enclosed

[ ] No filing fee is to be paid at this time.

2. Enclosed

[ X ] Filing fee

[ ] Recording assignment

[ X ] The Commissioner is hereby authorized to charge any additional fees associated with this communication or credit any overpayment to Deposit Account No.: 50-4160 . A duplicate copy of this authorization is enclosed.

[ X ] A check in the amount of $1,200.00.

[ ] Charge any fees required or credit any overpayments associated with this filing to Deposit Account No.: 50-4160.

This application is filed pursuant to 37 C.F.R. § 1.53 in the name of the above-identified Inventor(s).

[ X ] Customer No: 45590

Please direct all correspondence concerning the above-identified application to the following address:

**MURABITO, HAO & BARNES LLP**
Two North Market Street, Third Floor
San Jose, California 95113
(408) 938-9060

[ X ] This transmittal ends with this page.

Respectfully submitted,

Date: August 21, 2007

By: _____
Anthony C. Murabito
Reg. No. 35,295

Attorney Docket No.: TRAN-P059

# IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

## Patent Application

| I hereby certify that this transmittal of the below described document is being deposited with the United States Postal Service in an envelope bearing First Class Postage and addressed to the Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450 on the below date of deposit. | | | | | |
|---|---|---|---|---|---|
| Date of Deposit: | 8/21/2007 | Name of Person Making the Deposit: | Mina Oliveri | Signature of the Person Making the Deposit: | Mina Oliveri |

In re Application

Inventor(s): Andrew Read, Sameer Halapete, and Keith Klayman

Application No.: 09/694,433

Filed: 10/23/2000

Title: SAVING POWER WHEN IN OR TRANSITIONING TO A STATIC MODE OF A PROCESSOR

**Commissioner for Patents**
**P.O. Box 1450**
**Alexandria, VA 22313-1450**

NOTIFICATION OF FILING OF DIVISIONAL APPLICATION CLAIMING BENEFIT OF FILING DATE
*(THIS IS NOT A REQUEST FOR A CPA FILING)*

[X] Notification is hereby being made of the filing of a continuation application claiming benefit for filing date for this case

[X] concurrently herewith.
[ ] on .....

Please direct all correspondence concerning the above-identified application to the following address:

**MURABITO, HAO & BARNES LLP**
Two North Market Street, Third Floor
San Jose, California 95113
(408) 938-9060
Customer No: 45590

Respectfully submitted,

Date: August 21, 2007

By: _____
Anthony C. Murabito
Reg. No. 35,295



rev. 02/00 KGR

Notification to Parent of Divisional Application Filing
Applicant: Read et al. S/N.: 09/694,433
Docket No.: **TRAN-P059** Filed: 10/23/2000
Title: SAVING POWER WHEN IN OR TRANSITIONING TO A STATIC MODE OF A PROCESSOR
Sir:
Please acknowledge receipt of the following:
☑ Certificate of Mailing
☑ Conditional Petition for an Extension of Time
☑ Notification of Filing of Divisional Application

Submitted on: 8/21/2007

Attorney Docket No.: TRAN-P059

**IN THE UNITED STATES PATENT AND TRADEMARK OFFICE**

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In re Application of:

Inventor(s): Andrew Read, Sameer Halapete, and Keith Klayman

Application No.: 09/694,433

Filed: 10/23/2000

Title: SAVING POWER WHEN IN OR TRANSITIONING TO A STATIC MODE OF A PROCESSOR

**Commissioner for Patents**
**P.O. Box 1450**
**Alexandria, VA 22313-1450**

CONDITIONAL PETITION FOR EXTENSION OF TIME

This conditional petition is being filed along with the accompanying DIVISIONAL and provides for the possibility that applicant has inadvertently overlooked the need for a petition and fee for extension of time.

**Conditional petition for extension of time**

If any extension of time for the accompanying response is required, applicant requests that this be considered a petition therefor.

**Status**

This application is on behalf of

[X] other than a small entity
[ ] a small entity
A verified statement:
[ ] is attached
[ ] is already filed

[ ] The Commissioner is hereby authorized to charge any additional fees associated with this communication or credit any overpayment to Deposit Account No.: 50-4160.
A duplicate copy of this authorization is enclosed.



rev. 6/97 jpw

Please direct all correspondence concerning the above-identified application to the following address:

**MURABITO, HAO & BARNES LLP**
Two North Market Street, Third Floor
San Jose, California 95113
(408) 938-9060
Customer No: 45590

Respectfully submitted,

Date: August 21, 2007

By: _____
Anthony C. Murabito
Reg. No. 35,295



rev. 6/97 jpw

18351 U.S. PTO

082107

U.S. PTO
11/894991
08/21/2007

Attorney Docket No.: TRAN-P470

# IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

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| Express Mail Label No.: | EM061752383US | Name of Person Making the Deposit: | Anthony Chou |
| Date of Deposit: | 08/21/2007 | Signature of the Person Making the Deposit: | Anthony Chou |

Inventor(s): Andrew Read, Sameer Halapete, Keith Klayman

Title: SAVING POWER WHEN IN OR TRANSITIONING TO A STATIC MODE OF A PROCESSOR

This is a request for filing a Divisional application under 37 CFR 1.53(b), of pending prior application Application No. 09/694,433 filed on 10/23/2000

of Andrew Read, Sameer Halapete, Keith Klayman
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for SAVING POWER WHEN IN OR TRANSITIONING TO A STATIC MODE OF A PROCESSOR
*Title of invention*

Examiner: Art Unit:

Commissioner for Patents
P.O. Box 1450
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[ ] Application claims small entity status (if applicable) *37 CFR 1.27.*

[ X ] Specification [Total Pages 21 ]

[ X ] Drawings *(35 U.S.C. 113)* [Total Sheets 2 ]

[ X ] Oath or Declaration [Total Sheets 2 ]

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[ ] DELETION OF INVENTOR(S)
Signed statement attached deleting inventor(s) name in the prior application, *see 37 CFR 1.63 (d)(2) and 1.33(b)*

[ X ] Power of Attorney

## ACCOMPANYING APPLICATION PARTS

[ ] Assignment Papers (cover sheet & document(s))

Name of Assignee Transmeta Corporation

[ ] 37 CFR 3.73 (b) Statement (when there is an assignee)

[ ] English Translation Document (if applicable)

[ ] Information Disclosure Statement (PTO/SB/08 or PTO-1449)
[ ] Copies of citations attached

[ ] Preliminary Amendment

[ X ] Return Receipt Postcard (MPEP 503)
(Should be specifically itemized)

[ ] Certified Copy of Priority Document(s)
(if foreign priority is claimed)

[ X ] Nonpublication Request under 35 U.S.C. 122 (b)(2)(B)(i).
Applicant must attach form PTO/SB/35 or equivalent.

[ X ] Other: Power of Attorney by Assignee of Entire Interest (Revocation of Prior Powers) documents are included.

**Petition for Suspension of Prosecution for the Time Necessary to File an Amendment**

☐ There is provided herewith a Petition To Suspend Prosecution For The Time Necessary to File An Amendment (New Application Filed Concurrently).

**Priority Claim**

**35 U.S.C. 119**

☐ Priority of Application Number _____ filed on _____ in _____ is claimed under 35 U.S.C. 119.

☐ The certified copy has been filed in prior U.S. Application No. _____ in _____

☐ The certified copy will follow.

**35 U.S.C. 120, 121 and 365(c)**

"This application is a divisional and claims the benefit of copending application(s)

☒ application number 09/694,433 filed on 10/23/2000

☐ International Application _____ filed on _____

which designated the U.S."

**Inventorship Statement**

(a) With respect to prior copending U.S. application from which this application claims benefit under 35 USC 120 the inventor(s) in this application are:

☒ the same.

☐ less than those named in the prior application. It is requested that the following inventor(s) identified above for the prior application be deleted:

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*Type names of inventors to be deleted*

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### Notification in Parent Application of the Filing of This Divisional Application

[X] A notification of the filing of this divisional is being filed in the parent application from which this application claims priority under 35 USC § 120.

**FEE CALCULATION**

**1. BASIC FILING, SEARCH, AND EXAMINATION FEES**

| | Filing Fees | Search Fees | | Examination Fees | | | |
|---|---|---|---|---|---|---|---|
| | | Small Entity | | Small Entity | | Small Entity | |
| Application Type | Fee ($) | Fee ($) | Fee ($) | Fee ($) | Fee ($) | Fee ($) | Fees Paid ($) |
| Utility | 300 | 150 | 500 | 250 | 200 | 100 | $1,000.00 |
| Design | 200 | 100 | 100 | 50 | 130 | 65 | $ |
| Plant | 200 | 100 | 300 | 150 | 160 | 80 | $ |
| Reissue | 300 | 150 | 500 | 250 | 600 | 300 | $ |
| Provisional | 200 | 100 | | | | | $ |

**2. EXCESS CLAIM FEES**

| Fee Description | Small Entity Fee ($) | Fee ($) |
|---|---|---|
| Each claim over 20 or, for Reissues, each claim over 20 and more than in the original patent | 50 | 25 |
| Each independent claim over 3 or, for reissues, each independent claim more than in the original patent | 200 | 100 |

Multiple dependent claims 360 180

| Total Claims | | Extra Claims | Fee ($) | Fee Paid ($) | Multiple Dependent Claims | |
|---|---|---|---|---|---|---|
| 19 | minus 20 | 0 | x $50.00 | $0.00 | | |
| | HP = highest number of Independent Claims Paid for, if greater than 3 | | | | | |
| | | | | | | |
| **Indep. Claims** | | **Extra Claims** | **Fee ($)** | **Fee Paid ($)** | | |
| 4 | minus 3 | 1 | x $200.00 | $200.00 | | |
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**3. APPLICATION SIZE FEE**

If the specification and drawings exceed 100 sheets of paper, the application size fee due is &250 ($125 for small entity) for each additional 50 sheets or fraction thereof. See U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).

Total Sheets

| Total Sheets | | Extra Sheets | | Number of each additional 50 or fraction thereof | Fee $ | | Fee Paid $ |
|---|---|---|---|---|---|---|---|
| 23 | -100 | 0 | /50 | | | = | $0.00 |

**4. OTHER FEE(S)**

Non-English specification, $130 fee (no small entity discount)
Other:

**Total Fees Due ($)**
$1,200.00

**5. PAYMENT OF FEES**

The full fee due in connection with this communication is provided as follows:

1. Not enclosed

[ ] No filing fee is to be paid at this time.

2. Enclosed

[ X ] Filing fee

[ ] Recording assignment

[ X ] The Commissioner is hereby authorized to charge any additional fees associated with this communication or credit any overpayment to Deposit Account No.: 50-4160 . A duplicate copy of this authorization is enclosed.

[ X ] A check in the amount of $1,200.00.

[ ] Charge any fees required or credit any overpayments associated with this filing to Deposit Account No.: 50-4160.

This application is filed pursuant to 37 C.F.R. § 1.53 in the name of the above-identified Inventor(s).

[ X ] Customer No: 45590

Please direct all correspondence concerning the above-identified application to the following address:

**MURABITO, HAO & BARNES LLP**
Two North Market Street, Third Floor
San Jose, California 95113
(408) 938-9060

[ X ] This transmittal ends with this page.

Respectfully submitted,

Date: August 21, 2007

By: _____
Anthony C. Murabito
Reg. No. 35,295

Attorney Docket No.: TRAN-P059

# IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

## Patent Application

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|---|---|---|---|---|---|
| Date of Deposit: | 8/21/2007 | Name of Person Making the Deposit: | Mina Oliveri | Signature of the Person Making the Deposit: | Mina Oliveri |

In re Application

Inventor(s): Andrew Read, Sameer Halapete, and Keith Klayman

Application No.: 09/694,433

Filed: 10/23/2000

Title: SAVING POWER WHEN IN OR TRANSITIONING TO A STATIC MODE OF A PROCESSOR

**Commissioner for Patents**
**P.O. Box 1450**
**Alexandria, VA 22313-1450**

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*(THIS IS NOT A REQUEST FOR A CPA FILING)*

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[X] concurrently herewith.
[ ] on .....

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Two North Market Street, Third Floor
San Jose, California 95113
(408) 938-9060
Customer No: 45590

Respectfully submitted,

Date: August 21, 2007

By: _____
Anthony C. Murabito
Reg. No. 35,295



rev. 02/00 KGR

Notification to Parent of Divisional Application Filing
Applicant: Read et al. S/N.: 09/694,433
Docket No.: **TRAN-P059** Filed: 10/23/2000
Title: SAVING POWER WHEN IN OR TRANSITIONING TO A STATIC MODE OF A PROCESSOR
Sir:
Please acknowledge receipt of the following:
☑ Certificate of Mailing
☑ Conditional Petition for an Extension of Time
☑ Notification of Filing of Divisional Application

Submitted on: 8/21/2007

Attorney Docket No.: TRAN-P059

**IN THE UNITED STATES PATENT AND TRADEMARK OFFICE**

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|---|---|---|---|---|---|
| Date of Deposit: | 8/21/2007 | Name of Person Making the Deposit: | Mina Oliveri | Signature of the Person Making the Deposit: | Mina Oliveri |

In re Application of:

Inventor(s): Andrew Read, Sameer Halapete, and Keith Klayman

Application No.: 09/694,433

Filed: 10/23/2000

Title: SAVING POWER WHEN IN OR TRANSITIONING TO A STATIC MODE OF A PROCESSOR

**Commissioner for Patents**
**P.O. Box 1450**
**Alexandria, VA 22313-1450**

CONDITIONAL PETITION FOR EXTENSION OF TIME

This conditional petition is being filed along with the accompanying DIVISIONAL and provides for the possibility that applicant has inadvertently overlooked the need for a petition and fee for extension of time.

**Conditional petition for extension of time**

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**Status**

This application is on behalf of

[X] other than a small entity
[ ] a small entity
A verified statement:
[ ] is attached
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A duplicate copy of this authorization is enclosed.



rev. 6/97 jpw

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**MURABITO, HAO & BARNES LLP**
Two North Market Street, Third Floor
San Jose, California 95113
(408) 938-9060
Customer No: 45590

Respectfully submitted,

Date: August 21, 2007

By: _____
Anthony C. Murabito
Reg. No. 35,295



rev. 6/97 jpw

TRAN-P470

UNITED STATES PATENT APPLICATION

for

# SAVING POWER WHEN IN OR TRANSITIONING TO A STATIC MODE OF A PROCESSOR

Inventor(s):

Andrew Read

Sameer Halepete

Keith Klayman

Prepared by:

MURABITO HAO & BARNES, LLP
Two North Market Street, Third Floor
San Jose, California 95113
(408) 938-9060

# SAVING POWER WHEN IN OR TRANSITIONING TO A STATIC MODE OF A PROCESSOR

## RELATED APPLICATION

This Application is a Divisional Application of co-pending, commonly owned United States Patent Application Serial No. 09/694,433, attorney docket TRAN-P059, filed 10/23/2000, entitled "SAVING POWER WHEN IN OR TRANSITIONING TO A STATIC MODE OF A PROCESSOR" to Read et al., which is hereby incorporated herein by reference in its entirety.

BACKGROUND OF THE INVENTION

Field Of The Invention

This invention relates to computer systems and, more particularly, to apparatus and methods for reducing power use by a computer system during intervals in which processing is stopped.

History Of The Prior Art

As computer processors have increased in ability, the number of transistors utilized has increased almost exponentially. This increase in circuit elements has drastically increased the power requirements of such processors. As the need of power increases, the temperature at which a computer operates increases and the battery life of portable computers decreases. The loss of battery life with modern portable computers greatly reduces the time during which the computer can function as a portable device. In fact, the power usage has become so great that even with significant reduction in the process size utilized, a plethora of techniques have been implemented to reduce power usage to maintain the efficacy of portable computers.

One of these techniques monitors the use of the various devices within the computer and disables those devices that have not been utilized for some period. Because the processor utilizes a significant amount of the power (e.g., 50%) used by a portable computer, this technique is utilized to disable the processor itself when its processing requirements are unused for some interval. In the typical case, disabling the processor is

accomplished by terminating the system clocks furnished to the processor. When processor clocks have been disabled, controlling circuitry (typically a portion of the "Southbridge" circuitry of an X86-processor-based computer) remains enabled to detect interrupts requiring processor operation. The receipt of such an interrupt causes the controlling circuitry to once again enable clocks to the processor so that the processor may take whatever steps are necessary to handle the basis of the interrupt.

The technique of disabling the processor reduces significantly the dissipation of power caused by the operation of the processor even at a low frequency. In fact, the technique works quite well; and it is estimated that with many portable computers the processor is placed in the state in which system clocks are disabled during approximately ninety percent of the operation of the computer. However, use of this technique emphasizes another aspect of power loss using advanced processors. When system clocks for a processor are disabled, the processor must remain in a state (sometimes called "deep sleep") in which it is capable of rapidly responding to interrupts. Such a state requires the application of core voltage to the various circuits. The application of this voltage generates a power dissipation referred to in this specification as "static power" usage because the processor is in its static state in which clocks are disabled. To date there has been little attention paid to this static power usage. However, the usage is very significant when a processor functions in the deep sleep mode as much as ninety percent of the time. As process technologies continue to shrink

in dimension and lower operating voltages, this static power increases due to lower threshold voltages and thinner gate oxides.

It is desirable to furnish apparatus and methods for reducing the power use of a processor in the state in which its clocks are disabled.

## Summary Of The Invention

The present invention is realized by a method for reducing power utilized by a processor including the steps of determining that a processor is transitioning from a computing mode to a mode in which system clock to the processor is disabled, and reducing core voltage to the processor to a value sufficient to maintain state during the mode in which system clock is disabled.

These and other features of the invention will be better understood by reference to the detailed description which follows taken together with the drawings in which like elements are referred to by like designations throughout the several views.

## Brief Description Of The Drawings

Figure 1 is a diagram illustrating current-voltage characteristics of CMOS transistor devices utilized in microprocessors.

Figure 2 is another diagram illustrating current-voltage characteristics of CMOS transistor devices utilized in microprocessors.

Figure 3 is a circuit diagram illustrating a first circuit designed in accordance with the present invention for reducing static power usage.

Figure 4 is a circuit diagram illustrating a second circuit designed in accordance with the present invention for reducing static power usage.

Figure 5 is another circuit diagram illustrating a circuit designed in accordance with the present invention for reducing static power usage.

Detailed Description

Figure 1 is a first diagram displaying a number of curves illustrating the current-voltage characteristics of CMOS transistor devices utilized in the circuits of a microprocessor. This first diagram utilizes a linear scale for both current and voltage. As may be seen, each of the curves illustrates that the drain-to-source current of a transistor is essentially nonexistent until the voltage at the gate terminal of the transistor is raised to a threshold voltage. Once the threshold voltage of the transistor is reached, drain-to-source current increases either linearly or quadratically depending on whether the transistor is in the linear region or saturation region of operation.

Although the diagram of Figure 1 appears to illustrate that current flowing below the threshold value of the gate voltage is insignificant, this is not the case in some situations. Figure 2 illustrates current versus voltage curves of the typical transistor device below the threshold voltage with the voltage being plotted on a log scale. As may be seen, current in fact flows below the threshold voltage. If a transistor functions in the state below the threshold voltage for ninety percent of computer processor operation, then this current has a significant affect on power usage by the processor.

Since a processor is not capable of computing in the mode in which its clocks are disabled, it would at first glance appear that the solution would be to terminate the application of voltage to the processor. However, as suggested above, it is necessary that the processor be maintained in a condition in which it can respond rapidly to interrupts provided by the circuitry that controls application of the system clocks. To do this, the processor must maintain state sufficient to immediately return to an operating condition. Thus, prior art processors have been provided sufficient voltage to maintain such state and to keep their transistors ready to immediately respond to interrupts. In general, this has been accomplished by maintaining the processor core voltage at the same level as the operating voltage. With most prior art processors, the core voltage used by a processor is selected by use of motherboard switches or setup software at a level sufficient to provide the highest frequency operations specified for the particular processor. For example, many processors provide 1.8 volts as a core voltage. On the other hand, the voltage required to maintain state in a deep sleep mode may be significantly less, e.g., one volt or less. Since such processors function at the same voltage whether in a computing or a deep sleep mode, a significant amount of unnecessary power may be expended. In one typical state of the art X86 processor, the power usage averages approximately one-half watt in the deep sleep state because of the leakage illustrated by the diagram of Figure 2.

The present invention reduces the voltage applied to the processor significantly below the lowest voltage normally furnished as a core voltage for the processor during the mode in which system clocks are

disabled thereby reducing the power utilized by the processor in the deep sleep state.

Figure 3 is a circuit diagram illustrating a first embodiment of the invention. In the circuit 10 illustrated, a switching voltage regulator 11 receives an input signal at a terminal 12 which determines its output voltage value. Most modern processors utilize a voltage regulator which is capable of furnishing a range of core voltages for operating transistors; a typical regulator may furnish a range of voltages between 2 and 0.925 volts from which a particular core voltage may be selected for operation. Typically, a binary signal is provided a the terminal 12 which selects the particular output voltage level to be furnished by the regulator 11; in such a case, a number of individual pins may be utilized as the terminal 12.

Recently, a new power saving technique has been utilized which dynamically adjusts both the voltage and operating frequency to a level sufficient to maintain computing operations being conducted by a processor. The technique which offers significant power savings is described in detail in U. S. Patent application Serial No. 09/484,516, filed January 18, 2000, entitled Adaptive Power Control, assigned to the assignee of the present invention. A processor which utilizes this technique monitors operations within the processor to determine the frequency level at which the processor should operate. Depending on the particular operations being carried out by the processor, the value furnished at the terminal 12 of a regulator functioning in such a system will cause the regulator to produce an output voltage at some level

between the high and low values necessary for the particular processor to carry out computing functions.

In the circuit of Figure 3, input to the terminal 12 is furnished via a circuit 13 such as a multiplexor that is capable of providing one or more input values. In the embodiment illustrated, a value is provided at a first input 14 to the circuit 13 by the processor (or other circuitry) which determines the operating condition of the processor in its computing range; and a second value is provided at a second input 15 which is selected especially for the deep sleep condition. Either of these input values may be selected by a control signal provided at a control terminal 16 of the circuit 13. In one embodiment, a system control signal normally utilized to signal entry into the deep sleep condition (a stop clock signal) is used as the control signal to be furnished at the control terminal 16. This control signal selects the input value furnished at the input 15 which is especially chosen to cause a typical prior art regulator 11 to produce a voltage output for operating the processor in the deep sleep mode. In one embodiment of the invention, the value furnished for deep sleep mode is chosen to cause the regulator 11 to produce the lowest voltage possible in its range of output voltages. In one exemplary processor that utilizes the technique described in the above-mentioned patent application, the processor is specified as capable of conducting computing operations in a core voltage range from a low voltage of 1.2 volts to a high voltage of 1.6 volts. On the other hand, the processor when operating in deep sleep mode has no problem maintaining that state necessary to resume computing even though functioning at a core voltage of 0.925 volts, the lowest voltage which the regulator can provide.

Thus, although the voltage regulator 11 may typically provide a range of varying output voltage levels, the lowest voltage at which a processor is specified for conducting computing operations is typically significantly above the lowest value which the regulator is capable of furnishing.

In order to reduce power usage in one embodiment of the present invention, in response to a control signal indicating that the processor is about to go into the deep sleep state, the value at the input 15 is furnished by the circuit 13 to the regulator causing the regulator 11 to generate its lowest possible output voltage level for the deep sleep condition. In one exemplary embodiment, the high and low voltages generated in a computing mode are 1.6 volts and 1.2 volts while the deep sleep voltage is 0.925 volts.

Although the voltage level furnished by the regulator 11 for the deep sleep mode of the processor might appear to be only slightly lower than that furnished in the lowest operating condition for the exemplary processor, the reduction in power usage is quite significant. Because both the voltage and the leakage current are reduced, the reduction in power is approximately equal to the ratio in voltage levels raised to the power of about three to four. Over any period of processor use involving the deep sleep state, such a reduction is quite large.

One problem with this approach to reducing power is that it does not reduce the voltage level as far as might be possible and, thus, does not conserve as much power as could be saved. This approach only reduces the voltage level to the lowest level furnished by the regulator. This voltage is significantly greater than appears to be necessary for a

processor which also dynamically regulates voltage furnished during computing operations to save power. Two criteria control the level to which the core voltage may be reduced in deep sleep. The level must be sufficient to maintain state that the processor requires to function after returning from the deep sleep state. The level must be one that can be reached during the times allowed for transition to and from the deep sleep mode.

The first criterion is met so long as values of state stored are not lost during the deep sleep mode. Tests have shown that a core voltage significantly below one-half volt allows the retention of the memory state of a processor. Thus, using this criterion, it would be desirable to reduce the core voltage to a value such as one-half volt or lower.

However, depending on system configuration, the time allowed to transition to and from deep sleep in an X86 processor can be as low as 50 microseconds. Depending on the capacitive load of the particular circuitry, a voltage variation of about 0.5 to 0.6 volts may take place during this time in one exemplary configuration.

Thus, if the exemplary processor is operating at its lowest processing core voltage of 1.2 volts, its core voltage may be lowered in the time available to 0.6 - 0.7 volts. On the other hand, if the processor is operating at a processing core voltage of 1.5 volts, its core voltage may only be lowered in the time available to 0.9 - 1 volts. Consequently, it is desirable that the core voltage furnished during deep sleep be lowered to a level which may be below the level provided by a typical voltage

regulator but which varies depending on the core operating voltage from which it transitions.

This desirable result may be reached utilizing a circuit such as that described in Figure 4. The circuit of Figure 4 includes a feedback network 41 for controlling the level of voltage at the output of the regulator 11. Prior art regulators such as the Maxim 1711 provide a feedback terminal and describe how that terminal may be utilized with a resistor-voltage-divider network joined between the output terminal and ground to raise the output voltage level.

The embodiment of the present invention illustrated in Figure 4 utilizes the same feedback terminal and a similar resistor-voltage-divider network but joins the divider between the output terminal and a source of voltage 42 higher than the normal output voltage of the regulator to force the output voltage level to a lower value rather than a higher level. The particular source voltage and the particular resistor values may be selected to cause the voltage level at the output of the regulator to drop from a particular output value to a desired value such as 0.6 volts when transitioning from a computing level of 1.2 volts.

By appropriate choice of the resistor values of the divider network 41 and the source 42, the voltage drop provided by such a divider network accomplishes the desired result of providing an output voltage for the deep sleep mode of operation that varies from the previous processor computing core voltage by an amount attainable during the transition period available. In one embodiment, resistor 43 was chosen to be 1 Kohms, resistor 45 to be 2.7 Kohms, and source 42 to be 3.3 volts. Such

values cause the voltage drop into deep sleep mode to be between 0.5 and 0.6 volts whether beginning at core voltages of 1.2 or 1.6 volts. On the other hand, by using a higher value of voltage at source 45 and adjusting the values of resistors 41 and 43, the increments of voltage drop reached from different starting voltages to final deep sleep voltage values at the terminal 12 may be brought closer to one another.

It should be noted that the circuitry of Figures 3 and 4 may be combined so that both input selection and output adjustment are both used to adjust the core voltage value produced by a voltage regulator for deep sleep mode in particular instances where the load capacitance is relatively low.

Prior art voltage regulators function in at least two different modes of operation. A first mode of operation is often referred to as "low noise" or "continuous" mode. In this mode, the regulator responds as rapidly as possible to each change in voltage thereby maintaining the output voltage at the desired output level as accurately as possible. In order to maintain this mode of rapid response, regulators consume a certain amount of power. When a regulator is supplying a significant amount of power to the load, the power required to operate in continuous mode is relatively small. But, when a regulator is supplying a small amount of power to the load, the power used to operate the regulator in continuous mode becomes significant, and reduces the efficiency of the regulator significantly. It is common for regulators operating in the continuous mode to transfer charge from the supply capacitors back into the power source when the output voltage is changed from a higher voltage to a

lower voltage. The regulator can later transfer that charge back to the regulator output capacitors. Thus, most of the charge is not wasted.

A second mode of operation by voltage regulators is often referred to as "high efficiency," "burst," or "skip" mode. In this mode, a regulator detects the reduction in load requirements (such as that caused by a transition into the deep sleep state) and switches to a mode whereby the regulator corrects the output voltage less frequently. When there is an increase in load requirements, the regulator switches back to the continuous mode of regulation during which more rapid correction occurs. This has the positive effect of reducing the power consumed by the regulator during deep sleep thereby increasing the regulator efficiency and saving system power. But, as a result of reducing the regulator response rate, there is more noise on the regulator output.

It is common for regulators operating in the high efficiency mode to drain the charge on the supply capacitors during a high to low voltage transition on the power supply output or to allow the load to drain the charge. Thus, the charge is wasted during high to low voltage transitions.

It is typical to operate a voltage regulator in the high efficiency mode. Consequently, there is some waste of power whenever a regulated processor goes into the lower voltage deep sleep mode. If the processor is constantly being placed in deep sleep mode, then the loss of power may be quite high. Different operating systems may increase the waste of power by their operations. For example, an operating system that detects changes in operation through a polling process must constantly

bring a processor out of deep sleep to determine whether a change in operating mode should be implemented. For many such systems, such a system causes an inordinate amount of power waste if a processor would otherwise spend long periods in the deep sleep mode. On the other hand, an operating system that remains in deep sleep until an externally-generated interrupt brings it out of that state wastes power through operating the regulator in the high efficiency mode only when the processor is placed in the deep sleep state.

The present invention utilizes the ability of regulators to function in both the high efficiency mode and the continuous mode to substantially reduce power wasted by transitioning between a computing and a lower voltage deep sleep mode. Although regulators have not been dynamically switched between high efficiency and continuous modes, in one embodiment of the invention, an additional controlling input 50 as shown in Figure 5 is added to the regulator for selecting the mode of operation of the regulator based on whether the processor being regulated is transitioning between states. If the regulator receives a control signal 51 indicating that the processor is to be placed into the deep sleep mode, for example, then a regulator operating in the high efficiency mode immediately switches to the continuous mode during the voltage transition. Assuming that the regulator returns the charge to the battery during continuous mode, this has the effect of reducing the waste of power caused during the transition. Once the transition has completed, the regulator switches back to the high efficiency state for operation during the deep sleep mode of the processor.

For regulators that do not conserve capacitive charge by transferring the charge to the battery, a circuit for accomplishing this may be implemented or a capacitor storage arrangement such as a charge pump 53 for storage may be added. Alternatively, when transitioning to deep sleep, the regulator could switch to a mode where the regulator does not actively drive the voltage low but allows the capacitor charge to drain through the load. The selection of power savings modes is dependent on the processor leakage current, the voltage drop between the operating and deep sleep voltages, and the efficiency of the regulator in transferring charge from the capacitors to the power source and then back. If the leakage current is not sufficient to bring the voltage down more than (1 – efficiency) * (deep sleep voltage drop) during the deep sleep interval, then it is more advantageous to use the load to drain the charge on the capacitors. Otherwise, the charge on the capacitors should be transferred back to the power source.

The control signal utilized may be the same control signal (stop clocks) that signals the transition into the deep sleep state if the method is to be used only for transitions between operating and deep sleep states. Alternatively, a control signal generated by a particular increment of desired change may be utilized for voltage changes within the computing range of the processor as well as the transition to deep sleep mode.

Although the present invention has been described in terms of a preferred embodiment, it will be appreciated that various modifications and alterations might be made by those skilled in the art without departing from the spirit and scope of the invention. The invention should therefore be measured in terms of the claims which follow.

Claims

What is claimed is:

1. A computer system comprising:

a processing unit;

circuitry coupled to the processor unit, said circuitry configured to provide to said processing unit:

a sleep voltage;

a first operating voltage; and

a second operating voltage that is less than the first operating voltage;

wherein said computer system has a first transition time for transitioning from said sleep voltage to said first operating voltage;

wherein said computer system has a second transition time for transitioning from said sleep voltage to said second operating voltage;

wherein said second transition time is within an allowed time for transitioning from a sleep state to an operating state; and

wherein said first transition time is greater than said allowed time.

2. A computer system as recited in Claim 1 wherein said allowed time is based on a configuration of said computer system.

3. A computer system as recited in Claim 1 wherein said allowed time is based on timing requirements of said computer system.

4. A computer system as recited in Claim 3, wherein said timing requirements are based on interrupt response times.

5. A computer system as recited in Claim 1 wherein said first and second transition times are based on respective first and second voltage ramp times.

6. A computer system as recited in Claim 1 wherein said sleep voltage is sufficient to maintain state of said processing unit but is not sufficient to maintain processing activity in said processing unit.

7. A method of operating a computer processor, said method comprising:

transitioning from providing a sleep voltage to said computer processor to providing a first operating voltage to said computer processor within an allowed time for transitioning from a sleep state to an operating state; and

transitioning from said providing said first operating voltage to said computer processor to providing a second operating voltage to said computer processor, wherein a transition time for changing from said sleep voltage directly to said second operating voltage is greater than said allowed time for transitioning from said sleep state to said operating state.

8. A method in accordance with Claim 7 wherein said second operating voltage is greater than said first operating voltage.

9. A method in accordance with Claim 7 further comprising:

enabling a system clock to said computer processor when providing said first operating voltage to said computer processor; and

disabling said system clock to said computer processor when providing said sleep voltage to said computer processor.

10. A method in accordance with Claim 7, wherein said sleep voltage is sufficient to maintain state of said computer processor but is not sufficient to maintain processing activity in said computer processor.

11. A computer system comprising:

a processor;

an adjustable voltage supply configured to output to said processor:

a sleep voltage; and

a first operating voltage that, based on a rate of transitioning from said sleep voltage to said first operating voltage, is not achievable from said sleep voltage within an allowed time for transitioning from a sleep state to an operating state.

12. A computer system as recited in Claim 11, wherein said adjustable voltage supply is further configured to output to said processor a second operating voltage that, based on a rate of transitioning from said sleep voltage to said second operating voltage, is achievable from said sleep voltage within said allowed time for transitioning from said sleep state to said operating state.

13. A computer system as recited in Claim 11 wherein said allowed time is based on a configuration of said computer system.

14. A computer system as recited in Claim 11 wherein said adjustable voltage supply comprises a voltage regulator.

15. A computer system comprising:

a processing unit;

circuitry coupled to the processor unit, said circuitry configured to provide to said processing unit:

a first sleep voltage and a second sleep voltage;

a first operating voltage when transitioning from said first sleep voltage; and

a second operating voltage when transitioning from said second sleep voltage.

16. A computer system as recited in Claim 15, wherein said circuitry is further configured to provide to said processing unit:

said first sleep voltage when transitioning from said first operating voltage; and

said second sleep voltage when transitioning from said second operating voltage.

17. A computer system as recited in Claim 15 wherein a voltage difference between said first operating voltage and said first sleep voltage is approximately equal to a voltage difference between said second operating voltage and said second sleep voltage.

18. A computer system as recited in Claim 15 wherein said first operating voltage is greater than said second operating voltage and wherein said first sleep voltage is greater than said second sleep voltage.

19. A computer system as recited in Claim 18 wherein a voltage transition from said second sleep voltage to said first operating voltage is greater than a time allowed for transition from a sleep state to an operating state of said computer system.

ABSTRACT OF THE DISCLOSURE

A method for reducing power utilized by a processor including determining that a processor is transitioning from a computer mode to a mode in which system clock to the processor is disabled, and reducing core voltage to the processor to a value sufficient to maintain state during the mode in which system clock is disabled.

Figure 2




Figure 1

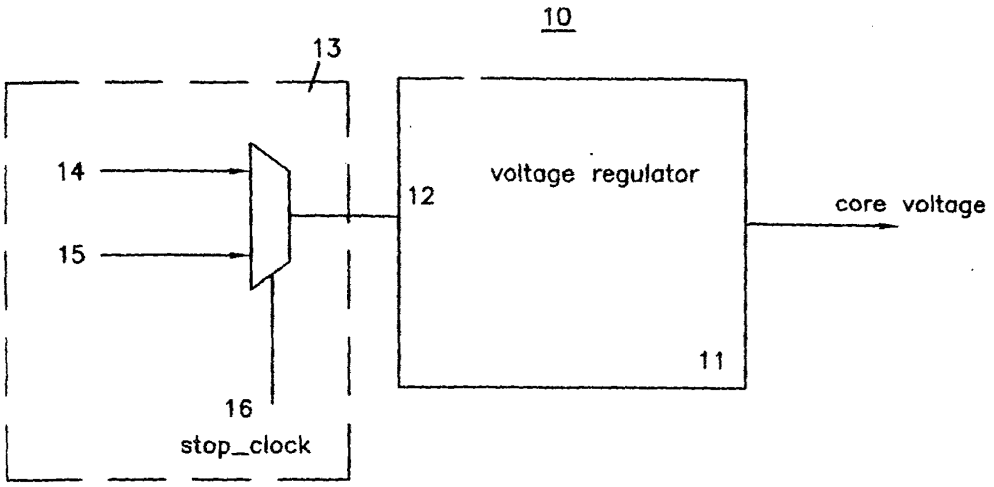


Figure 3

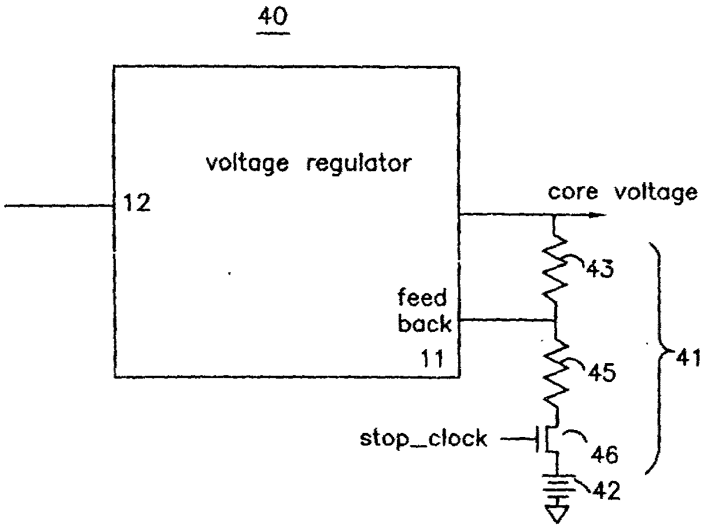


Figure 4

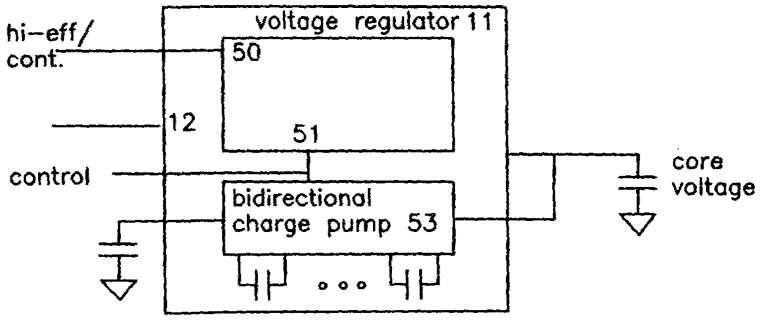


Figure 5

Attorney's Docket No.: Trans59 Patent

DECLARATION AND POWER OF ATTORNEY FOR PATENT APPLICATION

As a below named inventor, I hereby declare that:

My residence, post office address and citizenship are as stated below, next to my name.

I believe I am the original, first, and sole inventor (if only one name is listed below) or an original, first, and joint inventor (if plural names are listed below) of the subject matter which is claimed and for which a patent is sought on the invention entitled

STATIC POWER CONTROL

the specification of which was filed on October 23, 2000, and assigned Serial No. 09/694,433.

I hereby state that I have reviewed and understand the contents of the above-identified specification, including the claim(s), as amended by any amendment referred to above. I do not know and do not believe that the claimed invention was ever known or used in the United States of America before my invention thereof, or patented or described in any printed publication in any country before my invention thereof or more than one year prior to this application, that the same was not in public use or on sale in the United States of America more than one year prior to this application, and that the invention has not been patented or made the subject of an inventor's certificate issued before the date of this application in any country foreign to the United States of America on an application filed by me or my legal representatives or assigns more than twelve months (for a utility patent application) or six months (for a design patent application) prior to this application.

I acknowledge the duty to disclose all information known to me to be material to patentability as defined in Title 37, Code of Federal Regulations, Section 1.56.

I hereby appoint Stephen L. King, Reg. No. 19,180; with offices located at 30 Sweetbay Road, Rancho Palos Verdes, California 90275, telephone (310) 377-5073, with full power of substitution and revocation, to prosecute this application and to transact all business in the Patent and Trademark Office connected herewith.

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of

Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

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Attorney Docket No.: TRAN-P059

# IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Patent

In re Application of:

Inventor(s): Andrew Read, Sameer Halepete, and Keith Klayman

Serial No.: 09/694,433 Examiner:

Filed: 10/23/00 Art Unit: 2188

For: STATIC POWER CONTROL

Patent No.: Issued Date:

**Assistant Commissioner for Patents**
**Washington, D.C. 20231**

## POWER OF ATTORNEY BY ASSIGNEE OF ENTIRE INTEREST (REVOCATION OF PRIOR POWERS)

As assignee of record of the entire interest of the above identified

- ☒ application,
- ☐ patent,

### REVOCATION OF PRIOR POWERS OF ATTORNEY

all powers of attorney previously given are hereby revoked and

### NEW POWER OF ATTORNEY

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**ASSIGNEE CERTIFICATION**

Attached to this power is a "CERTIFICATE UNDER 37 CFR 3.73(b)."

Bryn Ekroot
Signature

9/9/2002
Date

Bryn C. Ekroot
*(type or print name of person authorized to sign on behalf of assignee)*

Director of Intellectual Property
Title

rev. 2/98 dbp

Docket No.: TRAN-P059
*Patent*

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of: Read et al.
Serial No.: 09/694,433
Filing Date: 10/23/00
For: STATIC POWER CONTROL

CERTIFICATE UNDER 37 CFR 3.73(b)

TRANSMETA CORPORATION, a corporation, certifies that it is the assignee of the entire right, title and interest in the patent application identified above by virtue of either:

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[ ] A chain of title from the inventor(s), of the patent application identified above, to the current assignees as shown below:

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The undersigned has reviewed all the documents in the chain of title of the patent application identified above and, to the best of undersigned's knowledge and belief, title is in the assignee identified above.

The undersigned (whose title is supplied below) avers that the undersigned is empowered to sign this certificate on behalf of the assignee.

I hereby declare that all statements made herein of my own knowledge are true, and that all statements made on information and belief are believed to be true; and further, that these statements are made with the knowledge that willful false statements, and the like so made, are punishable by fine

or imprisonment, or both, under Section 1001, Title 18 of the United States Code, and that such willful false statements may jeopardize the validity of the application or any patent issuing thereon.

9/9/2002
*Date*

*Signature*

Bryn C. Ekroot
*Typed or Printed Name*

Director of Intellectual Property
*Title*

PATENT APPLICATION SERIAL NO._____

**U.S. DEPARTMENT OF COMMERCE**
**PATENT AND TRADEMARK OFFICE**
**FEE RECORD SHEET**

08/24/2007 MGEBREM1 00000012 11894991

| | | |
|---|---|---|
| 01 FC:1611 | 300.00 | OP |
| 02 FC:1111 | 500.00 | OP |
| 03 FC:1311 | 200.00 | OP |
| 04 FC:1201 | 200.00 | OP |

PTO-1556
(5/87)

*U.S. Government Printing Office: 2002-489-267/69033

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PTO/SB/06 (02-07)
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# PATENT APPLICATION FEE DETERMINATION RECORD
Substitute for Form PTO-875

Application or Docket Number: 11894991

## APPLICATION AS FILED – PART I

| FOR | (Column 1) NUMBER FILED | (Column 2) NUMBER EXTRA | SMALL ENTITY RATE ($) | SMALL ENTITY FEE ($) | OR | OTHER THAN SMALL ENTITY RATE ($) | OTHER THAN SMALL ENTITY FEE ($) |
|---|---|---|---|---|---|---|---|
| BASIC FEE (37 CFR 1.16(a), (b), or (c)) | N/A | N/A | N/A | $150 | | N/A | $300 |
| SEARCH FEE (37 CFR 1.16(k), (l), or (m)) | N/A | N/A | N/A | $250 | | N/A | $500 |
| EXAMINATION FEE (37 CFR 1.16(o), (p), or (q)) | N/A | N/A | N/A | $100 | | N/A | $200 |
| TOTAL CLAIMS (37 CFR 1.16(i)) | 19 minus 20 = | * | x $25 = | | OR | x $50 = | |
| INDEPENDENT CLAIMS (37 CFR 1.16(h)) | 4 minus 3 = | * 1 | x $100 = | | | x $200 = | 200 |
| APPLICATION SIZE FEE (37 CFR 1.16(s)) | If the specification and drawings exceed 100 sheets of paper, the application size fee due is $250 ($125 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s). | | $125 | | | $250 | |
| MULTIPLE DEPENDENT CLAIM PRESENT (37 CFR 1.16(j)) | | | +180 = | | | +360 = | |
| * If the difference in column 1 is less than zero, enter "0" in column 2. | | | TOTAL | | | TOTAL | 1200 |

## APPLICATION AS AMENDED – PART II

| | | (Column 1) CLAIMS REMAINING AFTER AMENDMENT | | (Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR | (Column 3) PRESENT EXTRA | SMALL ENTITY RATE ($) | SMALL ENTITY ADDITIONAL FEE ($) | OR | OTHER THAN SMALL ENTITY RATE ($) | OTHER THAN SMALL ENTITY ADDITIONAL FEE ($) |
|---|---|---|---|---|---|---|---|---|---|---|
| AMENDMENT A | Total (37 CFR 1.16(i)) | * | Minus | ** | = | x $25 = | | OR | x $50 = | |
| | Independent (37 CFR 1.16(h)) | * | Minus | *** | = | x $100 = | | OR | x $200 = | |
| | Application Size Fee (37 CFR 1.16(s)) | | | | | $125 | | | $250 | |
| | FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j)) | | | | | +180 = | | OR | +360 = | |
| | | | | | | TOTAL ADD'L FEE | | OR | TOTAL ADD'L FEE | |

| | | (Column 1) CLAIMS REMAINING AFTER AMENDMENT | | (Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR | (Column 3) PRESENT EXTRA | RATE ($) | ADDITIONAL FEE ($) | OR | RATE ($) | ADDITIONAL FEE ($) |
|---|---|---|---|---|---|---|---|---|---|---|
| AMENDMENT B | Total (37 CFR 1.16(i)) | * | Minus | ** | = | x $25 = | | OR | x $50 = | |
| | Independent (37 CFR 1.16(h)) | * | Minus | *** | = | x $100 = | | OR | x $200 = | |
| | Application Size Fee (37 CFR 1.16(s)) | | | | | $125 | | | $250 | |
| | FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j)) | | | | | +180 = | | OR | +360 = | |
| | | | | | | TOTAL ADD'L FEE | | OR | TOTAL ADD'L FEE | |

* If the entry in column 1 is less than the entry in column 2, write "0" in column 3.
** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20".
*** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3".
The "Highest Number Previously Paid For" (Total or Independent) is the highest number found in the appropriate box in column 1.

This collection of information is required by 37 CFR 1.16. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

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| APPLICATION NUMBER | FILING or 371(c) DATE | GRP ART UNIT | FIL FEE REC'D | ATTY.DOCKET.NO | TOT CLAIMS | IND CLAIMS |
|---|---|---|---|---|---|---|
| 11/894,991 | 08/21/2007 | 2115 | 1200 | TRAN-P470 | 19 | 4 |

**CONFIRMATION NO. 9781**

MURABITO, HAO & BARNES LLP
Third Floor
Two North Market Street
San Jose, CA95113

**FILING RECEIPT**

Date Mailed: 09/13/2007

Receipt is acknowledged of this non-provisional patent application. The application will be taken up for examination in due course. Applicant will be notified as to the results of the examination. Any correspondence concerning the application must include the following identification information: the U.S. APPLICATION NUMBER, FILING DATE, NAME OF APPLICANT, and TITLE OF INVENTION. Fees transmitted by check or draft are subject to collection. Please verify the accuracy of the data presented on this receipt. **If an error is noted on this Filing Receipt, please write to the Office of Initial Patent Examination's Filing Receipt Corrections. Please provide a copy of this Filing Receipt with the changes noted thereon. If you received a "Notice to File Missing Parts" for this application, please submit any corrections to this Filing Receipt with your reply to the Notice. When the USPTO processes the reply to the Notice, the USPTO will generate another Filing Receipt incorporating the requested corrections**

**Applicant(s)**

Andrew Read, Sunnyvale, CA;
Sameer Halepete, San Jose, CA;
Keith Klayman, Sunnyvale, CA;

**Power of Attorney:** None

**Domestic Priority data as claimed by applicant**

This application is a DIV of 09/694,433 10/23/2000 PAT 7,260,731

**Foreign Applications**

**If Required, Foreign Filing License Granted:** 09/10/2007

The country code and number of your priority application, to be used for filing abroad under the Paris Convention, is **US11/894,991**

**Projected Publication Date:** 12/20/2007

**Non-Publication Request:** No

**Early Publication Request:** No

**Title**

Saving power when in or transitioning to a static mode of a processor

**Preliminary Class**

## PROTECTING YOUR INVENTION OUTSIDE THE UNITED STATES

Since the rights granted by a U.S. patent extend only throughout the territory of the United States and have no effect in a foreign country, an inventor who wishes patent protection in another country must apply for a patent in a specific country or in regional patent offices. Applicants may wish to consider the filing of an international application under the Patent Cooperation Treaty (PCT). An international (PCT) application generally has the same effect as a regular national patent application in each PCT-member country. The PCT process **simplifies** the filing of patent applications on the same invention in member countries, but **does not result** in a grant of "an international patent" and does not eliminate the need of applicants to file additional documents and fees in countries where patent protection is desired.

Almost every country has its own patent law, and a person desiring a patent in a particular country must make an application for patent in that country in accordance with its particular laws. Since the laws of many countries differ in various respects from the patent law of the United States, applicants are advised to seek guidance from specific foreign countries to ensure that patent rights are not lost prematurely.

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For information on preventing theft of your intellectual property (patents, trademarks and copyrights), you may wish to consult the U.S. Government website, http://www.stopfakes.gov. Part of a Department of Commerce initiative, this website includes self-help "toolkits" giving innovators guidance on how to protect intellectual property in specific countries such as China, Korea and Mexico. For questions regarding patent enforcement issues, applicants may call the U.S. Government hotline at 1-866-999-HALT (1-866-999-4158).

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## Title 37, Code of Federal Regulations, 5.11 & 5.15

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espionage and the national security or the export of technical data. Licensees should apprise themselves of current regulations especially with respect to certain countries, of other agencies, particularly the Office of Defense Trade Controls, Department of State (with respect to Arms, Munitions and Implements of War (22 CFR 121-128)); the Bureau of Industry and Security, Department of Commerce (15 CFR parts 730-774); the Office of Foreign AssetsControl, Department of Treasury (31 CFR Parts 500+) and the Department of Energy.

**NOT GRANTED**

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**CONFIRMATION NO. 9781**

MURABITO, HAO & BARNES LLP
Third Floor
Two North Market Street
San Jose, CA95113

**FILING RECEIPT**

Date Mailed: 09/17/2007

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| APPLICATION NUMBER | FILING OR 371(c) DATE | FIRST NAMED APPLICANT | ATTY. DOCKET NO./TITLE |
|---|---|---|---|
| 11/894,991 | 08/21/2007 | Andrew Read | TRAN-P470 |

**CONFIRMATION NO. 9781**

MURABITO, HAO & BARNES LLP
Third Floor
Two North Market Street
San Jose, CA 95113

Date Mailed: 09/17/2007

## RESPONSE TO REQUEST FOR CORRECTED FILING RECEIPT

**Publication and General Rules Issues**

In response to your request for a corrected Filing Receipt, the Office is unable to comply with the request because:

- ☐ The articles such as "a", "an", and "the" are not included as the first words in the title of an application. They are considered to be unnecessary to the understanding of the title.
- ☐ The words "new", "improved", "improvement of", "improvement in", or "improvement relating to" are not included as the first words in the title of an application because a patent application is, by nature, a new idea or improvement. See MPEP 606.
- ☐ The title appears on the filing receipt in sentence case for publication in the Annual Index of Patents.
- ☐ Amendments are not accepted in provisional applications. See 37 CFR 1.53(c).
- ☐ An amendment or Application Data Sheet is needed to make this change.
- ☐ The inventor's residence will only include the city and state for U.S. residences or city and country for residences outside the U.S. (See MPEP 605.02.)
- ☐ Continuity claimed under 35 USC 120 cannot be added to the Filing Receipt without the applicant supplying the relationship (continuation, divisional, or continuation-in-part) in an Application Data Sheet or amendment to the first page of the specification.
- ☐ Small entity status was previously claimed in this application. To notify the Office of a loss of entitlement to small entity status, see 37 CFR 1.27(g). To have a good faith error in claiming small entity status excused, see 37 CFR 1.28(c).

- ☐ The request for non-publication was not timely filed. A request for non-publication must be submitted upon filing of an application. The application is scheduled to be published on the date specified on the filing receipt. See 37 CFR 1.213(a)(1)

- ☐ The request for non-publication has not been recognized because it is not conspicuous as required by 37 CFR 1.213(a)(2)

- ☐ The request for non-publication has not been recognized because it does not contain the certification as required by 37 CFR 1.213(a)(3).

- ☐ The request for non-publication has not been recognized because it is not signed in compliance with 37 CFR 1.33(b) as required by 37 CFR 1.213(a)(4).

- ☐ There was no prior request for non-publication in this application. The request to rescind the non-publication request will not be processed.

- ☐ Your request for non-publication will not be acknowledged because this application is not eligible for publication. Only utility and plant applications filed on or after November 29, 2000 are eligible for publication.

- ☐ The "Non-Publication Request" indicator is correct. If there was a proper request submitted at the time of filing, the notation on the filing receipt will be "Yes". If no such request was made, the notation will be "No".

- ☐ Assignment information will only be included for applications that are eligible for publication.

F. Asta

Office of Initial Patent Examination (571) 272-4000, or 1-800-PTO-9199

PART 3 - OFFICE COPY

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|---|---|---|---|
| 11/894,991 | 08/21/2007 | Andrew Read | TRAN-P470 |

**CONFIRMATION NO. 9781**

MURABITO, HAO & BARNES LLP
Third Floor
Two North Market Street
San Jose, CA95113

**Title:** Saving power when in or transitioning to a static mode of a processor

**Publication No.** US-2007-0294555-A1
**Publication Date:** 12/20/2007

## NOTICE OF PUBLICATION OF APPLICATION

The above-identified application will be electronically published as a patent application publication pursuant to 37 CFR 1.211, et seq. The patent application publication number and publication date are set forth above.

The publication may be accessed through the USPTO's publically available Searchable Databases via the Internet at www.uspto.gov. The direct link to access the publication is currently http://www.uspto.gov/patft/.

The publication process established by the Office does not provide for mailing a copy of the publication to applicant. A copy of the publication may be obtained from the Office upon payment of the appropriate fee set forth in 37 CFR 1.19(a)(1). Orders for copies of patent application publications are handled by the USPTO's Office of Public Records. The Office of Public Records can be reached by telephone at (703) 308-9726 or (800) 972-6382, by facsimile at (703) 305-8759, by mail addressed to the United States Patent and Trademark Office, Office of Public Records, Alexandria, VA 22313-1450 or via the Internet.

In addition, information on the status of the application, including the mailing date of Office actions and the dates of receipt of correspondence filed in the Office, may also be accessed via the Internet through the Patent Electronic Business Center at www.uspto.gov using the public side of the Patent Application Information and Retrieval (PAIR) system. The direct link to access this status information is currently http://pair.uspto.gov/. Prior to publication, such status information is confidential and may only be obtained by applicant using the private side of PAIR.

Further assistance in electronically accessing the publication, or about PAIR, is available by calling the Patent Electronic Business Center at 1-866-217-9197.

Pre-Grant Publication Division, 703-605-4283

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| APPLICATION NO. | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. | CONFIRMATION NO. |
|---|---|---|---|---|
| 11/894,991 | 08/21/2007 | Andrew Read | TRAN-P470 | 9781 |

7590 07/02/2009

MURABITO, HAO & BARNES LLP
Third Floor
Two North Market Street
San Jose, CA 95113

| EXAMINER | |
|---|---|
| CAO, CHUN | |
| ART UNIT | PAPER NUMBER |
| 2115 | |

| MAIL DATE | DELIVERY MODE |
|---|---|
| 07/02/2009 | PAPER |

**Please find below and/or attached an Office communication concerning this application or proceeding.**

The time period for reply, if any, is set in the attached communication.

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 11/894,991 | READ ET AL. | |
| | Examiner | Art Unit | |
| | Chun Cao | 2115 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *21 August 2007*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *1-19* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-19* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

## DETAILED ACTION

1. Claims 1-19 are presented for examination.

2. The title of the invention is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed. The current title is imprecise.

### *Claim Rejections - 35 USC § 112*

3. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

4. Claims 1-19 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the enablement requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention. There is no teaching in applicant's specification which suggests that 1) Claims 1, 7, 11 and 19 recites that second transition time is within an allowed time for transitioning from a sleep state to an operating state; and said first transition time is greater than said allowed time. 2) Claim 15 recites that circuitry configured to provide a second sleep voltage to said processing unit. However, the specification only seems to be enabling for circuitry configured to provide a first sleep voltage to said processing unit while the processing unit is in a deep sleep mode.

5. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

6. Claims 1-6 and 15-19 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

As per claim 1, recites the limitations" "the processor unit" in line 3. There is insufficient antecedent basis for this limitation in the claim.

As per claim 15, recites the limitations" "the processor unit" in line 3. There is insufficient antecedent basis for this limitation in the claim.

7. Claims 2-6, 8-10, 12-14 and 16-19 are rejected because they incorporate the deficiencies of claims 1, 7, 11 and 15 respectively.

***Conclusion***

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Chun Cao whose telephone number is 571-272-3664. The examiner can normally be reached on Monday-Friday from 7:30 am-4:00 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Thomas C. Lee can be reached on 571-272-3667. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Any inquiry of a general nature or relating to the status of this application should be directed to the Group receptionist whose telephone number is 571-272-2100.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

June 30, 2009

/Chun Cao/

Primary Examiner, Art Unit 2115

| Notice of References Cited | Application/Control No. 11/894,991 | Applicant(s)/Patent Under Reexamination READ ET AL. | |
|---|---|---|---|
| | Examiner Chun Cao | Art Unit 2115 | Page 1 of 3 |

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**NON-PATENT DOCUMENTS**

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Dates in MM-YYYY format are publication dates. Classifications may be US or foreign.

| Notice of References Cited | Application/Control No. 11/894,991 | Applicant(s)/Patent Under Reexamination READ ET AL. | |
|---|---|---|---|
| | Examiner Chun Cao | Art Unit 2115 | Page 2 of 3 |

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| * | | Document Number Country Code-Number-Kind Code | Date MM-YYYY | Name | Classification |
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| Notice of References Cited | Application/Control No. 11/894,991 | Applicant(s)/Patent Under Reexamination READ ET AL. | |
|---|---|---|---|
| | Examiner Chun Cao | Art Unit 2115 | Page 3 of 3 |

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Dates in MM-YYYY format are publication dates. Classifications may be US or foreign.

| Index of Claims | Application/Control No. | Applicant(s)/Patent Under Reexamination |
|---|---|---|
| | 11894991 | READ ET AL. |
| | Examiner | Art Unit |
| | Chun Cao | 2115 |

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| ✓ | Rejected | - | Cancelled | N | Non-Elected | A | Appeal |
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☐ Claims renumbered in the same order as presented by applicant ☐ CPA ☐ T.D. ☐ R.1.47

| CLAIM | | DATE | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|
| Final | Original | 06/30/2009 | | | | | | | | |
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| Search Notes | Application/Control No. | Applicant(s)/Patent Under Reexamination |
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| | 11894991 | READ ET AL. |
| | Examiner | Art Unit |
| | Chun Cao | 2115 |

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| SEARCH NOTES | | |
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| Inventor name search | 6/30/09 | cc |

| INTERFERENCE SEARCH | | | |
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# BIB DATA SHEET

**CONFIRMATION NO. 9781**

| SERIAL NUMBER | FILING or 371(c) DATE<br>RULE | CLASS | GROUP ART UNIT | ATTORNEY DOCKET NO. |
|---|---|---|---|---|
| 11/894,991 | 08/21/2007 | 713 | 2115 | TRAN-P470 |

**APPLICANTS**

Andrew Read, Sunnyvale, CA;
Sameer Halepete, San Jose, CA;
Keith Klayman, Sunnyvale, CA;

**** CONTINUING DATA **************************

This application is a DIV of 09/694,433 10/23/2000 PAT 7,260,731

**** FOREIGN APPLICATIONS **************************

**** IF REQUIRED, FOREIGN FILING LICENSE GRANTED ****

09/10/2007

| Foreign Priority claimed ❑ Yes ☑ No<br>35 USC 119(a-d) conditions met ❑ Yes ❑ No<br>Verified and Acknowledged /CHUN CAO/ Examiner's Signature | ❑ Met after Allowance<br>Initials | STATE OR COUNTRY | SHEETS DRAWINGS | TOTAL CLAIMS | INDEPENDENT CLAIMS |
|---|---|---|---|---|---|
| | | CA | 2 | 19 | 4 |

**ADDRESS**

MURABITO, HAO & BARNES LLP
Third Floor
Two North Market Street
San Jose, CA 95113
UNITED STATES

**TITLE**

Saving power when in or transitioning to a static mode of a processor

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# Inventor Information for 11/894991

| Inventor Name | City | State/Country |
|---|---|---|
| READ, ANDREW | SUNNYVALE | CALIFORNIA |
| HALEPETE, SAMEER | SAN JOSE | CALIFORNIA |
| KLAYMAN, KEITH | SUNNYVALE | CALIFORNIA |

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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of: Read et al.

| | | | |
|---|---|---|---|
| Serial: | 11/894,991 | Group Art Unit: | 2115 |
| Filed: | August 21, 2007 | Examiner: | Chun Cao |

For: SAVING POWER WHEN IN OR TRANSITIONING TO A STATIC MODE OF A PROCESSOR (as filed)

AMENDMENT and RESPONSE

Honorable Commissioner for Patents
PO Box 1450
Alexandria, VA 22313-1450

Dear Sir:

In response to the Office Action mailed July 7, 2009 in the above captioned Patent Application, Applicants respectfully request the Examiner to enter the following amendments and to consider the following remarks.

Title:

Please amend the title of the application as follows:

~~SAVING POWER WHEN IN OR~~ TRANSITIONING TO AND FROM A ~~STATIC MODE~~SLEEP STATE OF A PROCESSOR

In the Claims:

1. (currently amended) A computer system comprising:

a processing unit;

circuitry coupled to the processing ~~processor~~ unit, said circuitry configured to provide to said processing unit:

a sleep voltage;

a first operating voltage; and

a second operating voltage that is less than the first operating voltage;

wherein said computer system has a first transition time for transitioning from said sleep voltage to said first operating voltage;

wherein said computer system has a second transition time for transitioning from said sleep voltage to said second operating voltage;

wherein said second transition time is within an allowed time for transitioning from a sleep state to an operating state; and

wherein said first transition time is greater than said allowed time.

2. (original) A computer system as recited in Claim 1 wherein said allowed time is based on a configuration of said computer system.

3. (original) A computer system as recited in Claim 1 wherein said allowed time is based on timing requirements of said computer system.

4. (original) A computer system as recited in Claim 3, wherein said timing requirements are based on interrupt response times.

5. (original) A computer system as recited in Claim 1 wherein said first and second transition times are based on respective first and second voltage ramp times.

6. (original) A computer system as recited in Claim 1 wherein said sleep voltage is sufficient to maintain state of said processing unit but is not sufficient to maintain processing activity in said processing unit.

7. (original) A method of operating a computer processor, said method comprising:

transitioning from providing a sleep voltage to said computer processor to providing a first operating voltage to said computer processor within an allowed time for transitioning from a sleep state to an operating state; and

transitioning from said providing said first operating voltage to said computer processor to providing a second operating voltage to said computer processor, wherein a transition time for changing from said sleep voltage directly to said second operating voltage is greater than said allowed time for transitioning from said sleep state to said operating state.

8. (original) A method in accordance with Claim 7 wherein said second operating voltage is greater than said first operating voltage.

9. (original) A method in accordance with Claim 7 further comprising:

enabling a system clock to said computer processor when providing said first operating voltage to said computer processor; and

disabling said system clock to said computer processor when providing said sleep voltage to said computer processor.

10. (original)A method in accordance with Claim 7, wherein said sleep voltage is sufficient to maintain state of said computer processor but is not sufficient to maintain processing activity in said computer processor.

11. (original)A computer system comprising:

a processor;

an adjustable voltage supply configured to output to said processor:

a sleep voltage; and

a first operating voltage that, based on a rate of transitioning from said sleep voltage to said first operating voltage, is not achievable from said sleep voltage within an allowed time for transitioning from a sleep state to an operating state.

12. (original)A computer system as recited in Claim 11, wherein said adjustable voltage supply is further configured to output to said processor a second operating voltage that, based on a rate of transitioning from said sleep voltage to said second

operating voltage, is achievable from said sleep voltage within said allowed time for transitioning from said sleep state to said operating state.

13. (original)A computer system as recited in Claim 11 wherein said allowed time is based on a configuration of said computer system.

14. (original)A computer system as recited in Claim 11 wherein said adjustable voltage supply comprises a voltage regulator.

15. (currently amended) A computer system comprising:

a processing unit;

circuitry coupled to the processing ~~processor~~ unit, said circuitry configured to provide to said processing unit:

a first sleep voltage and a second sleep voltage;

a first operating voltage when transitioning from said first sleep voltage; and

a second operating voltage when transitioning from said second sleep voltage.

16. (original)A computer system as recited in Claim 15, wherein said circuitry is further configured to provide to said processing unit:

said first sleep voltage when transitioning from said first operating voltage; and

said second sleep voltage when transitioning from said second operating voltage.

17. (original)A computer system as recited in Claim 15 wherein a voltage difference between said first operating voltage and said first sleep voltage is approximately equal to a voltage difference between said second operating voltage and said second sleep voltage.

18. (original)A computer system as recited in Claim 15 wherein said first operating voltage is greater than said second operating voltage and wherein said first sleep voltage is greater than said second sleep voltage.

19. (original)A computer system as recited in Claim 18 wherein a voltage transition from said second sleep voltage to said first operating voltage is greater than a time allowed for transition from a sleep state to an operating state of said computer system.

20. (new) A computer system comprising:

means for processing;

means for supplying a voltage coupled to said processing means for providing to said processing means:

a first and a second sleep voltage;

a first operating voltage responsive to a transition from said first sleep voltage; and

a second operating voltage responsive to a transition from said second sleep voltage.

21. (new) The computer system of Claim 20 wherein:

said means for supplying a voltage are further for providing to said means for processing:

said first sleep voltage re responsive to a transition from said first operating voltage; and

said second sleep voltage responsive to a transition from said second operating voltage.

22. (new) The computer system of Claim 20 wherein a voltage difference between said first operating voltage and said first sleep voltage is approximately equal to a voltage difference between said second operating voltage and said second sleep voltage.

23. (new) The computer system of Claim 20 wherein said first operating voltage is greater than said second operating voltage and wherein said first sleep voltage is greater than said second sleep voltage.

24. (new) The computer system of Claim 20 wherein said means for supplying a voltage requires a greater time duration for a voltage transition from said second

sleep voltage to said first operating voltage than a time duration allowed for transition from a sleep state to an operating state of said computer system.

## REMARKS

Claims 1-24 are pending in the present application. Claims 1 and 15 are amended. Claims 20-24 are newly added. No new matter is added. Applicants respectfully request reconsideration of the present application in view of the amendments presented herein and the following remarks.

There are no art-based rejections.

## 35 U.S.C. § 112

Claims 1-19 are rejected under 35 U.S.C. § 112, first paragraph, as failing to comply with the enablement requirement. The rejection alleges that the claimed limitations of "said second transition time is within an allowed time for transitioning from a sleep state to an operating state; and wherein said first transition time is greater than said allowed time" are not supported. Applicants respectfully traverse.

At page 9 line 21 *et seq*., the present application discloses that certain time intervals are "allowed for transition to and from the deep sleep mode." An exemplary time allowance is given for transitions "to and from deep sleep."

At page 10, line 18 *et seq.*, the present application discloses, "if the exemplary processor is operating at its lowest processing core voltage of 1.2 volts (e.g., a second operating voltage), its core voltage may be lowered in the time available to 0.6-0.7 volts." However, a similar time interval may be required for a transition from a voltage of 0.9-.01 volts to a first operating voltage of 1.5 volts. Accordingly, the present application teaches that a transition from the range of 0.6-0.7 volts to a first operating voltage of 1.5 volts, e.g., a first transition time, is greater than the allowed time, which only allows for a transition from 0.6-0.7 to 1.2 volts.

While the examples cited present exemplary voltages and duration, the cited passages, as well as the application as a whole, provide enabling support for the Claims. Accordingly, Applicants respectfully solicit withdrawal of the 35 U.S.C. § 112, first paragraph, rejections.

Claim 15 is rejected under 35 U.S.C. § 112, first paragraph, as failing to comply with the enablement requirement. The rejection alleges that the claimed limitations of "a second sleep voltage " are not supported. Applicants respectfully traverse.

With reference to page 9 line 21 *et seq.*, the present application discloses that the previously disclosed embodiment of the present invention "does not reduce the voltage level as far as might be possible." The present application further describes a sleep voltage of 0.9-1.0 volts, and a lower sleep voltage of 0.6-0.7 volts.

Accordingly first and second sleep voltages are disclosed and enabled. Thus, Applicants respectfully solicit withdrawal of this 35 U.S.C. § 112, first paragraph, rejection.

Claims 1-6 and 15-19 stand rejected under 35 U.S.C. § 112, second paragraph, as being indefinite for antecedent issues. Applicants respectfully assert that amendments presented herein to independent Claims 1 and 15 correct the cited informalities, and respectfully solicit withdrawal of this rejection.

Title

The title is objected to as not descriptive. Applicants herein amend the title of the present application.

Applicants respectfully assert that the amended title is brief, technically accurate and descriptive, as required by MPEP § 606, and respectfully request withdrawal of this objection.

## CONCLUSION

Claims 1-19 are pending in the present application. Applicants respectfully request reconsideration of the present application in view of the amendments and remarks presented herein.

The Examiner is invited to contact Applicants' undersigned representative if the Examiner believes such action would expedite resolution of the present Application.

Please charge any additional fees or apply any credits to our PTO deposit account number: 504160.

Respectfully submitted,

MURABITO, HAO & BARNES LLP

Date: October 5, 2009

/Anthony C. Murabito/
Anthony C. Murabito
Reg. No. 35,295

Two North Market Street
Third Floor
San Jose, California 95113
(408) 938-9060

# Electronic Patent Application Fee Transmittal

| | |
|---|---|
| **Application Number:** | 11894991 |
| **Filing Date:** | 21-Aug-2007 |
| **Title of Invention:** | Saving power when in or transitioning to a static mode of a processor |
| **First Named Inventor/Applicant Name:** | Andrew Read |
| **Filer:** | Anthony C. Murabito/Julie Giaramita |
| **Attorney Docket Number:** | TRAN-P470 |

Filed as Large Entity

## Utility under 35 USC 111(a) Filing Fees

| Description | Fee Code | Quantity | Amount | Sub-Total in USD($) |
|---|---|---|---|---|
| **Basic Filing:** | | | | |
| **Pages:** | | | | |
| **Claims:** | | | | |
| Claims in excess of 20 | 1202 | 5 | 52 | 260 |
| Independent claims in excess of 3 | 1201 | 1 | 220 | 220 |
| **Miscellaneous-Filing:** | | | | |
| **Petition:** | | | | |
| **Patent-Appeals-and-Interference:** | | | | |
| **Post-Allowance-and-Post-Issuance:** | | | | |

| Description | Fee Code | Quantity | Amount | Sub-Total in USD($) |
|---|---|---|---|---|
| **Extension-of-Time:** | | | | |
| Extension - 1 month with $0 paid | 1251 | 1 | 130 | 130 |
| **Miscellaneous:** | | | | |
| | | | **Total in USD ($)** | **610** |

| Electronic Acknowledgement Receipt | |
|---|---|
| **EFS ID:** | 6205964 |
| **Application Number:** | 11894991 |
| **International Application Number:** | |
| **Confirmation Number:** | 9781 |
| **Title of Invention:** | Saving power when in or transitioning to a static mode of a processor |
| **First Named Inventor/Applicant Name:** | Andrew Read |
| **Correspondence Address:** | MURABITO, HAO & BARNES LLP<br>-<br>Third Floor<br>Two North Market Street<br>San Jose CA 95113<br>US 4089389060<br>- |
| **Filer:** | Anthony C. Murabito/Julie Giaramita |
| **Filer Authorized By:** | Anthony C. Murabito |
| **Attorney Docket Number:** | TRAN-P470 |
| **Receipt Date:** | 05-OCT-2009 |
| **Filing Date:** | 21-AUG-2007 |
| **Time Stamp:** | 19:51:34 |
| **Application Type:** | Utility under 35 USC 111(a) |

## Payment information:

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| Submitted with Payment | yes |
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## File Listing:

| Document Number | Document Description | File Name | File Size(Bytes)/ Message Digest | Multi Part /.zip | Pages (if appl.) |
|---|---|---|---|---|---|
| 1 | | TRAN-P059D2_AMDT_10-05-09.pdf | 64957<br>2081c5a3722250df5eeeadfdc04afdb1e6f4cc9f | yes | 13 |

| Multipart Description/PDF files in .zip description | | |
|---|---|---|
| **Document Description** | **Start** | **End** |
| Amendment/Req. Reconsideration-After Non-Final Reject | 1 | 1 |
| Specification | 2 | 2 |
| Claims | 3 | 9 |
| Applicant Arguments/Remarks Made in an Amendment | 10 | 13 |

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|---|---|---|---|---|---|
| **Warnings:** | | | | | |
| **Information:** | | | | | |
| 2 | Fee Worksheet (PTO-875) | fee-info.pdf | 33558<br>1e6adba8bfe7376ca09d86812f8cef466d0d8bb5 | no | 2 |
| **Warnings:** | | | | | |
| **Information:** | | | | | |
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**If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.**

**National Stage of an International Application under 35 U.S.C. 371**
**If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.**

**New International Application Filed with the USPTO as a Receiving Office**
**If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.**

PTO/SB/06 (07-06)
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| **PATENT APPLICATION FEE DETERMINATION RECORD**<br>Substitute for Form PTO-875 | Application or Docket Number<br>11/894,991 | Filing Date<br>08/21/2007 | ☐ To be Mailed |
|---|---|---|---|

## APPLICATION AS FILED – PART I

| | (Column 1) | (Column 2) | SMALL ENTITY ☐ | | OR | OTHER THAN SMALL ENTITY | |
|---|---|---|---|---|---|---|---|
| FOR | NUMBER FILED | NUMBER EXTRA | RATE ($) | FEE ($) | | RATE ($) | FEE ($) |
| ☐ BASIC FEE (37 CFR 1.16(a), (b), or (c)) | N/A | N/A | N/A | | | N/A | |
| ☐ SEARCH FEE (37 CFR 1.16(k), (i), or (m)) | N/A | N/A | N/A | | | N/A | |
| ☐ EXAMINATION FEE (37 CFR 1.16(o), (p), or (q)) | N/A | N/A | N/A | | | N/A | |
| TOTAL CLAIMS (37 CFR 1.16(i)) | minus 20 = | * | X $ = | | OR | X $ = | |
| INDEPENDENT CLAIMS (37 CFR 1.16(h)) | minus 3 = | * | X $ = | | | X $ = | |
| ☐ APPLICATION SIZE FEE (37 CFR 1.16(s)) | If the specification and drawings exceed 100 sheets of paper, the application size fee due is $250 ($125 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s). | | | | | | |
| ☐ MULTIPLE DEPENDENT CLAIM PRESENT (37 CFR 1.16(j)) | | | | | | | |
| * If the difference in column 1 is less than zero, enter "0" in column 2. | | | TOTAL | | | TOTAL | |

## APPLICATION AS AMENDED – PART II

| | | (Column 1) | | (Column 2) | (Column 3) | SMALL ENTITY | | OR | OTHER THAN SMALL ENTITY | |
|---|---|---|---|---|---|---|---|---|---|---|
| AMENDMENT | **10/05/2009** | CLAIMS REMAINING AFTER AMENDMENT | | HIGHEST NUMBER PREVIOUSLY PAID FOR | PRESENT EXTRA | RATE ($) | ADDITIONAL FEE ($) | | RATE ($) | ADDITIONAL FEE ($) |
| | Total (37 CFR 1.16(i)) | * 25 | Minus | ** 20 | = 5 | X $ = | | OR | X $52= | 260 |
| | Independent (37 CFR 1.16(h)) | * 5 | Minus | ***4 | = 1 | X $ = | | OR | X $220= | 220 |
| | ☐ Application Size Fee (37 CFR 1.16(s)) | | | | | | | | | |
| | ☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j)) | | | | | | | OR | | |
| | | | | | | TOTAL ADD'L FEE | | OR | TOTAL ADD'L FEE | **480** |

| | | (Column 1) | | (Column 2) | (Column 3) | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|
| AMENDMENT | | CLAIMS REMAINING AFTER AMENDMENT | | HIGHEST NUMBER PREVIOUSLY PAID FOR | PRESENT EXTRA | RATE ($) | ADDITIONAL FEE ($) | | RATE ($) | ADDITIONAL FEE ($) |
| | Total (37 CFR 1.16(i)) | * | Minus | ** | = | X $ = | | OR | X $ = | |
| | Independent (37 CFR 1.16(h)) | * | Minus | *** | = | X $ = | | OR | X $ = | |
| | ☐ Application Size Fee (37 CFR 1.16(s)) | | | | | | | | | |
| | ☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j)) | | | | | | | OR | | |
| | | | | | | TOTAL ADD'L FEE | | OR | TOTAL ADD'L FEE | |

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|---|---|---|
| | Application Number | 11894991 |
| | Filing Date | 2007-08-21 |
| | First Named Inventor | Andrew Read |
| | Art Unit | 2115 |
| | Examiner Name | Chun Cao |
| | Attorney Docket Number | TRAN-P059D2 |

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| | Examiner Name | Chun Cao |
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| | First Named Inventor | Andrew Read |
| | Art Unit | 2115 |
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| | Attorney Docket Number | TRAN-P059D2 |

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| | Filing Date | 2007-08-21 |
| | First Named Inventor | Andrew Read |
| | Art Unit | 2115 |
| | Examiner Name | Chun Cao |
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| Signature | Anthony C. Murabito | Date (YYYY-MM-DD) | 2009-10-19 |
| Name/Print | Anthony C. Murabito | Registration Number | 35295 |

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# EP0381021

Publication Title:

Power saving system.

Abstract:

In a personal computer having a logic circuit constituted by low-power consumption elements such as CMOS elements, a power saving system includes a register (41) in which control data can be set from a keyboard (29) or by software, and switches (43) for allowing and stopping power supply from a power supply to an oscillator on the basis of control data from the register. Supply of clock signals to a disabled logic circuit can be stopped by an operator's decision. In initialization processing of a driver routine of an extended card optionally connected to the personal computer, power supply designation information is set in the register. In the completion routine, power supply stop designation information is set in the register.

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(11) Publication number: **0 381 021 A2**

# (12) EUROPEAN PATENT APPLICATION

(21) Application number: 90101338.3

(51) Int. Cl.5: G06F 1/32

(22) Date of filing: 23.01.90

(30) Priority: 31.01.89 JP 19645/89

(43) Date of publication of application: 08.08.90 Bulletin 90/32

(84) Designated Contracting States: DE FR GB

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## (54) Power saving system.

(57) In a personal computer having a logic circuit constituted by low-power consumption elements such as CMOS elements, a power saving system includes a register (41) in which control data can be set from a keyboard (29) or by software, and switches (43) for allowing and stopping power supply from a power supply to an oscillator on the basis of control data from the register. Supply of clock signals to a disabled logic circuit can be stopped by an operator's decision. In initialization processing of a driver routine of an extended card optionally connected to the personal computer, power supply designation information is set in the register. In the completion routine, power supply stop designation information is set in the register.

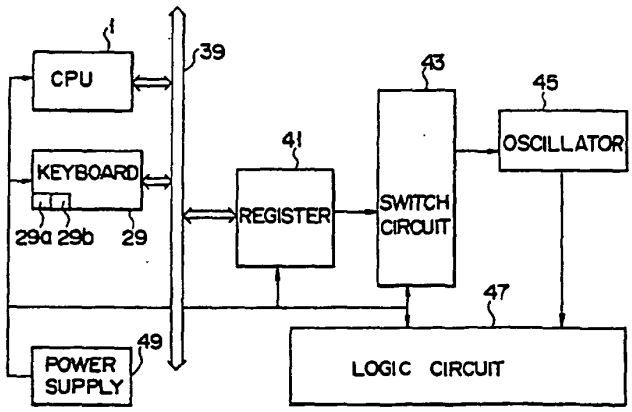



FIG. 2



EP 0 381 021 A2

# Power saving system

The present invention relates to a power saving system having a logic circuit constituted by CMOS (Complementary Metal Oxide Semiconductor) elements and applied to, e.g., a personal computer.

In recent years, various types of chips such as microprocessor, memory and LSI chips are manufactured along with developments in semiconductor technologies, and packing densities of these chips are increasing year by year. As a result, compact personal computers have been developed, and for example, compact, light-weight, portable personal computers called lap-top computers have been very popular in place of desk-top personal computers. Most of the lap-top computers are designed as battery-operated computers. For this reason, these computers are designed to minimize power consumption of the internal circuits in order to prolong the operating time.

It is known that power consumption of a CMOS is minimized when a clock pulse is not supplied. A power-saving implementation is proposed wherein LSIs (Large Scale Integration Circuits) used in internal circuits of computers are arranged by CMOS elements.

Wasteful power consumption such as power consumption required for waiting for a key input from a keyboard is still present. Strong demand has arisen for further power saving.

It is an object of the present invention to provide a power saving system which utilizes CMOS characteristics which exhibit minimum power consumption in the absence of input clock pulses, thereby performing power saving in accordance with a software instruction.

According to the first aspect of the present invention, a power saving system for a personal computer which includes a logic circuit constituted by highly integrated semiconductor elements, comprises: a power supply for supplying power; clock signal generating means for receiving the power from the power supply and supplying a clock signal to the logic circuit; keyboard means including at least a power supply designation key for designating power supply to the clock signal generating means and a power supply stop designation key for designating stop of power supply to the clock signal generating means, and for outputting power supply designation information and power supply stop designation information; latch means for latching the power supply designation information or the power supply stop designation information from the keyboard means; and switch means, connected between the latch means and the clock signal generating means, for supplying the power to the clock signal generating means on the basis of the power supply designation information supplied from the latch means and for stopping power supply to the clock signal generating means on the basis of the power supply stop designation information supplied from the latch means.

According to the second aspect of the present invention, a power saving system for a personal computer which includes a logic circuit constituted by highly integrated semiconductor elements and receives an input signal and outputs a predetermined signal, comprises: a power supply for supplying power; clock signal generating means for receiving the power from the power supply and supplying a clock signal to the logic circuit; latch means for latching power supply stop designation information; memory means for storing a control program serving as a logic circuit driver routine executed by the personal computer, the control program determining whether a predetermined signal is output from the logic circuit within a predetermined period of time and setting the power supply stop designation information in the latch means when the predetermined signal is not output within the predetermined period of time; and switch means, connected between the latch means and the clock signal generating means, for stopping power supply to the clock signal generating means on the basis of the power supply stop designation information supplied from the latch means.

According to the third aspect of the present invention, a power saving system for a personal computer, comprises: a power supply for supplying power; extended card means, optionally connectable to the personal computer, for executing a predetermined logical function; clock signal generating means for receiving the power from the power supply and supplying a clock signal to the extended card means; latch means for latching power supply designation information or power supply stop designation information; memory means for storing a program serving as an extended card driver routine executed by the personal computer, the program including an initialization routine for setting the power supply designation information in the latch means and a completion routine for setting the power supply stop designation information in the latch means after a predetermined function is executed by the extended card means; and switch means, connected between the latch means and the clock signal generating means, for supplying the power to the clock signal generating means on the basis of the power supply designation information supplied from the latch means and for stopping power supply to the clock signal generating means on the

basis of the power supply stop designation information supplied from the latch means.

Additional objects and advantages of the invention will be set forth in the description which follows, and in part will be obvious from the description, or may be learned by practice of the invention. The objects and advantages of the invention may be realized and obtained by means of the instrumentalities and combinations particularly pointed out in the appended claims.

Other objects and features of the present invention will be apparent from the following description taken in connection with the accompanying drawings, in which:

Fig. 1 is a block diagram showing an arrangement of a personal computer which employs a power saving system according the present invention;

Fig. 2 is a block diagram of a power saving system according to the first embodiment of the present invention;

Fig. 3 is a data format showing bit assignment of a register shown in Fig. 2;

Fig. 4 is a flow chart for controlling power supply upon operations of power ON and OFF keys arranged on a keyboard;

Fig. 5 is a flow chart for controlling power supply by time-out;

Fig. 6 is a flow chart in which power supply control is utilized in a driver routine of an extended card optionally connected to the power saving system; and

Fig. 7 is a block diagram showing a power saving system according to the second embodiment of the present invention.

Fig. 1 is a block diagram showing an arrangement of a personal computer which employs a power saving system according to the present invention.

Referring to Fig. 1, a CPU (Central Processing Unit) 1 controls the overall system operations of the personal computer. A ROM (Read Only Memory) 3 stores a basic input and output operating system (BIOS) program for controlling inputs/outputs of the personal computer. This BIOS includes programs represented by flow charts of Figs. 4 to 6. A RAM (Random Access Memory) 5 stores application programs executed by this personal computer and various data. A DMAC (Direct Memory Access Controller) 7 comprises a commercially available LSI for controlling DMA. A PIC (Interrupt Controller) 9 comprises a commercially available LSI for controlling various circuit interrupts. A PIT (timer) 11 measures time. An RTC (Real Time Clock) 13 comprises a commercially available LSI for storing date, time, an the like.

An HDC (Hard Disk Controller) 15 comprises a commercially available LSI for controlling an HDD (Hard Disk Driver) 17. The HDD (Hard Disk Drive) 17 serves as an external storage unit for storing programs and data. An FDC (Floppy Disk Controller) 19 comprises a commercially available LSI for controlling an FDD (Floppy Disk Drive) 21. The FDD 21 serves as an external storage unit for storing programs and data as in the HDD 17. A PRTCONT (Printer Controller) 23 controls a printer. An SIO (Serial Input and Output Control Circuit) 25 comprises a commercially available LSI for controlling communication. A KBC (Keyboard Controller) 27 comprises a commercially available LSI for controlling a keyboard 29. The keyboard 29 comprises various keys for inputting various data and includes a power ON command key 29a for designating power supply and a power OFF command key 29b for designating power of power supply. A PDPC (Plasma Display Controller) 31 controls a PDP (Plasma Display) 33. A VRAM (Video RAM) 35 serves as a memory for storing the content displayed on the PDP 33. Data is read out from a kanji ROM 37 to display kanji characters, and the readout kanji information is displayed on the PDP 33. The CPU 1, the ROM 3, the RAM 5, the DMAC 7, the PIC 9, the PIT 11, the RTC 13, the HDC 15, the FDC 19, the PRTC 23, the SIO 25, the KBC 27, the PDPC 31, the VRAM 35, and the kanji ROM 37 are connected to a system bus 39.

Fig. 2 is a block diagram showing a power saving system according to the first embodiment of the present invention.

A register 41 is connected to the system bus 39. The register 41 stores control data for ON/OFF-controlling the power supply. More specifically, the register 41 comprises, e.g., a 16-bit register. As shown in Fig. 3, bit information for controlling power ON/OFF is assigned to, e.g., bit 0. That is, when bit 0 is set at logic "1", the power is supplied to the respective circuits. However, when bit 0 is set at logic "0", the power OFF state is set. A bit output from the register 41 is supplied to a switch circuit 43. This register 41 may be assigned to the RAM 5 in the form of, e.g., a memory mapped I/O. Alternatively, I/O device addresses may be assigned to this register. In either case, the register 41 can be accessed by software.

The switch circuit 43 comprises an electronic switch (constituted by, e.g., transistors) or a relay circuit. When a bit output from the register 41 is set at logic "1", the power is supplied from a power supply 49 to an oscillator 45. However, when the bit output is set at logic "0", the power supply is stopped. When the oscillator 45 receives the power through the switch circuit 43, the oscillator 45 outputs a clock signal to a logic circuit 7. The power supply 49 is connected to supply the power to the CPU 1, the keyboard 29, the register 41, the switch circuit 43, and the logic circuit 47. The logic

circuit 47 comprises a CMOS circuit for performing a predetermined function. For example, in the block diagram of Fig. 1, the logic circuit 47 corresponds to the DMAC 7, the PIC 9, the PIT 11, the RTC 13, the FDC 19, the PRTC 23, the SIO 25, the KBC27, the PDC 31, and the like. Although not illustrated, the logic circuit 47 also includes a LAN (Local Area Network) controller and a MODEM (Modulator Demodulator).

Power supply or stop of power supply can be designated automatically or by an operator. The flow chart shown in Fig. 4 exemplifies an operation for detecting depression of the power OFF or ON command key 29a or 29b arranged on the keyboard 29 and for allowing or stopping power supply from the power supply to the oscillator 45.

The CPU 1 determines in step 51 whether a key input is detected. If YES in step 51, the CPU 1 determines in step 53 whether the depressed key is the power OFF command key 29a. If YES in step 53, data "01" (hex) is set in the register 41 in step 55. As a result, bit data of "1" is supplied from the register 41 to the switch circuit 43, and then the switch circuit 43 supplies the power from the power supply 49 to the oscillator 45. Therefore, the oscillator 45 supplies a clock signal to the logic circuit 47, and the logic circuit is operated.

When the CPU 1 determines in step 57 that the power ON command key 29b is depressed, the CPU 1 sets data "00" (hex) in the register 41 in step 59.

Bit data of "0" is supplied from the register 41 to the switch circuit 43, and the switch circuit 43 does not supply the power to the oscillator 45. In this case, no clock signal is supplied from the oscillator 45 to the logic circuit 47. The power consumption of the logic circuit 47 becomes minimum, and the power can be saved.

Fig. 5 is a flow chart showing an operation for automatically controlling power supply to the KBC (Keyboard Controller) 27.

The CPU 1 determines in step 61 whether a key input is detected. If NO in step 61, a time-measuring software counter is incremented in step 63. The CPU 1 then determines in step 65 whether a predetermined period of time has elapsed. If NO in step 65, the CPU 1 repeats the operations in steps 61, 63, and 65. When the CPU 1 determines in step 65 that the predetermined period of time has elapsed, the CPU 1 sets data "00" (hex) in the register 41 in step 67. As described above, in this case, the switch circuit 43 does not supply the power to the oscillator 45, and the oscillator 45 does not supply the clock signal to the logic circuit 47 accordingly. As a result, the power consumption of the logic circuit 47 becomes minimum, and the power can be saved.

Fig. 6 is a flow chart showing an operation for automatically controlling power supply or stop of power supply when, e.g., a LAN drive routine is loaded or unloaded.

Assume that the system bus of the personal computer shown in Fig. 1 is connected to an external connector (not shown), and that a LAN control card serving as an extended card can be optionally connected to this personal computer. In this case, the LAN driver routine is prestored in the HDD 17. In order to perform LAN control, the LAN driver routine stored in the HDD 17 is loaded in the RAM 5 and is executed by the CPU 1.

In step 71 as an initialization routine, the CPU 1 sets data "01" (hex) in the register 41. The switch circuit 43 supplies the power to the oscillator 45, and the oscillator 45 then supplies a clock signal to the logic circuit 47 (in this case, to the LAN card). The LAN card is then operated. After the predetermined LAN processing routine is executed, the CPU 1 performs completion processing in step 73. In this completion processing, the CPU 1 sets data "00" (hex) in the register 41. In this case, the switch circuit 43 stops supplying the power to the oscillator 45. Therefore, the power consumption of the LAN card becomes minimum, and the power can be saved.

Fig. 7 is a block diagram of a power saving system according to the second embodiment of the present invention. The same reference numerals as in Fig. 1 denote the same parts in Fig. 2, and a detailed description thereof will be omitted.

In the embodiment shown in Fig. 7, power from a power supply 49 is always supplied to an oscillator 45. A clock signal is supplied from the oscillator 45 to a gate circuit 75. The gate circuit 75 comprises, e.g., an AND gate and supplies a clock signal from the oscillator 45 to a logic circuit 47 in response to an enable signal from a CPU 1. The enable signal supplied from the CPU 1 may be supplied from a keyboard as in Fig. 2 or may be obtained by utilizing the concept of time-out, as shown in Fig. 4, or an enable or disable signal may be formed in the initialization and completion routines in the extended load module, as shown in Fig. 6. The same effect as in the embodiment of Fig. 2 can be obtained in the above modifications.

In the second embodiment, the LAN card is exemplified as the extended card. However, the present invention is not limited to this. For example, power supply of various external optional cards such as an SCSI (Small Computer System Interface) control card, various communication boards, a keyboard controller, a printer controller, a display circuit controller, and a modem card can be controlled.

In the above embodiment, the programs shown in Figs. 4 to 6 are stored in the ROM 3. However, these programs may be stored in, e.g., the HDD 17

and the FDD 21.

Additional advantages and modifications will readily occur to those skilled in the art. Therefore, the invention in its broader aspects is not limited to the specific details, representative devices, and illustrated examples shown and described. Accordingly, departures may be made from such details without departing from the spirit or scope of the general inventive concept as defined by the appended claims and their equivalents.

## Claims

1. A power saving system for a personal computer having a logic circuit (47) constituted by highly integrated semiconductor elements, a power supply (49) for supplying power, and an oscillator (45) for receiving the power from said power supply and supplying a clock signal to said logic circuit, characterized by comprising:
means (29a, 29b, Figs. 4, 5, and 6) for designating supply and stop of supply of the clock signal to said logic circuit; and
control means (41, 43, 75) for controlling the supply or the stop of supply of the clock signal to said logic circuit in response to designation information from said designating means.

2. A system according to claim 1, characterized in that said designating means comprises a keyboard (29) including at least a power supply designation key (29a) for designating power supply from said power supply to said oscillator and a power supply stop key (29b) for designating stop of power supply from said power supply to said oscillator, said keyboard (29) being arranged to output power supply designation information and power supply stop designation information.

3. A system according to claim 1, characterized in that said logic circuit receives an input signal and outputs a predetermined signal, and
said designating means comprises memory means (3, 17, 21) for storing a control program serving as a logic circuit driver routine executed by said personal computer, the control program setting the power supply stop designation information when the predetermined signal is not output from said logic circuit within a predetermined period of time.

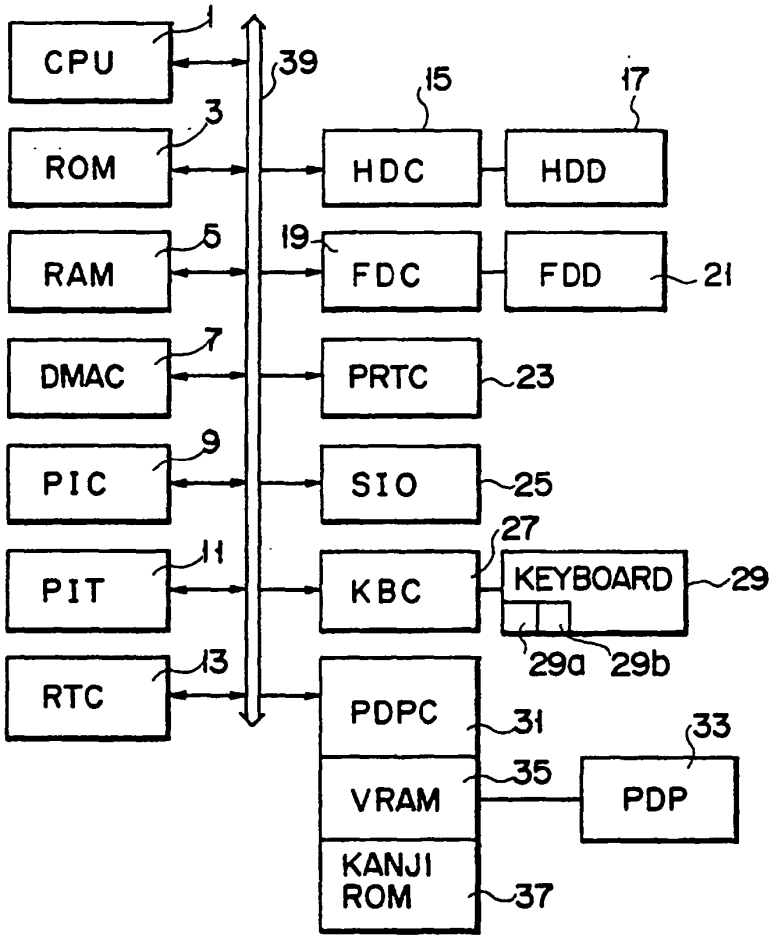
4. A system according to claim 1, characterized in that said logic circuit includes optional extended card means, connectable to said personal computer, for executing a predetermined logic function, and said designating means comprises memory means for storing a program serving as an extended card driver routine executed by said personal computer, the control program including an initialization routine for outputting power supply designation information and a completion routine for outputting the power supply stop designation information after the predetermined function is performed by said extended card means.

5. A system according to any one of claims 1 to 4, characterized in that said control means comprises:
latch means (41) for latching information for designating supply and stop of supply of the clock signal; and
switch means (43), connected between said latch means and said oscillator, for supplying the power to said oscillator on the basis of the clock supply designation information supplied from said latch circuit and for stopping power supply to said oscillator on the basis of the clock supply stop designation information supplied from said latch circuit.

6. A system according to any one of claims 1 to 4, characterized in that said control means comprises gate means (75), connected between said oscillator and said logic circuit, for receiving the clock supply designation information and supplying the clock signal from said oscillator to said logic circuit, and for stopping supply of the clock signal to said logic circuit on the basis of the clock supply stop designation information.

7. A system according to any one of claims 1 to 6, characterized in that said logic circuit comprises CMOS (Complementary Metal Oxide Semiconductor) elements.

8. A system according to any one of claims 1 to 7, characterized in that said logic circuit includes a LAN (Local Area Network) control circuit, an SCSI (Small Computer System Interface) control circuit, a communication board, a keyboard controller, a printer controller, a display controller, and a model control circuit.


CPU
1
39
ROM
3
HDC
15
HDD
17
RAM
5
FDC
19
FDD
21
DMAC
7
PRTC
23
PIC
9
SIO
25
PIT
11
KBC
27
KEYBOARD
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29a
29b
RTC
13
PDPC
31
33
VRAM
35
PDP
KANJI ROM
37

FIG. 1

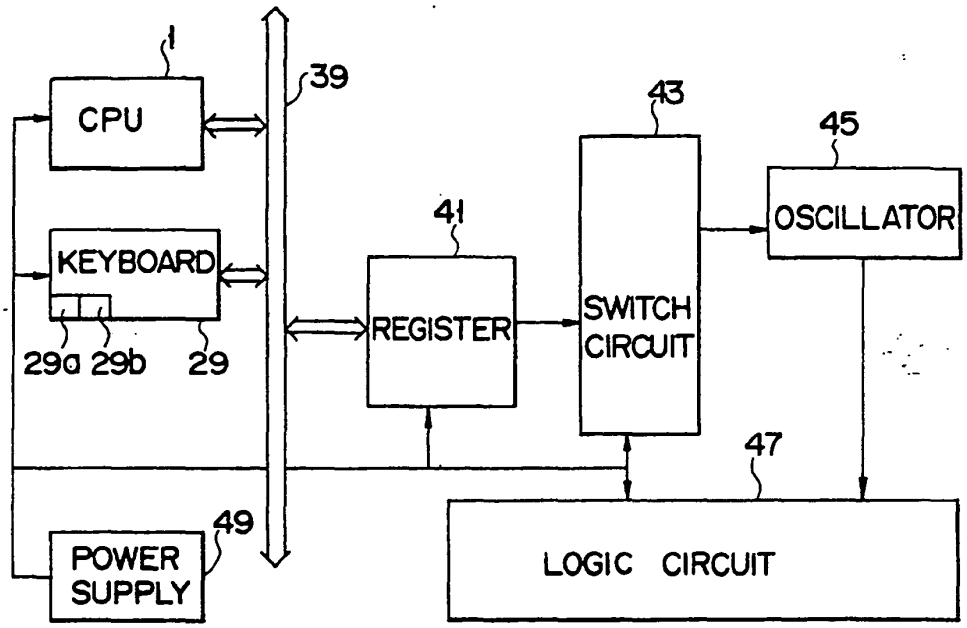
1
39
CPU
43
45
41
KEYBOARD
OSCILLATOR
REGISTER
SWITCH CIRCUIT
29a 29b 29
47
49
POWER SUPPLY
LOGIC CIRCUIT

FIG. 2

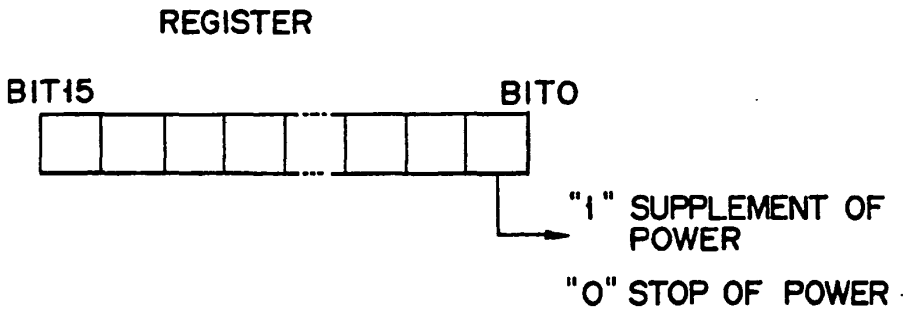
REGISTER
BIT15
BIT0
"1" SUPPLEMENT OF POWER
"0" STOP OF POWER

FIG. 3

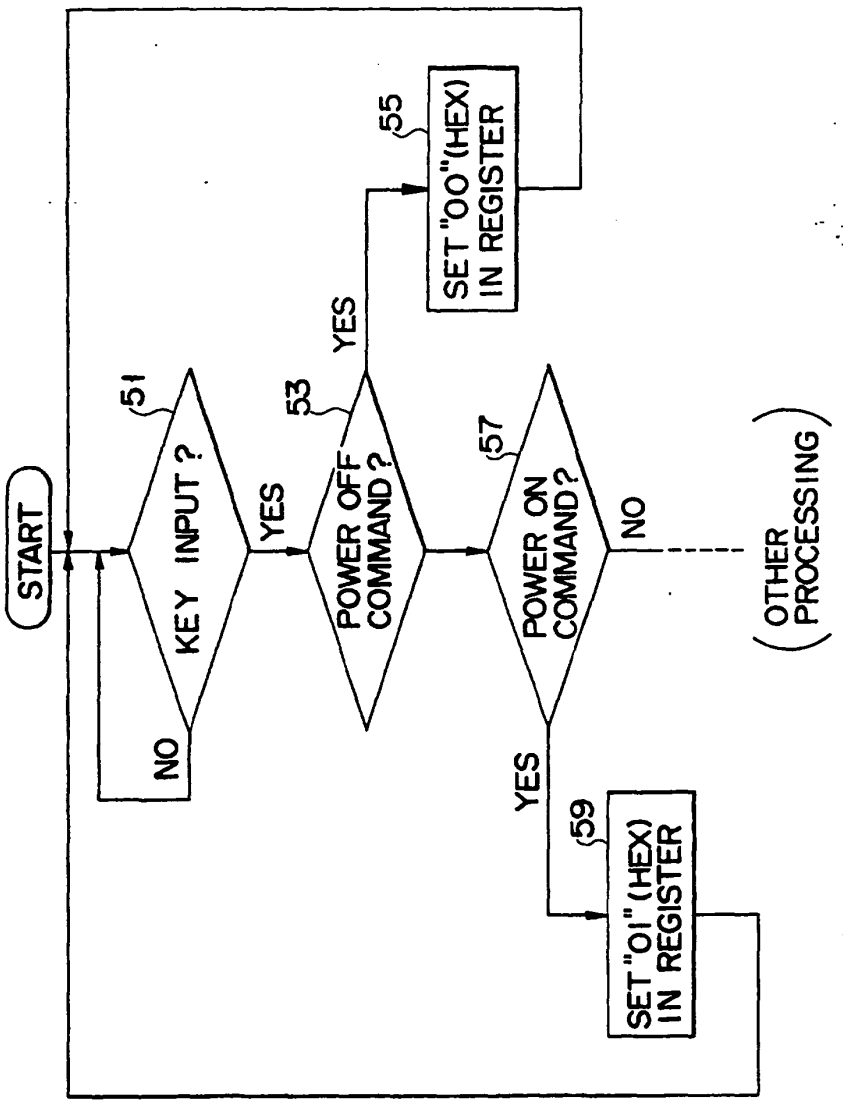
START
KEY INPUT ?
51
NO
YES
POWER OFF COMMAND ?
53
YES
SET "00" (HEX) IN REGISTER
55
POWER ON COMMAND ?
57
NO
(OTHER PROCESSING)
YES
SET "01" (HEX) IN REGISTER
59

FIG. 4

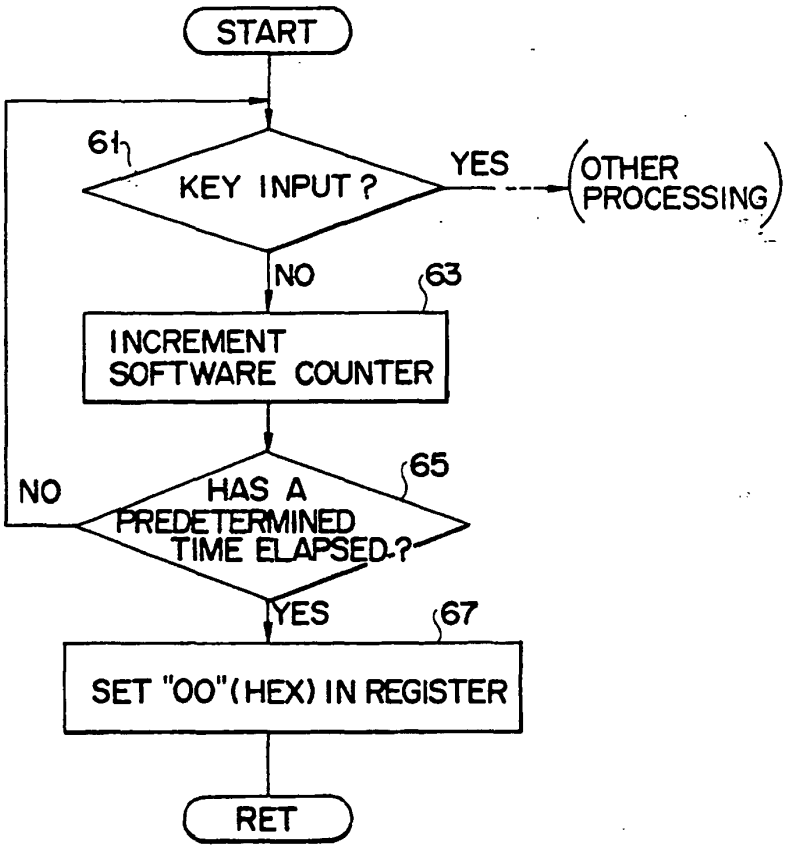


FIG. 5

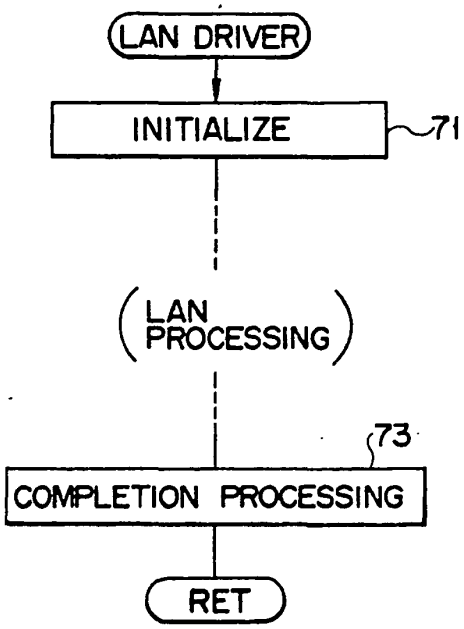
LAN DRIVER
INITIALIZE
71
LAN PROCESSING
73
COMPLETION PROCESSING
RET

FIG. 6

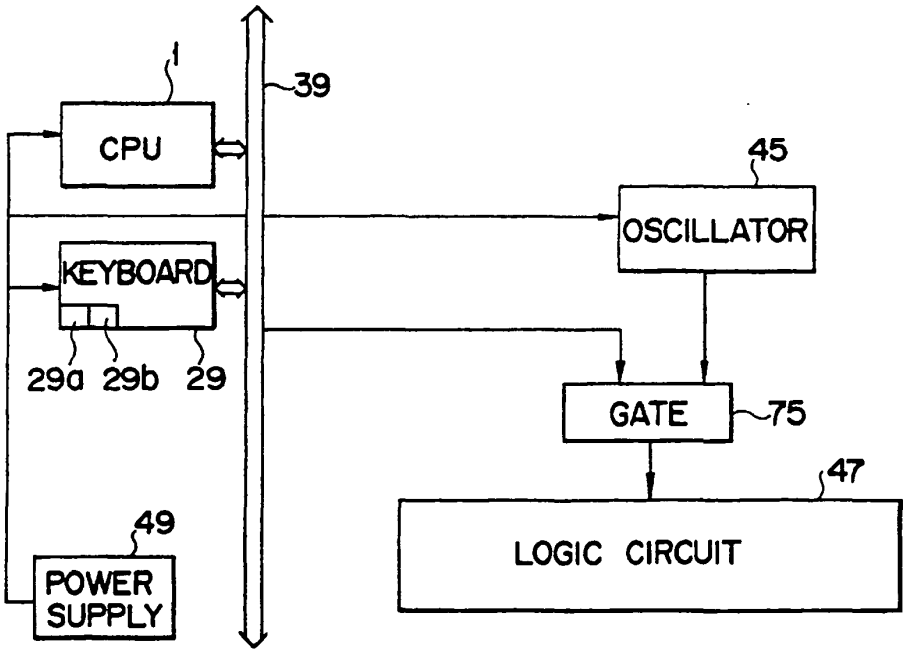
1
39
CPU
45
OSCILLATOR
KEYBOARD
29a
29b
29
GATE
75
47
LOGIC CIRCUIT
49
POWER SUPPLY

FIG. 7

| Electronic Patent Application Fee Transmittal | |
|---|---|
| **Application Number:** | 11894991 |
| **Filing Date:** | 21-Aug-2007 |
| **Title of Invention:** | Saving power when in or transitioning to a static mode of a processor |
| **First Named Inventor/Applicant Name:** | Andrew Read |
| **Filer:** | Anthony C. Murabito/Julie Giaramita |
| **Attorney Docket Number:** | TRAN-P470 |
| Filed as Large Entity | |

**Utility under 35 USC 111(a) Filing Fees**

| Description | Fee Code | Quantity | Amount | Sub-Total in USD($) |
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| **Basic Filing:** | | | | |
| **Pages:** | | | | |
| **Claims:** | | | | |
| **Miscellaneous-Filing:** | | | | |
| **Petition:** | | | | |
| **Patent-Appeals-and-Interference:** | | | | |
| **Post-Allowance-and-Post-Issuance:** | | | | |
| **Extension-of-Time:** | | | | |

| Description | Fee Code | Quantity | Amount | Sub-Total in USD($) |
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| **Miscellaneous:** | | | | |
| Submission- Information Disclosure Stmt | 1806 | 1 | 180 | 180 |
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| **EFS ID:** | 6288900 |
| **Application Number:** | 11894991 |
| **International Application Number:** | |
| **Confirmation Number:** | 9781 |
| **Title of Invention:** | Saving power when in or transitioning to a static mode of a processor |
| **First Named Inventor/Applicant Name:** | Andrew Read |
| **Correspondence Address:** | MURABITO, HAO & BARNES LLP<br>-<br>Third Floor<br>Two North Market Street<br>San Jose CA 95113<br>US 4089389060<br>- |
| **Filer:** | Anthony C. Murabito/Julie Giaramita |
| **Filer Authorized By:** | Anthony C. Murabito |
| **Attorney Docket Number:** | TRAN-P470 |
| **Receipt Date:** | 19-OCT-2009 |
| **Filing Date:** | 21-AUG-2007 |
| **Time Stamp:** | 19:16:17 |
| **Application Type:** | Utility under 35 USC 111(a) |

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| | |
|---|---|
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| Deposit Account | |
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| **Warnings:** | | | | | |
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| 6 | NPL Documents | GOVIL.pdf | 642937<br>da37bf50598576961ef98fe660347a81cf9ac56c | no | 13 |
| **Warnings:** | | | | | |
| **Information:** | | | | | |
| 7 | NPL Documents | HIGH_SPEED.pdf | 850742<br>ca630a7003c40f943534d129499351249 05ae28a | no | 16 |
| **Warnings:** | | | | | |
| **Information:** | | | | | |
| 8 | NPL Documents | HIGH_SPEED_DIGITALLY.pdf | 1685758<br>89380bd2cdf15af48305cb993ed2bc6ec75de8f4 | no | 28 |

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| **Information:** | | | | | |
| 9 | NPL Documents | HIGH_SPEED_MAX17101711.pdf | 134656<br>25da96707c9fc1d0b93cc15421c91b71f3af6559 | no | 2 |
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| **Information:** | | | | | |
| 10 | NPL Documents | MADHAV.pdf | 418329<br>4ad0de90e117f669d970bfffa636040791d65b12 | no | 6 |
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| **Information:** | | | | | |
| 11 | NPL Documents | MANUAL_FOR_KINETIZ.pdf | 1676872<br>45c0625eecc9dedba8c522bb8854d4b5ecb14953 | no | 54 |
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| **Information:** | | | | | |
| 12 | NPL Documents | OPERATION_U.pdf | 98951<br>e924ce4e4a4b08694edbfd0e75d80a517305e2fd | no | 1 |
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| 13 | NPL Documents | PENTIUM_III_PROCESSOR_DATASHEET.pdf | 1583194<br>6d2615aa398405fced2a7a9e392433374149 8c6e | no | 32 |
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| 14 | NPL Documents | SUPER_SOUTH.pdf | 6214170<br>57d2f1b770d89c54814b5b56d8d707e6efe0dc30 | no | 129 |
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| 15 | NPL Documents | WEISER.pdf | 724767<br>b39e89282dad9aa8511dbb96b73fecfce32860e0 | no | 12 |
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| 16 | Fee Worksheet (PTO-875) | fee-info.pdf | 30235<br>7fdcb367089102224820c7d68cdfd348c6cdb09e | no | 2 |
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PTO/SB/08a (07-09)
Approved for use through 07/31/2012. OMB 0651-0031
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE



| **INFORMATION DISCLOSURE STATEMENT BY APPLICANT** ( **Not for submission under 37 CFR 1.99)** | | |
|---|---|---|
| | Application Number | 11894991 |
| | Filing Date | 2007-08-21 |
| | First Named Inventor | Andrew Read |
| | Art Unit | 2115 |
| | Examiner Name | Chun Cao |
| | Attorney Docket Number | TRAN-P059D2 |

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| | 2 | 6415388 | | 2002-07-02 | Browning , et al. | |
| | 3 | 6427211 | | 2002-07-30 | Watts, Jr. | |
| | 4 | 6477654 | | 2002-11-05 | Dean , et al. | |
| | 5 | 6487668 | | 2002-11-26 | Thomas , et al. | |
| | 6 | 6510400 | | 2003-01-21 | Moriyama | |
| | 7 | 6510525 | | 2003-01-21 | Nookala , et al. | |
| | 8 | 6513124 | | 2003-01-28 | Furuichi , et al. | |

| INFORMATION DISCLOSURE STATEMENT BY APPLICANT ( Not for submission under 37 CFR 1.99) | | |
|---|---|---|
| | Application Number | 11894991 |
| | Filing Date | 2007-08-21 |
| | First Named Inventor | Andrew Read |
| | Art Unit | 2115 |
| | Examiner Name | Chun Cao |
| | Attorney Docket Number | TRAN-P059D2 |

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|---|---|---|---|---|---|---|
| | 9 | 6519706 | | 2003-02-11 | Ogoro | |
| | 10 | 6574739 | | 2003-06-03 | Kung , et al. | |

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| | 2 | 20020073348 | | 2002-06-13 | Tani, Takenobu | |
| | 3 | 20020083356 | | 2002-06-27 | Dai, Xia | |
| | 4 | 20020087896 | | 2002-07-04 | Cline, Leslie E. ; et al. | |
| | 5 | 20020138778 | | 2002-09-26 | Cole, James R. ; et al. | |
| | 6 | 20030065960 | | 2003-04-03 | Rusu, Stefan ; et al. | |
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| | Art Unit | 2115 |
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# EP0474963

Publication Title:

Computer system having sleep mode function.

Abstract:

A personal computer having a sleep mode function for reducing power consumption by lowering the frequency of a clock pulse to be supplied to a CPU includes a clock control circuit (18) for generating a high-frequency first clock pulse, and a low-frequency second clock pulse. When a power supply is turned on, an initial program loader (IPL) discriminates whether or not an AC adapter (105) is connected. The computer also includes a sleep mode controller (16) for, when the AC adapter is connected, disabling a signal, to be supplied to the clock control circuit, for instructing generation of the second clock pulse.

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(19) Europäisches Patentamt
European Patent Office
Office européen des brevets

(11) Publication number: 0 474 963 A2

# (12) EUROPEAN PATENT APPLICATION

(21) Application number: 91106249.5

(51) Int. Cl.5: G06F 1/32

(22) Date of filing: 18.04.91

(30) Priority: 13.09.90 JP 241082/90
27.09.90 JP 255069/90
11.04.91 JP 78927/91

(43) Date of publication of application:
18.03.92 Bulletin 92/12

(84) Designated Contracting States:
DE FR GB

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## (54) Computer system having sleep mode function.

(57) A personal computer having a sleep mode function for reducing power consumption by lowering the frequency of a clock pulse to be supplied to a CPU includes a clock control circuit (18) for generating a high-frequency first clock pulse, and a low-frequency second clock pulse. When a power supply is turned on, an initial program loader (IPL) discriminates whether or not an AC adapter (105) is connected. The computer also includes a sleep mode controller (16) for, when the AC adapter is connected, disabling a signal, to be supplied to the clock control circuit, for instructing generation of the second clock pulse.

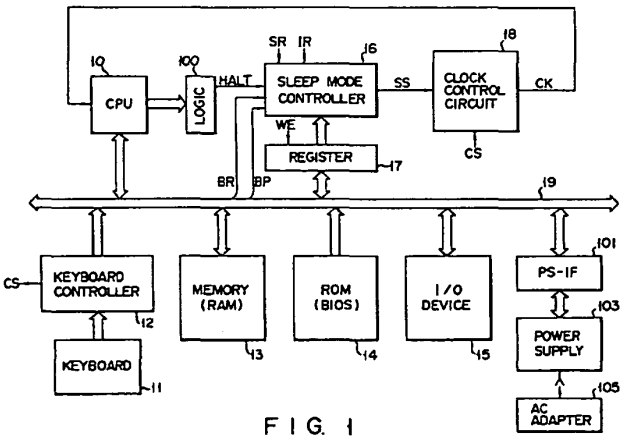


FIG. 1

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The present invention relates to a personal computer and, more particularly, to a computer system having a sleep mode function of decreasing a processing speed of a CPU to save power of the system (i.e., to reduce power consumption).

In recent years, a lap-top type personal computer which employs a battery (rechargeable internal battery) as a power supply for a computer system has been developed. Such a computer must have some means for saving power since continuous use of its power supply is limited.

For the purpose of saving power of the power supply, a so-called sleep mode function of decreasing a processing speed of a CPU (microprocessor) under a predetermined condition is known. When no input/output (I/O) operation is performed, the CPU does not require a normal processing speed (relatively high speed), and the processing speed of the CPU can be decreased. The processing speed of the CPU is determined by the frequency of a clock pulse. For this reason, the sleep mode function switches a high-frequency clock pulse normally supplied to the CPU to a low-frequency clock pulse, and supplies it to the CPU.

When the following conditions are satisfied, the sleep mode function is started upon execution of a HALT instruction by a basic input and output system (BIOS).

(1) Although a keyboard control routine of the BIOS is executed, no key input data is set in a key buffer.

(2) No key input data is set in the key buffer, and the CPU is in an idle state.

On the other hand, the sleep mode function is released when an external interrupt, e.g., a timer interrupt occurs, or when the CPU is reset. Once the sleep mode function is released, it will not be enabled unless the BIOS executes a HALT instruction again.

In order to enable the sleep mode function, the BIOS must execute a HALT instruction under the above-mentioned conditions. When the sleep mode function is permitted to be enabled, the BIOS must always monitor whether the above-mentioned conditions are satisfied. More specifically, time is undesirably wasted for processing which is not associated with actual execution of a program.

When the sleep mode function is enabled, and when it is released in response to an interrupt (e.g., a timer interrupt for monitoring a status of the system) or resetting of the CPU, the low-frequency clock (e.g., 4 MHz) must be restored to the high-frequency clock (32 MHz). This operation requires a plurality of cycles, and time is wasted for processing which is not associated with actual execution of the program, as described above.

As described above, the sleep mode function is set to prolong a battery driving time by reducing power consumption. Therefore, when the computer receives an external power supply, e.g., when an AC adapter is connected to the computer, a power supply from the AC adapter has priority over a power supply from the battery. Therefore, the sleep mode function need not be enabled.

However, the sleep mode function of a conventional battery driven personal computer is enabled as long as the conditions are satisfied even when the computer is operated by a mounted battery, and when it receives an external power supply, e.g., when it is operated by an externally connected AC adapter or when it receives power from a master station which can be connected to the battery driven personal computer. Therefore, the processing speed of a program is decreased, and performance of the personal computer cannot be fully exhibited.

It is an object of the present invention to provide a personal computer which can disable a sleep mode function when the personal computer which is battery driven is operated by externally supplied power, and can fully exhibit its performance.

In order to achieve the above object, according to the present invention, a computer system having a sleep mode function, comprises: processor means for performing various data processing operations; clock control means for selecting one of a first clock pulse at a predetermined high frequency required in a normal mode of the processor means, and a second clock pulse at a predetermined low frequency required in a sleep mode of the processor means, and supplying the selected clock pulse to the processor means; discrimination means for discriminating whether or not the computer system receives an external power supply; and sleep operation control means for, when the discrimination means discriminates that the computer system receives an external power supply, prohibiting the clock control means to supply the second clock pulse to the processor means.

According to the present invention, the computer can automatically recognize that power is externally supplied, and can automatically disable the sleep mode function. As a result, a personal computer having a sleep mode function, which can fully exhibit its performance can be provided.

This invention can be more fully understood from the following detailed description when taken in conjunction with the accompanying drawings, in which:

Fig. 1 is a block diagram showing a personal computer having a sleep mode function according to an embodiment of the present invention;

Fig. 2 is a detailed circuit diagram of a sleep mode controller shown in Fig. 1;

Fig. 3 is a detailed circuit diagram of a logic

circuit shown in Fig. 1;

Fig. 4 is a detailed circuit diagram of a clock control circuit shown in Fig. 1;

Fig. 5 is a detailed circuit diagram of a circuit for discriminating connection of an AC adapter; and

Figs. 6A and 6B are flow charts showing an operation of the embodiment shown in Fig. 1.

Fig. 1 is a block diagram showing a personal computer having a sleep mode function according to an embodiment of the present invention. The personal computer shown in Fig. 1 is a lap-top type personal computer which can be operated by a rechargeable battery. As shown in Fig. 1, this system comprises a microprocessor 10 constituting a central processing unit (CPU), a keyboard 11, a keyboard controller (KBC) 12, a memory 13, a read only memory (ROM) 14 for storing a basic input and output system (BIOS), an I/O device 15, and a power supply 103 connected to a system bus 19 via a power supply control interface (PS-IF) 101.

The keyboard 11 and the KBC 12 constitute an input device for inputting data upon various key operations on the keyboard 11. The memory 13 comprising a random access memory (RAM) constitutes various registers such as key buffers for storing data inputted from the keyboard 11. As described above, the ROM 14 stores the BIOS for performing an I/O control operation. The I/O device 15 is an external storage device such as a floppy disk drive.

The system further comprises a sleep mode controller 16 and a control register 17. The sleep mode controller 16 discriminates based on a command outputted from, e.g., the CPU 10 whether or not predetermined conditions for executing a sleep mode are satisfied. If the predetermined conditions are satisfied, the sleep mode controller 16 outputs a control signal SS to a clock control circuit 18. The control register 17 stores mode control data for enabling or disabling execution of a control operation of the sleep mode controller 16.

The clock control circuit 18 generates a clock pulse CK for determining a processing speed of the CPU 10, as shown in Fig. 4. A clock generator 40 generates clock pulses NCK1 and NCK2 necessary for a normal operation (high-speed processing) of the CPU 10, and a low-frequency (e.g., 4 MHz) clock pulse SCK necessary for the sleep mode. The clock pulse NCK1 is a high-frequency (e.g., 32 MHz) pulse, and the clock pulse NCK2 is a high-frequency (e.g., 16 MHz) pulse. The clock control circuit 18 comprises first and second clock switching circuits 41 and 42.

The first clock switching circuit 41 selects one of the clock pulses NCK1 and NCK2 on the basis of a clock switch signal CS outputted from the KBC 12, and outputs the selected pulse as a normal-mode clock pulse NCK. The first clock switching circuit 41 is constituted by a logic circuit comprising AND gates 41a and 41b, an OR gate 41c, and an inverter 41d. The second clock switching circuit 42 selects and outputs the clock pulse SCK in accordance with the clock switch signal SS from the sleep mode controller 16 in the sleep mode, and selects and outputs the clock pulse NCK from the first clock switching circuit 41 in the normal mode. The second clock switching circuit 42 is constituted by a logic circuit comprising AND gates 42a and 42b, an OR gate 42c, and an inverter 42d.

The sleep mode controller 16 has a circuit shown in Fig. 2. More specifically, the controller 16 is a logic circuit comprising AND gates 20a and 20b, flip-flops 21a through 21e, NAND gates 22a and 22b, inverters 23a and 23b, an OR gate 24, and buffer circuits 25a and 25b. The first input terminal of the AND gate 20a receives the mode control data CD stored in the control register 17, and the second input terminal thereof receives a HALT instruction from the CPU 10. When the HALT instruction is at logic level "H" (High), it becomes a significant signal. When the mode control data CD is at logic level "H", the sleep mode is disabled, and when it is at logic level "L" (low), the sleep mode is enabled. Therefore, when the mode control data CD at logic level "L" is stored in the control register 17, and the HALT instruction at logic level "H" is inputted, the AND gate 20a outputs a signal at logic level "H" to the OR gate 24. The control register 17 is set in a write enable state in response to a write enable signal WE generated by decoding an I/O address outputted from the CPU 10. The mode control data CD is set in the control register 17 by the CPU 10 on the basis of a content (whether the sleep mode is enabled or disabled) set in a setup menu or a pop-up menu by a user via the keyboard 11.

The first input terminal of the NAND gate 22a receives a system reset signal SR1, and the second input terminal thereof receives a sleep mode release signal (interrupt request) IR. The system reset signal SR1 is a reset signal (logic level "H") outputted from a gate array (not shown). The gate array generates the reset signal upon reception of a power ON/OFF signal from the power supply 103 or upon reception of a control signal from the keyboard 11. The release signal IR is a power OFF signal (power ON reset signal) outputted from the power supply 103, or an interrupt signal from an interrupt controller (not shown). The first input terminal of the NAND gate 22b receives, e.g., a signal BR outputted from a DMA controller (not shown) to request release of the system bus 19, and the second input terminal thereof receives a signal BP outputted from the CPU 10 to enable use of the system bus 19. The signals BR and BP which are significant at logic level "H" are generated when a

file is to be accessed. For this reason, when a file is not accessed, the signals BR and BP are at logic level "L". The clock terminals of the flip-flops 21a through 21e receive a clock CLK from a clock generator (not shown). The AND gate 20b outputs the control signal SS as an output signal from the controller 16. When the mode control data CD is at logic level "L", the HALT instruction is at logic level "H", and the signals BR and BP are at logic level "L". As a result, the AND gate 20b outputs the "H"-level control signal SS which means to setting of the sleep mode. When one of the system reset signal SR1 and the release signal IR is at logic level "H", the sleep mode is released. When the "H"-level mode control data CD which means prohibition of the control operation of the sleep mode controller 16 is set in the control register 17, the sleep mode is released. In Fig. 2, the flip-flops 21c and 21d are arranged to synchronize the system reset signal SR1 and the interrupt signal IR with the HALT signal. More specifically, the system reset signal SR1 and the interrupt signal IR are generated at arbitrary timings. However, the HALT signal is generated by decoding the HALT instruction by the CPU upon an instruction from the BIOS. Therefore, the HALT signal and the system reset signal SR1 or the interrupt signal IR are synchronized with each other. Fig. 2 shows system result signals SR1 and SR0. The system reset signal SR0 is an inverted signal of SR1. More specifically, the system reset signal SR1 goes active at logic "1" ("H"), and the system reset signal SR0 goes active at logic "0" ("L"). The HALT instruction is generated by a status decode circuit shown in Fig. 3 (a logic circuit 100 shown in Fig. 1). This circuit comprises AND gates 30a through 30c, and inverters 31a and 31b. The CPU 10 outputs various status signals MI, WR, DC, BH, BL, and AS to the status decode circuit. The signal MI means memory access when it is at logic level "H"; and means I/O access when it is at logic level "L". The signal WR means a write mode when it is at logic level "H"; and means a read mode when it is at logic level "L". The signal DC means data when it is at logic level "H"; and means a command when it is a logic level "L". For example, when 16-bit data is to be accessed, the signal BH at logic level "H" means that an upper byte of data is enabled, and the signal BL at logic level "H" means that a lower byte of the data is enabled. When the signal AS is at logic level "H" it means that an address signal is correct. When the status decode circuit receives the "H"-level signal MI, the "H"-level signal WR, the "L"-level signal DC, the "H"-level signal BH, the "L"-level signal BL, and "H"-level signal AS, it causes the AND gate 30a to output the "H"-level HALT instruction.

Fig. 5 is a circuit for discriminating that an AC adapter 105 is connected as an external power supply. An output voltage from the AC adapter 105 is voltage-divided by voltage-dividing resistors 107 and 109, and the divided voltage is supplied to the input terminal of a sub CPU 121 in the power supply 103. An analog divided voltage supplied to the input terminal A is converted into a digital value by an internal first A/D converter 111. An output voltage from a battery 113 is voltage-divided by voltage-dividing resistors 115 and 117, and the divided voltage is supplied to an input terminal B of the sub CPU 121. The sub CPU 121 has a ground terminal. One of the output terminals of the AC adapter 105 and the battery 113 is connected to the ground terminal via the voltage-dividing resistors, and the other output terminal is directly connected to the ground terminal. When the AC adapter 105 is connected, a voltage divided by the voltage-dividing resistors 107 and 109 is supplied to the terminal A, and is converted into a digital value by the A/D converter 111. Therefore, the sub CPU 121 reads an output value from the A/D converter 111 to detect connection of the AC adapter 105. Data indicating connection of the AC adapter 105 is outputted onto the system bus 19 via the PS-IF 101. The CPU 10 receives the connection data of the AC adapter 105 when the BIOS (e.g., an initial program loader (IPL)) stored in the ROM 14 is executed, and sets the "H"-level mode control data CD in the register 17.

The operation of this embodiment will be described below with reference to the flow charts shown in Figs. 6A and 6B.

When the power supply of the battery in the power supply 103 is set ON, the clock generator 40 in the clock control circuit 18 is activated, and generates the clock pulses NCK1, NCK2, and SCK (steps S1 and S3). The first clock switching circuit 41 selects the clock pulse NCK1 or NCK2 in accordance with the clock switch signal CS outputted from the KBC 12, and outputs the selected pulse as a normal-mode clock pulse. When the predetermined conditions for setting the sleep mode are not satisfied, the sleep mode controller 16 outputs the "L"-level control signal SS to the clock control circuit 18. In other words, the second clock switching circuit 42 of the clock control circuit supplies the clock pulse NCK as the clock CK to the CPU in a normal mode. In response to the clock pulse NCK (NCK1 or NCK2), the CPU 10 performs normal high-speed data processing (normal mode).

The CPU 10 checks in step S5 if the AC adapter 105 is connected. If the CPU 10 determines in step S5 that the AC adapter 105 is connected, the flow advances to step S17. On the other hand, if it is determined in step S5 that the AC adapter 105 is not connected, the CPU 10 checks in step S7 if the "H"-level mode control

data CD indicating that the control operation of the sleep mode controller 16 is to be prohibited is set in the control register 17. If YES in step S7, the CPU 10 advances the flow to step S17. On the other hand, if NO in step S7, the CPU 10 enables the sleep mode in step S9. More specifically, the CPU 10 executes the BIOS stored in the ROM 14 to detect a state wherein no key input is made from the keyboard 11 for a predetermined period of time. More specifically, the CPU 10 outputs a HALT instruction when input data from the KBC 12 is not stored in the key buffer of the memory 13 for a predetermined period of time. In other words, if no input data is stored in the key buffer, the logic circuit 100 (Fig. 3) outputs an "H"-level HALT instruction to the controller 16. If there is no file access for the I/O device 15 as an external device via the system bus 19 for a predetermined period of time, "L"-level signals BR and BP are outputted to the controller 16 (NO in step S13). When these conditions are satisfied (YES in step S11 and NO in step S13), the controller 16 outputs an "H"-level control signal SS to the clock control circuit 18. Upon reception of the "H"-level control signal SS, the second clock switching circuit 42 of the clock control circuit 18 supplies the low-frequency clock pulse SCK as the clock CK to the CPU 10. As a result, the mode of the CPU 10 is switched from the normal mode, i.e., a high-speed mode to the sleep mode, and the CPU 10 performs low-speed data processing in accordance with this clock pulse (steps S15 and S23). The sleep mode is released when a signal IR is generated in response to a data input from the keyboard 11 or when file access is made.

When the AC adapter 105 is connected (YES in step S5), or when the mode control data CD at logic level "H" for prohibiting the control operation of the sleep mode controller 16 is inputted from the keyboard 11, the data CD is set in the control register 17 (YES in step S7). As shown in Fig. 2, since the "L"-level signal is supplied from the control register 17 to the first input terminal of the AND gate 20a, setting of the sleep mode is prohibited. Therefore, even when the above-mentioned conditions are satisfied (YES in step S11 and NO in step S13), the sleep mode operation is disabled (step S17). More specifically, the second clock switching circuit 42 of the clock control circuit 18 supplies the clock NCK as the clock CK to the CPU 10 in response to the input "L"-level control signal SS. The CPU 10 executes normal high-speed data processing (normal mode) in response to the clock pulse NCK (step S19 and S21).

According to the present invention, when the power supply of the computer system is turned on, the initial program loader determines whether or not the AC adapter is connected, and if the AC adapter is connected, the clock control circuit prohibits supply of the low-frequency clock pulse to the CPU 10. As a result, the high-speed operation of the CPU can be maintained.

In the above embodiment, data set by a user in the setup menu or the pop-up menu and indicating whether the sleep mode is enabled or disabled is set in the register 17. However, the memory 13 may comprise a battery backup RAM, and the data may be stored in the memory 13.

In the above embodiment, whether or not the AC adapter is connected or whether or not the computer receives a power supply from an expansion unit for expanding a function of the personal computer is determined when the power supply is turned on. However, execution of the sleep mode may be disabled when the AC adapter is connected or when the computer receives a power supply from the expansion unit in a state wherein the personal computer is driven by the battery.

## Claims

1. A computer system having a sleep mode function, characterized by comprising:

   processor means (10) for performing various data processing operations;

   clock control means (18) for selecting one of a first clock pulse at a predetermined high frequency required in a normal mode of said processor means, and a second clock pulse at a predetermined low frequency required in a sleep mode of said processor means, and supplying the selected clock pulse to said processor means;

   discrimination means (14) for discriminating whether or not said computer system receives an external power supply; and

   sleep operation control means (16) for, when said discrimination means discriminates that said computer system receives an external power supply, prohibiting said clock control means to supply the second clock pulse to said processor means.

2. A system according to claim 1, characterized in that said discrimination means includes means for discriminating whether or not an AC adapter is connected to said system to check whether or not a power is externally supplied.

3. A system according to claim 1, characterized in that said discrimination means includes means for discriminating whether or not said computer system receives a power supply from an expansion unit for expanding a function of said computer system which is releasably connected to said system.

4. A system according to claim 1, characterized in that said discrimination means includes initial program loader means for, when a power is supplied to said computer system, discriminating whether or not said computer system receives an external power supply.

5. A system according to claim 1, characterized in that said sleep operation control means comprises memory means for storing mode control data indicating that the sleep mode operation is prohibited.

6. A system according to claim 5, characterized in that said memory means comprises a register.

7. A system according to claim 5, characterized in that said memory means comprises a battery-backup random access memory (RAM).

8. A computer system including a main body having a battery and an external terminal for receiving an external power source, comprising:

a central processing unit (CPU) (10) performing data processing operations;

a clock control circuit (18) selecting one of a high clock pulse for operating said CPU at a high speed and a low clock pulse for operating said CPU at a low speed, the clock control circuit supplying the selected clock pulse to said CPU;

determination means (14) for determinating whether or not the main body receives the external power source through the external terminal; and

a sleep mode controller (16) instructing said clock control circuit to supply the high clock pulse to said CPU when said determination means determinates that the main body receives the external power source through the external terminal.

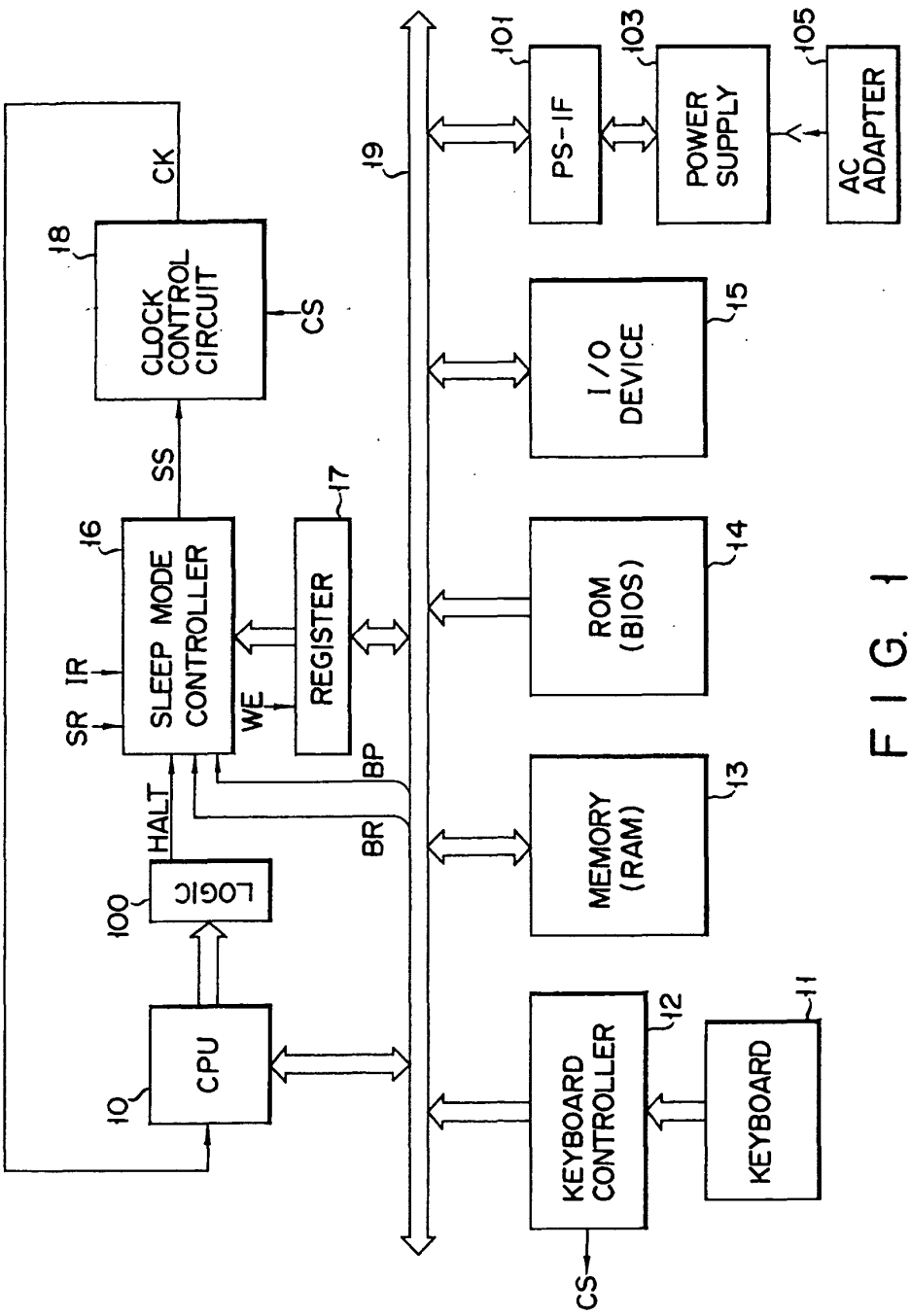


FIG. 1

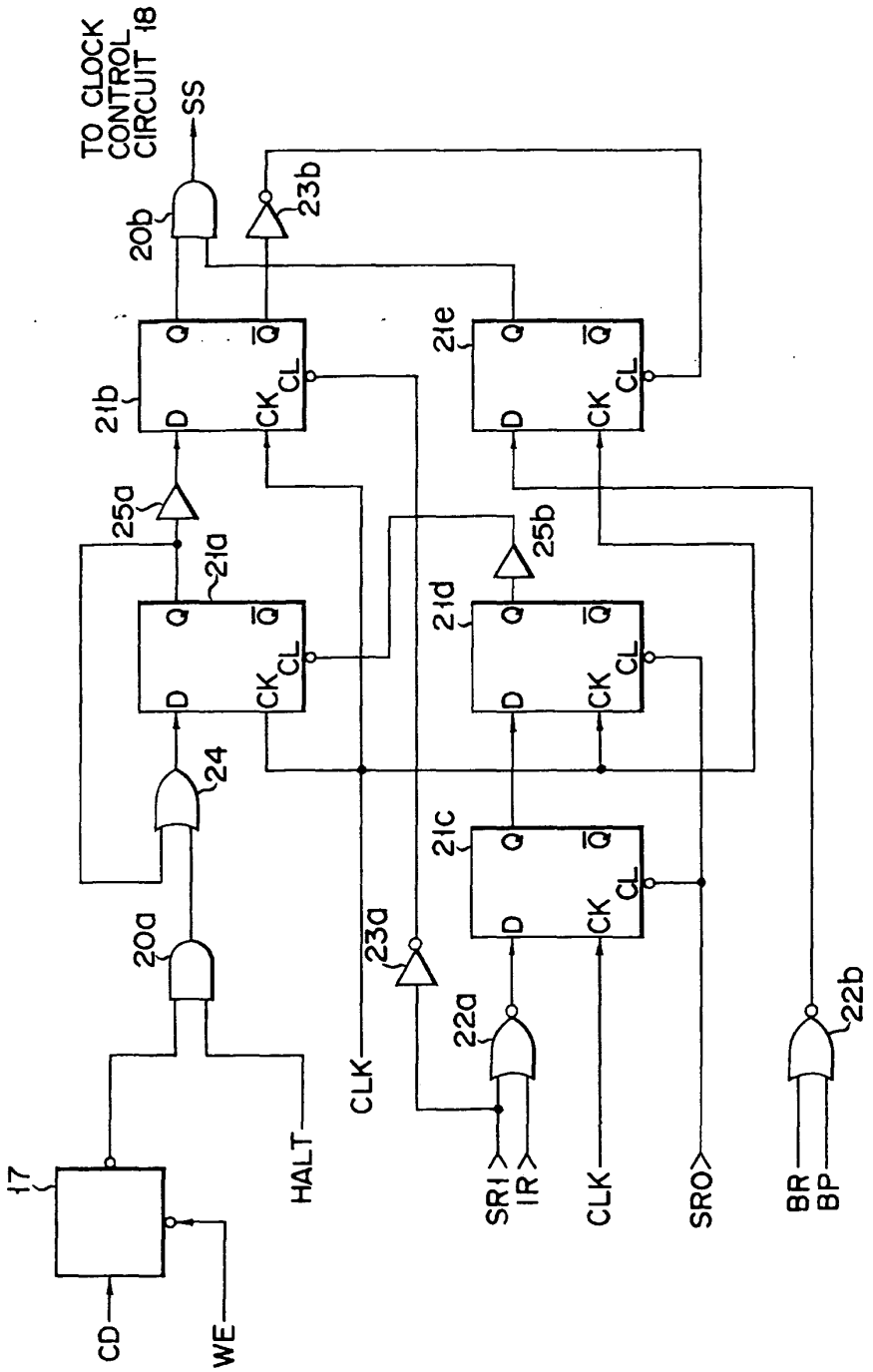


FIG. 2

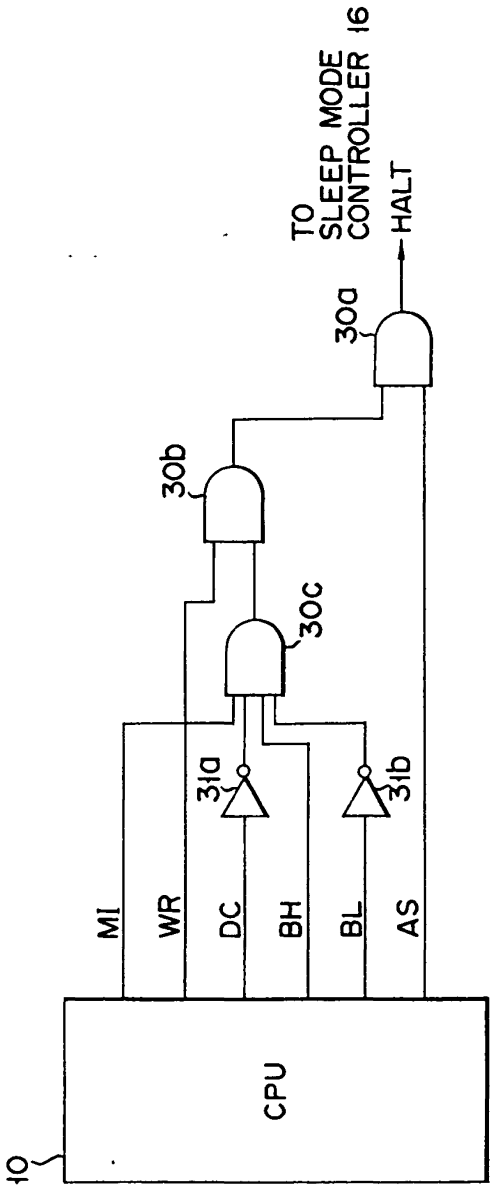


FIG. 3

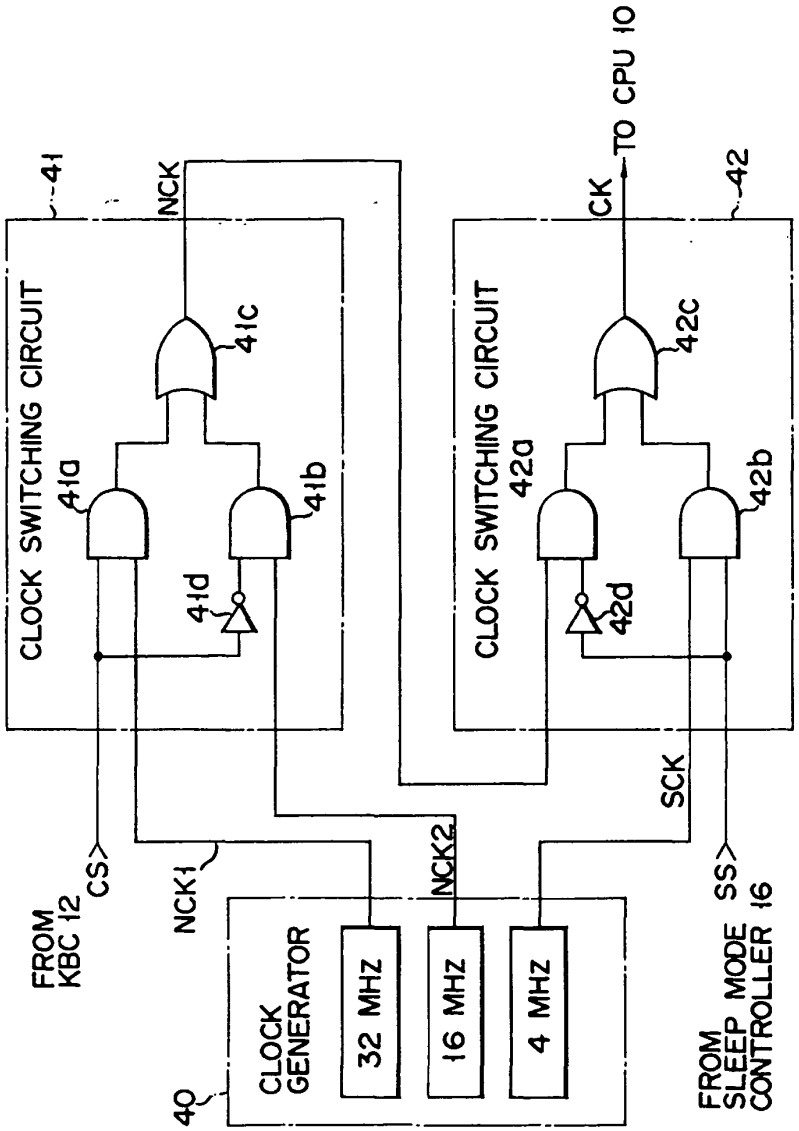


FIG. 4

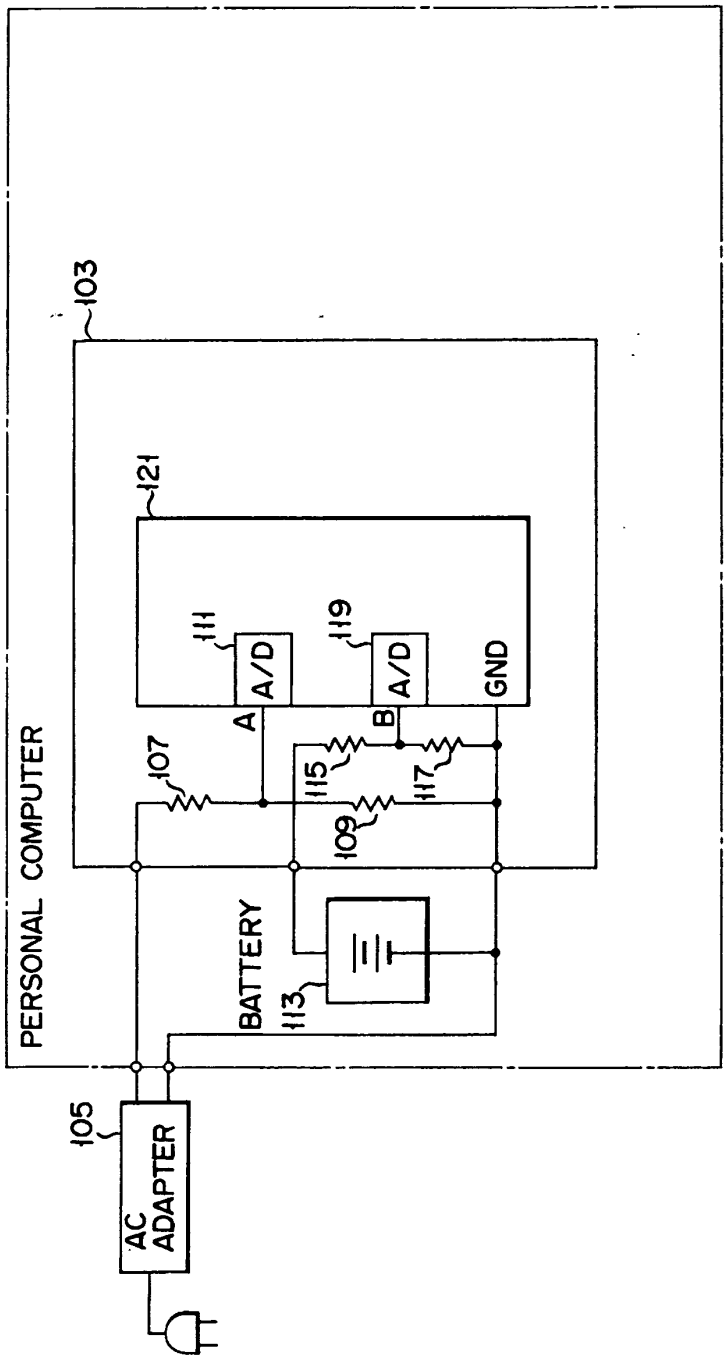


FIG. 5

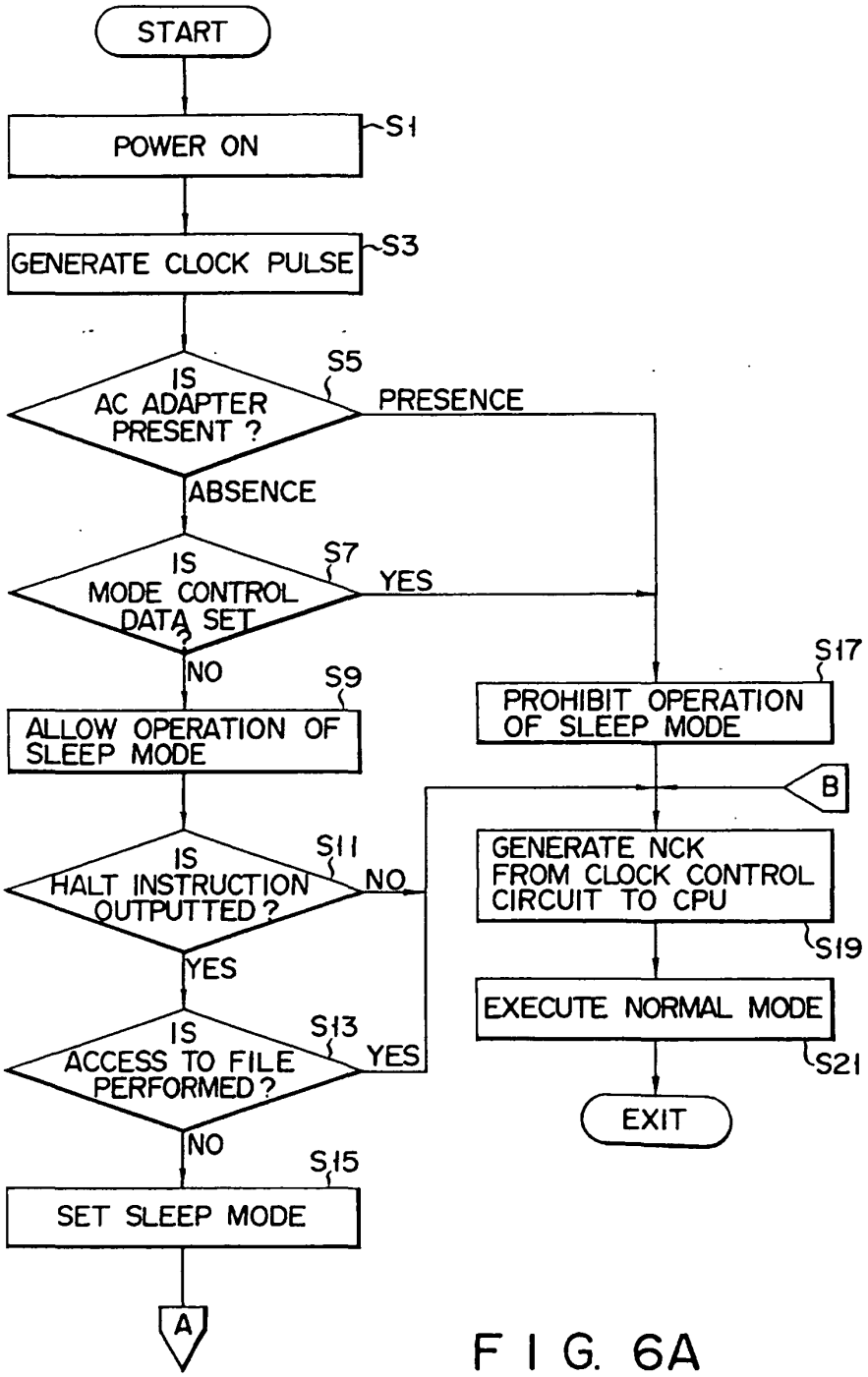


FIG. 6A

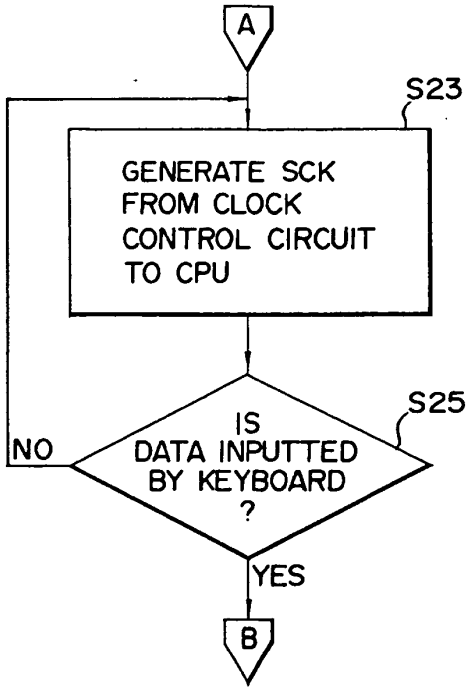


FIG. 6B

(19) Europäisches Patentamt
European Patent Office
Office européen des brevets

(11) Publication number : **0 501 655 A2**

# (12) EUROPEAN PATENT APPLICATION

(21) Application number : **92301314.8**

(51) Int. Cl.[5] : **G06F 1/32**

(22) Date of filing : **18.02.92**

(30) Priority : **25.02.91 JP 50307/91**

(43) Date of publication of application :
**02.09.92 Bulletin 92/36**

(84) Designated Contracting States :
**CH DE ES FR GB IT LI NL SE**

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## (54) Reducing power consumption in a digital processor.

(57) The supply of the clock signal to the processor in a multi-tasking system is controlled by a program (CCP) that runs in the lowest priority under the operating system (OS), so that applications (A,B,) are not affected when clock signals are stopped or slowed to reduce power dissipation.

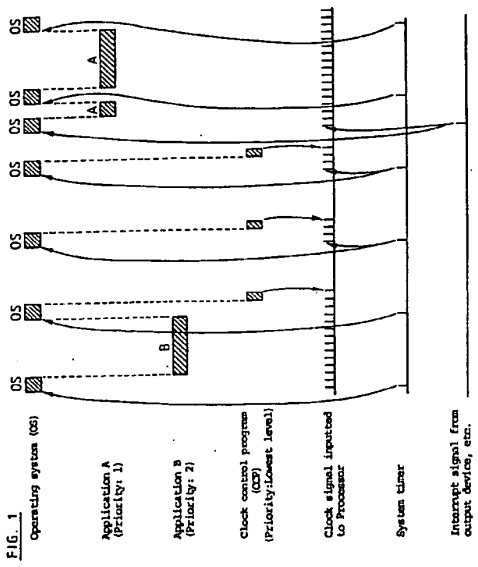


FIG. 1

EP 0 501 655 A2

The present invention relates to reducing the power consumption of a digital processor. Such reduction is desirable particularly to reduce heat dissipation in data processing apparatus including digital processors.

In a known type of processor the contents of its internal registers are not lost even if the supply of a clock signal to the processor is stopped. Operations can be resumed from the stop state by reopening the supply of the clock signal. Such a processor is referred to herein as a full-static processor and, if it uses CMOS logic, power consumption and heat dissipation can be greatly reduced by stopping the supply of a clock signal to the processor, or decreasing the frequency of the clock signal, while the processor idle.

Japanese Published Unexamined Patent Application (PUPA) No.62-169219 (U.S. Pat. No.4,851,987) discloses an information processing system in which the supply of a clock signal to a processor is stopped according to a result of the execution of a program which determines whether the system is currently in a state where it waits for the completion of an operation of an input/output device or key input by an operator. However, even though the system waits for the completion of the operation of the input/output device or key input by the operator, the processor is not always used to be in an idle time. Particularly, in an information processing system using a multi-tasking operating system, possibility that a processor runs a second task while waiting for the completion of an operation of an input/output device or key input by an operator is not insignificant. In such a conventional apparatus there is therefore a danger that the supply of a clock signal to the processor may be stopped while the processor runs the task.

It is accordingly an object of the present invention to provide an information processing system and a method for operating such a system which minimises this danger.

According to the present invention there is provided an information processing apparatus using a multi-tasking operating system, a method for controlling a processor clock signal wherein the supply of a processor clock signal to a processor is controlled by a program which runs in the lowest priority under said multi-tasking operating system.

There is further provided an information processing system including a full static processor, a clock signal generator for supplying the clock signal to said processor, and a clock signal controller for controlling the supply of the clock signal to said processor from said clock signal generator when a program given the lowest priority runs under a multi-tasking operating system.

An information processing system is usually provided with a system timer for synchronising the entire system in addition to a generator or oscillator for generating the clock signal to be supplied to the processor. Under the multi-tasking operating system, tasks to run are switched to one another according to a priority given to each task for each time interval indicated by the system timer. Now in a case where a program (clock control program) that controls the supply of the clock signal to the processor is provided, and the clock control program is given the lowest priority, the clock control program runs if only the clock control program runs and any other tasks does not run, that is, only if the processor may be stopped. Thereby, the supply of the clock signal to the processor can be certainly controlled on or off for each time interval indicated by the system timer. Instead of stopping the supply of the clock signal to the processor, the frequency of the clock signal may be controlled so that it can be decreased.

In order that the invention may be well understood a preferred embodiment thereof will now be described by reference to the accompanying drawings, in which:-

FIG.1 is a time chart showing the operations of the embodiment of an information processing system constructed in accordance with the present invention.

FIG.2 is a block diagram showing the overall construction of said embodiment.

FIG.3 is a flowchart showing a method for controlling processor clock signals and processing steps according to the present invention.

FIG.2 shows the overall construction of an embodiment of an information processing system according to the present invention. Referring to the figure, a processor 10 connects to a clock signal line 21, an interrupt signal line 22, and a signal lines 23. The signal line 23 is comprised of a plurality of signal lines for a control signal, an address signal, and a data signal other than an interrupt signal and connected to a memory 30 and a system timer 70. The signal line 23 and the interrupt signal line 22 may be called a system bus 20. The memory 30 stores a multi-tasking operating system MOS, a clock control program CCP that runs in the lowest priority under the multi-tasking operating system MOS, and application programs A and B.

The clock signal line 21 and the interrupt signal line 22 connect to a clock signal controller 40. The clock signal controller 40 comprises a clock signal on-off switcher 41, a signal transition detector 42, and a register 43. The clock signal on-off switcher 41 is always supplied with a clock signal for the processor from a generator 50, stopping the supply of the clock signal to the processor 10 in response to a clock stopping signal from the register 43, reopening the supply of the clock signal to the processor 10 in response to a clock reopening signal from the signal transition detector 42. The signal transition detector 42 connects to an interrupt signal controller 60. The signal transition detector 42, when receiving an interrupt signal from the interrupt signal controller 60, gives the

interrupt signal to the processor 10 and the clock reopening signal to the clock signal on-off switcher 41.

To the interrupt signal controller 60, in addition to interrupt signals from input/output devices such as a keyboard, a disk storage, a printer, etc., a signal from the system timer are inputted. When receiving these signals, the interrupt signal controller 60 outputs the interrupt signal to the signal transition detector 42. Thereby, except that the interrupt signals from the input/output devices are received, the supply of the clock signal to the processor 10 is reopened when the system timer 70 indicates the lapse of a predetermined time. Under the multi-tasking operating system MOS, task execution is switched for each time interval indicated by the system timer 70. The register 43 is used for receiving and holding a result of the execution of the clock control program CCP given the lowest priority.

Now the operations of the embodiment are described by reference to FIG.1 in addition to FIG.2. Generally, in the multi-tasking operating system, a task scheduler, which is one of the component programs of the operating system, switches tasks on or off based on time slicing in which the task scheduler gives plural tasks the execute right of the processor according to their priority for each predetermined time interval at the completion of a running task or based on a event-driven method in which the execute right of the processor is transferred in response to occurrence of an event such as an interruption, as in the embodiment. Time quanta of time slices are determined by the system timer 70.

FIG.1 shows a state where the execution of plural tasks including the clock control program CCP given the lowest priority is switched under the multi-tasking operating system OS and a condition that the supply of a clock signal to the processor 10 is controlled on or off. Now if the system timer 70 issues a signal indicating the lapse of a predetermined time interval over the signal line 23 while the application program B given priority 2 is running, an object of program execution temporarily changes from the application program B to the operating system OS. The operating system OS not only determines whether the application program B has the execute right of the processor 10 even in the following quantum of time, but also selects any of programs that require the execute right of the processor 10 in the following quantum of time and gives it the execution right.

FIG.1 shows a case where only the clock control program CCP requires the execute right of the processor 10. In this case, the clock control program CCP runs and, as a result, a signal indicating that a clock signal may be stopped is sent to the register 43 of the clock controller 40 through the signal line 23. Since the clock control program CCP does nothing but simple work as described above, its execution time is very short. The register 43 not only holds said signal, but also provides a clock stopping signal to the clock signal on-off switcher 41 to stop the supply of the clock signal to the processor 10.

If the supply of the clock signal to the processor 10 stops and then the system timer 70 issues a signal indicating the lapse of a predetermined time, the interrupt signal controller 60 provides an interrupt signal to the signal transition detector 42 and then the signal transition detector 42 provides a clock reopening signal to the clock signal on-off switcher 41 to not only reopen the supply of the clock signal to the processor 10, but also provide an interrupt signal to the processor 10. The processor 10, on receiving the interrupt signal, prompts a timer interrupt handler and a dispatcher, which are the component programs of the operating system OS, to run and determines a program to be run in the following quantum of time after they run.

FIG.1 shows also a case where a program to be run in the following quantum of time is only the clock control program CCP. Also in this case, the clock control program CCP runs to stop the supply of a clock signal to the processor 10. If the interrupt signal controller 60 issues an interrupt signal while the supply of the clock signal to the processor 10 is stopping, not only the supply of the clock signal to the processor 10 is reopened, but also the operating system OS performs functions to determine a program to be run in the following quantum of time. If the program to be run is the application program A given priority 1, the application program A runs until the system timer 70 issues the following signal. When the system timer 70 issues the signal, the operating system functions to determine a program to be run in the following quantum of time and if the program thus determined is the application program A, the program A runs again until the system timer 70 issues the following signal.

FIG.3 shows processing steps for stopping the supply of a clock signal to the processor under the multi-tasking operating system. In the figure, both an interrupt handler and a task dispatcher are the component programs of a task scheduler of the operating system. The interrupt handler is a program that runs in response to an interrupt signal to do work required for stopping and then reopening an application running before receiving the interrupt signal. The task dispatcher is a program that determines the following task to be run according to priority given to each task and transfers the execute right of the processor to the task thus determined.

Referring to FIG.3, in a step S11 an application program given priority other than the lowest priority runs. In a subsequent step S12, whether said application program is completed or not is determined. If the application program is not completed, the processing proceeds to a step S13 where the application program continues to run. If the application program is completed, the processing proceeds to a step S16.

If an interrupt signal is encountered in a step S14 during the run of the application program, the processing proceeds to a step S15 where the interrupt handler runs and then the task dispatcher is started in the step S16. The task dispatcher determines whether the running application program is authorised to run also in the subsequent quantum of time or not (in a step S17). If the application program is authorised to run in the subsequent quantum of time, the processing returns to the step S11. If the application program is not authorised to run, whether another application program requests authorisation for running or not is determined in a step S18. If another application requests to be authorised to run, the application program runs in a step S19. Otherwise, the processing proceeds to a step S21 where the clock control program (given the lowest priority) for stopping a clock signal is started. In a subsequent step S22, the clock control program runs to send a signal indicating that the supply of the clock signal is stopped, to the register 43 of the clock signal controller 40 and in a step S23 the supply of the clock signal is stopped.

According to the above embodiment, since the clock control program runs only if there is no other tasks to be run, the supply of the clock signal is not in danger of being stopped while some task is running in a background. Further, according to the embodiment, since the on-off control for the clock signal is performed for each timer interval indicated by the system timer, the clock signal is stopped in a small slice of the idle time for the processor and thereby low power dissipation is offered.

It will be recognised that said clock signal controller 40 may be connected to a processor, not the processor 10 and added to another program. It will be appreciated that instead of stopping the supply of a clock signal to the processor 10, the frequency of the clock signal may be decreased to attempt low power dissipation.

As described above, according to the present invention, a method and an information processing system which ensure that an allowed time to stop a processor or an allowed time to delay an operation of the processor is determined to stop the supply of a clock signal to the processor or decrease the frequency of the clock signal, can be provided.

## Claims

1 In an information processing apparatus using a multi-tasking operating system, a method for controlling a processor clock signal wherein the supply of a processor clock signal to a processor is controlled by a program which runs in the lowest priority under said multi-tasking operating system.

2 The method for controlling a processor clock signal according to claim 1 wherein said program is adapted to open or to close the supply of clock signals to the processor.

3 The method for controlling a processor clock signal according to claim 1 wherein said program is adapted to change the frequency of the clock signal provided to the processor from an operating frequency to a reduced idle frequency and vice versa.

4 An information processing system including a full static processor, a clock signal generator for supplying the clock signal to said processor, and a clock signal controller for controlling the supply of the clock signal to said processor from said clock signal generator when a program given the lowest priority runs under a multi-tasking operating system.

5 A system as claimed in claim 4 in which said clock signal controller is adapted to change the frequency of said clock signal from an operating frequency to an idling frequency and vice versa.

6 A system as claimed in claim 4 in which said clock signal controller is adapted to open or to close the supply of clock signals to said processor.

7 The information processing system according to claim 6 wherein said clock signal controller is adapted to reopen the supply of a clock signal to said processor in response to an interrupt signal to said processor.

8 The information processing system according to claim 7 wherein said interrupt signal is an output signal from a system timer for synchronising the entire information processing system.

9 An information processing system as claimed in any of claims 4 to 8 including a memory, a processor, an input/output device, a generator for supplying a clock signal to said processor, and a system timer for synchronising among the parts of the system, wherein a clock signal controller is provided for the purpose of stopping the supply of the clock signal to the processor by means of a program that runs in the lowest priority under a multi-tasking operating system and reopening the supply of said clock signal in response to an interrupt signal from said input/output device or said system timer.

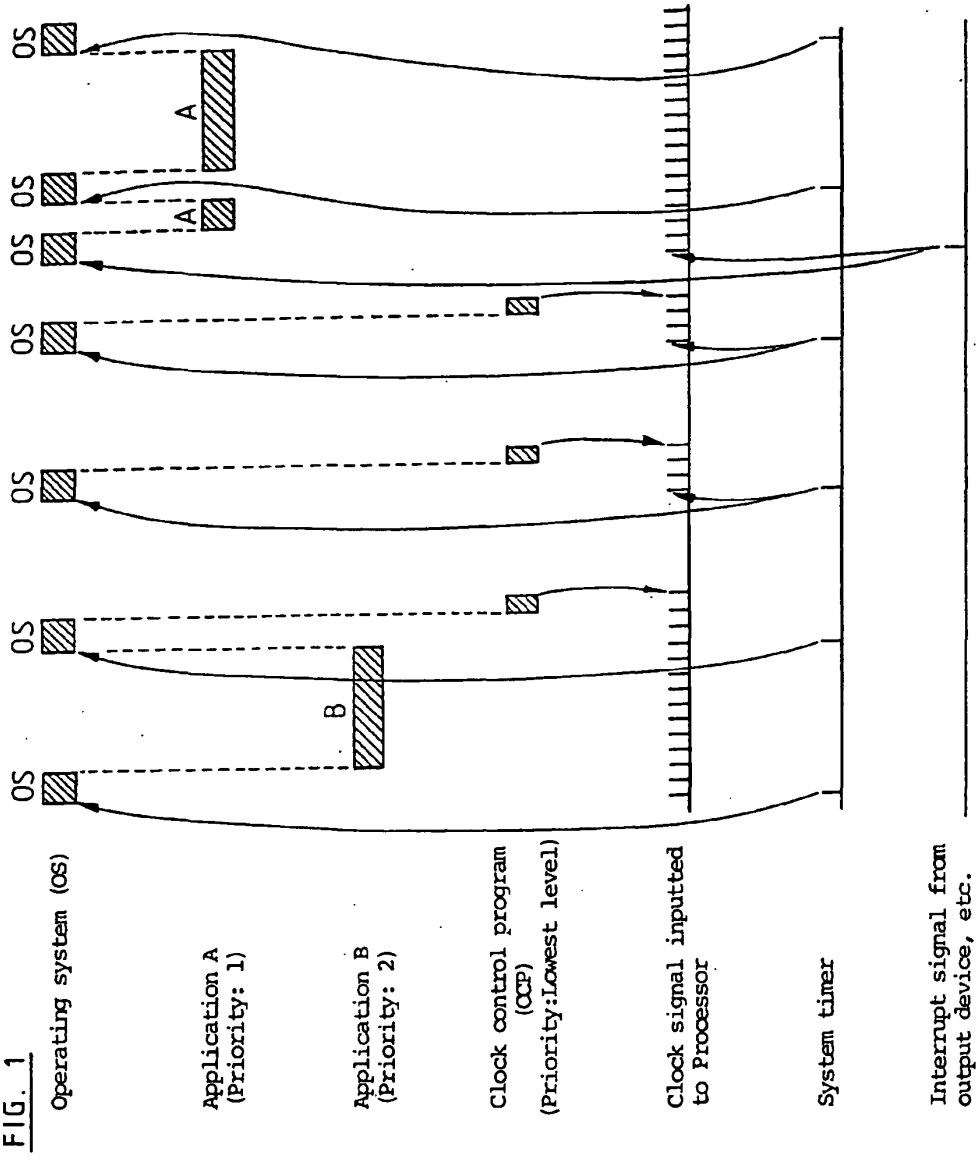


FIG. 1

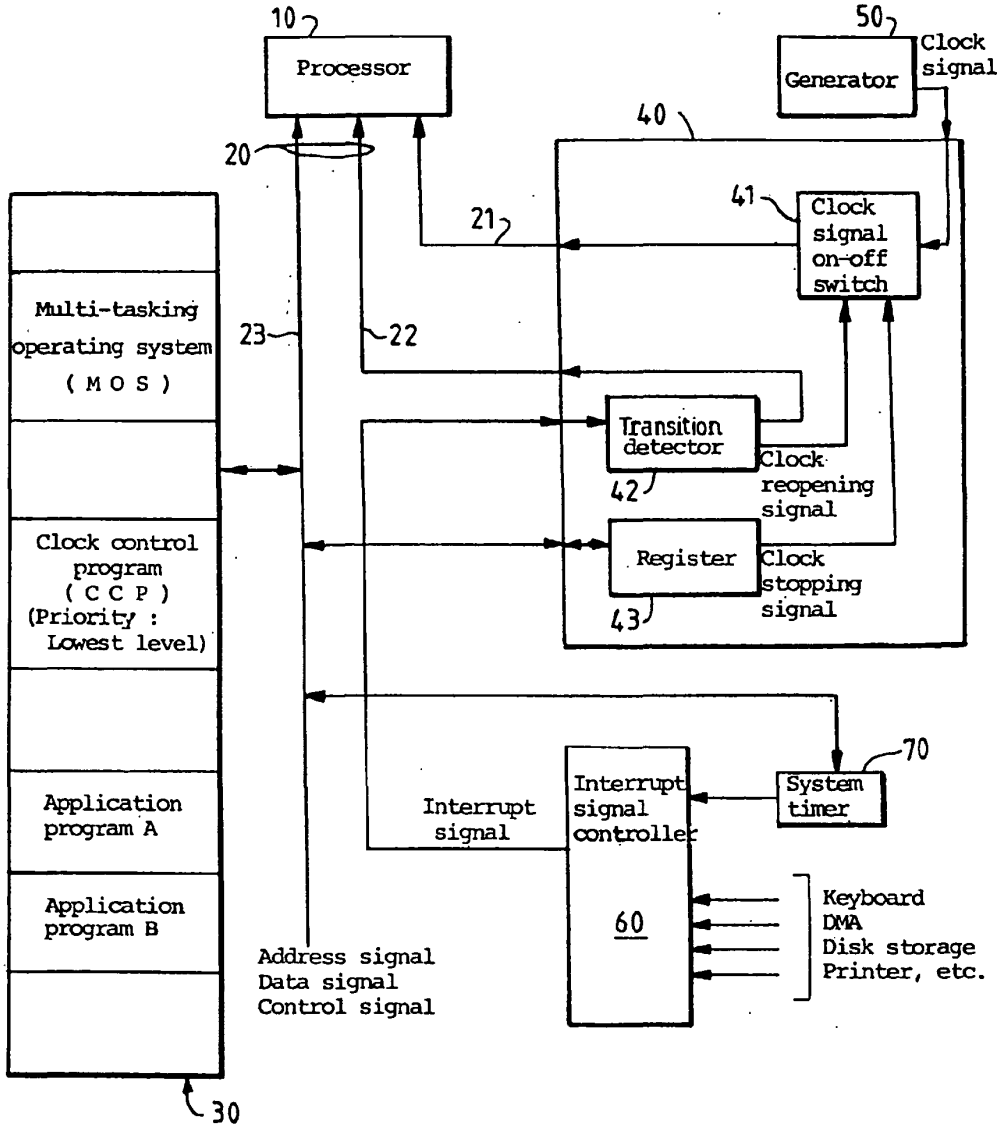


FIG 2

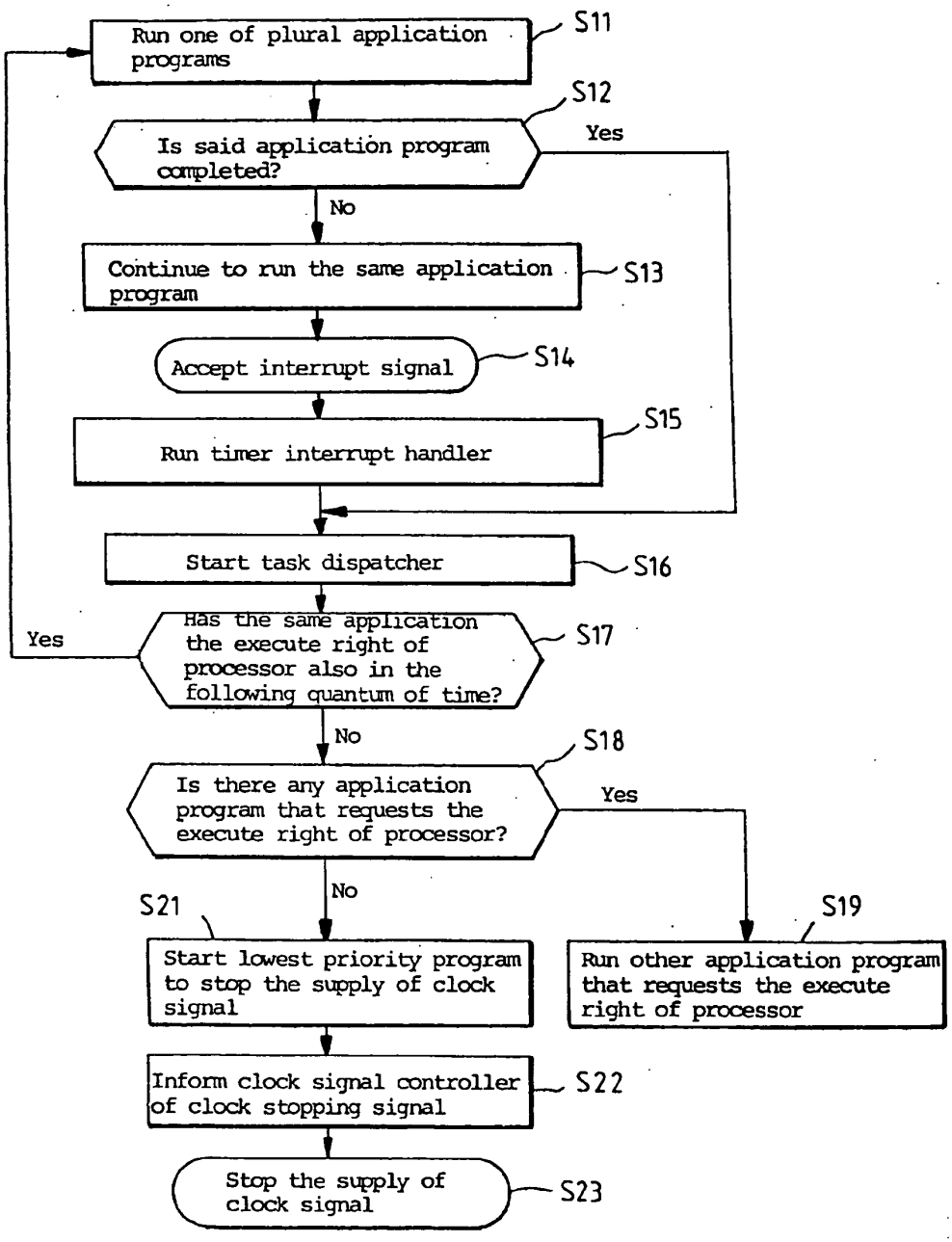


FIG. 3

(19) Europäisches Patentamt
European Patent Office
Office européen des brevets

(11) Publication number: **0 632 360 A1**

# (12) EUROPEAN PATENT APPLICATION

(21) Application number: **94304457.8**

(51) Int. Cl.[6]: **G06F 1/32**

(22) Date of filing: **20.06.94**

(30) Priority: **29.06.93 US 84688**

(43) Date of publication of application:
**04.01.95 Bulletin 95/01**

(84) Designated Contracting States:
**DE FR GB**

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## (54) Reducing computer power consumption by dynamic voltage and frequency variation.

(57) A method for dynamically varying the power consumption of computer circuits (20) under program control. A power control subsystem (22) determines the minimum required level of power (52;Fig. 2) based on a number of factors (Fig. 3) including the particular operation and the recent amount of idle time of the circuit. Voltage (42) and clock speed (38) are determined for the circuit (20) to provide the minimum level of power. The system (22) for controlling the power consumption of the computer circuit (20) comprises a power control subsystem (22) for determining the power level (24), a sequencer (26) for controlling the change in voltage and clock speed, a variable voltage source (40), and a variable clock source (36).

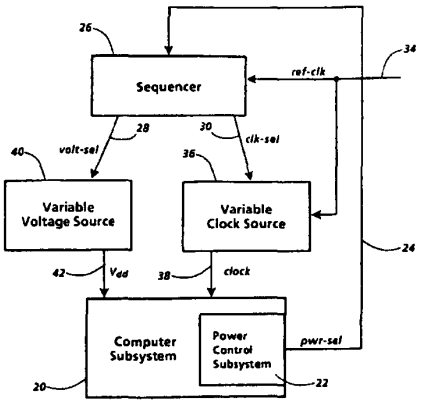


*Fig. 1*

EP 0 632 360 A1

The present invention relates to the reduction of power consumption in computers. More specifically, the invention relates to techniques for reducing the power consumption in computers by dynamically varying the voltage and frequency of computer systems under program control.

In computer systems, and especially in portable computer systems, power consumption is an important consideration. Conservation of power extends the period of time that portable computing devices are able to operate effectively from an internal battery when the computer is disconnected from an external power source. Among users of the portable computers there is a need for the same or more computational capability as found in desktop machines placed in a low-power environment.

Power dissipation in "well-designed" CMOS circuits is dominated by the switching component, which may be approximated by the formula

$$P = fCV_{dd}^2,$$

where $f$ is the clock frequency, $C$ is the average effective capacitance being switched at each clock cycle, and $V_{dd}$ is the supply voltage. Thus, the task of reducing power needs becomes that of minimizing $f$, $C$, and $V_{dd}$, while retaining the required functionality. Since the maximum frequency decreases in roughly linear proportion to $V_{dd}$, it can be approximated it by the formula

$$f = kV_{dd},$$

where $k$ is a constant factor. Thus, lowering the voltage from 5 volts to 2 volts, by a factor of 2.5, offers a possible fifteen fold reduction in power ($2.5*5^2/2^2$) while similarly slowing the maximum operating frequency of the computer by only a factor of about two and a half. Many integrated circuit (IC) manufacturers sell chips that operate over a range of supply voltages. In some cases, chips have simply been recharacterized, and work unchanged for different voltage modes. Some systems achieve a reduction in power consumption by running at a constant lower voltage However, running at a continuously lowered voltage can result in poorer performance, which may be unacceptable to the user.

Other low power computer systems vary their clock rate to conserve power. Varying the clock rate alone gives a linear decrease in power usage. For static ICs that can actually stop their clock altogether when they are not busy, however, there is little advantage in slowing the clock over simply running the clock as fast as possible when there is work, and stopping it completely when there is no work.

US-A-5,167,024 describes a power management method for a portable computer which controls various units within the computer through transistor switches which control the distribution of power by deactivating clock signals to the various units within the computer when they are not in use, removing the supply voltage from a device until usage is requested, or decreasing the frequency of clock signals for a "slow mode", providing a 25-30% power saving.

Some applications require real-time operation. Radio modem, speech and video compression, and speech recognition operations may require computation at near-peak rates. However, once the real-time requirements of the applications are met, there may be no real advantage in increasing the computational throughput.

It is an object of the invention to reduce the power consumption in a computer system by dynamically reducing both voltage and clock speed without significantly affecting the user's perception of performance.

It is a further object of the Invention to reduce power consumption by dynamically reducing voltage and clock speed to a computer system or portions of a computer system under program control.

The present invention describes a method for reducing the power consumption of an electrical circuit by determining a task to be performed, determining the lowest level of power needed to perform the task, and determining the voltage and clock speed necessary to run at that power level. The clock speed and supply voltage are set to the determined levels and the task is performed.

The method may further be performed by determining the lowest acceptable voltage for the task to be performed and the clock speed necessary to run at that voltage, or by determining the minimum clock speed needed to complete the task and the voltage needed to support that clock speed. The clock speed and supply voltage are set to the determined levels and the task is performed.

The invention further provides a method for dynamically adjusting the power consumption of an electrical circuit for performing a second task, the circuit comprising a supply voltage source and a clock source and set at a first power level for performing a first task, the method comprising: determining the second task to be performed by the electrical circuit; determining a second power level necessary to perform the second task; determining a change in voltage to provide the determined second power level; determining a change in clock speed to provide the determined second power level; changing the supply voltage to the electrical circuit according to said determined change in voltage; changing the clock source according to said determined change in clock speed; and performing the second task.

In another aspect of the invention, a method for determining the power level is performed by determining the amount of recent idle time in the circuit. The power level is chosen based on the amount of recent idle time, and voltage and clock speed are adjusted to provide that power level to perform the task.

In the present system, power consumption is reduced by dynamically varying the voltage under program control. An IC or computer subsystem running at a lower voltage also requires a lower clock rate, since it cannot switch as quickly The operating system software of the computer determines the appropriate power level for the task being run at a given time, lowering the voltage and clock speed for tasks that can take longer to run.

Running the whole computer at a low voltage or speed all the time has the problem that it may not be fast enough for some tasks. Dynamically varying the voltage and speed under operating system control means the CPU can be fast when needed and power conservative at other times, depending on the task to be performed.

Embodiments of the invention will now be described, by way of example, with reference to the accompanying drawings, in which:

Fig. 1 shows a block diagram of the system of the invention;

Fig. 2 describes a general method for performing power level selection for the system of Fig. 1;

Fig 3 describes a method for determining necessary power requirements;

Fig. 4 describes the timing implemented in the sequencer;

Fig. 5 shows a block diagram of the sequencer of Fig. 1;

Fig. 6 shows a more detailed block diagram of the delay circuit for the sequencer of Fig. 5;

Fig. 7 shows a block diagram of the variable clock source of the system of Fig. 1; and

Fig. 8 shows a block diagram of the variable voltage source of the system of Fig. 1.

Fig. 1 shows a block diagram for general system 10. The system is based on a general computer system 20. For the purposes of the description here, computer system 20 may be an integrated circuit (IC), a computer board, some subsystem, or a computer itself. Further, in a computer there may be several of these systems, each controlling different parts of a system

A portion of computer system 20 comprises a power control subsystem 22, which performs calculations to determine the power level needed to run an operation of computer system 20 This desired power level is provided to sequencer 26 by a power select signal *pwr−sel* 24. Although for illustrative purposes *pwr−sel* 24 is shown and described in this figure in terms of a single signal, it will be obvious that *pwr−sel* could be a number of lines *n* describing a desired power level.

Sequencer 26 selects the clock speeds and voltage values that achieve the desired power level. The voltage is required at all times to be greater than or equal to the minimum voltage for the current clock speed. Thus, if the clock speed is being reduced, the voltage must be lowered later than the clock, but if the clock speed is being increased, the voltage needs to be raised in advance of the clock.

Variable clock source 36 is provided with a reference frequency *ref−clk* signal 34. This clock may come from the computer or a dedicated or external source. *clk−sel* signal 30 provides the desired clock speed to variable clock source 36. Although for illustrative purposes *clk−sel* signal 30 is shown and described in this figure in terms of a single signal, it will be obvious that *clk−sel* could be a number of signals *m* describing a desired clock speed. The output of variable clock source 36, *clock* signal 38, is provided to computer system 20 to perform the desired operation.

Variable voltage source 40 is provided a voltage select *volt−sel* signal 28 Although for illustrative purposes *volt−sel* signal 30 is shown and described in this figure in terms of a single signal, it will be obvious that *volt−sel* could be a number of signals *p* describing a desired voltage level. The selected voltage $V_{dd}$ 42 is provided to computer system 20 to perform the desired operation.

Fig. 2 describes a general overview of the present method for performing power level selection for system 10. These steps may be performed by a combination of the subsystems of system 10.

The step in box 50 finds the operation or task to be performed. The step in box 52 determines the minimum power requirements to perform the operation at an acceptable performance level. There are many ways by which a lower power consumption rate might be chosen. Some tasks may be labeled "background" or not time critical. A mail delivery process, for example, must eventually complete, but it can afford to take longer without significantly affecting the user's perception of the performance of the machine. Some tasks have a scheduled time to complete, and have a very predictable performance. Such a task might have the clock slowed so that the task completes exactly on time, within its margin of performance prediction, and no sooner. The appropriate voltage would be derived from the calculated clock value. Tasks may be relabeled with different priorities, with the voltage and clock rate determined based on their priority User interactive tasks might have a high priority, work that requires less interaction a medium priority, and work that is permitted to go slowly a background priority.

Voltage could also be lowered in a portable computer when the battery life is low, thus permitting a user to continue useful work but at a reduced speed. This might be an acceptable tradeoff for a user who could otherwise do nothing at all Or the user might be given control over the tasks, for instance, by having a "speed bar" on each window which could be varied by the user to control the speed of activities of the tasks in that window, so that activities that are allowed to run more slowly will consume less power.

For each chip or subsystem, the minimum and maximum voltages at which the chip will run must be characterized, and an appropriate clock level for each voltage chosen. Some chips which have already been characterized by their manufacturer from 3.3V to 5V, for example, may have a clock speed specified for each of 3.3V and 5V, but not for voltages in between. These values could be determined experimentally, or experimentation may be reduced by choosing a conservative clock speed.

The step in box 54 determines if the new power requirement is a decreased level from the previous power level If so, the step in box 56 initiates a reduction in the clock speed, and the step in box 58, after a delay period, initiates a decrease in the voltage. Note that this delay can be omitted for some circuits. Then the step in box 66 initiates the operation. In the figure, the reduction in clock speed and voltage are initiated, but may not complete before the operation itself is initiated. The operation may also be initiated before both steps 56 and 58 have been performed. Thus the clock and voltage adjustment may be performed in parallel with the operation. The operation may run slower later in its process than at the beginning due to this slowdown. In systems or operations where this may cause timing problems, the operation may not be initiated until a sufficient time has passed for the clock and voltage to reach the desired level.

If the new power requirement is not a decrease from the previous level, the step in box 60 checks for an increase in power required. If no increase is required, the operation simply begins in the step in box 66. If an increase in power is necessary, the step in box 62 initiates an increase in the voltage. After a delay period sufficient for the voltage increase to have taken effect throughout the computer system, the step in box 64 initiates an increase in the clock speed. The operation is initiated in the step in box 66. Again, the increase in voltage and clock speed are initiated, but may not complete before the operation itself is initiated, and the operation may be performed in parallel with the voltage and clock speed increase. In systems or operations where increasing the speed of the operation during its performance may cause timing problems, the operation may not be initiated until a sufficient time has passed for the clock and voltage to reach the desired level.

The flowchart of Fig 3 describes an example method that could be used to determine the necessary power requirements as described in step 52. It is essentially a test for a number of conditions. Other conditions could easily be added. This code may be simply added to an operating system since it does not interfere with the task scheduling activity and it can be executed quickly. In the step in box 70, the operating system scheduler chooses the next job or task to run. The step in box 72 determines the priority of the task. If it is a low priority task, the minimum clock speed may be chosen by the step in box 88.

If the current task is not low priority, the step in box 74 determines if there has been a large proportion of idle time recently For example, if the system is running so fast that it completes all it operations and still has a great deal of idle time, then perhaps the system might be run slower and at a lower voltage, in order to optimize the power consumption. This proportion may be set by the user or the system designer, and may vary according to the perceived speed and/or operational needs of the system.

If there has been a lot of recent idle time, the step in box 80 determines if screen or keyboard I/O operations are necessary for this task. To perform screen or keyboard I/O operations, the step in box 86 may set the clock to the maximum clock speed, and correspondingly set the voltage level to the maximum voltage. If there are no screen or keyboard I/O operations in the current task, however, the step in box 84 will reduce the clock speed and the voltage. This should reduce the amount of idle time while reducing the power consumption.

In most instances, the voltage and clock speed should be lowered if there is too much idle time. Checking for a screen or I/O operation is shown in the method above to be an exception to lowering the clock speed, since these operations generally require a faster or maximum speed. However, in some systems it may be necessary to always increase the clock speed to the maximum for screen or keyboard or other I/O operations, rather than just when there has been recent idle time, to prevent effects on the performance of the system. This would require the test in box 80 to be performed earlier, perhaps before the steps in boxes 74 or 72.

If there has not been a great deal of recent idle time, the step in box 76 determines if there has been no recent idle time For example, if the system is running at such a slow speed that it is

running constantly, the performance of the system may suffer. If there has been no recent idle time, the step in box 82 increases the clock to a faster clock speed, with a corresponding increase in voltage If there has been some recent idle time, the step in box 78 determines that no change is needed in the clock speed and it remains at the current settings. The scheduler in the operating system is returned control in the step in box 90.

The average desired amount of idle time to provide the optimum power consumption and performance may be tuned to the particular system to allow the system to run as slowly as possible without significantly detrimentally affecting the user's perception of system performance. The steps in Fig. 3 may further be repeated during the operation of the task, adjusting the voltage and clock speed iteratively throughout the operation based on the amount of idle time during operation. This works particularly for tasks in which the parameters of the task are fairly stationary throughout operation.

Fig. 4 describes the timing implemented in system 10 by sequencer 26. For example, when the *pwr−sel* line indicates an increase in power, the *volt−sel* line goes up $t_1$ later. The clock speed should not be raised until the voltage has reached a suitable level to support that clock speed, so *clk−sel* is delayed $t_2$. When power is reduced, *clk−sel* is reduced at $t_3$ after *pwr−sel* is reduced. Since the voltage should not be reduced until the clock is slow enough to support a lower voltage, *volt−sel* is delayed to $t_4$ later. Note that $t_2$ is likely to be much longer than $t_1$, $t_3$, and $t_4$. The delay values may be derived by experimentation, since manufacturers do not currently anticipate dynamically varying the voltage supply or specify such delays for chips. However, experimentation may be reduced by choosing a conservative value, say one millisecond, for the delay

Figs. 5-8 describe block diagrams of circuits that may be used to create system 10 as shown in Fig. 1. For clarity, the circuitry is described herein in terms of two selectable clock speeds and two selectable voltage levels. However, it will be clear to one skilled in the art that the circuitry may be expanded to provide a greater number of both clock speeds and voltage levels.

A block diagram of sequencer 26 is shown in Fig 5. The signal *pwr−sel* is input to a delay circuit 100 which is clocked by the *ref−clk* line 34 The delayed output is input to a multiplexer 104. *ref−clk* 34 is inverted and input to a D-flipflop 108 which is triggered by the *pwr−sel* line 24. The output of the flipflop is a delayed *pwr−sel−delay*, which is input to the multiplexer This delayed power signal is triggered on the opposite clock edge from the delay units, so that the *clk−sel* line does not cause a glitch on the *clock* output line.

*pwr−sel* signal 24 is inverted and input into a second delay 102, the inverted output of which is input to a second multiplexer 106. The output of multiplexer 104 provides the clk-sel signal 30, and the output of multiplexer 106 provides the volt-sel signal 28.

Fig. 6 describes delay circuit 100 or 102 of Fig. 5. The input (In) is coupled with the reference clock input (clk) at AND gate 118 A positive output from gate 118 begins a counter 120. The output of counter 120 is compared by comparator 122 with a fixed delay 128. When the counter has reached the delay value, the comparator output signal is ORed (at gate 124) with the output of flipflop 126, and the result is input to flipflop 126. Both the counter 120 and the flipflop 126 may be cleared by the reset line (Reset).

For more than one *pwr−sel* line, delay circuit 100 may further have a decoder before gate 118.

Fig. 7 shows a block diagram of a circuit that may be used for variable clock source 36. The signal *ref−clk*, which runs at the maximum clock speed of the system, is provided to a programmable frequency divider In this case, the frequency divider comprises a flipflop 140, which divides the clock source ref-clk, and a multiplexer 142 which isolates the frequency selected by *clk−sel*. There may be more than one *clk−sel* line 30 and a plurality of clock frequencies, and it will be obvious that the clock source must be designed so as to avoid introducing glitches on the clock output.

Fig. 8 shows a block diagram of a circuit that may be used for variable voltage source 40. *volt−sel* line 28 is input to the voltage source circuitry. *volt−sel* may comprise several signals for indicating a desired voltage level, and may be input to a decoder. The appropriate lines of transistors in the feedback amplifier 147 are energized by *volt−sel* to produce output $V_{dd}$. The voltage source 40 may also require a low-pass filter so that the voltage changes gradually across the subsystem This filter value may be determined experimentally for a system Experimentation may be reduced by adding a relatively large filter, which will cause the voltage to take longer to change.

Varying the clock to subsystems or ICs in a computer may mean that the CPU will either need to buffer its data for delivery for a different external clock rate, or entire systems will need to change the clock rate to match the CPU Multiple different clock rates within a computer system are not uncommon, and there are standard methods of moving data among parts of the system using different clocks. In this case the problem may be simplified, since the slowed CPU clock could still be synchronized with other clocks, running at an integral multiple or traction of the base rate. Performance en-

hancements, such as parallel processing circuitry or pipelining circuitry, may increase the performance of the system, and may be used in conjunction with the present invention.

**Claims**

1. A method for dynamically adjusting the power consumption of an electrical circuit (20), the circuit comprising a supply voltage source (40) and a clock source (36), the method comprising:
   determining (50) a task to be performed by the electrical circuit (20);
   determining (52) the required level of power to perform the task;
   determining a change in voltage to provide the determined level of power;
   determining a change in clock speed to provide the determined level of power;
   changing (62,58) the supply voltage to the electrical circuit according to said determined change in voltage;
   changing (64,56) the clock source according to said determined change in clock speed.

2. The method of claim 1, wherein (1) said step of determining a change in voltage (62) is performed before said step of determining a change in clock speed (64), or (2) said step of determining a change in clock speed (56) is performed before said step of determining a change in voltage (58).

3. The method of claim 1, further including the step of commencing performance of said task before completion of said supply voltage changing and said clock source changing steps.

4. A method for reducing the power consumption of an electrical circuit (20), comprising:
   determining (50) a task to be performed;
   determining (52) a lowest acceptable voltage for the task to be performed;
   determining (78-88) a clock speed of the circuit at said determined voltage;
   setting (56) the clock of said electrical circuit to said determined clock speed;
   setting (58) the supply voltage of said electrical circuit to said determined voltage.

5. The method of claim 5, wherein (1) if said determined voltage is less than an immediately previous voltage, said step of setting the clock is done before said step of setting the supply voltage, and (2)
   if said determined voltage is greater that an immediately previous voltage, said step of setting the supply voltage is done before said step of setting the clock.

6. A method for reducing the power consumption of an electrical circuit, comprising:
   determining (50) a task to be performed;
   determining (52) a lowest acceptable clock speed for the task to be performed;
   determining a voltage of the circuit for said determined clock speed;
   setting (56) the clock of said electrical circuit to said determined clock speed;
   setting (58) the supply voltage of said electrical circuit to said determined voltage.

7. A method for dynamically adjusting the power consumption of an electrical circuit (20) for performing a second task, the circuit comprising a supply voltage source (40) and a clock source (36) and set at a first power level for performing a first task, the method comprising:
   determining (50) the second task to be performed by the electrical circuit;
   determining (52) a second power level necessary to perform the second task;
   determining a change in voltage to provide the determined second power level;
   determining a change in clock speed to provide the determined second power level;
   changing (62) the supply voltage to the electrical circuit according to said determined change in voltage;
   changing (64) the clock source according to said determined change in clock speed.

8. The method of claim 9, wherein (1) if said determined change in voltage is negative, said step of changing the clock source is performed before said step of changing the supply voltage, and (2) if said determined change in voltage is positive, said step of changing the supply voltage is done before said step of changing the clock source.

9. A method for dynamically adjusting the power consumption of an electrical circuit (20), the circuit comprising a supply voltage source (40) and a clock source (36), the method comprising:
   determining a task to be performed by the electrical circuit;
   determining the amount of recent idle time of said circuit;
   determining a level of power for said task based on said amount of recent idle time;
   determining a change in voltage to provide said determined level of power;

determining a change in clock speed to provide said determined level of power;

changing the supply voltage to the electrical circuit according to said determined change in voltage;

changing the clock source according to said determined change in clock speed.

**10.** The method of claim 9, wherein the step of determining a level of power for said task is further based upon the priority of said task, and/or wherein the steps of determining the amount of recent idle time of said circuit, determining a level of power, determining a change in voltage, determining a change in clock speed, changing the supply voltage, and changing the clock source are performed repeatedly during operation of said task.

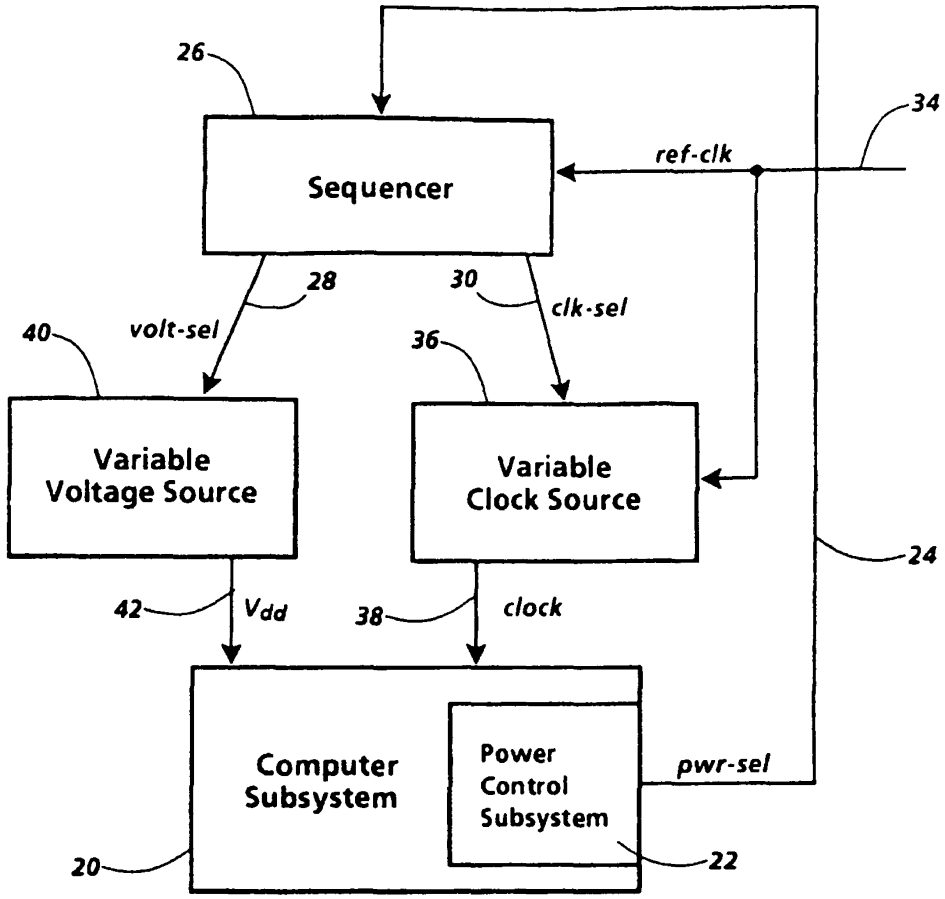


*Fig. 1*

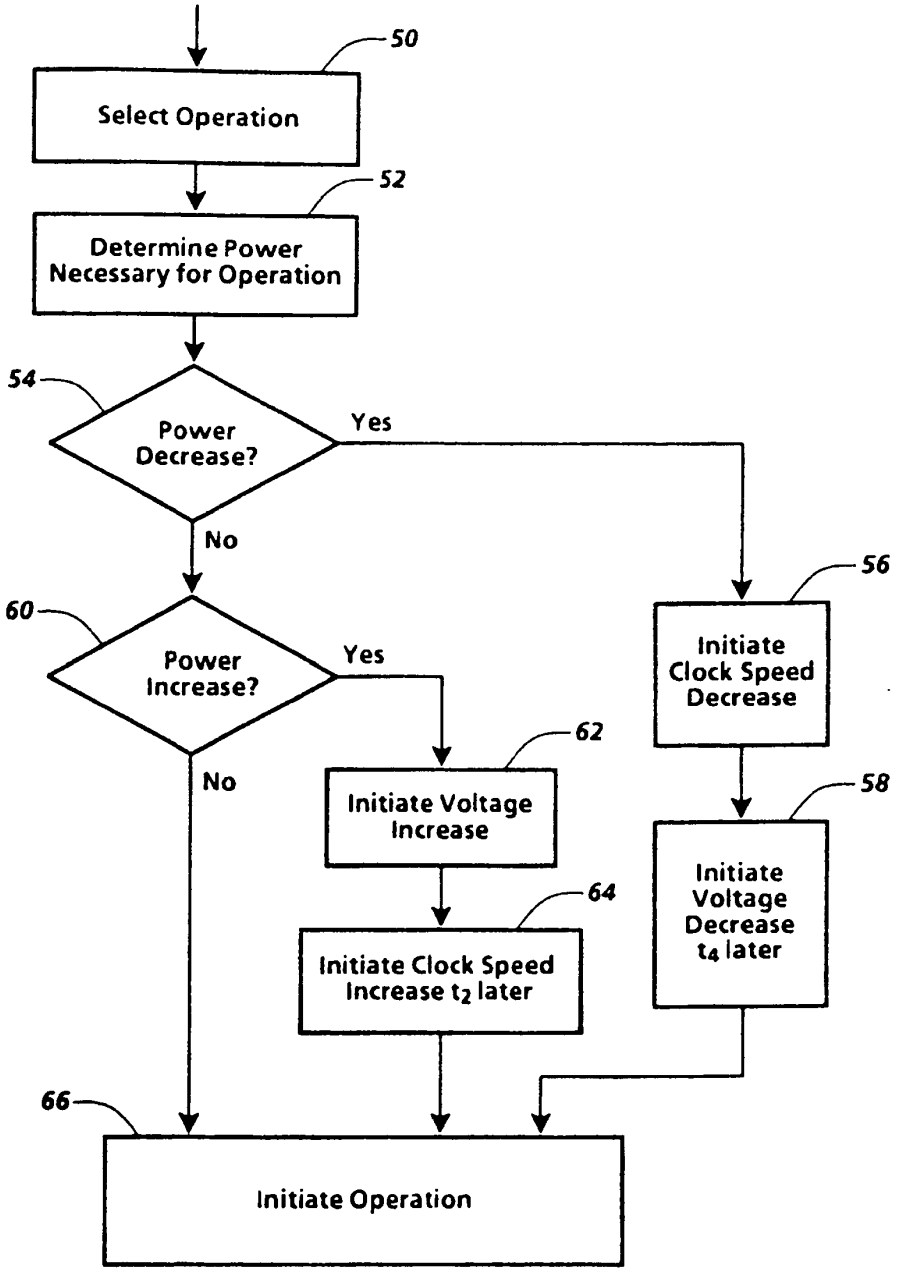


*Fig. 2*

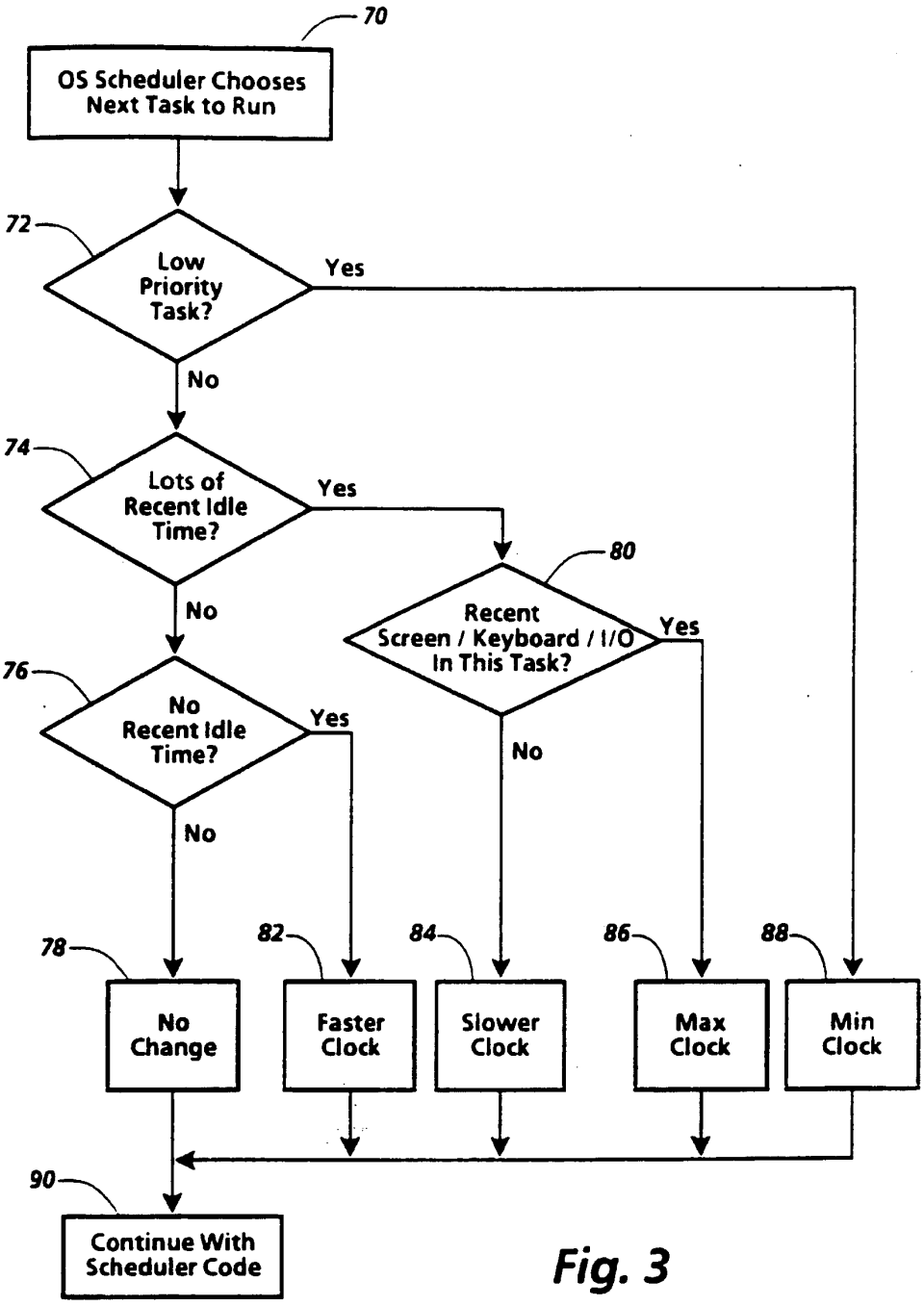


Fig. 3

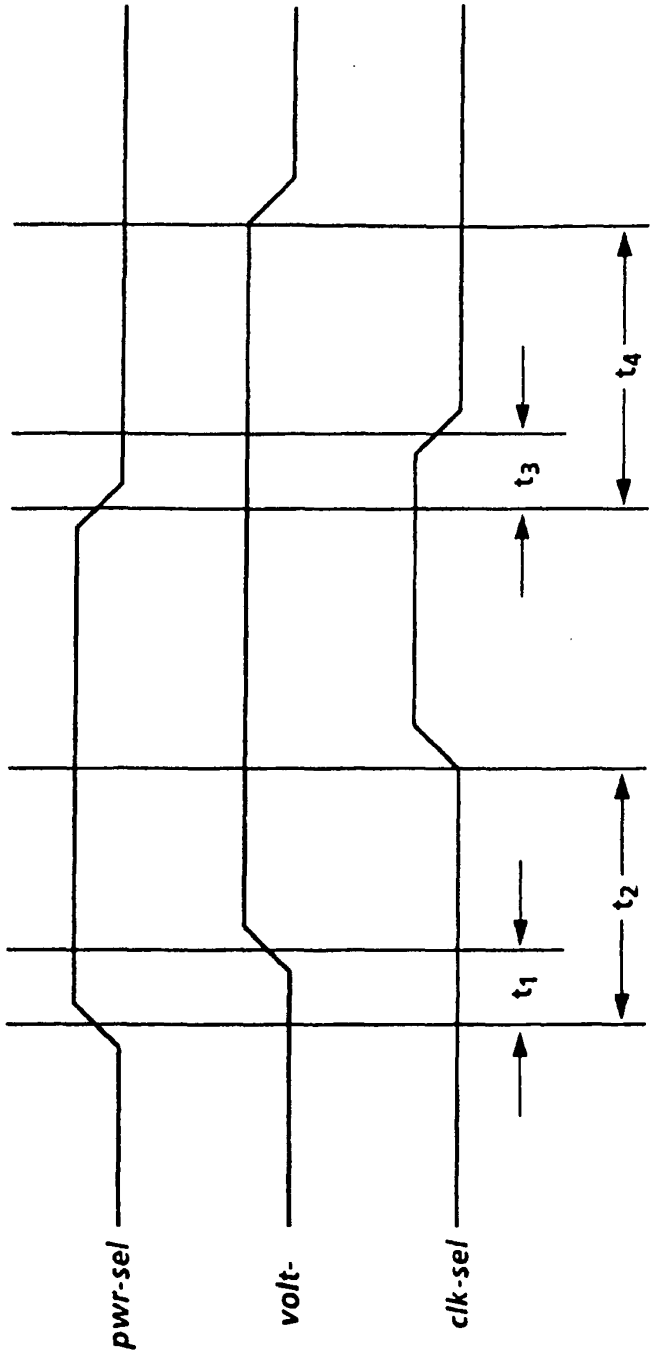


Fig. 4

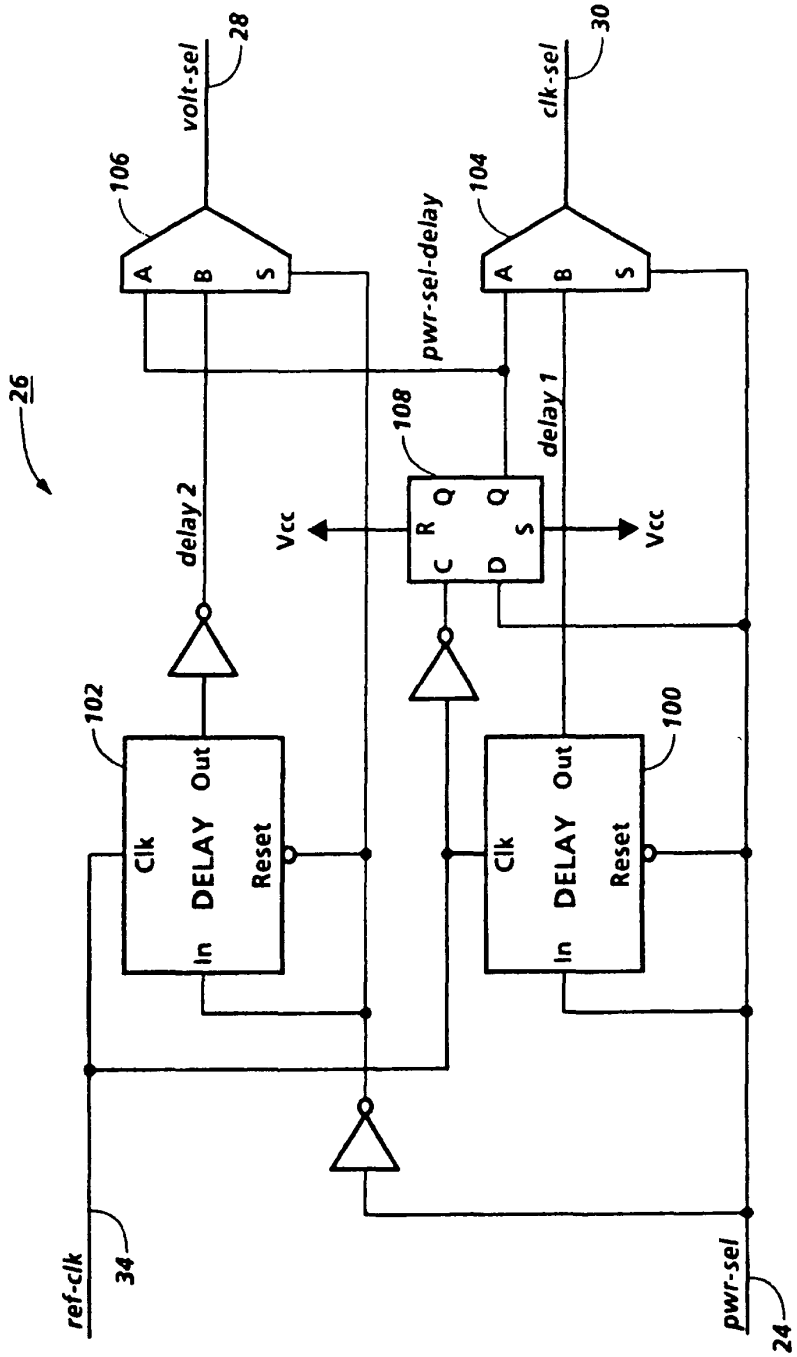


Fig. 5

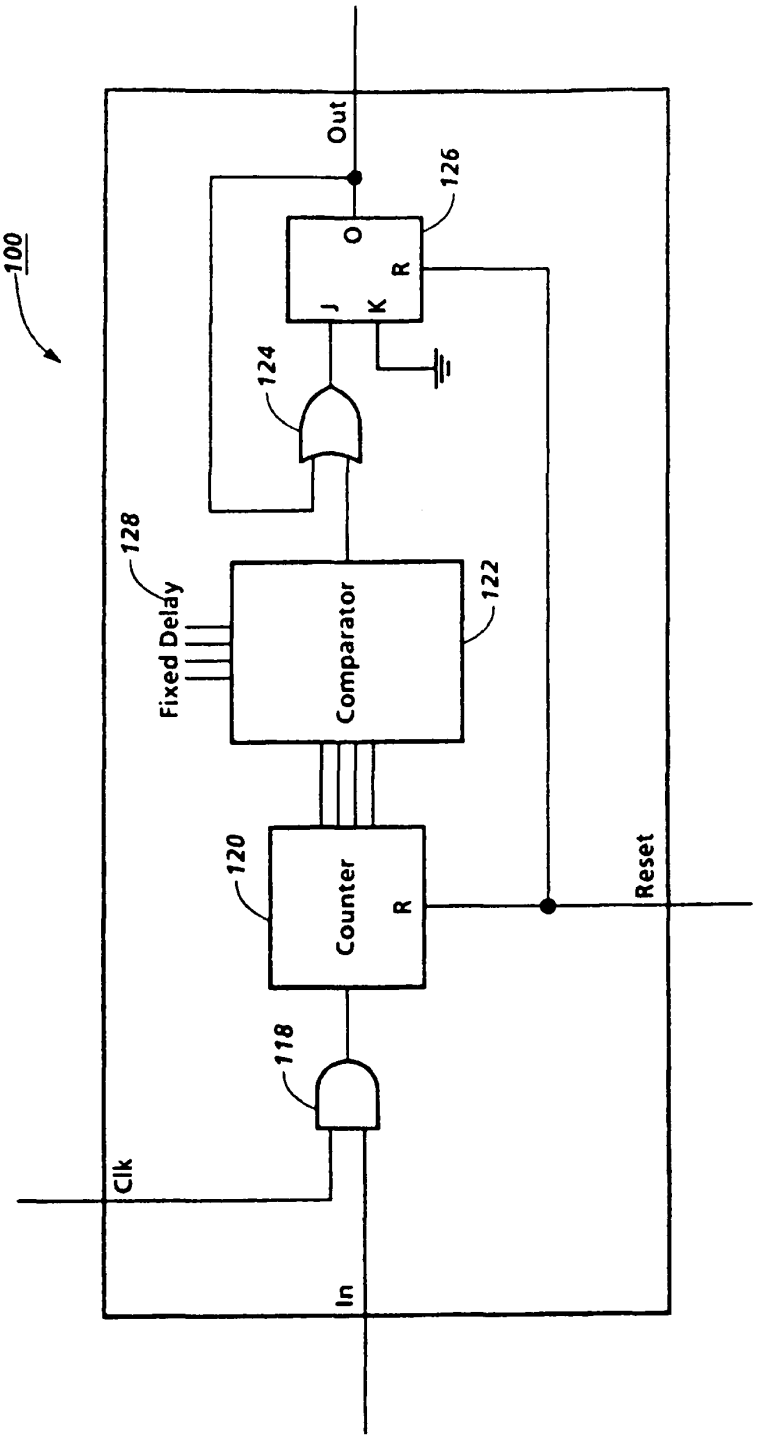


Fig. 6

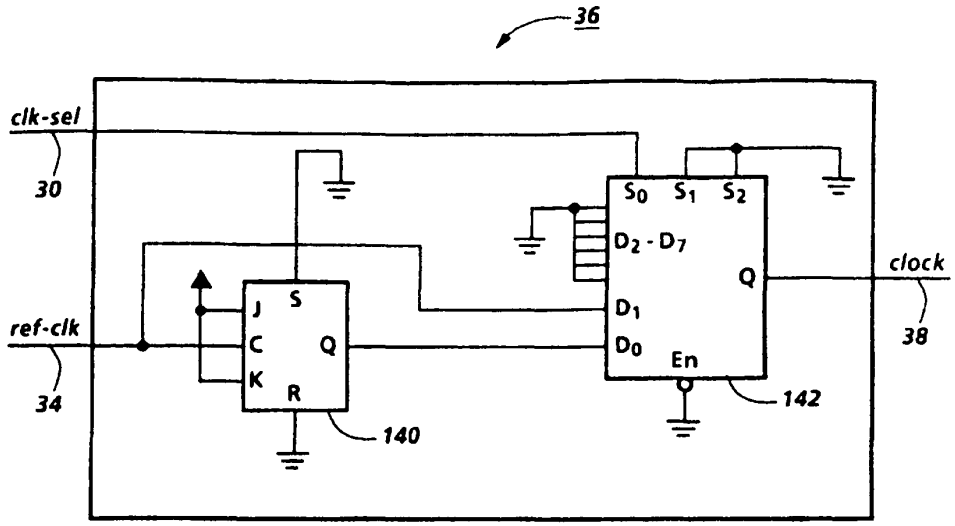


Fig. 7

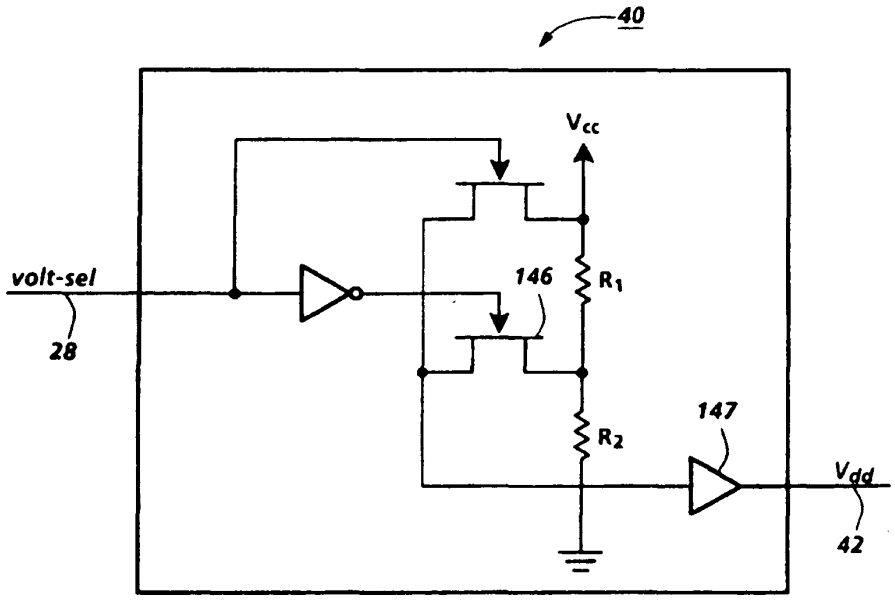


Fig. 8

European Patent Office

# EUROPEAN SEARCH REPORT

Application Number
EP 94 30 4457

## DOCUMENTS CONSIDERED TO BE RELEVANT

| Category | Citation of document with indication, where appropriate, of relevant passages | Relevant to claim | CLASSIFICATION OF THE APPLICATION (Int.Cl.6) |
|---|---|---|---|
| X | EP-A-0 539 884 (TOSHIBA)<br>* column 1, line 33 - column 3, line 29 *<br>* column 4, line 1 - column 5, line 12 * | 1,2,7 | G06F1/32 |
| Y | | 4-6,8-10 | |
| X | WO-A-91 00564 (POQET COMPUTER)<br>* page 2, line 8 - page 5, line 2 * | 1,2,4-6 | |
| X | PATENT ABSTRACTS OF JAPAN<br>vol. 9, no. 127 (P-360)31 May 1985<br>& JP-A-60 010 318 (SANYO) 19 January 1985<br>* abstract * | 1,7 | |
| A | | 4,6,7 | |
| Y | ELECTRONIC COMPONENTS AND APPLICATIONS<br>vol. 7, no. 3 , 1986 , EINDHOVEN NL<br>pages 179 - 186<br>CROES R. 'Battery backup of HCMOS logic ICs'<br>* page 181, left column, line 15 - line 21 * | 4-6 | |
| | | | TECHNICAL FIELDS SEARCHED (Int.Cl.6) |
| Y | MOTOROLA TECHNICAL DEVELOPMENTS<br>vol. 14 , December 1991 , SCHAUMBURG, ILLINOIS US<br>pages 53 - 54 XP276157<br>SCHULTZ C. P. 'DYNAMIC CLOCK CONTROL FOR MICROPROCESSOR SYSTEM ENERGY MANAGEMENT'<br>* page 53, left column, line 1 - line 20 * | 8-10 | G06F |
| A | MOTOROLA TECHNICAL DEVELOPMENTS<br>vol. 15 , May 1992 , SCHAUMBURG, ILLINOIS US<br>pages 43 - 44 XP306138<br>YOUNG R. ET AL 'ADDPTIVE CLOCK SPEED CONTROL FOR VARIABLE PROCESSOR LOADING'<br>* the whole document * | 1,4,7,9 | |

The present search report has been drawn up for all claims

| Place of search | Date of completion of the search | Examiner |
|---|---|---|
| THE HAGUE | 12 October 1994 | Bailas, A |

CATEGORY OF CITED DOCUMENTS

X : particularly relevant if taken alone
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(11) EP 0 978 781 A2

# (12) EUROPEAN PATENT APPLICATION

(43) Date of publication:
**09.02.2000 Bulletin 2000/06**

(51) Int Cl.[7]: **G06F 1/32**

(21) Application number: **99305916.1**

(22) Date of filing: **26.07.1999**

(84) Designated Contracting States:
**AT BE CH CY DE DK ES FI FR GB GR IE IT LI LU MC NL PT SE**
Designated Extension States:
**AL LT LV MK RO SI**

(30) Priority: **03.08.1998 US 128030**

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## (54) Power reduction in a multiprocessor digital signal processor

(57) Improved operation of multi-processor chips is achieved by dynamically controlling processing load of chips and controlling, significantly greater than on/off granularity, the operating voltages of those chips so as to minimize overall power consumption. A controller in a multi-processor chip allocates tasks to the individual processors to equalize processing load among the chips, then the controller lowers the clock frequency on the chip to as low a level as possible while assuring proper operation, and finally reduces the supply voltage. Further improvement is possible by controlling the supply voltage of individual processing elements within the multi-processor chip, as well as controlling the supply voltage of other elements in the system within which the multi-processor chip operates.

EP 0 978 781 A2

Printed by Jouve, 75001 PARIS (FR)

BNSDOCID: <EP_____0978781A2_I_>

## Description

### Background

**[0001]** This invention relates to electronic circuits and, more particularly to power consumption within electronic circuits.

**[0002]** Integrated circuits are designed to meet speed requirements under worst-case operating conditions. In Lucent Technology's 0.35μm 3.3V CMOS technology, the "worst-case-slow" condition is specified for a temperature of 125C and a chip supply voltage, $V_{dd}$, of 2.7V. The worst-case power consumption of the chip is quoted at the maximum supply voltage of 3.6V. The difference in chip performance at the "worst-case slow", nominal, and "worst-case-fast" conditions is shown in FIG. 1, where the frequency of a 25-stage ring oscillator is shown at different supply voltages and process corners. At the nominal operating voltage of 3.3V, the speed difference between "worst case slow" (WCS) and "worst case fast" (WCF) is a factor of 2.2. From the graph it can be seen that if a chip is designed to operate at 140MHz and at 2.1V supply even when it is "worst-case-slow", a manufactured chip whose characteristics happen to be nominal will continue to operate at 140MHz even when the chip supply is reduced to 2.1V.

**[0003]** The power consumption of a CMOS circuit increases linearly with operating frequency and quadratically with supply voltage. Therefore, a reduction in supply voltage can significantly reduce power consumption. For example, by reducing the nominal operating voltage from 3.3V to 2.1 V, the nominal power consumption of a 140MHz chip is reduced by 60% without altering the circuit. This, of course, presumes an ability to identify and measure a chip's variation from nominal characteristics, and an ability to modify the supply voltage based on this measurement.

**[0004]** To achieve variable power supply voltage scaling, a programmable dc-dc converter may be used. Probably, the most efficient approach in use today is the buck converter circuit. These are well known in the art.

**[0005]** Voltage scaling as a function of temperature has been incorporated into the Intel Pentium product family as a technique to achieve high performance at varying operating temperatures and process corners. It is described in US Patent No. 5,440,520. The approach uses an on-chip temperature sensor and associated processing circuitry which issues a code to the off-chip power supply to provide a particular supply voltage. The process variation information is hard-coded into each device as a final step of manufacturing. This approach has the disadvantage of costly testing of each chip to determine its variance from nominal processing. Several manufacturers make Pentium-compatible dc-dc converter circuits, which are highlighted in "Powering the Big Microprocessors", by B. Travis, *EDN*, August 15, pp. 31-44, 1997.

**[0006]** Recently, there has been considerable interest in integrating much of the buck controller circuit onto the chip. The only off-chip components are the inductor (typically about 10μH) and capacitor (typically about 30μF) used in the buck converter. Efficiencies in excess of 80% are typical for a range of voltages and load currents. See, for example, "A High-Efficiency Variable Voltage CMOS Dynamic dc-dc Switching Regulator," by W. Namgoong, M. Yu, and T. Meng, Proceedings ISSCC97 pp. 380-381, February, 1997. Researchers have been also experimenting with on-chip voltage scaling techniques to counter process and temperature variations. See "Variable Supply-Voltage Scheme for Low Power High-Speed COMS Digital Design," by T. Kuroda et al, *CICC97 Conference Proceedings, and JSSC Issue of CISS97*, May, 1998. The Kuroda et al paper demonstrates that the speed of the circuit can be maintained (or at least the speed degradation can be minimized) by tuning the threshold voltages even as the supply voltage is lowered. The tuning is achieved on-chip by varying the substrate-bias voltage. These techniques are needed to ensure that the leakage current, which increasing as the threshold voltage is reduced, does not become too large.

**[0007]** Thus, it is known that varying supply voltage to a chip can improve performance by eliminating unexpected variability in the supply voltage, and by accounting for process and operating temperature variations.

### Summary of the Invention

**[0008]** Improved performance of multi-processor chips is achieved by dynamically controlling the processing load of chips and controlling, which significantly greater than on/off granularity, the operating voltages of those chips so as to minimize overall power consumption. A controller in a multi-processor chip allocates tasks to the individual processors to equalize processing load among the chips, then the controller lowers the clock frequency on the chip to as low a level as possible while assuring proper operation, and finally reduces the supply voltage. Further improvement is possible by controlling the supply voltage of individual processing elements within the multi-processor chip, as well as controlling the supply voltage of other elements in the system within which the multi-processor chip operates.

### Brief Description of the Drawings

**[0009]**

FIG. 1 illustrates the maximum operating frequency that is achievable with a 0.35μm technology CMOS chip as a function of supply voltage;

FIG. 2 presents a block diagram of a multi-processor chip with supply voltage control in accordance with the principles disclosed herein;

FIG. 3 shows the relationship between the voltage control clock, Clk, of FIG. 2, the clock applied to the processing elements of FIG. 2, Clk-L, and the supply voltage applied to the processing elements, $V_{dd}$-local; and

FIG. 4 depicts the block diagram of a multi-processor chip with supply voltage control that is individual to each of the processing elements.

## Detailed Description

**[0010]** FIG. 2 depicts a block diagram of a multi-processor chip. It contains processing elements (PEs) 100, 101, 102, 103, ... 104, and each PE contains a central processing unit (CPU) and a local cache memory (not shown). A real-time operating system resides in PE 100 and allocates tasks to the other PEs from a mix of many digital signal processing applications. The load ofthe FIG. 2 system is time varying and is dependent on the applications that are being executed at any given time. For example, a set-top-box for a multimedia broadband access system might need to receive an HDTV signal. It could also be transmitting data from a computer, to the Internet, and responding to button requests from a remote control handset. Over time, this dynamic mix of applications places different load requirements on the system.

**[0011]** For a maximally utilized system, all of the available processors ought to be operating at full speed when satisfying the maximum load encountered by the system. At such a time, the power consumption of the multiprocessor chip is at its maximum level. However, as the load requirements are lowered, the system should, advantageously, reduce its power consumption. It may be noted that, typically, computers spend 99% of their time waiting for a user to press a key. This presents a great opportunity to drastically reduce the average power consumption. The specific approach by which the system "scales back" its performance can greatly impact the realizable power savings.

**[0012]** In the FIG. 2 arrangement, in accordance with the principles disclosed herein, the applications that need to be processed are mapped to the N PEs under control of real time operating system (RTOS) executed on PE 100. If the number of instructions that need to be executed for each task is known and made available to the operating system, a scheduler within the operating system can use this information to determine the best way to allocate the tasks to the available processors in order to balance the computation. The intermediate goal, of course, is to maximize the parallelism and to evenly distribute the load presented to the FIG. 2 system among all of the PE's.

**[0013]** When an application that is running on the FIG. 2 system is subdivided into N concurrent task streams, as suggested above, each of the PEs become lightly loaded. This allows the clock frequency of the PEs to be reduced, and if the task division can be carried out perfectly, then the clock frequency of the FIG. 2 system can be reduced by a factor of N. Reducing the frequency, as indicated above, allows reducing the necessary supply voltage, and reducing the supply voltage reduces the system's power consumption (quadratically). To illustrate, if a given application that is executed on 1 PE requires operating the PE at 140MHz, it is known from FIG. 1 that the PE can be operated at approximately a 2.7V supply. When the application is divided into two concurrent tasks and assigned to two PEs that are designed to operate at 140MHz from a 2.7V supply, then the PEs can be operated at 70 MHz and at a supply voltage of 1.8V. This reduction in operating voltage represents a power saving of 55%. Of course, it is unlikely that an application can be perfectly divided into two equal load task streams and, therefore, the 55% power saving is the maximum achievable power saving for two PEs.

**[0014]** It should be understood that in the above example, when two PEs are employed and their operating frequency can be reduced to 70 MHz, the indicated reduction presumes that it is desired to perform the given tasks as if there was a single PE that operates at 140MHz. That is, the presumption is that there is a certain time when the tasks assigned to the chip must be finished. In fact, there might not be any particular requirement for when the tasks are to be finished. Alternatively, a requirement for when the tasks are to be finished might not be related to the highest operating frequency of the chip.

**[0015]** For example, the above-illustrated chip (where each of the PEs is designed to operate at 140 MHz) might be employed in a system whose basic frequency is related to 160 MHz. In such an arrangement, dividing tasks between the two PEs of the chip and operating each of the PEs at 80MHz would be preferable because it would be easier to synchronize the chip's input and output functions to the other elements in the system. Thus, in a sense it is the expected completion time for the collection of assigned tasks that is controlling, and the reduction of frequency from the maximum that the chip can support may be controlled by the division of tasks that may be accomplished.

**[0016]** Hence, the operating system of PE 100 needs to ascertain the required completion time, divide the collection of tasks as evenly as possible (in terms of needed processing time), consider the PE with the tasks that require the most time to carry out, and adjust the clock frequency to insure that the most heavily loaded PE carries out its assigned tasks within the required completion time. Once the frequency is thus determined, a minimum supply voltage can be determined. The supply voltage determination can be made by reference to a plot like the one shown in FIG. 1 or, advantageously, by evaluating the actual performance of the multiprocessor at hand.

**[0017]** As indicated above, the operating system can

reduce the supply voltage even further by tracking temperature and process variations. For example, when the chip is nominal in its characteristics, then it can be operated along line 20 of FIG. 1, which calls for only 1.5V supply when operating at 70MHz.

**[0018]** Returning the discussion to FIG. 2, the programmable-frequency clock is generated using an appropriately multiplied input reference clock (line 101) via a phase lock loop frequency synthesizer circuit 110 which has a high resolution, e.g., can be altered in increments of 5MHz. Advantageously, two clocks are generated by PLL 110 (requiring two synthesizer circuits), a Clk clock, and a Clk-L which is 1 frequency step lower than Clk when Clk is being increased. For example, in a PLL 110 unit that provides 5MHz resolution, when Clk is being increased from 75 MHz to 80MHz, the value of Clk-L is set to 75MHz.

**[0019]** Clk-L is applied to the PEs, while Clk is applied to calibration circuit 120, which generates a supply voltage command. The supply voltage command is applied to dc-dc converter 130 followed by L-C circuit 140 to cause the combination of converter 130 and L-C circuit 140 to create the supply voltage $V_{dd}$-local, which is fed back to calibration circuit 120 via line 102. The $V_{dd}$-local supply voltage is also applied to all of the PEs (excluding perhaps the operating system PE 100).

**[0020]** The reason for having the frequency Clk-L lag behind the frequency Clk is that the clock frequency applied to the PEs should not be increased prior to the supply voltage being increased to accommodate the higher frequency. Otherwise, the PEs might fail to perform properly. Circuit 120 observes the level on line 102 to determine whether it corresponds to the voltage necessary to make PEs 100-104 operate properly (described below), and it also waits till the signal on line 102 is stable (following whatever ringing occurs at the output of L-C circuit 140. The signal on line 121 provides information to PE 100 (yes/no) to inform the operating system of when the supply voltage is stable. When the voltage is stable and Clk has reached the required frequency, the operating system sets Clk-L to Clk and then changes the task allocation on the PEs to correspond to that which the PEs were set up to accommodate.

**[0021]** FIG. 3 demonstrates the timing associated with increasing Clk, Clk-L and $V_{dd}$-local when a new task is created and the load on the multiprocessor is thus increased, and the timing associated with decreasing Clk, Clk-L and $V_{dd}$-local when the load on the multiprocessor is decreased. Specifically, it shows the system operating at 70MHz from a 1.8V supply when the load is increased in three steps to 140MHz. When the 2.7V supply is stable, as shown by the supply voltage plot, the new task is enabled for execution. Some time thereafter according to FIG. 3, a task completes, which reduces the load on the multiprocessor. The reduced load permits lowering the clock frequency to 100MHz and lowering the supply voltage to 2.1V. This, too, is accommodated in steps (two steps, this time), with Clk-L preceding Clk to insure, again, that the PEs continue to operate properly while the supply voltage is decreased.

**[0022]** Calibration block 120 can use one of several techniques to determine the voltage required to operate the circuit at a given clock frequency. One technique is given in Koruda et al article. Recognizing that each of the PEs (101-104) has a critical path which controls the ultimate speed of the PE, block 120 uses two copies of that portion of the PE circuit that contains the critical path of the PE circuit, with one of the copies being purposely designed to be just slightly slower. Both of the copies are operated from clock signal Clk and from the $V_{dd}$-local supply voltage of line 102, and that voltage is adjusted within block 120 so that, while operating at frequency Clk, the slightly slower PE fails to operate properly while the other PE does operate properly. This guarantees that the PE's are operating from a supply voltage that is "just above" the point at which they are likely to fail. Since the two critical path copies within element 120 experience the same variations in temperature as do PEs 101-104, the $V_{dd}$-local supply voltage appropriately tracks the temperature variations as well as the different operating frequency specifications.

**[0023]** The FIG. 2 system uses the operating system to react to variations in the system load. As more tasks are entered into the "to-do" list, the operating system of PE 100 computes the correct way to balance the additional computational requirements and allocates the tasks to the processors. It then computes the required operating frequency.

**[0024]** It is noted that the frequency is gradually programmed into the system (as shown by the stepped changes in FIG. 3). This prevents excessive noise on the $V_{dd}$-local supply voltage and possible circuit failure. For example, if the system is operating at 50MHz and it needs to operate at 75MHz, the clock frequency is increased slowly, perhaps even as slowly as in 5MHz increments. In addition, as indicated above, the $V_{dd}$-local supply voltage is increased ahead of increasing the frequency of the clock the operates the PEs, when increased processing capability is desired, and the clock is reduced ahead of reducing the supply voltage when reduced processing capability will suffice.

**[0025]** Of course, $V_{dd}$-local can only be reduced so far before the circuits start to fail, at which point the operating system employs gated clocking techniques to "shut down" PEs that are not needed. Of course, the fact that supply voltage $V_{dd}$-local varies as a function of load should be accounted for in the interface between the PEs 101-104 and PE 100 (as well as in the interface between the multiprocessor chip and the "outside world". This is accomplished with level converter 150, which is quite conventional. It basically converts between the voltage level of PEs 101-104 and the voltage level of PE 100.

**[0026]** The notion of adjusting operating frequency to load and adjusting supply voltage to track the operating frequency can be extended to allow each PE to have its

own supply voltage. The benefit of this approach for some applications becomes apparent when it is realized that the chip-wise voltage scaling is most effective when the load of the computation can be evenly distributed across all of the PEs. In some applications, however, one may encounter tasks that cannot be partitioned into concurrent evenly-loaded threads and, therefore, some PE within the multiprocessor would require a higher operating frequency and a higher operating voltage. This would require raising the frequency and voltage of the entire multiprocessor chip.

**[0027]** A separate power supply for each PE in a chip overcomes this limitation by allowing the operating system to independently program the lowest operating frequency and corresponding lowest supply voltage for each PE. The architecture of such an arrangement is shown in FIG. 4. Each PE in FIG. 4 needs an independent controller that performs the functions of PE 100 (except it does not divide tasks among PEs). As shown in FIG. 4, all of the controllers are embodied in a single controller 200, which may be just another processing element of the integrated circuit that contains the other processing elements. Each processing element also requires a calibration circuit like circuit 120, and a voltage converter circuit like circuits 130 and 140. It also has a PE 200 that assigns the tasks given to the multi-processor chip of FIG. 4 among the PEs.

**[0028]** It may be noted that if the frequencies at which the individual PEs operate differ from one another and from other elements within the system where the multiprocessor chip is employed, there is an issue of synchronization that must be addressed. That is, a synchronization schema must be implemented when there is a need to communicate data between PEs (or with other system elements) that operate at different frequencies. It is possible to arrange the frequencies so that the collection of tasks that are assigned to the multiprocessor is completed at a predetermined time. In such a case, the synchronization problem of the multiprocessor vis-a-vis other elements within the system where the multiprocessor is employed is minimized. However, that leaves the issue of synchronizing the exchange of data among the PEs of a multiprocessor chip.

**[0029]** To effect such synchronization, each PE within the FIG. 4 arrangement is connection to an arrangement comprising elements 150 and 160. Level converter 150 converts the variable voltage swings of the PEs to a fixed level swing, and network 160 resolves the issue of different clock domains.

**[0030]** The principles disclosed above for a multiprocessor is extendible to other system arrangements. This includes systems with a plurality of separate processor elements that operate at different frequencies and operating voltages, as well as components that are not typically thought of as processor elements. For example, there is a current often-used practice to maintain program code and data for different applications of a personal computer in a fast memory. As each new application is called, more information is stored in the fast memory, until that memory is filled. Thereafter, when a new application is called, some of the information in the fast memory is discarded, some other information is placed in the slower hard drive, and the released memory is populated with the new application. It is possible to anticipate that memory stored in the fast memory is so old as to be unlikely to be accessed before a new application is called. When so anticipated, some of the fast memory can be released (storing some of the data that needed to be remembered) at a leisurely pace. That is, lower clock frequency can be employed in connection with the fast memory and the hard drive, with a corresponding lower supply voltage, resulting in an overall power saving in both the memory's operation and in the operation of the hard drive.

**[0031]** The above description illustrated the principles of this invention, but it should be realized that a skilled artisan may easily make various modifications and improvements that are within the scope of this invention as defined by the appended claims. For example, in one of the embodiment disclosed above all of the PEs in a multi-processor chip are subjected to a single controlled supply voltage. In another embodiment disclosed above each of the PEs in a multi-processor chip is subjected to its own, individually controlled, supply voltage. It should be realized, however, that a middle ground is also possible; i.e., the PEs of a multi-processor chip can be divided into groups, and each group of PEs can be arranged to operate from its own controlled supply voltage. To cite another example, the FIG. 2 embodiment employs two almost identical critical path circuits to establish the minimum supply voltage. Alternatively, the voltage may be set in accordance with a preset frequency-voltage relationship that is not unlike the one depicted in FIG. 1.

**[0032]** It should also be noted that level converter 150 is interposed in FIG. 2 between PE 100 and the other PEs because PE 100 is operating off $V_{dd}$. PE 100 can also be operated off $V_{dd}$-local, in which case the level converter is interposed between PE 100 and the input/output port of the FIG. 2 circuits that interacts with PE 100.

**[0033]** It should further be noted that the power supply circuit need not have any elements outside the circuit itself (as depicted in FIG. 2). A skilled artisan would be aware that circuit design exists that can be manufactured wholly within an integrated circuit.

**[0034]** Yet another modification may be implemented by discarding the two-step application of voltages and frequencies of FIG. 3 when appropriate timing conditions are met.

## Claims

1. A method for controlling power consumption of a system sub-circuit comprising the steps of:

ascertaining time allotted for carrying out an assigned task;
determining a lowest frequency at which or above which the sub-circuit must operate in order to complete execution of the assigned task within the allotted time; and
based on characteristics of the sub-circuit, setting a supply voltage that is applied to the sub-circuit to a lowest level that insures proper operation of the sub-circuit at the determined frequency.

2. The method of claim 1, carried out in a multiprocessor sub-circuit, wherein said assigned task comprises a plurality of sub-tasks, the method further comprising the step of

apportioning said sub-tasks among processors of said multiprocessor sub-circuit, resulting in one of said processors carrying the largest load of sub-tasks processing, compared to the sub-tasks processing load of others of said processors, where
said step of apportioning is executed prior to said step of determining, and
said step of determining ascertains the lowest frequency at which the processor carrying the largest load of sub-tasks processing may operate in order to complete its assigned sub-tasks processing within the allotted time.

3. The method of claim 2 further comprising the steps of:

determining a new lowest frequency, when a new task is assigned, at which or above which the sub-circuit must operate in order to complete execution of the assigned task within the allotted time;
comparing the lowest frequency to the new lowest frequency to determine whether a new operating frequency should be set for said sub-circuit;
when said step of comparing determines that the new lowest frequency may be lower than said lowest frequency, reducing the frequency at which said sub-circuit is set to operate and, thereafter, reducing the supply voltage that is applied to the sub-circuit; and
when said step of comparing determines that the new lowest frequency must be higher than said lowest frequency, increasing the supply voltage that is applied to the sub-circuit and, thereafter, increasing the frequency at which said sub-circuit is set to operate to said new lowest frequency.

4. A circuit that includes a processor, comprising:

a controller, responsive to an applied task and to a specification for a time interval that may be devoted to executing said task, for developing a frequency of operation for said processor that is the lowest frequency of operation that allows completion of said applied task within said time interval;
a calibration circuit responsive to said controller for directing creation of a supply voltage for said processor, and
a power supply responsive to said calibration circuit, for developing said supply voltage for said processor and applying said supply voltage to said processor;

wherein said controller directs said processor to execute said task after said supply voltage is applied to said processor and the frequency of a clock applied to said processor is set to said lowest frequency of operation that allows completion of said applied task within said time interval.

5. The circuit of claim 4 further comprising a level converter circuit interposed between input/output ports of said circuit and said processor, to convert voltages levels passing between said input/output ports and said processor.

6. The circuit of claim 4 wherein said controller includes a generator of clock signals that develops a first clock signal having a first frequency and applied to said calibration circuits, and a second clock signal having a second frequency applied to said processor, wherein the second frequency can be set to said first frequency or to a lower frequency.

7. The circuit of claim 4 wherein said task includes a plurality of sub-tasks, said processor comprises a plurality of processing elements, said controller partitions said sub-tasks among said processing element and develops said frequency of operation for said processor based on said partitioning.

8. The circuit of claim 7 wherein said controller develops said frequency of operation for said processor by evaluating the lowest frequency of operation for a most-burdened processing element that would still complete execution within said time interval, wherein the most-burdened processing element is a processing element to which sub-tasks are allocated that require, in the aggregate, the most processing time.

9. The circuit of claim 4 wherein said processor comprises N processing elements, said controller comprises N controller sub-modules, said calibration circuit comprises N calibration circuit sub-modules, and said power supply comprises N power supply

modules, and wherein

the i-th calibration circuit sub-module is responsive to the i-th controller sub-module and directs the i-th power supply module, the i-th power supply module provides power to the i-th processing element and the i-th processing element is responsive to the i-th controller sub-module.

**10.** The apparatus of claim **9** further comprising a processing element for accepting said task and, when Said task comprises a plurality of sub-tasks, for partitioning said sub-tasks among the N processing elements.

**11.** The apparatus of claim **9** further comprising a level converter associated with each of said processing elements and coupled to input/output ports of said associated processing elements.

**12.** A circuit comprising:

a controller processing element;
a plurality of task-handling processing elements;
a calibration circuit responsive to said controller processing element for directing creation of a supply voltage for said processor; and
a power supply circuit, responsive to said calibration circuit, for developing a supply voltage for said task-handling processing elements;
wherein said controller processing element directs said task-handling processing elements to execute tasks at a selected processing frequency.

**13.** A method for operating a processor comprising the step of applying a supply voltage to said processor as a function of frequency necessary to operate said processor to complete an assigned task within an assigned time interval.

**14.** The method of claim **13** wherein said function substantially minimizes power consumption in said processor.

*FIG. 1*

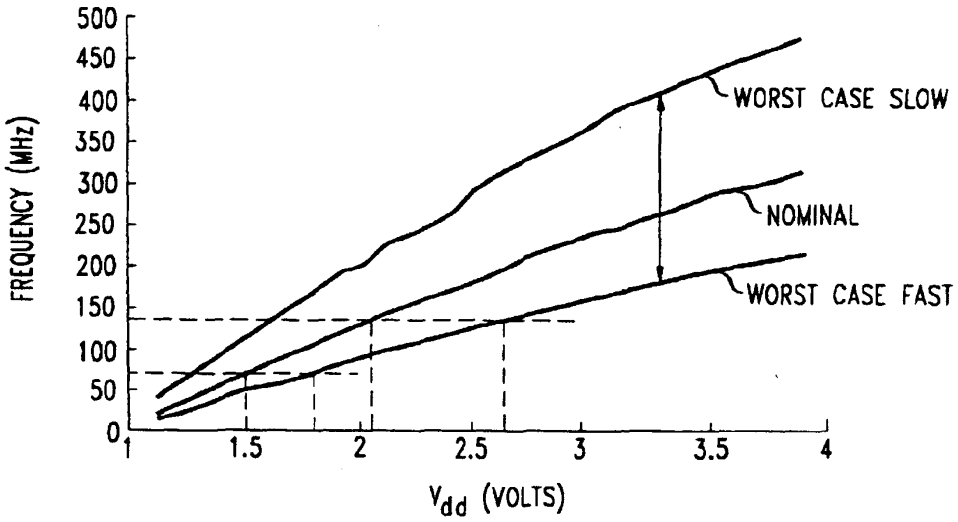



*FIG. 2*

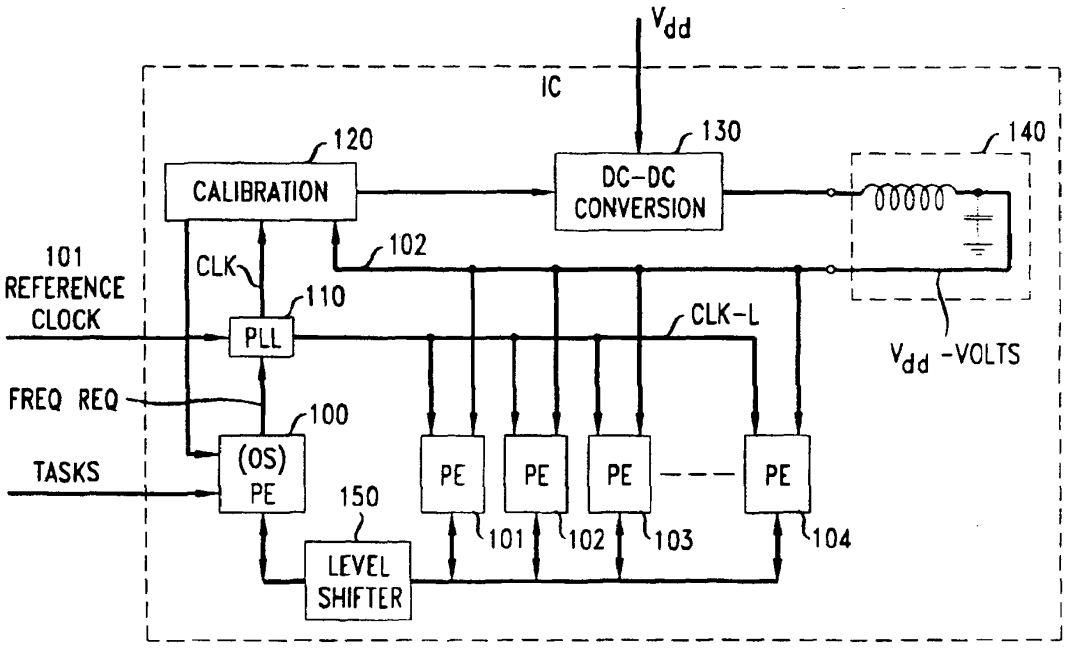


*FIG. 3*

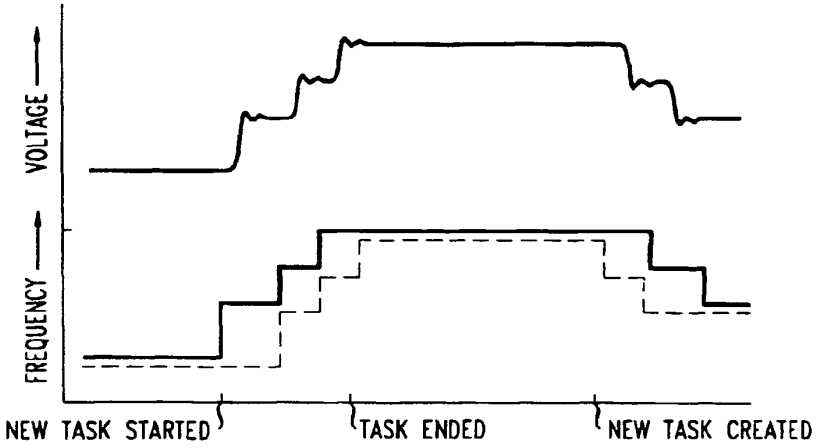
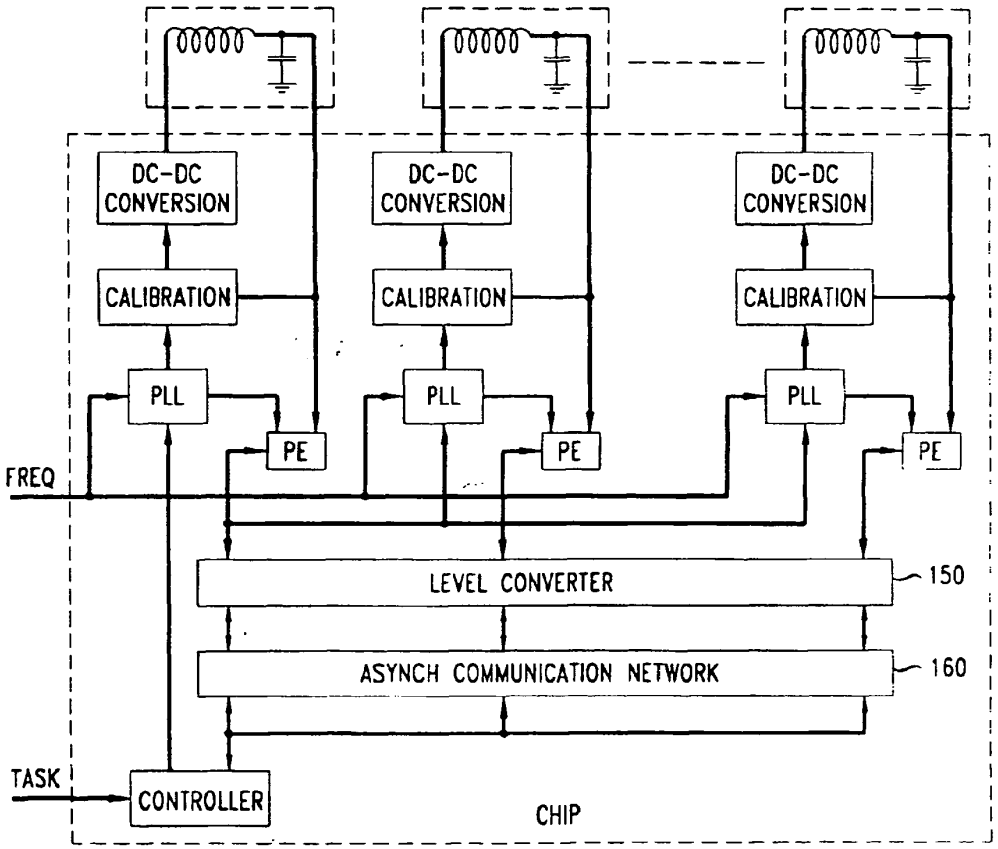



*FIG. 4*



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(19) Europäisches Patentamt
European Patent Office
Office européen des brevets

(11) EP 0 978 781 A3

(12) **EUROPEAN PATENT APPLICATION**

(88) Date of publication A3:
**02.04.2003 Bulletin 2003/14**

(43) Date of publication A2:
**09.02.2000 Bulletin 2000/06**

(21) Application number: **99305916.1**

(22) Date of filing: **26.07.1999**

(51) Int Cl.[7]: **G06F 1/32**

(84) Designated Contracting States:
**AT BE CH CY DE DK ES FI FR GB GR IE IT LI LU MC NL PT SE**
Designated Extension States:
**AL LT LV MK RO SI**

(30) Priority: **03.08.1998 US 128030**

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# (54) Power reduction in a multiprocessor digital signal processor

(57) Operation of multi-processor chips is achieved by dynamically controlling processing load of chips and controlling, significantly greater than on/off granularity, the operating voltages of those chips so as to minimize overall power consumption. A controller in a multi-processor chip allocates tasks to the individual processors to equalize processing load among the chips, then the controller lowers the clock frequency on the chip to as low a level as possible while assuring proper operation, and finally reduces the supply voltage. Further reduction is possible by controlling the supply voltage of individual processing elements within the multi-processor chip, as well as controlling the supply voltage of other elements in the system within which the multi-processor chip operates.

EP 0 978 781 A3

Printed by Jouve, 75001 PARIS (FR)

BNSDOCID: <EP_____0978781A3_I_>

European Patent Office

# EUROPEAN SEARCH REPORT

Application Number
EP 99 30 5916

## DOCUMENTS CONSIDERED TO BE RELEVANT

| Category | Citation of document with indication, where appropriate, of relevant passages | Relevant to claim | CLASSIFICATION OF THE APPLICATION (Int.Cl.7) |
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| X | EP 0 632 360 A (XEROX CORP) 4 January 1995 (1995-01-04) | 1,4 | G06F1/32 |
| Y | * column 2, line 34 - line 54 * * column 4, line 4 - line 11 * | 12-14 | |
| A | * column 5, line 12 - line 42 * * column 8, line 21 - line 46 * * column 10, line 5 - line 15 * * figure 1 * | 3 | |
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The present search report has been drawn up for all claims

| Place of search | Date of completion of the search | Examiner |
|---|---|---|
| BERLIN | 28 January 2003 | de la Torre, D |

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X : particularly relevant if taken alone
Y : particularly relevant if combined with another document of the same category
A : technological background
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E : earlier patent document, but published on, or after the filing date
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EPO FORM 1503 03.82 (P04C01)

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28-01-2003

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For more details about this annex : see Official Journal of the European Patent Office, No. 12/82

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PAT-NO: JP409185589A

DOCUMENT-IDENTIFIER: JP 09185589 A

TITLE: INFORMATION PROCESSING SYSTEM AND POWER SAVING METHOD
FOR THE SYSTEM

PUBN-DATE: July 15, 1997

INVENTOR-INFORMATION:
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KATO, MASAYA

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TOSHIBA CORP N/A

APPL-NO: JP08000201

APPL-DATE: January 5, 1996

INT-CL (IPC): G06F015/16, G06F015/16 , G06F001/32 , G06F001/04

ABSTRACT:

PROBLEM TO BE SOLVED: To effectively suppress the power consumption of the whole system by positively generating inactive processors even in a state where the number of tasks is over that of processors.

SOLUTION: In this information processing system, OS previously knows the resource request quantity of the processors 11 and 12 of the processing unit of each task including OS itself to centralize the group of tasks to the specific processor 11 within a range in which the resources of the processors 11 and 12 are not short (a range in which the sum of the request quantity of the

processor resources is not over 100). Thereby, the other **processor** 12 is brought into an inactive state so that power source supply for the inactive **processor is stopped or a clock** frequency is **lowered**. Thereby the power consumption of the whole system is effectively suppressed.

(19)日本国特許庁（ＪＰ）　(12) 公開特許公報（A）　(11)特許出願公開番号

特開平9－185589

(43)公開日　平成９年(1997)７月15日

| (51)Int.Cl.[6] | | 識別記号 | 庁内整理番号 | ＦＩ | | 技術表示箇所 |
|---|---|---|---|---|---|---|
| Ｇ０６Ｆ | 15/16 | | | Ｇ０６Ｆ | 15/16 | Ｅ |
| | | ４３０ | | | | ４３０Ｂ |
| | 1/32 | | | | 1/04 | ３０１Ｃ |
| | 1/04 | ３０１ | | | 1/00 | ３３２Ｂ |

審査請求　未請求　請求項の数５　ＯＬ　（全７頁）

(21)出願番号　特願平8－201

(22)出願日　平成８年(1996)１月５日

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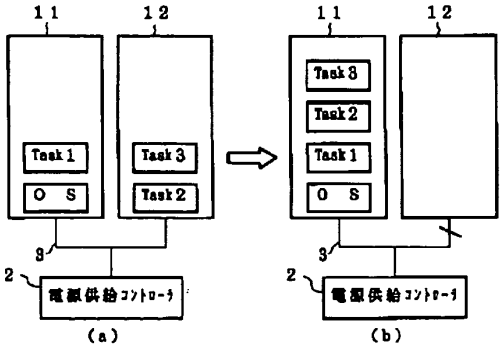
(74)代理人　弁理士　須山　佐一

(54)【発明の名称】　情報処理システムと情報処理システムの省電力方法

(57)【要約】
【課題】　従来、複数のプロセッサを有する情報処理システムにおいては、かりにプロセッサ毎にクロック周波数を可変できたとしても、この省電力機構による消費電力の節減効果は十分には得られないと言う課題があった。
【解決手段】　本発明の情報処理システムは、ＯＳが、ＯＳ自身を含め各タスクの処理単位のプロセッサ資源の要求量を事前に知り、プロセッサ資源が不足しない範囲（プロセッサ資源の要求量の和が１００を越えない範囲）でタスク群を特定のプロセッサに集中させる。これにより、他のプロセッサが休止状態となるので、この休止状態のプロセッサに対する電源供給を停止、或いはクロック周波数を下げる。これによりシステム全体の消費電力を効果的に抑制することが可能となる。



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【特許請求の範囲】
【請求項1】　複数のタスクを並列に処理可能な複数のプロセッサと、
前記タスクを構成する処理単位毎のプロセッサ資源の要求量に基づき、休止状態のプロセッサが発生するように前記複数のプロセッサのうちの特定のプロセッサにプロセッサ資源の不足が生じない範囲で複数のタスクを集めるタスク管理手段と、
前記休止状態のプロセッサに対する電源供給を停止する電源供給制御手段とを具備することを特徴とする情報処理システム。
【請求項2】　複数のタスクを並列に処理可能な複数のプロセッサと、
前記タスクを構成する処理単位毎のプロセッサ資源の要求量に基づき、休止状態のプロセッサが発生するように前記複数のプロセッサのうちの特定のプロセッサにプロセッサ資源の不足が生じない範囲で複数のタスクを集めるタスク管理手段と、
前記休止状態のプロセッサの動作クロック周波数を下げる手段とを具備することを特徴とする情報処理システム。
【請求項3】　複数のタスクを並列に処理可能な複数のプロセッサを備えた情報処理システムの省電力方法において、
前記タスクを構成する処理単位毎のプロセッサ資源の要求量に基づき、休止状態のプロセッサが発生するように前記複数のプロセッサのうちの特定のプロセッサにプロセッサ資源の不足が生じない範囲で複数のタスクを集め、前記休止状態のプロセッサに対する電源供給を停止することを特徴とする情報処理システムの省電力方法。
【請求項4】　複数のタスクを並列に処理可能な複数のプロセッサを備えた情報処理システムの省電力方法において、
前記タスクを構成する処理単位毎のプロセッサ資源の要求量に基づき、休止状態のプロセッサが発生するように前記複数のプロセッサのうちの特定のプロセッサにプロセッサ資源の不足が生じない範囲で複数のタスクを集め、前記休止状態のプロセッサの動作クロック周波数を下げることを特徴とする情報処理システムの省電力方法。
【請求項5】　請求項3または4記載の情報処理システムの省電力方法において、
前記タスクの処理単位の処理に要した時間と要求処理時間とから前記処理単位のプロセッサ資源の要求量を求めることを特徴とする情報処理システムの省電力方法。
【発明の詳細な説明】
【0001】
【発明の属する技術分野】本発明は、複数のプロセッサを備えた情報処理システムとその省電力化の方法に関する。

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【0002】
【従来の技術】プロセッサの高速化に伴う消費電力の増大を抑えるための手段としてクロックギアシステムがある。このクロックギアシステムは、プロセッサの動作クロック周波数を段階的に可変できるものとし、プロセッサが休止状態にある時はクロック周波数を下げることによってシステム全体の消費電力の節減効果を得るものである。
【0003】ここで、複数のタスクを並列（時分割多重）に処理することが可能な複数のプロセッサを持つ情報処理システムを考える。また、処理の最大効率を得るため、タスク群は各プロセッサに均等な数で割り当てられるものとする。そして個々のプロセッサのクロック周波数は2段階に可変できるものとする。
【0004】このような情報処理システムにおいて、全てのプロセッサがタスクを処理している場合、全プロセッサのクロック周波数は同一に設定され、全プロセッサの消費電力もほぼ同じである。また、タスクの数がプロセッサの数を下回った場合、休止状態のプロセッサが発生する。そこでこのプロセッサのクロック周波数を下げることによって、このプロセッサの消費電力が節減される。
【0005】以下に、かかる省電力機構を備えた情報処理システムの問題点を述べる。
【0006】上記情報処理システムにおいて消費電力の節減効果が得られるのは、タスクの数がプロセッサの数を下回った場合のような特定の状況に限られる。タスクの数がプロセッサの数以上の場合は、全てのプロセッサがタスク処理を実行するから、全てのプロセッサのクロック周波数は高いほうの値に設定される。タスクの数がプロセッサの数を下回ることは稀れであり、よって、かかる従来方式では、消費電力の十分な節減効果が期待できないと考えられる。
【0007】
【発明が解決しようとする課題】このように従来、複数のプロセッサを有する情報処理システムにおいては、かりにプロセッサ毎にクロック周波数を可変できたとしても、この省電力機構による消費電力の節減効果は十分には得られないと言う問題があった。
【0008】本発明はこのような課題を解決するためのもので、タスクの数がプロセッサの数を上回る状況においても休止状態のプロセッサを積極的につくりだすことによって、システム全体の消費電力を効果的に抑制することのできる情報処理システムとその省電力方法の提供を目的としている。
【0009】
【課題を解決するための手段】本発明の情報処理システムは上記した目的を達成するために、複数のタスクを並列に処理可能な複数のプロセッサと、タスクを構成する処理単位毎のプロセッサ資源の要求量に基づき、休止状

態のプロセッサが発生するように複数のプロセッサのうちの特定のプロセッサにプロセッサ資源の不足が生じない範囲で複数のタスクを集めるタスク管理手段と、休止状態のプロセッサに対する電源供給を停止する電源供給制御手段とを具備することを特徴とする。

【００１０】また、本発明の情報処理システムの省電力方法は、複数のタスクを並列に処理可能な複数のプロセッサを備えた情報処理システムの省電力方法において、タスクを構成する処理単位毎のプロセッサ資源の要求量に基づき、休止状態のプロセッサが発生するように複数のプロセッサのうちの特定のプロセッサにプロセッサ資源の不足が生じない範囲で複数のタスクを集め、休止状態のプロセッサに対する電源供給を停止することを特徴とする。

【００１１】これらの発明においては、タスクを構成する処理単位毎のプロセッサ資源の要求量に基づき、複数のプロセッサのうちの特定のプロセッサにプロセッサ資源の不足が生じない範囲で複数のタスクを集めることで、特定プロセッサをフル稼働に近い状態にする一方、休止状態のプロセッサをつくりだす。この休止状態のプロセッサに対する電源供給を停止することによって、システム全体の消費電力を節減することができる。

【００１２】さらに本発明の情報処理システムは上記した目的を達成するために、複数のタスクを並列に処理可能な複数のプロセッサと、タスクを構成する処理単位毎のプロセッサ資源の要求量に基づき、休止状態のプロセッサが発生するように複数のプロセッサのうちの特定のプロセッサにプロセッサ資源の不足が生じない範囲で複数のタスクを集めるタスク管理手段と、休止状態のプロセッサの動作クロック周波数を下げる手段とを具備することを特徴とする。

【００１３】また、本発明の情報処理システムの省電力方法は、複数のタスクを並列に処理可能な複数のプロセッサを備えた情報処理システムの省電力方法において、タスクを構成する処理単位毎のプロセッサ資源の要求量に基づき、休止状態のプロセッサが発生するように複数のプロセッサのうちの特定のプロセッサにプロセッサ資源の不足が生じない範囲で複数のタスクを集め、休止状態のプロセッサの動作クロック周波数を下げることを特徴とする。

【００１４】これらの発明においては、タスクを構成する処理単位毎のプロセッサ資源の要求量に基づき、複数のプロセッサのうちの特定のプロセッサにプロセッサ資源の不足が生じない範囲で複数のタスクを集めることで、特定プロセッサをフル稼働に近い状態にする一方、休止状態のプロセッサをつくりだす。この休止状態のプロセッサの動作クロック周波数を下げることによって、システム全体の消費電力を節減することができる。

【００１５】

【発明の実施の形態】以下、この発明の実施の形態について図面を参照して説明する。



【００１６】図１は本実施形態である情報処理システムの全体的な構成を示す図である。

【００１７】同図に示すように、この情報処理システムは複数例えば４つのプロセッサ１１、１２、１３、１４と各プロセッサへの電源供給を制御する電源供給コントローラ２とを備えて構成される。各プロセッサと電源供給コントローラ２とは相互にバス３及び電源線４を通じて接続されている。個々のプロセッサは各々、複数のタスクを並列（時分割多重）に処理することが可能である。

【００１８】この情報処理システムにおいては、タスク群を特定のプロセッサにそのプロセッサの資源が許す範囲で集中させることで、できるだけ多くのプロセッサが休止状態となるように、各プロセッサに対するタスクの割り当てが行われる。

【００１９】その様子を図２に示す。簡単化のため、この例では２つのプロセッサ１１、１２間でのタスクの移動を示す。同図（ａ）はタスク移動前の状態であり、プロセッサ１１はＯＳとタスク（Task１）を有する。またプロセッサ２はタスク（Task２）とタスク（Task３）を有する。

【００２０】ここで、ＯＳ、タスクの“プロセッサ資源の要求量”について説明する。“プロセッサ資源の要求量”とは、ＯＳ、タスクの処理を行う上でプロセッサの能力のどのくらいの割合を必要とするかを示す値であり、プロセッサをフル稼働させてＯＳ、タスク内の処理単位（関数単位、ブロック単位等の各部位、１つのタスクが１つの処理単位となる場合もある。）を実行した場合の処理時間をＴ１とし、その処理単位の要求処理時間をＴ２として、（Ｔ１／Ｔ２）×１００の計算式で求めることができる。例えば、タスク内のある処理単位の要求処理時間Ｔ２を１０ｍｓ、その処理単位をプロセッサをフル稼働させて実行した場合の処理時間Ｔ１を５ｍｓとすれば“プロセッサ資源の要求量”は（５／１０）×１００＝５０（％）となる。

【００２１】図２において、ＯＳの現在の処理単位のプロセッサ資源の要求量は２５、同じくタスク（Task１）は３０、タスク（Task２）は２０、タスク（Task３）は２０とする。また２つのプロセッサ１１、１２の性能は同一とする。図２（ａ）のタスク移動前の状態において、一方のプロセッサ１１が所有するＯＳとタスク（Task１）の現在のプロセッサ資源の要求量の和は５５、他方のプロセッサ１２が所有するタスク（Task２）とタスク（Task３）の現在のプロセッサ資源の要求量の和は４０である。したがって、プロセッサ１１は１００－５５＝４５のプロセッサ資源を余しており、図２（ｂ）に示すように、プロセッサ１２の所有するタスク（Task２）とタスク（Task３）をプロセッサ１１に移動させても、プロセッサ１１においてＯＳと全タスクを並列に処理す

ることが可能である。

【００２２】本実施形態の情報処理システムは、このようなタスクの移動・割り当て処理をＯＳの管理の下で実行する。ＯＳはＯＳ自身を含め各タスクの処理単位のプロセッサ資源の要求量を事前に知り、プロセッサ資源が不足しない範囲（プロセッサ資源の要求量の和が１００を越えない範囲）でタスク群を特定のプロセッサに集中させるように各プロセッサに対するタスクの割り当てを制御する。各タスクには、プロセッサ資源の要求量を示す情報が処理単位毎に付加されており、これを基にＯＳは現在の各タスクのプロセッサ資源の要求量を知る。勿論、ＯＳ自身にもプロセッサ資源の要求量を示す情報が付加されている。

【００２３】図２に示したように、プロセッサ１２の全てのタスク（Task２，Task３）をプロセッサ１１に移動させたことによって、プロセッサ１２は休止状態となる。ＯＳは、プロセッサ１２が休止状態になったことを知ると、電源供給コントローラ２に命令を出し、プロセッサ１２への電源供給を停止させる。

【００２４】図３は新たなタスク（Task４）が発生した場合を示している。このタスク（Task４）のこれから処理しようとしている処理単位のプロセッサ資源の要求量は２０である。今、プロセッサ１１が所有しているＯＳと３つのタスク（Task１，Task２，Task３）のプロセッサ資源の要求量の和は９５であるから、これに新たなタスク（Task４）のプロセッサ資源の要求量を加えると９５＋２０＝１１５となってプロセッサ１１のプロセッサ資源を越えてしまう。そこでこの場合、ＯＳは電源供給コントローラ２に命令を出してプロセッサ１２への電源供給を復活させると共に、新たなタスク（Task４）をプロセッサ１２に割り当てて、プロセッサ１２にタスク（Task４）の処理を実行させる。

【００２５】また、図２に示すプロセッサ１１がＯＳと３つのタスク（Task１，Task２，Task３）を保有する状態において、いずかのタスクのこれから処理しようとする処理単位のプロセッサ資源の要求量が増加してプロセッサ１１に対するプロセッサ資源の要求量の和が１００を越える場合、ＯＳはこれを判断していずかのタスクを他方のプロセッサ１２に移動させる。

【００２６】例えば、図４に示すように、タスク（Task２）のこれから処理する処理単位のプロセッサ資源の要求量が３０であるとする。この場合、ＯＳと３つのタスク（Task１，Task２，Task３）のプロセッサ資源の要求量の和は２５＋３０＋３０＋２０＝１０５となり、１００を越えてしまため、いずかのタスクを他方のプロセッサ１２に移動させる。この例では、どのタスクを移動させてもプロセッサ１１に要求されるプロセッサ資源量の和は１００未満となるので、どのタスクをプロセッサ１２に移動させてもよい。

【００２７】前述したように、以上のタスク移動・割り当て制御を実現するためには、各タスクにプロセッサ資源の要求量を示す情報を付加しておく必要がある。タスクにプロセッサ資源の要求量を示す情報を付加する方法としては次のようなものを挙げることができる。

【００２８】図５において、５１はソースプログラム、５２はソースプログラム５１からオブジェクトプログラム５３を生成するコンパイラ、アセンブラ等の言語処理系、５４はオブジェクトプログラム５３を連結編集して一つのプロセッサ実行形式のプログラム（タスク）５５を生成するリンカである。

【００２９】タスクにプロセッサ資源の要求量を示す情報を付加する第１の方法は、プログラム製作者自身がタスクの処理単位毎のプロセッサ資源の要求量を求めることによってソースコード或いはオブジェクコードで記述された資源記述ファイル６を作成し、言語処理時或いはリンカ時に、資源記述ファイル６の記述内容をタスク本体に付加する方法である。また、タスクのソースプログラム１自体にプロセッサ資源の要求量のソースコードを一体化させてもよい。この場合、タスクのソースプログラム１の各部位にＣ言語におけるpragmaのような記述方法でプロセッサ資源の要求量を示す情報を挿入する方法が考えられる。

【００３０】第２の方法は、第１の方法の資源記述ファイル６に代えてタスクの処理単位の要求処理時間を記述した要求処理時間記述ファイルをプログラム製作者自身が作成し、言語処理系が、そのファイルに記述された要求処理時間に基づいて各処理単位のプロセッサ資源の要求量を算出してオブジェクトコード化し、これをタスク本体のオブジェクトコードに付加する方法である。この第２の方法は、第１の方法に比べプログラム製作者の作業負担を軽くすることができる。

【００３１】第３の方法は、プロセッサにおいてタスクの処理を実際に実行してみて、その処理に要した時間と、第２の方法で用いた要求処理時間記述ファイルに記述された要求処理時間とからプロセッサ資源の要求量を計算する方法である。前述したように、プロセッサ資源の要求量は、例えば、プロセッサをフル稼働させてタスク内の処理単位を実行した場合の処理時間をＴ１、その処理単位の要求処理時間をＴ２として（Ｔ１／Ｔ２）×１００の計算式で求めることができる。

【００３２】このプロセッサ資源の要求量の計算は、情報処理システムを実際に運用する前にプロファイリング期間を設け、このプロファイリング期間に全てのタスクの処理単位について行うようにすることが望ましい。

【００３３】かくして本実施形態の情報処理システムによれば、特定のプロセッサにそのプロセッサ資源の不足が生じない範囲で多くのタスクを集中させることで、その他のプロセッサを積極的に休止状態にし、これら休止状態のプロセッサに対する電源供給を停止することによって、システム全体の消費電力を効果的に抑制すること

が可能となる。

【００３４】なお、本実施形態では、休止状態のプロセッサに対する電源供給を停止するようにしたが、プロセッサ毎のクロック周波数を可変できるように構成し、休止状態のプロセッサに対するクロック周波数を下げることによっても消費電力の節減効果が得られる。

【００３５】

【発明の効果】以上説明したように本発明によれば、タスクを構成する処理単位毎のプロセッサ資源の要求量に基づき、複数のプロセッサのうちの特定のプロセッサにプロセッサ資源の不足が生じない範囲で複数のタスクを集めることで、特定プロセッサをフル稼働に近い状態にする一方、休止状態のプロセッサをつくりだし、この休止状態のプロセッサに対する電源供給を停止することによって、システム全体の消費電力を節減することができる。

【００３６】また、本発明によれば、タスクを構成する処理単位毎のプロセッサ資源の要求量に基づき、複数のプロセッサのうちの特定のプロセッサにプロセッサ資源の不足が生じない範囲で複数のタスクを集めることで、特定プロセッサをフル稼働に近い状態にする一方、休止状態のプロセッサをつくりだし、この休止状態のプロセッサの動作クロック周波数を下げることによって、システム全体の消費電力を節減することができる。

【図面の簡単な説明】

【図１】本実施形態である情報処理システムの全体的な構成を示す図

【図２】図１の情報処理システムにおけるタスク移動を説明するための図

【図３】図１の情報処理システムにおいて新たなタスクが発生した場合のタスク割り当てを説明するための図

【図４】図１の情報処理システムにおいて処理単位のプロセッサ資源の要求量が増大した場合のタスク移動を説明するための図

【図５】プロセッサ資源の要求量の情報をタスクに付加する方法を説明するための図

【符号の説明】

２……電源供給コントローラ

３……バス

４……電源線

１１、１２、１３、１４……プロセッサ

５６……資源記述ファイル

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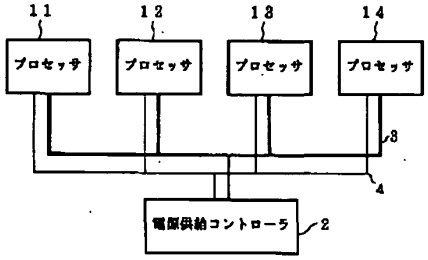


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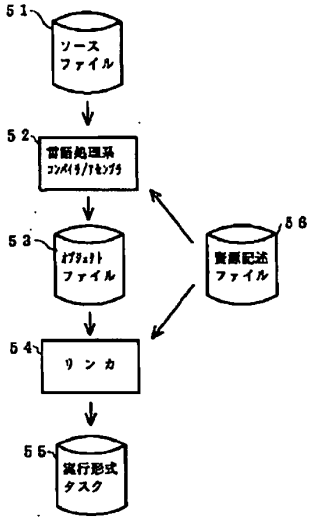

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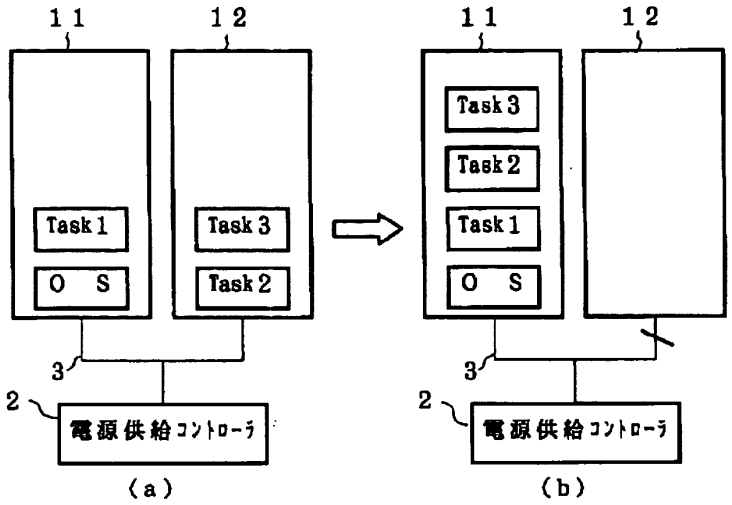


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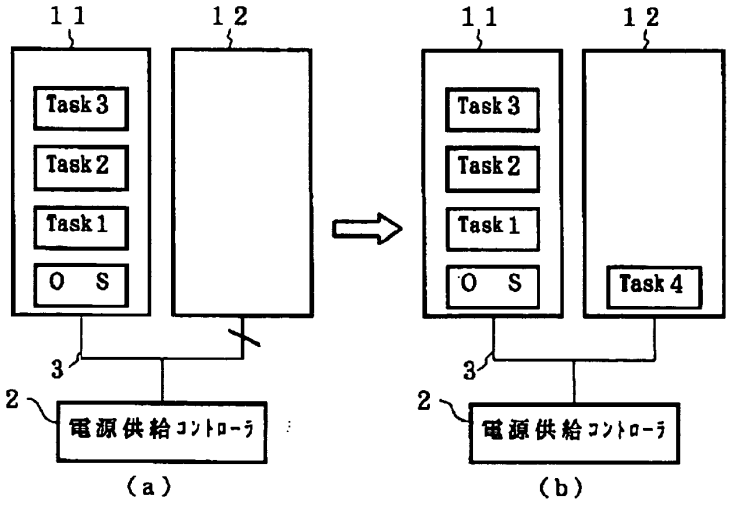

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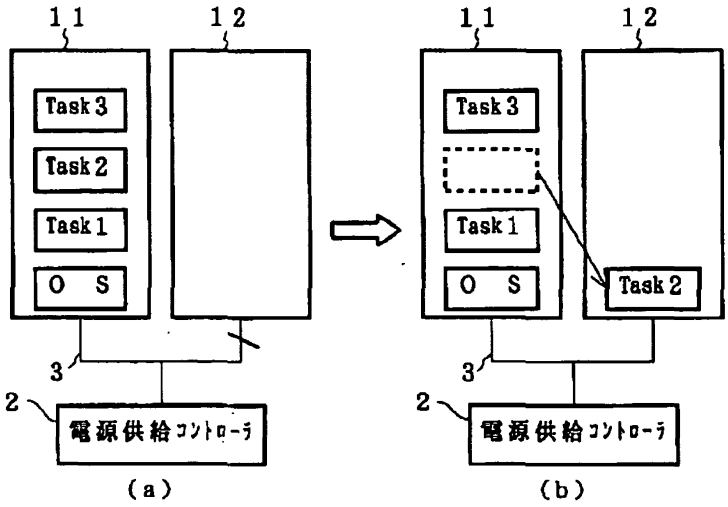
11
12
Task 3
Task 2
Task 1
O S
3
2
電源供給コントローラ
(a)
11
12
Task 3
Task 1
O S
Task 2
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2
電源供給コントローラ
(b)

(12) INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(19) World Intellectual Property Organization
International Bureau

(43) International Publication Date
19 April 2001 (19.04.2001)

PCT

(10) International Publication Number
WO 01/27728 A1

(51) International Patent Classification[7]: G06F 1/32

(21) International Application Number: PCT/US00/11062

(22) International Filing Date: 25 April 2000 (25.04.2000)

(25) Filing Language: English

(26) Publication Language: English

(30) Priority Data:
09/418,291 14 October 1999 (14.10.1999) US

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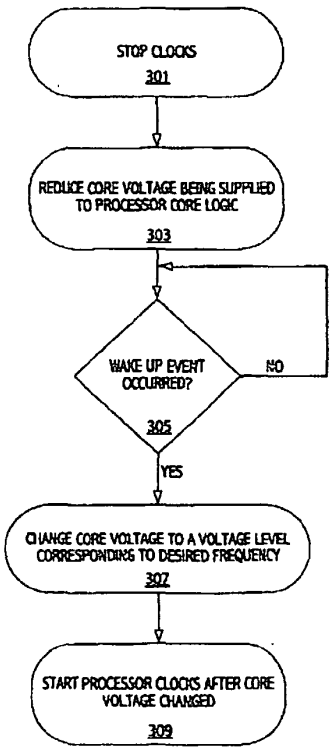
(81) Designated States *(national)*: JP, KR.

(84) Designated States *(regional)*: European patent (AT, BE, CH, CY, DE, DK, ES, FI, FR, GB, GR, IE, IT, LU, MC, NL, PT, SE).

Published:
— *With international search report.*

*For two-letter codes and other abbreviations, refer to the "Guidance Notes on Codes and Abbreviations" appearing at the beginning of each regular issue of the PCT Gazette.*

(54) Title: MINIMIZING POWER CONSUMPTION DURING SLEEP MODES BY USING MINIMUM CORE VOLTAGE NECESSARY TO MAINTAIN SYSTEM STATE




(57) Abstract: A control circuit reduces voltage being supplied to an integrated circuit in a sleep mode in which context (e.g. CPU state) is maintained. Because the voltage required to maintain the integrated circuit state intact may be significantly less than the voltage at which the integrated circuit can functionally operate at a predetermined frequency, significant power savings can be achieved by reducing voltage while the clocks are stopped, thereby reducing leakage current and saving power.

WO 01/27728 A1

# MINIMIZING POWER CONSUMPTION DURING SLEEP MODES BY USING MINIMUM CORE VOLTAGE NECESSARY TO MAINTAIN SYSTEM STATE

## Technical Field

This invention relates to power consumption in integrated circuits and more specifically to reducing power consumption on an integrated circuit while clocks are stopped.

## Background Art

A conventional notebook computer has power constraints that cause it to employ techniques to reduce power consumption to conserve battery life. In addition, the conventional notebook computer has thermal constraints due to a small, densely packed system construction that limits its ability to safely dissipate the heat generated by computer operation. The power savings techniques also beneficially reduce the amount of heat needed to be dissipated.

The frequency of operation (clock frequency) of the processor and its operating voltage are primary determinants of power consumption. Since power consumption and dissipation are roughly proportional to the processor's frequency of operation, scaling down the processor's frequency has been a common method of staying within notebook computer power and thermal limitations.

A common power management technique, called "throttling", temporarily stops processor clocks, to reduce power consumption and thus reduce heat generation. Throttling continuously stops and starts processor operation by turning its clocks off and on according to a predefined duty cycle with a period of a few milliseconds. The reduction in the effective speed of the processor reduces power dissipation and thus the processor's temperature. A clock control signal (e.g., STPCLK# in x86 architectures) modulates the duty cycle of processor operation. The clock control signal, when asserted, causes the processor to gate off the clocks being supplied to core logic in the processor. In some current processor designs, e.g., x86 processors, a Stop Grant cycle on a host or system bus is executed to indicate that the stop clock request on the asserted clock control signal has been completed. A temperature sensor placed on or near the processor's heat sink can initiate throttling when needed.

In addition, when operating from its battery, most notebooks take advantage of the processor's idle periods by periodically stopping processor operation to reduce power consumption. Applications like word processors typically leave the processor idle much of the time. For example, in a word processing application, a processor will do a brief burst of work after each letter is typed, then its operation is stopped until the next keystroke. As a result, the typical processor power consumption when running a word processing application, can be as much as 30-50% below the maximum. That idle time can be exploited by the computer system to achieve additional power savings by putting the processor to sleep temporarily.

Current x86 based computer systems utilize an industry supported power management approach described in the Advanced Configuration and Power Interface Specification (ACPI), Revision 1.0a, by Intel, Microsoft and Toshiba dated November 19, 1998, which is incorporated herein by reference. The ACPI is an

operating system (OS) controlled power management scheme that uses features built into the Windows 95, 98 and Windows NT or other compatible operating systems. It defines a standard interrupt (System Control Interrupt or SCI) that handles all ACPI events. System control interrupts are generated by devices to inform the OS about system events.

As part of that power management approach, ACPI specifies sleep and suspend states. Sleep states temporarily halt processor operation and operation can be restored in a few milliseconds. A computer system processor enters the sleep state when internal activity monitors indicate no processing is taking place. When a keystroke is entered, a mouse moves or data is received via a modem, the processor wakes up in order to resume operation, the clocks are turned on and the CPU continues executing from where it left off.

Other modes save processor context external to the processor such as to system memory or even to hard disk. Suspend states shut down more of the notebook's system (e.g. display or hard drive) and take a few seconds for operation to be restored. Suspend states copy the present context of the system (sufficient for the computer to resume processing the application(s) presently opened) into memory (suspend to RAM) or to the hard drive (suspend to disk) and power down peripherals. Obviously in these other modes, longer latency is incurred to resume normal system operation.

When computer systems stop the central processing unit (CPU) clocks during a sleep mode or during throttling, a short latency for resuming processor operation is desirable. One way to achieve that short latency is to ensure that CPU context is not lost. That means that the various latches and other circuit nodes in the CPU that hold information required (e.g., the state of processor registers) for the processor to resume operations where it left off, are maintained in the CPU while clocks are stopped. Maintaining processor context requires that the CPU receive power even though the clocks are stopped.

Note that processors typically have separate regions of the chip that receive separate power supply voltages. For example, such regions may include a core region, as well as a peripheral region where input/output (I/O) circuits are located. The peripheral region often remains powered up even if the core voltage is turned off. Therefore, core voltage which must be maintained to ensure processor context is maintained (assuming I/O voltage is also on). In most current notebook designs, CPU core voltage is typically set during initialization, and is not changed after that.

When power is supplied during the sleep state to maintain CPU context, the CPU still consumes power because of leakage current. The leakage current is generally proportional to the core voltage, and the power consumption is proportional to the square of the core voltage. The leakage current can be significant enough to drain the battery. For example, an AMD-K-6®-2 processor can consume several hundred milliwatts while in sleep mode. Additionally, some circuit designs may be more leaky than others, resulting in even more power being consumed in sleep mode.

It is desirable to reduce power consumption in computers, particularly in portable computers where maximizing battery life and reducing heat generation by reducing power consumption is particularly

advantageous. Therefore it would be desirable to reduce power consumption, if possible, when clocks are stopped and power is being consumed due to leakage current.

## DISCLOSURE OF INVENTION

Accordingly, the invention provides a way to save power while a processor (or other integrated circuit) is in a sleep mode in which context is maintained. Because the voltage required to maintain the integrated circuit context (e.g. processor state) intact may be significantly less than the voltage at which the processor can functionally operate at a particular frequency, significant power savings can be achieved by reducing processor voltage while the processor clocks are stopped.

In one embodiment, the invention provides a method of supplying a first voltage to at least a first circuit portion of an integrated circuit during an operational mode. The method further includes stopping clocks which are being supplied to the first circuit portion to place the integrated circuit in a reduced power consumption state and then supplying a second voltage, less than the first voltage, to the first circuit portion while the clocks are stopped, the second voltage being at a voltage sufficient to maintain context of the first circuit portion in existence at a time when the clocks were stopped.

In another embodiment, the invention provides an apparatus that includes an integrated circuit that has a plurality of circuits holding, at least in substantial part, context indicative of a current operational state of the integrated circuit. A power supply circuit supplies variable voltages to the integrated circuit. A control circuit is coupled to the power supply circuit, and supplies the power supply circuit with first voltage control information, indicating a first voltage to be supplied, while clocks are being supplied to the plurality of circuits. The control circuit supplies the power supply circuit with second voltage control information, indicating a second voltage to be supplied, while the clocks are stopped, the second voltage being lower than the first voltage.

## BRIEF DESCRIPTION OF DRAWINGS

The present invention may be better understood, and its numerous objects, features, and advantages made apparent to those skilled in the art by referencing the accompanying drawings, wherein:

Fig. 1 illustrates an exemplary system that can exploit the present invention;

Fig. 2 illustrates additional details over a control circuit used in one embodiment of the present invention; and

Fig. 3 is a flow chart of an embodiment of the present invention.

## MODE(S) FOR CARRYING OUT THE INVENTION

Additional power savings can be realized in computer systems by reducing the voltage supplied to the processor during a state in which processor clocks are stopped and processor context is maintained. With the

clocks off, the voltage level required to maintain processor context can be reduced to levels below that needed for proper operation of the clocked circuits. Put another way, the voltage required to maintain state, is lower than that needed to change state reliably.

In an exemplary embodiment illustrated in Fig. 1, voltage regulator 101 supplies core voltage 102 to processor (CPU) 103. In the embodiment illustrated, integrated circuit 105 controls the voltage level that is supplied to CPU 103 by supplying voltage control signals VID[0:4] to voltage regulator 101. VID refers to "voltage ID" which is commonly used in the industry to describe the voltage control signals. Integrated circuit 105 may be a south bridge integrated circuit, which is known in the art as one chip of a chipset pair. The south bridge, originally providing a bridge between the Peripheral Component Interconnect (PCI) bus and the ISA bus, also typically incorporates power management functions. The south bridge may also contain integrated legacy functions, as well as interfaces for newer buses such as Universal Serial Bus (USB) and other additional functions. The chipset pair also typically includes a north bridge integrated circuit (not shown) that provides a memory control function as well as a bridge function between the host bus connected to the processor and the Peripheral Component Interconnect (PCI) bus. Clock generator 107 supplies a clock signal 106 used by CPU 103 to generate clocks supplied to core logic in the processor. Clock generator 107 can be controlled by clock stop signal 112 to selectably turn on and off clocks supplied to CPU 103 and other system components.

The variable voltage regulator 101 may be, e.g., the National Semiconductor's LM4130, whose output voltage can be controlled by an external device such as south bridge 105. It is desirable for the voltage regulator to support at least four control bits and for the output voltage to be controllable in steps of 50mV (or smaller) covering a minimum range of from 1.45 to 2.2 volts. A wider range or different granularity may be desirable in some applications.

The CPU clocks can be stopped as follows. The "stop clock" signal refers to STPCLK# signal 110 (where # indicates an active low signal), which causes CPU 103 to stop execution at the end of the current instruction, and turn off internal distribution of the CPU's clock, to most, if not all sections of processor core logic. The CPU executes a "Stop Grant" bus cycle to indicate that the CPU has entered the Stop Grant state.

In addition to stopping distribution internally, clocks to the CPU and other components may be stopped using the "clock stop" signal 112 provided by south bridge 105 to clock generator 107. One typical sequence to stop the clocks is to assert the STPCLK# signal 110 to enter the Stop Grant state, wait for the Stop Grant bus cycle and then turn off the clock generator 107 distribution of clocks using the clock stop signal 112 to enter the Stop Clock state.

Assume that the clocks to the processor are stopped as described above. The particular mechanism to stop clocks may vary in different embodiments and is not critical to the present invention. The clocks may be stopped in association with throttling or because of the processor entering a sleep mode or any other scenario in which clocks are stopped and power is left on. After the clocks are stopped, the south bridge 105 (or any other suitable logic device) supplies new voltage control signals to the CPU core voltage regulator 101 instructing the voltage regulator to supply a reduced voltage to the CPU core. Depending on the sleep mode, it

may still be important that the voltages supplied to other areas of the CPU, such as the I/O circuits are maintained at suitable levels since such circuits may be interfacing with I/O devices, external circuits or buses that may be active when the processor has its core logic clocks stopped.

Because sleep and throttle (and suspend) states require the processor operation to be stopped, it is impossible for system software to control all sleep, and recover operations. To overcome this problem, control logic is typically implemented external to the processor. For example, such control logic may be implemented in the input/output integrated circuit (referred to herein as south bridge 105) to control the final stages of sleep and suspend operations and the resume operation and other common power management features. One such integrated circuit is the Intel Corp. 82371AB PCI-TO-ISA/IDE XCELERATOR (PIIX4). The power management features contained therein reduce power consumption to extend battery life and control heat generation and dissipation to safely operate the processor. While some computer systems use a separate microcontroller for the task, most computer systems, including most notebook computers rely on the south bridge to provide the hardware needed for controlling thermal and power management. South bridge chips from various manufacturers have typically utilized the registers, timers and state machine definitions used in the Intel PIIX4 South Bridge. PIIX4 compatibility in current south bridge chips can be extended to support managing the core voltage during sleep states as described herein.

The control logic to reduce the core voltage after the clocks are turned off may be implemented as a state machine in south bridge 105. It may be particularly advantageous to augment or modify existing power management control logic in the south bridge to provide the enhanced functionality described herein. Once the voltage to the core has been reduced, the control logic waits for a system event that causes the CPU to resume processing. In the meantime the processor is in a quiescent state with the current consumption lower than it otherwise would have been. The system event causing the processor to wake-up, such as mouse movement or depressing a keyboard key, causes the CPU to resume normal operations. The control logic ensures that the core voltage is returned back to an operational level sufficient to support the desired clock frequency prior to the clocks being turned on. Otherwise, unpredictable results may be caused by clocking circuits when the power supply voltage is too low. Thus, the control logic issues new voltage control settings to voltage regulator 101 corresponding to a desired frequency and then the clocks are turned back on by, e.g., enabling clocks at clock generator 107, if necessary, and deasserting STPCLK#.

For a particular processor, the minimum operating core voltage ($V_{coremin}$), which specifies the minimum operating voltage required and the minimum static core voltage ($V_{coremins}$), which specifies the voltage necessary to maintain context with clocks stopped, can be specified over the entire product line. In one embodiment, the voltage control signal (VID) settings corresponding to $V_{coremin}$ and $V_{coremins}$ may be built into BIOS tables. When the system management software determines that the system needs to be put into a mode where clocks are stopped (e.g., a sleep mode or a throttle clock state), the core voltage is reduced to $V_{coremins}$ after the clock has been stopped. Note that if clocks are stopped externally, it may also be possible to reduce the voltage being supplied to I/O regions of the processor under some circumstances. When the system needs to be restored to operating conditions, the system automatically increases the core voltage to the setting needed

for the CPU operation at the desired frequency using the VID settings in the BIOS tables. The control settings may of course be located in any suitable location in the computer system.

Power savings will vary according to the leakage current present in the particular integrated circuit. For example, a processor consuming hundreds milliwatts of power while clocks are stopped in the Stop Grant state (on chip clock multiplier logic is still active) might reduce leakage current by lowering the power supply voltage enough to reduce power consumption by approximately 10%.

The voltage regulator's control pins should be configured for appropriate default operation upon power-up. Accordingly, as shown in Fig. 1, south bridge 105 in one embodiment, has jumper inputs IV[4:0]. The settings of the jumpers 111 (open or short), along with resistors 113, determine the default values for the VID signals. The IBF[2:0] inputs are for frequency control and a description of their use is not critical to understand the present invention. In addition to default modes, the south bridge 105 (or other suitable circuit) supplies the voltage regulator 101 with appropriate voltage control settings during operational modes and during sleep modes in which processor context is maintained.

Referring to Fig. 2, a high level block diagram shows one approach an integrated circuit (such as the south bridge in current x86 based computer systems) may use to provide appropriate voltage control settings for voltage regulator 101 (Fig. 1). In the embodiment illustrated in Fig. 2, multiplexer 201 receives three voltage controls settings as inputs. The first voltage control setting is from VID jumper settings 111, which as previously described, provide for default voltage settings on power-up. Multiplexer 201 also receives inputs from VID stop clock register 202, which provides the voltage control setting for the reduced processor voltage during stop clock modes ($V_{coremins}$). Multiplexer 201 receives inputs from VID operational register 203, which provides VID values for operational modes of the processor, i.e., when core clocks are running. Multiplexer 201 selects between the various voltage control settings according to a select line 204 supplied by control logic 210. Control logic 210 receives reset signal 207 and selects the jumper settings as the appropriate voltage control settings when reset (power on or other hard or soft reset) is asserted. Control logic 210 also receives a stop clock signal 208 which indicates that the processor has or is about to enter a stop clock state with core power maintained. In addition, control logic 210 receives indication 209 that a wakeup event has occurred, i.e., that the processor is going to resume normal operation.

The control logic also supplies load signal 211 to output register 205. During regular operational modes in which clocks are running, multiplexer 201 selects the operational VID register 203. Note that register 203 may be programmable to provide various VID signals during various operational modes. When the processor is in a sleep or throttle mode in which clocks are stopped, the control logic selects the VID stop clock register settings as the source for the voltage control signals VID. Thus, after the clocks are stopped (or simultaneously therewith), the select line selects the VID values from the stop clock VID register 202. The control logic then waits for a wake-up event to occur. When the wake-up event occurs as indicated by wake up signal 209 and before the clocks are started, the control logic causes the operational voltage control signals corresponding to the desired frequency of operation to be loaded into output register 205 from VID operational register 203. The clocks may then be enabled.

A variety of other circuit implementations would be readily apparent to one of skill in the art to accomplish the function of the circuit illustrated in Fig. 2. For example, the multiplexer may only select between jumper settings and a VID register with the VID register being appropriately updated before values in the register are supplied to the voltage regulator 100. That is, south bridge 105 can utilize a programmable register that can be written to update the VID pins with the appropriate voltage control settings available from, e.g., the BIOS tables rather than have separate operational and stop clock registers.

Referring to Fig. 3, a flow chart illustrates the operation of a system incorporating one embodiment for controlling core voltage to effectuate greater power savings according to the present invention. Assume that the clocks are stopped in 301. The clocks may be stopped using the STPCLK# signal 110 or using clock stop signal 112 to turn off the clock signal 106 being supplied to the processor clock multiplier logic, or both, or in any other manner appropriate for the particular implementation. After the clocks are stopped, the system reduces the core voltage being supplied to processor core logic in 303. That is accomplished, e.g., by selecting the appropriate voltage control settings and supplying those settings to the CPU core voltage regulator. Once the processor is maintaining its context with the reduced core voltage, and thereby realizing greater power savings, the control logic waits for a wake-up event in 305. Once the wake-up event occurs, the core logic voltage is changed to a level corresponding to the desired frequency of operation in 307 and then, after the processor is receiving the higher voltage, the clocks are turned on and the processor resumes normal operation.

The description of the invention set forth herein is illustrative, and is not intended to limit the scope of the invention as set forth in the following claims. For instance, while this invention has been described with relation generally to x86 based computer systems and is particularly relevant to notebook computers (which may also be referred to as laptops, portable or mobile computers), the teachings herein may also be utilized in any computing device such as personal digital assistants (PDAs), as well as systems containing any variety of processor in which it is desirable to save power by reducing voltage while clocks are stopped in a power savings mode and still maintain context. Further, while the description herein has focused on reducing core voltages in processors or CPUs, the power savings is equally applicable to any integrated circuit in which clocks are stopped to save power while context is maintained. Other variations and modifications of the embodiments disclosed herein, may be made based on the description set forth herein, without departing from the scope and spirit of the invention as set forth in the following claims

WHAT IS CLAIMED IS:

1. A method comprising:
supplying a first voltage to at least a first circuit portion of an integrated circuit during an operational mode;
stopping clocks which are being supplied to the first circuit portion to place the integrated circuit in a reduced power consumption state; and
then supplying a second voltage, less than the first voltage, to the first circuit portion while the clocks are stopped, the second voltage being at a voltage level sufficient to maintain context of the first circuit portion in existence at a time when the clocks were stopped.

2. The method as recited in claim 1 wherein the integrated circuit is a microprocessor including core logic, the first circuit portion being the core logic.

3. The method as recited in claim 1 further comprising:
supplying a third voltage to the integrated circuit after supplying the integrated circuit with the second voltage, the third voltage being greater than the second voltage; and
then starting the clocks being supplied to the first circuit portion to resume integrated circuit operations.

4. The method as recited in claim 3 wherein the first and third voltages are equal.

5. The method as recited in claim 3 wherein the third voltage is supplied in response to a wake-up event.

6. A computing device comprising:
an integrated circuit including a circuit region holding, at least in substantial part, context indicative of a current operational state of the integrated circuit;
a power supply circuit responsive to control inputs to supply variable voltages to the integrated circuit;
a control circuit coupled to the control inputs of the power supply circuit, wherein the control circuit supplies the control inputs with first voltage control information, indicating an operational voltage, while clocks are being supplied to the circuit region and the control circuit supplies the control inputs with second voltage control information indicating a second voltage, while the clocks are stopped, the second voltage being lower than the operational voltage.

7. The computing device as recited in claim 6 wherein the operational voltage is at a voltage level required to clock the circuit region at a predetermined frequency and the second voltage is below the voltage level required to clock the circuit region at the predetermined frequency.

8. An integrated circuit comprising:

a logic circuit responsive to an indication of normal clock operation in which internal clocks are running, to selectably provide first voltage control information indicative of a first voltage level and responsive to an indication of a stop clock state in which internal clocks are stopped to provide second voltage control information indicative of a second voltage level, the second voltage level being lower than the first voltage level; and

an output circuit coupled to receive the selectably provided first and second voltage control information, the first and second voltage control information for coupling to control inputs of a voltage generator.

9. The integrated circuit as recited in claim 8 wherein the logic circuit includes a selector circuit coupled to selectably provide to the output circuit the first or second voltage control information as the control inputs of the voltage generator and further includes at least a first programmable register coupled to the selector circuit and holding at least one of the first voltage control information and the second voltage control information.

10. The integrated circuit as recited in claim 9 further comprising control logic coupled to receive an indication of a wake-up event, an indication of a reset and an indication of the clock stop state, and generating a select signal for the selector circuit in response thereto.

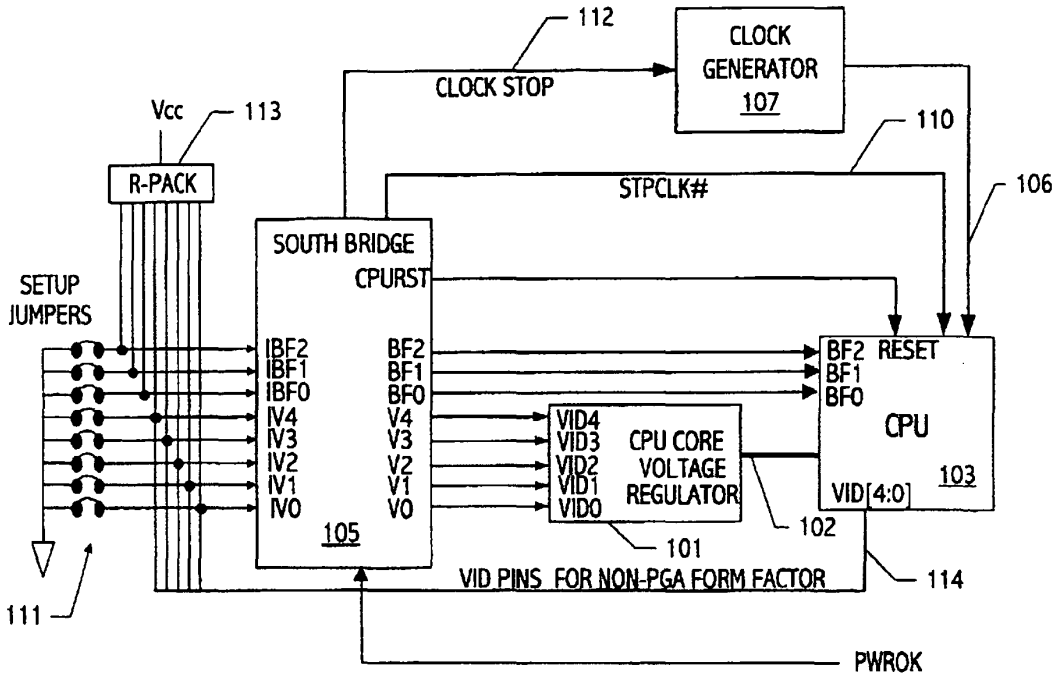

112
CLOCK STOP
CLOCK GENERATOR 107
Vcc
113
110
R-PACK
STPCLK#
106
SOUTH BRIDGE
CPURST
SETUP JUMPERS
IBF2
IBF1
IBF0
IV4
IV3
IV2
IV1
IV0
105
BF2
BF1
BF0
V4
V3
V2
V1
V0
VID4
VID3
VID2
VID1
VID0
CPU CORE VOLTAGE REGULATOR
101
102
BF2 RESET
BF1
BF0
CPU
103
VID[4:0]
VID PINS FOR NON-PGA FORM FACTOR
114
111
PWROK

FIG. 1

2/3

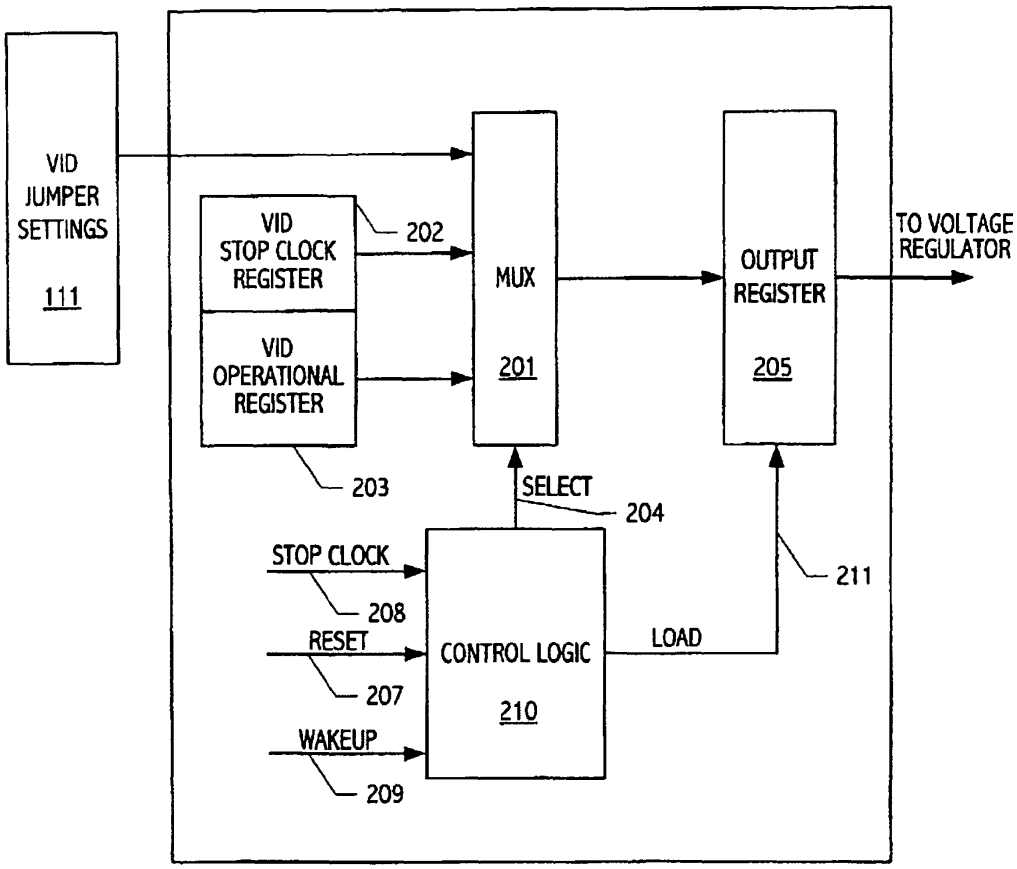

VID JUMPER SETTINGS 111
VID STOP CLOCK REGISTER
202
VID OPERATIONAL REGISTER
203
MUX 201
SELECT
204
OUTPUT REGISTER 205
TO VOLTAGE REGULATOR
211
STOP CLOCK
208
RESET
207
WAKEUP
209
CONTROL LOGIC 210
LOAD

FIG. 2

3/3

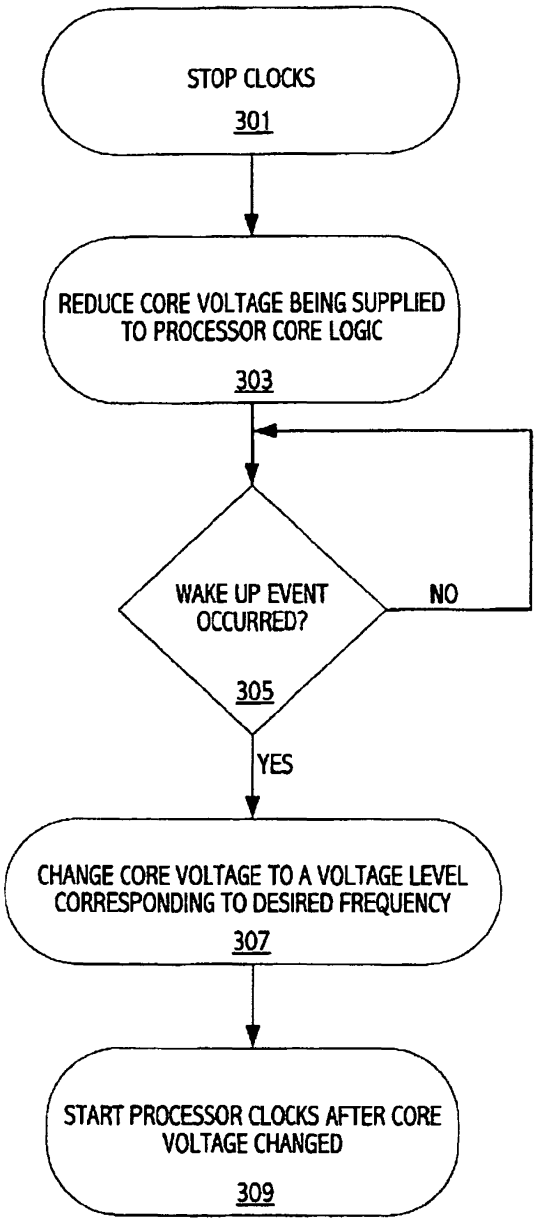

STOP CLOCKS
301
REDUCE CORE VOLTAGE BEING SUPPLIED TO PROCESSOR CORE LOGIC
303
WAKE UP EVENT OCCURRED?
305
NO
YES
CHANGE CORE VOLTAGE TO A VOLTAGE LEVEL CORRESPONDING TO DESIRED FREQUENCY
307
START PROCESSOR CLOCKS AFTER CORE VOLTAGE CHANGED
309

FIG. 3

INTERNATIONAL SEARCH REPORT

Into ional Application No
PCT/US 00/11062

A. CLASSIFICATION OF SUBJECT MATTER
IPC 7 G06F1/32

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
IPC 7 G06F

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)
EPO-Internal, WPI Data, PAJ, IBM-TDB

C. DOCUMENTS CONSIDERED TO BE RELEVANT

| Category * | Citation of document, with indication, where appropriate, of the relevant passages | Relevant to claim No. |
|---|---|---|
| X | US 5 745 375 A (GUNTHER STEPHEN H ET AL)<br>28 April 1998 (1998-04-28)<br>column 1, paragraph 3<br>column 5, paragraph 2<br>figure 5 | 1-10 |
| X | EP 0 632 360 A (XEROX CORP)<br>4 January 1995 (1995-01-04)<br>column 4, paragraph 2<br>column 7, paragraph 3<br>figures 1-3 | 1-10 |
| X | US 5 852 737 A (BIKOWSKY ZEEV)<br>22 December 1998 (1998-12-22)<br>column 3, line 20 - line 38<br>column 7, paragraph 2; figures 2,3,6 | 1-10 |

☐ Further documents are listed in the continuation of box C.

☒ Patent family members are listed in annex.

* Special categories of cited documents :

"A" document defining the general state of the art which is not considered to be of particular relevance

"E" earlier document but published on or after the international filing date

"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)

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"&" document member of the same patent family

| Date of the actual completion of the international search | Date of mailing of the international search report |
|---|---|
| 14 September 2000 | 22/09/2000 |

| Name and mailing address of the ISA | Authorized officer |
|---|---|
| European Patent Office, P.B. 5818 Patentlaan 2<br>NL - 2280 HV Rijswijk<br>Tel. (+31-70) 340-2040, Tx. 31 651 epo nl,<br>Fax: (+31-70) 340-3016 | Ciarelli, N |

Form PCT/ISA/210 (second sheet) (July 1992)

INTERNATIONAL SEARCH REPORT

Information on patent family members

International Application No
PCT/US 00/11062

| Patent document cited in search report | Publication date | Patent family member(s) | Publication date |
|---|---|---|---|
| US 5745375 A | 28-04-1998 | AU 7247296 A | 17-04-1997 |
| | | EP 0858634 A | 19-08-1998 |
| | | WO 9712329 A | 03-04-1997 |
| | | US 5825674 A | 20-10-1998 |
| EP 0632360 A | 04-01-1995 | JP 7020968 A | 24-01-1995 |
| US 5852737 A | 22-12-1998 | NONE | |

Form PCT/ISA/210 (patent family annex) (July 1992)

| Electronic Acknowledgement Receipt | |
|---|---|
| **EFS ID:** | 6288944 |
| **Application Number:** | 11894991 |
| **International Application Number:** | |
| **Confirmation Number:** | 9781 |
| **Title of Invention:** | Saving power when in or transitioning to a static mode of a processor |
| **First Named Inventor/Applicant Name:** | Andrew Read |
| **Correspondence Address:** | MURABITO, HAO & BARNES LLP<br>-<br>Third Floor<br>Two North Market Street<br>San Jose CA 95113<br>US 4089389060<br>- |
| **Filer:** | Anthony C. Murabito/Julie Giaramita |
| **Filer Authorized By:** | Anthony C. Murabito |
| **Attorney Docket Number:** | TRAN-P470 |
| **Receipt Date:** | 19-OCT-2009 |
| **Filing Date:** | 21-AUG-2007 |
| **Time Stamp:** | 19:22:21 |
| **Application Type:** | Utility under 35 USC 111(a) |

## Payment information:

| | |
|---|---|
| Submitted with Payment | no |

## File Listing:

| Document Number | Document Description | File Name | File Size(Bytes)/ Message Digest | Multi Part /.zip | Pages (if appl.) |
|---|---|---|---|---|---|
| 1 | Information Disclosure Statement (IDS) Filed (SB/08) | TRAN-P059D2_IDS_PT_2.pdf | 608757<br>c8fdd508ca78b925d78fc4b4b6951494988d7f02 | no | 6 |
| **Warnings:** | | | | | |
| **Information:** | | | | | |
| 2 | Foreign Reference | EP0474963.pdf | 514852<br>87efbd690cc9bce3ec3907ce1ba9b8f0e52eff16 | no | 14 |
| **Warnings:** | | | | | |
| **Information:** | | | | | |
| 3 | Foreign Reference | EP0501655.pdf | 354333<br>f668f0de699d0beac2d613df18a53d3ed5d70009 | no | 7 |
| **Warnings:** | | | | | |
| **Information:** | | | | | |
| 4 | Foreign Reference | EP0632360.pdf | 571425<br>ce579729d1527839a95febe2193e1102793caa85 | no | 15 |
| **Warnings:** | | | | | |
| **Information:** | | | | | |
| 5 | Foreign Reference | EP0978781.pdf | 699539<br>76df739a505cd305ac613eb5bd08a56703793e66 | no | 14 |
| **Warnings:** | | | | | |
| **Information:** | | | | | |
| 6 | Foreign Reference | JP409185589.pdf | 422491<br>d9b30c3c1ce96df6c1a8a7ea76b0f8ceb0214f1f | no | 9 |
| **Warnings:** | | | | | |
| **Information:** | | | | | |
| 7 | Foreign Reference | WO0127728.pdf | 656134<br>d695001dc1521680d4e3df57f2797d2f20d45689 | no | 15 |
| **Warnings:** | | | | | |
| **Information:** | | | | | |
| | | **Total Files Size (in bytes):** | 3827531 | | |

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New Applications Under 35 U.S.C. 111

If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371

If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office

If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

Doc code: IDS
Doc description: Information Disclosure Statement (IDS) Filed

PTO/SB/08a (07-09)
Approved for use through 07/31/2012. OMB 0651-0031
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
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# INFORMATION DISCLOSURE STATEMENT BY APPLICANT

( Not for submission under 37 CFR 1.99)

| | |
|---|---|
| Application Number | 11894991 |
| Filing Date | 2007-08-21 |
| First Named Inventor | Andrew Read |
| Art Unit | 2115 |
| Examiner Name | Chun Cao |
| Attorney Docket Number | TRAN-P059D2 |

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OCT 21 2009
PATENT & TRADEMARK OFFICE

## U.S.PATENTS

| Examiner Initial* | Cite No | Patent Number | Kind Code[1] | Issue Date | Name of Patentee or Applicant of cited Document | Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear |
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## U.S.PATENT APPLICATION PUBLICATIONS

| Examiner Initial* | Cite No | Publication Number | Kind Code[1] | Publication Date | Name of Patentee or Applicant of cited Document | Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear |
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| Examiner Initial* | Cite No | Foreign Document Number[3] | Country Code[2] | Kind Code[4] | Publication Date | Name of Patentee or Applicant of cited Document | Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear | T[5] |
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| Examiner Initials* | Cite No | Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc), date, pages(s), volume-issue number(s), publisher, city and/or country where published. | T[5] |
|---|---|---|---|

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| INFORMATION DISCLOSURE STATEMENT BY APPLICANT ( Not for submission under 37 CFR 1.99) | | |
|---|---|---|
| | Application Number | 11894991 |
| | Filing Date | 2007-08-21 |
| | First Named Inventor | Andrew Read |
| | Art Unit | 2115 |
| | Examiner Name | Chun Cao |
| | Attorney Docket Number | TRAN-P059D2 |

| | | | |
|---|---|---|---|
| | 1 | INTEL CORPORATION; "INTEL 82801 CAM I/O CONTROLLER HUB (ICH3-M)" DATASHEET; JUL. 2001 | ☐ |

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**EXAMINER SIGNATURE**

| Examiner Signature | | Date Considered | |
|---|---|---|---|

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through a citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

[1] See Kind Codes of USPTO Patent Documents at www.USPTO.GOV or MPEP 901.04. [2] Enter office that issued the document, by the two-letter code (WIPO Standard ST.3). [3] For Japanese patent documents, the indication of the year of the reign of the Emperor must precede the serial number of the patent document. [4] Kind of document by the appropriate symbols as indicated on the document under WIPO Standard ST.16 if possible. [5] Applicant is to place a check mark here if English language translation is attached.

| INFORMATION DISCLOSURE STATEMENT BY APPLICANT ( Not for submission under 37 CFR 1.99) | | |
|---|---|---|
| | Application Number | 11894991 |
| | Filing Date | 2007-08-21 |
| | First Named Inventor | Andrew Read |
| | Art Unit | 2115 |
| | Examiner Name | Chun Cao |
| | Attorney Docket Number | TRAN-P059D2 |

**CERTIFICATION STATEMENT**

Please see 37 CFR 1.97 and 1.98 to make the appropriate selection(s):

☐ That each item of information contained in the information disclosure statement was first cited in any communication from a foreign patent office in a counterpart foreign application not more than three months prior to the filing of the information disclosure statement. See 37 CFR 1.97(e)(1).

**OR**

☐ That no item of information contained in the information disclosure statement was cited in a communication from a foreign patent office in a counterpart foreign application, and, to the knowledge of the person signing the certification after making reasonable inquiry, no item of information contained in the information disclosure statement was known to any individual designated in 37 CFR 1.56(c) more than three months prior to the filing of the information disclosure statement. See 37 CFR 1.97(e)(2).

☐ See attached certification statement.

☒ Fee set forth in 37 CFR 1.17 (p) has been submitted herewith.

☐ None

**SIGNATURE**

A signature of the applicant or representative is required in accordance with CFR 1.33, 10.18. Please see CFR 1.4(d) for the form of the signature.

| Signature | | Date (YYYY-MM-DD) | 2009-10-19 |
|---|---|---|---|
| Name/Print | Anthony C. Murabito | Registration Number | 35295 |

This collection of information is required by 37 CFR 1.97 and 1.98. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 1 hour to complete, including gathering, preparing and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

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United States Patent and Trademark Office
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www.uspto.gov

| APPLICATION NO. | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. | CONFIRMATION NO. |
|---|---|---|---|---|
| 11/894,991 | 08/21/2007 | Andrew Read | TRAN-P470 | 9781 |

7590 01/26/2010

MURABITO, HAO & BARNES LLP
Third Floor
Two North Market Street
San Jose, CA 95113

| EXAMINER | |
|---|---|
| CAO, CHUN | |
| ART UNIT | PAPER NUMBER |
| 2115 | |

| MAIL DATE | DELIVERY MODE |
|---|---|
| 01/26/2010 | PAPER |

**Please find below and/or attached an Office communication concerning this application or proceeding.**

The time period for reply, if any, is set in the attached communication.

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 11/894,991 | READ ET AL. | |
| | Examiner | Art Unit | |
| | Chun Cao | 2115 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *05 October 2009*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *1-24* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *1-10* is/are allowed.

6)☒ Claim(s) *11-18 and 20-23* is/are rejected.

7)☒ Claim(s) *19 and 24* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *10/19/09,10/21/09*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

## DETAILED ACTION

1. Claims 1-24 are presented for examination.

### *Claim Rejections - 35 USC § 112*

2. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

3. Claims 11-14 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the enablement requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention. There is no teaching in applicant's specification which suggests that a first operating voltage that, based on a rate of transitioning from said sleep voltage to said first operating voltage, is not achievable from said sleep voltage within an allowed time for transitioning from a sleep state to an operating state.

4. Claims 12-14 are rejected because they incorporate the deficiencies of claim 11.

### *Claim Rejections - 35 USC § 102*

5. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

The changes made to 35 U.S.C. 102(e) by the American Inventors Protection Act of 1999 (AIPA) and the Intellectual Property and High Technology Technical Amendments Act of 2002 do not apply when the reference is a U.S. patent resulting directly or indirectly from an international application filed before November 29, 2000. Therefore, the prior art date of the reference is determined under 35 U.S.C. 102(e) prior to the amendment by the AIPA (pre-AIPA 35 U.S.C. 102(e)).

6. Claims 11-18 and 20-23 are rejected under 35 U.S.C. 102(e) as being anticipated by Pole II et al. (Pole)[1], U.S. patent no. 6,675,304.

As per claim 11, Pole discloses a computer system [Fig. 1] comprising: a processor; an adjustable voltage supply configured to output to said processor: a sleep voltage [col. 1, lines 20-40]; and a first operating voltage that, based on a rate of transitioning from said sleep voltage to said first operating voltage, is not achievable from said sleep voltage within an allowed time for transitioning from a sleep state to an operating state [col. 1, lines 41-64].

As per claim 12, Pole discloses that adjustable voltage supply is further configured to output to said processor a second operating voltage that, based on a rate of transitioning from said sleep voltage to said second operating voltage, is achievable from said sleep voltage within said allowed time for transitioning from said sleep state to said operating state [col. 1, lines 41-64; col. 3, lines 31-38].

As per claim 13, Pole discloses that allowed time is based on a configuration of said computer system [col. 3, lines 31-67].

As per claim 14, Pole discloses that adjustable voltage supply comprises a voltage regulator [fig. 1; col. 3, lines 31-38].

As per claim 15, Pole discloses a computer system [fig. 1] comprising: a processing unit; circuitry coupled to the processing unit, said circuitry configured to provide to said processing unit [fig. 1; col. 2; lines 30-40]: a first sleep voltage and a second sleep voltage [col. 1, lines 20-40; "a plurality of low activity states such as C1, C2, C3"]; a first operating voltage when transitioning from said first sleep voltage; and a second operating voltage when transitioning from said second sleep voltage [col. 1, lines 41-56; col. 3, lines 31-67; col. 4, lines 2-24].

As per claim 16, Pole discloses that circuitry is further configured to provide to said processing unit: said first sleep voltage when transitioning from said first operating voltage; and said second sleep voltage when transitioning from said second operating voltage [col. 1, lines 41-56; col. 3, lines 31-67; col. 4, lines 2-24].

As per claim 17, Pole inherently discloses that a voltage difference between said first operating voltage and said first sleep voltage is approximately equal to a voltage difference between said second operating voltage and said second sleep voltage [col. 1, lines 41-56; col. 3, lines 31-67; col. 4, lines 2-24].

As per claim 18, Pole discloses that first operating voltage is greater than said second operating voltage and wherein said first sleep voltage is greater than said second sleep voltage [col. 1, lines 41-56; col. 3, lines 31-67; col. 4, lines 2-24].

---

[1] Pole is cited in prior office action.

As to claims 20-23 are written in mean plus function and contained the same limitations as claims 15-18. Therefore, same rejection is applied.

***Allowable Subject Matter***

7. Claims 19 and 24 objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

***Conclusion***

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Chun Cao whose telephone number is 571-272-3664. The examiner can normally be reached on Monday-Friday from 7:30 am-4:00 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Thomas C. Lee can be reached on 571-272-3667. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Any inquiry of a general nature or relating to the status of this application should be directed to the Group receptionist whose telephone number is 571-272-2100.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Jan. 20, 2010

/Chun Cao/

Primary Examiner, Art Unit 2115

PTO/SB/08a (07-09)
Approved for use through 07/31/2012. OMB 0651-0031
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE



| **INFORMATION DISCLOSURE STATEMENT BY APPLICANT** ( **Not for submission under 37 CFR 1.99)** | | |
|---|---|---|
| | Application Number | 11894991 |
| | Filing Date | 2007-08-21 |
| | First Named Inventor | Andrew Read |
| | Art Unit | 2115 |
| | Examiner Name | Chun Cao |
| | Attorney Docket Number | TRAN-P059D2 |

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| | Filing Date | 2007-08-21 |
| | First Named Inventor | Andrew Read |
| | Art Unit | 2115 |
| | Examiner Name | Chun Cao |
| | Attorney Docket Number | TRAN-P059D2 |

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| Examiner Signature | /Chun Cao/ | Date Considered | 01/11/2010 |
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| Index of Claims | Application/Control No. | Applicant(s)/Patent Under Reexamination |
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| | Examiner | Art Unit |
| | Chun Cao | 2115 |

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| = | Allowed | ÷ | Restricted | I | Interference | O | Objected |

☐ Claims renumbered in the same order as presented by applicant ☐ CPA ☐ T.D. ☐ R.1.47

| CLAIM | | DATE | | | | | | | | |
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| Final | Original | 06/30/2009 | 01/20/2010 | | | | | | | |
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| | Examiner Name | Chun Cao |
| | Attorney Docket Number | TRAN-P059D2 |

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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of: Read et al.

| | | | |
|---|---|---|---|
| Serial: | 11/894,991 | Group Art Unit: | 2115 |
| Filed: | August 21, 2007 | Examiner: | Chun Cao |

For: SAVING POWER WHEN IN OR TRANSITIONING TO A STATIC MODE OF A PROCESSOR (as filed)

RESPONSE

Honorable Commissioner for Patents
PO Box 1450
Alexandria, VA 22313-1450

Dear Sir:

In response to the Office Action mailed January 26, 2010 in the above captioned Patent Application, Applicants respectfully request the Examiner to consider the following remarks.

REMARKS

Claims 1-24 are pending in the present application. Applicants respectfully request reconsideration of the present application in view of the following remarks.

Allowable Matter

The Official Action indicates that Claims 1 – 10 are allowed.

The Official Action indicates that Claims 19 and 24 would be allowable if rewritten in independent form including all of the recitations of the base claim and any intervening claims.

Applicants thank the Examiner for indicating allowable material.

35 U.S.C. § 112

Claims 11-14 are rejected under 35 U.S.C. § 112, first paragraph, as failing to comply with the enablement requirement. The rejection alleges that the claimed limitations of "a first operating voltage that, based on a rate of transitioning from said sleep voltage to said first operating voltage, is not achievable from said sleep voltage within an allowed time for transitioning from a sleep state to an operating state" are not supported. Applicants respectfully traverse.

At page 9 line 21 *et seq*., the present application discloses that certain time intervals are "allowed for transition to and from the deep sleep mode." An exemplary time allowance is given for transitions "to and from deep sleep."

At page 10, line 18 *et seq*., the present application discloses, "if the exemplary processor is operating at its lowest processing core voltage of 1.2 volts (e.g., a second operating voltage), its core voltage may be lowered in the time available to 0.6-0.7 volts." However, a similar time interval may be used for a transition from a voltage of 0.9-.01 volts to a first operating voltage of 1.5 volts. Accordingly, the present application teaches that a transition from the range of 0.6-0.7 volts to a first operating voltage of 1.5 volts, e.g., a first transition time, is greater than the allowed time, which allows for a transition from 0.6-0.7 to 1.2 volts but not beyond that voltage. If the first transition time is greater than the allowed time, as disclosed, then a transition within the allowed time is disclosed as <u>not</u> <u>achievable</u>.

While the examples cited present exemplary voltages and duration, the cited passages, as well as the application as a whole, provide ample enabling support for the Claims. Accordingly, Applicants respectfully solicit withdrawal of the 35 U.S.C. § 112, first paragraph, rejections.

35 U.S.C. § 102

Claims 11-18 and 20-23 stand rejected under 35 USC § 102(e) as being allegedly unpatentable over Pole II et al., (US 6,675,304, "Pole"). Applicants do not concede that the cited art is in fact prior art, and reserve the right to antedate the reference. Applicants respectfully assert that embodiments in accordance with the present invention as recited in Claims 11-18 and 20-23 are patentable over Pole for the following reasons.

With respect to independent Claim 11, Applicants respectfully assert that Pole fails to teach or suggest the claimed recitations of "a first operating voltage that, based on a rate of transitioning from said sleep voltage to said first operating voltage, is not achievable from said sleep voltage within an allowed time for transitioning from a sleep state to an operating state" as recited by Claim 11.

Applicants respectfully assert that Pole is silent as to a transition from "sleep" to a "first operating voltage is not achievable… within an allowed time." The rejection cites to column 1 lines 41-64 as allegedly suggesting these claimed recitations. Applicants respectfully traverse. The cited passage teaches a "transition() from a higher to a lower voltage" (emphasis added). Thus, this cited passage deals with a transition in the opposite direction, e.g., "from a higher to a lower voltage" than the claimed recitations, e.g., "from said sleep voltage to said first operating voltage." As the cited passage is not related to the claimed

recitations, this cited passage, as well as the whole of the reference, fails to teach or suggest the instant claimed recitations.

For this reason, Applicants respectfully assert that Claim 11 overcomes the rejections of record, and respectfully solicit allowance of these Claims.

Moreover, the cited passage fails to teach that the transition is "not achievable," as recited. Applicants respectfully assert that Pole's teaching of a "need to improve the latency of voltage regulator output level transitions" fails to teach or suggest that the transition is "not achievable… within an allowed time" as recited by Claim 11.

For this additional reason, Applicants respectfully assert that Claim 11 overcomes the rejections of record, and respectfully solicit allowance of these Claims.

Applicants respectfully assert that Claims 12-14 overcome the rejections of record at least by virtue of their dependence from Claim 11, and respectfully solicit allowance of these Claims.

With respect to independent Claim 15, Applicants respectfully assert that Pole fails to teach or suggest the claimed recitations of first and second "sleep voltage(s)" as recited by Claim 15. The rejection alleges that Pole's teaching of "a

plurality of low activity states such as the C1, C2 or C3 states" suggests these instant claimed recitations. Applicants respectfully traverse.

Applicants respectfully assert that the taught "states" do not teach or suggest different "sleep voltages" as recited. Moreover, Pole only teaches than one of these states may be a sleep state, "[i]n the deep sleep state, which may be the C3 state." In state C2, "processor performs minimal activity." Accordingly, the C2 state is not taught to be a sleep state. Thus, even if, *arguendo*, such states correspond to different voltage levels, Pole's teaching of only one sleep state fails to teach or suggest the instant claimed recitations of two sleep voltages.

For this reason, Applicants respectfully assert that Claim 15 overcomes the rejections of record, and respectfully solicit allowance of these Claims.

In addition with respect to independent Claim 15, Applicants respectfully assert that Pole fails to teach or suggest the claimed recitations of "a first operating voltage when transitioning from said first sleep voltage; and a second operating voltage when transitioning from said second sleep voltage" as recited by Claim 15.

As Pole is silent as to first and second sleep voltages, Pole is further silent about first and second operating voltages based on transitions from the untaught first and second sleep voltages.

For this additional reason, Applicants respectfully assert that Claim 15 overcomes the rejections of record, and respectfully solicit allowance of these Claims.

Moreover, Pole teaches "[a] signal VRHI/LO# is provided by the control logic 100 to the voltage regulator 52 to adjust the voltage levels supplied by the voltage regulator 52" (column 3 line 42 *et seq.*). Elsewhere, Pole teaches,

> the voltage regulator 52 settles to an output selected by VRHI/LO# (a low level or high level). By way of example, a low voltage level may be 1.3 volts while a high voltage level may be about 1.8 volts." (column 4, lines 1-7).

As is known by those of skill in the art such a single signal is capable of only two states. Accordingly, Pole teaches a system limited to two voltages, the taught "low" and "high" voltages.

Pole teaches that the low voltage corresponds to deep sleep, and the high voltage corresponds to other operational states. Accordingly, Pole fails to teach first and second sleep voltages as well as failing to teach first and second operational voltages, as recited by Claim 15.

For this further reason, Applicants respectfully assert that Claim 15 overcomes the rejections of record, and respectfully solicit allowance of these Claims.

Applicants respectfully assert that Claims 16-19, including the presently rejected Claims 16-18 overcome the rejections of record at least by virtue of their dependence from Claim 15, and respectfully solicit allowance of these Claims.

With respect to independent Claim 20, Applicants respectfully assert that Claim 20 overcome the rejections of record for at least the rationale previously presented with respect to Claim 15, and respectfully solicit allowance of this Claim.

Applicants respectfully assert that Claims 21-24, including the presently rejected Claims 21-23 overcome the rejections of record at least by virtue of their dependence from Claim 15, and respectfully solicit allowance of these Claims.

## CONCLUSION

Claims 1-24 are pending in the present application. Applicants respectfully request reconsideration of the present application in view of the amendments and remarks presented herein.

The Examiner is invited to contact Applicants' undersigned representative if the Examiner believes such action would expedite resolution of the present Application.

Please charge any additional fees or apply any credits to our PTO deposit account number: 504160.

Respectfully submitted,

MURABITO, HAO & BARNES LLP

Date: April 19, 2010

/Anthony C. Murabito/
Anthony C. Murabito
Reg. No. 35,295

Two North Market Street
Third Floor
San Jose, California 95113
(408) 938-9060

| Electronic Acknowledgement Receipt | |
|---|---|
| **EFS ID:** | 7444275 |
| **Application Number:** | 11894991 |
| **International Application Number:** | |
| **Confirmation Number:** | 9781 |
| **Title of Invention:** | Saving power when in or transitioning to a static mode of a processor |
| **First Named Inventor/Applicant Name:** | Andrew Read |
| **Correspondence Address:** | MURABITO, HAO & BARNES LLP<br>-<br>Third Floor<br>Two North Market Street<br>San Jose CA 95113<br>US 4089389060<br>- |
| **Filer:** | Anthony C. Murabito/Tatiana Carvalho |
| **Filer Authorized By:** | Anthony C. Murabito |
| **Attorney Docket Number:** | TRAN-P470 |
| **Receipt Date:** | 19-APR-2010 |
| **Filing Date:** | 21-AUG-2007 |
| **Time Stamp:** | 18:53:00 |
| **Application Type:** | Utility under 35 USC 111(a) |

## Payment information:

| | |
|---|---|
| Submitted with Payment | no |

## File Listing:

| Document Number | Document Description | File Name | File Size(Bytes)/ Message Digest | Multi Part /.zip | Pages (if appl.) |
|---|---|---|---|---|---|
| 1 | | TRAN-P059D2_AMDT_04-19-2010.pdf | 50005<br>14042236a1e776421a7419e2f991bfbb7e422925 | yes | 9 |

| | Multipart Description/PDF files in .zip description | | |
|---|---|---|---|
| | **Document Description** | **Start** | **End** |
| | Amendment/Req. Reconsideration-After Non-Final Reject | 1 | 1 |
| | Applicant Arguments/Remarks Made in an Amendment | 2 | 9 |

| | |
|---|---|
| **Warnings:** | |
| **Information:** | |
| **Total Files Size (in bytes):** | 50005 |

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**New Applications Under 35 U.S.C. 111**
**If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.**

**National Stage of an International Application under 35 U.S.C. 371**
**If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.**

**New International Application Filed with the USPTO as a Receiving Office**
**If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.**

PTO/SB/06 (07-06)
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| **PATENT APPLICATION FEE DETERMINATION RECORD**<br>Substitute for Form PTO-875 | Application or Docket Number<br>11/894,991 | Filing Date<br>08/21/2007 | ☐ To be Mailed |
|---|---|---|---|

## APPLICATION AS FILED – PART I

| | (Column 1) | (Column 2) | SMALL ENTITY ☐ | | OR | OTHER THAN SMALL ENTITY | |
|---|---|---|---|---|---|---|---|
| FOR | NUMBER FILED | NUMBER EXTRA | RATE ($) | FEE ($) | | RATE ($) | FEE ($) |
| ☐ BASIC FEE (37 CFR 1.16(a), (b), or (c)) | N/A | N/A | N/A | | | N/A | |
| ☐ SEARCH FEE (37 CFR 1.16(k), (i), or (m)) | N/A | N/A | N/A | | | N/A | |
| ☐ EXAMINATION FEE (37 CFR 1.16(o), (p), or (q)) | N/A | N/A | N/A | | | N/A | |
| TOTAL CLAIMS (37 CFR 1.16(i)) | minus 20 = | * | X $ = | | OR | X $ = | |
| INDEPENDENT CLAIMS (37 CFR 1.16(h)) | minus 3 = | * | X $ = | | | X $ = | |
| ☐ APPLICATION SIZE FEE (37 CFR 1.16(s)) | If the specification and drawings exceed 100 sheets of paper, the application size fee due is $250 ($125 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s). | | | | | | |
| ☐ MULTIPLE DEPENDENT CLAIM PRESENT (37 CFR 1.16(j)) | | | | | | | |
| * If the difference in column 1 is less than zero, enter "0" in column 2. | | | TOTAL | | | TOTAL | |

## APPLICATION AS AMENDED – PART II

| | | (Column 1) | | (Column 2) | (Column 3) | SMALL ENTITY | | OR | OTHER THAN SMALL ENTITY | |
|---|---|---|---|---|---|---|---|---|---|---|
| AMENDMENT | **04/19/2010** | CLAIMS REMAINING AFTER AMENDMENT | | HIGHEST NUMBER PREVIOUSLY PAID FOR | PRESENT EXTRA | RATE ($) | ADDITIONAL FEE ($) | | RATE ($) | ADDITIONAL FEE ($) |
| | Total (37 CFR 1.16(i)) | * 25 | Minus | ** 25 | = 0 | X $ = | | OR | X $52= | 0 |
| | Independent (37 CFR 1.16(h)) | * 5 | Minus | ***5 | = 0 | X $ = | | OR | X $220= | 0 |
| | ☐ Application Size Fee (37 CFR 1.16(s)) | | | | | | | | | |
| | ☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j)) | | | | | | | OR | | |
| | | | | | | TOTAL ADD'L FEE | | OR | TOTAL ADD'L FEE | 0 |

| | | (Column 1) | | (Column 2) | (Column 3) | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|
| AMENDMENT | | CLAIMS REMAINING AFTER AMENDMENT | | HIGHEST NUMBER PREVIOUSLY PAID FOR | PRESENT EXTRA | RATE ($) | ADDITIONAL FEE ($) | | RATE ($) | ADDITIONAL FEE ($) |
| | Total (37 CFR 1.16(i)) | * | Minus | ** | = | X $ = | | OR | X $ = | |
| | Independent (37 CFR 1.16(h)) | * | Minus | *** | = | X $ = | | OR | X $ = | |
| | ☐ Application Size Fee (37 CFR 1.16(s)) | | | | | | | | | |
| | ☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j)) | | | | | | | OR | | |
| | | | | | | TOTAL ADD'L FEE | | OR | TOTAL ADD'L FEE | |

* If the entry in column 1 is less than the entry in column 2, write "0" in column 3.
** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20".
*** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3".
The "Highest Number Previously Paid For" (Total or Independent) is the highest number found in the appropriate box in column 1.

Legal Instrument Examiner:
/SONYA HILLIARD/

This collection of information is required by 37 CFR 1.16. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

*If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.*

PTO/SB/06 (07-06)
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U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
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| **PATENT APPLICATION FEE DETERMINATION RECORD**<br>Substitute for Form PTO-875 | Application or Docket Number<br>11/894,991 | Filing Date<br>08/21/2007 | ☐ To be Mailed |
|---|---|---|---|

## APPLICATION AS FILED – PART I

| | (Column 1) | (Column 2) | SMALL ENTITY ☐ | | OR | OTHER THAN SMALL ENTITY | |
|---|---|---|---|---|---|---|---|
| FOR | NUMBER FILED | NUMBER EXTRA | RATE ($) | FEE ($) | | RATE ($) | FEE ($) |
| ☐ BASIC FEE (37 CFR 1.16(a), (b), or (c)) | N/A | N/A | N/A | | | N/A | |
| ☐ SEARCH FEE (37 CFR 1.16(k), (i), or (m)) | N/A | N/A | N/A | | | N/A | |
| ☐ EXAMINATION FEE (37 CFR 1.16(o), (p), or (q)) | N/A | N/A | N/A | | | N/A | |
| TOTAL CLAIMS (37 CFR 1.16(i)) | minus 20 = | * | X $ = | | OR | X $ = | |
| INDEPENDENT CLAIMS (37 CFR 1.16(h)) | minus 3 = | * | X $ = | | | X $ = | |
| ☐ APPLICATION SIZE FEE (37 CFR 1.16(s)) | If the specification and drawings exceed 100 sheets of paper, the application size fee due is $250 ($125 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s). | | | | | | |
| ☐ MULTIPLE DEPENDENT CLAIM PRESENT (37 CFR 1.16(j)) | | | | | | | |
| * If the difference in column 1 is less than zero, enter "0" in column 2. | | | TOTAL | | | TOTAL | |

## APPLICATION AS AMENDED – PART II

| | | (Column 1) | | (Column 2) | (Column 3) | SMALL ENTITY | | OR | OTHER THAN SMALL ENTITY | |
|---|---|---|---|---|---|---|---|---|---|---|
| AMENDMENT | **04/19/2010** | CLAIMS REMAINING AFTER AMENDMENT | | HIGHEST NUMBER PREVIOUSLY PAID FOR | PRESENT EXTRA | RATE ($) | ADDITIONAL FEE ($) | | RATE ($) | ADDITIONAL FEE ($) |
| | Total (37 CFR 1.16(i)) | * 25 | Minus | ** 25 | = 0 | X $ = | | OR | X $52= | 0 |
| | Independent (37 CFR 1.16(h)) | * 5 | Minus | ***5 | = 0 | X $ = | | OR | X $220= | 0 |
| | ☐ Application Size Fee (37 CFR 1.16(s)) | | | | | | | | | |
| | ☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j)) | | | | | | | OR | | |
| | | | | | | TOTAL ADD'L FEE | | OR | TOTAL ADD'L FEE | **0** |

| | | (Column 1) | | (Column 2) | (Column 3) | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|
| AMENDMENT | | CLAIMS REMAINING AFTER AMENDMENT | | HIGHEST NUMBER PREVIOUSLY PAID FOR | PRESENT EXTRA | RATE ($) | ADDITIONAL FEE ($) | | RATE ($) | ADDITIONAL FEE ($) |
| | Total (37 CFR 1.16(i)) | * | Minus | ** | = | X $ = | | OR | X $ = | |
| | Independent (37 CFR 1.16(h)) | * | Minus | *** | = | X $ = | | OR | X $ = | |
| | ☐ Application Size Fee (37 CFR 1.16(s)) | | | | | | | | | |
| | ☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j)) | | | | | | | OR | | |
| | | | | | | TOTAL ADD'L FEE | | OR | TOTAL ADD'L FEE | |

* If the entry in column 1 is less than the entry in column 2, write "0" in column 3.

** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20".

*** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3".

The "Highest Number Previously Paid For" (Total or Independent) is the highest number found in the appropriate box in column 1.

Legal Instrument Examiner:
/SONYA HILLIARD/

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| APPLICATION NO. | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. | CONFIRMATION NO. |
|---|---|---|---|---|
| 11/894,991 | 08/21/2007 | Andrew Read | TRAN-P470 | 9781 |

7590 06/25/2010

MURABITO, HAO & BARNES LLP
Third Floor
Two North Market Street
San Jose, CA 95113

| EXAMINER | |
|---|---|
| CAO, CHUN | |
| ART UNIT | PAPER NUMBER |
| 2115 | |

| MAIL DATE | DELIVERY MODE |
|---|---|
| 06/25/2010 | PAPER |

**Please find below and/or attached an Office communication concerning this application or proceeding.**

The time period for reply, if any, is set in the attached communication.

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 11/894,991 | READ ET AL. | |
| | Examiner | Art Unit | |
| | Chun Cao | 2115 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *19 April 2010*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *1-24* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *1-10* is/are allowed.

6)☒ Claim(s) *11-18 and 20-23* is/are rejected.

7)☒ Claim(s) *19 and 24* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

**FINAL REJECTION**

1. Claims 1-24 are presented for examination.

2. The rejections are respectfully maintained and incorporated by reference as set forth in the last office action.

3. Claims 11-14 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the enablement requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention. There is no teaching in applicant's specification which suggests that a first operating voltage that, based on a rate of transitioning from said sleep voltage to said first operating voltage, is not achievable from said sleep voltage within an allowed time for transitioning from a sleep state to an operating state.

4. Claims 12-14 are rejected because they incorporate the deficiencies of claim 11.

5. Claims 15-18 and 20-23 are rejected under 35 U.S.C. 102(e) as being anticipated by Pole II et al. (Pole)[1], U.S. patent no. 6,675,304.

As per claim 15, Pole discloses a computer system [fig. 1] comprising: a processing unit; circuitry coupled to the processing unit, said circuitry configured to provide to said processing unit [fig. 1; col. 2; lines 30-40]: a first sleep voltage and a second sleep voltage [col. 1, lines 20-40; "a plurality of low activity states such as C1, C2, C3"]; a first operating voltage when transitioning from said first sleep voltage; and a

[1] Pole is cited in prior office action.

second operating voltage when transitioning from said second sleep voltage [col. 1, lines 41-56; col. 3, lines 31-67; col. 4, lines 2-24].

As per claim 16, Pole discloses that circuitry is further configured to provide to said processing unit: said first sleep voltage when transitioning from said first operating voltage; and said second sleep voltage when transitioning from said second operating voltage [col. 1, lines 41-56; col. 3, lines 31-67; col. 4, lines 2-24].

As per claim 17, Pole inherently discloses that a voltage difference between said first operating voltage and said first sleep voltage is approximately equal to a voltage difference between said second operating voltage and said second sleep voltage [col. 1, lines 41-56; col. 3, lines 31-67; col. 4, lines 2-24].

As per claim 18, Pole discloses that first operating voltage is greater than said second operating voltage and wherein said first sleep voltage is greater than said second sleep voltage [col. 1, lines 41-56; col. 3, lines 31-67; col. 4, lines 2-24].

As to claims 20-23 are written in mean plus function and contained the same limitations as claims 15-18. Therefore, same rejection is applied.

***Allowable Subject Matter***

6. Claims 19 and 24 objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

7. Applicant's arguments filed 4/19/2010 have been fully considered but are not persuasive.

8. In the remarks, 1) applicant respectively traverses 35 U.S.C. 112 1st paragraph rejection in claim 11; 2) applicant argued in substance that Pole does not disclose that a first sleep voltage and a second sleep voltage; a first operating voltage and a second operating voltage.

9. The examiner respectfully traverses. As to 1) applicant pointed out in the specification, page 9, line 21 et seq. ; page 10, line 18 et seq. In summary, the cited specification teaches of the processor operates in different core voltage values at different states. There is no specific language to support the limitations cited in claim 1, such as "…based on a rate of transitioning from said sleep voltage to said first operating voltage, is not achievable from said sleep voltage within an allowed time for transitioning from a sleep state to an operating state". Therefore, the rejection of claim 11 is maintained.

As to 2), Pole discloses a first sleep voltage and a second sleep voltage [col. 1, lines 20-40; "a plurality of low activity states such as C1, C2, C3"]; a first operating voltage when transitioning from said first sleep voltage; and a second operating voltage when transitioning from said second sleep voltage [col. 1, lines 41-56; col. 3, lines 31-67; col. 4, lines 2-24]. In summary, Pole teaches a processor operates under the ACPI specification (C1-C5) states, therefore, the supply voltage of the processor should have different values under C1-C5 states respectively.

Also see rejection above.

10. **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

**Conclusion**

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Chun Cao whose telephone number is 571-272-3664. The examiner can normally be reached on Monday-Friday from 7:30 am-4:00 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Thomas C. Lee can be reached on 571-272-3667. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Any inquiry of a general nature or relating to the status of this application should be directed to the Group receptionist whose telephone number is 571-272-2100.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

June 23, 2010

/Chun Cao/

Primary Examiner, Art Unit 2115

| Index of Claims | Application/Control No. | Applicant(s)/Patent Under Reexamination |
|---|---|---|
| | 11894991 | READ ET AL. |
| | Examiner | Art Unit |
| | Chun Cao | 2115 |

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| ✓ | Rejected | - | Cancelled | N | Non-Elected | A | Appeal |
| = | Allowed | ÷ | Restricted | I | Interference | O | Objected |

☐ Claims renumbered in the same order as presented by applicant ☐ CPA ☐ T.D. ☐ R.1.47

| CLAIM | | DATE | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|
| Final | Original | 06/30/2009 | 01/20/2010 | 06/23/2010 | | | | | | |
| | 1 | ✓ | = | = | | | | | | |
| | 2 | ✓ | = | = | | | | | | |
| | 3 | ✓ | = | = | | | | | | |
| | 4 | ✓ | = | = | | | | | | |
| | 5 | ✓ | = | = | | | | | | |
| | 6 | ✓ | = | = | | | | | | |
| | 7 | ✓ | = | = | | | | | | |
| | 8 | ✓ | = | = | | | | | | |
| | 9 | ✓ | = | = | | | | | | |
| | 10 | ✓ | = | = | | | | | | |
| | 11 | ✓ | ✓ | ✓ | | | | | | |
| | 12 | ✓ | ✓ | ✓ | | | | | | |
| | 13 | ✓ | ✓ | ✓ | | | | | | |
| | 14 | ✓ | ✓ | ✓ | | | | | | |
| | 15 | ✓ | ✓ | ✓ | | | | | | |
| | 16 | ✓ | ✓ | ✓ | | | | | | |
| | 17 | ✓ | ✓ | ✓ | | | | | | |
| | 18 | ✓ | ✓ | ✓ | | | | | | |
| | 19 | ✓ | O | O | | | | | | |
| | 20 | | ✓ | ✓ | | | | | | |
| | 21 | | ✓ | ✓ | | | | | | |
| | 22 | | ✓ | ✓ | | | | | | |
| | 23 | | ✓ | ✓ | | | | | | |
| | 24 | | O | O | | | | | | |

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of: Read et al.

| | | | |
|---|---|---|---|
| Serial: | 11/894,991 | Group Art Unit: | 2115 |
| Filed: | August 21, 2007 | Examiner: | Chun Cao |
| For: | SAVING POWER WHEN IN OR TRANSITIONING TO A STATIC MODE OF A PROCESSOR (as filed) | | |

AMENDMENT and RESPONSE

Honorable Commissioner for Patents
PO Box 1450
Alexandria, VA 22313-1450

Dear Sir:

In response to the Office Action mailed June 25, 2010 in the above captioned Patent Application, Applicants respectfully request the Examiner to enter the following amendments and to consider the following remarks.

## REMARKS

Claims 1-17 and 20-23 are pending in the present application. Claims 11, 15 and 20 are amended. Claims 18, 19 and 24 are cancelled. No new matter is added. Applicants respectfully request reconsideration of the present application in view of the amendments presented herein and the following remarks.

### Allowable Matter

The Official Action indicates that Claims 1-10 are allowed.

The Official Action indicates that Claims 19 and 24 would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Applicants thank the Examiner for indicating allowable material.

### 35 U.S.C. § 112

Claims 11-14 are rejected under 35 U.S.C. § 112, first paragraph, as failing to comply with the enablement requirement.

Applicants respectfully assert that the amendments presented herein to independent Claim 11 overcome this 35 U.S.C. § 112, first paragraph, rejection.

Amendments

Independent Claim 15 is amended to incorporate the indicated allowed material from Claim 19 and Claim 18 (prior Claim 19 depended from Claim 18). Accordingly, Claim 15, and Claims 16-17, which depend therefrom, are allowable.

Independent Claim 20 is amended to incorporate the indicated allowed material from Claim 24. Accordingly, Claim 20, and Claims 21-23, which depend therefrom, are allowable.

Independent Claim 11 is amended to mirror Claim 20, as apparatus, and incorporates the indicated allowed material from Claim 24. Accordingly, Claim 11 and Claims 12-14, which depend therefrom, are allowable.

## CONCLUSION

Claims 1-17 and 20-23 are pending in the present application. Applicants believe that all remaining Claims are in condition for allowance, and such allowance is earnestly solicited.

The Examiner is invited to contact Applicants' undersigned representative if the Examiner believes such action would expedite resolution of the present Application.

Please charge any additional fees or apply any credits to our PTO deposit account number: 504160.

Respectfully submitted,

MURABITO, HAO & BARNES LLP

Date: August 25, 2010

/Anthony C. Murabito/
Anthony C. Murabito
Reg. No. 35,295

Two North Market Street
Third Floor
San Jose, California 95113
(408) 938-9060

| Electronic Acknowledgement Receipt | |
|---|---|
| **EFS ID:** | 8294030 |
| **Application Number:** | 11894991 |
| **International Application Number:** | |
| **Confirmation Number:** | 9781 |
| **Title of Invention:** | Saving power when in or transitioning to a static mode of a processor |
| **First Named Inventor/Applicant Name:** | Andrew Read |
| **Correspondence Address:** | MURABITO, HAO & BARNES LLP<br>-<br>Third Floor<br>Two North Market Street<br>San Jose CA 95113<br>US 4089389060<br>- |
| **Filer:** | Anthony C. Murabito/Tatiana Carvalho |
| **Filer Authorized By:** | Anthony C. Murabito |
| **Attorney Docket Number:** | TRAN-P470 |
| **Receipt Date:** | 25-AUG-2010 |
| **Filing Date:** | 21-AUG-2007 |
| **Time Stamp:** | 20:36:44 |
| **Application Type:** | Utility under 35 USC 111(a) |

## Payment information:

| | |
|---|---|
| Submitted with Payment | no |

## File Listing:

| Document Number | Document Description | File Name | File Size(Bytes)/ Message Digest | Multi Part /.zip | Pages (if appl.) |
|---|---|---|---|---|---|
| 1 | | TRAN-P059D2_AMDTafterFinal_08-25-2010.pdf | 49836<br>2e165c44326a4dc5c4fd7842ae7f181da9ca7117 | yes | 11 |

| Multipart Description/PDF files in .zip description | | |
|---|---|---|
| **Document Description** | **Start** | **End** |
| Amendment After Final | 1 | 1 |
| Claims | 2 | 8 |
| Applicant Arguments/Remarks Made in an Amendment | 9 | 11 |

| | |
|---|---|
| **Warnings:** | |
| **Information:** | |
| **Total Files Size (in bytes):** | 49836 |

**This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.**

**New Applications Under 35 U.S.C. 111**
**If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.**

**National Stage of an International Application under 35 U.S.C. 371**
**If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.**

**New International Application Filed with the USPTO as a Receiving Office**
**If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.**

PTO/SB/06 (07-06)
Approved for use through 1/31/2007. OMB 0651-0032
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

| **PATENT APPLICATION FEE DETERMINATION RECORD**<br>Substitute for Form PTO-875 | Application or Docket Number<br>11/894,991 | Filing Date<br>08/21/2007 | ☐ To be Mailed |
|---|---|---|---|

## APPLICATION AS FILED – PART I

| | (Column 1) | (Column 2) | SMALL ENTITY ☐ | | OR | OTHER THAN SMALL ENTITY | |
|---|---|---|---|---|---|---|---|
| FOR | NUMBER FILED | NUMBER EXTRA | RATE ($) | FEE ($) | | RATE ($) | FEE ($) |
| ☐ BASIC FEE (37 CFR 1.16(a), (b), or (c)) | N/A | N/A | N/A | | | N/A | |
| ☐ SEARCH FEE (37 CFR 1.16(k), (i), or (m)) | N/A | N/A | N/A | | | N/A | |
| ☐ EXAMINATION FEE (37 CFR 1.16(o), (p), or (q)) | N/A | N/A | N/A | | | N/A | |
| TOTAL CLAIMS (37 CFR 1.16(i)) | minus 20 = | * | X $ = | | OR | X $ = | |
| INDEPENDENT CLAIMS (37 CFR 1.16(h)) | minus 3 = | * | X $ = | | | X $ = | |
| ☐ APPLICATION SIZE FEE (37 CFR 1.16(s)) | If the specification and drawings exceed 100 sheets of paper, the application size fee due is $250 ($125 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s). | | | | | | |
| ☐ MULTIPLE DEPENDENT CLAIM PRESENT (37 CFR 1.16(j)) | | | | | | | |
| * If the difference in column 1 is less than zero, enter "0" in column 2. | | | TOTAL | | | TOTAL | |

## APPLICATION AS AMENDED – PART II

| AMENDMENT | 08/25/2010 | (Column 1) CLAIMS REMAINING AFTER AMENDMENT | | (Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR | (Column 3) PRESENT EXTRA | SMALL ENTITY RATE ($) | ADDITIONAL FEE ($) | OR | OTHER THAN SMALL ENTITY RATE ($) | ADDITIONAL FEE ($) |
|---|---|---|---|---|---|---|---|---|---|---|
| | Total (37 CFR 1.16(i)) | * 21 | Minus | ** 25 | = 0 | X $ = | | OR | X $52= | 0 |
| | Independent (37 CFR 1.16(h)) | * 5 | Minus | ***5 | = 0 | X $ = | | OR | X $220= | 0 |
| | ☐ Application Size Fee (37 CFR 1.16(s)) | | | | | | | | | |
| | ☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j)) | | | | | | | OR | | |
| | | | | | | TOTAL ADD'L FEE | | OR | TOTAL ADD'L FEE | 0 |

| AMENDMENT | | (Column 1) CLAIMS REMAINING AFTER AMENDMENT | | (Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR | (Column 3) PRESENT EXTRA | RATE ($) | ADDITIONAL FEE ($) | | RATE ($) | ADDITIONAL FEE ($) |
|---|---|---|---|---|---|---|---|---|---|---|
| | Total (37 CFR 1.16(i)) | * | Minus | ** | = | X $ = | | OR | X $ = | |
| | Independent (37 CFR 1.16(h)) | * | Minus | *** | = | X $ = | | OR | X $ = | |
| | ☐ Application Size Fee (37 CFR 1.16(s)) | | | | | | | | | |
| | ☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j)) | | | | | | | OR | | |
| | | | | | | TOTAL ADD'L FEE | | OR | TOTAL ADD'L FEE | |

* If the entry in column 1 is less than the entry in column 2, write "0" in column 3.
** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20".
*** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3".
The "Highest Number Previously Paid For" (Total or Independent) is the highest number found in the appropriate box in column 1.

Legal Instrument Examiner:
/Debra R. Wyatt/

This collection of information is required by 37 CFR 1.16. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

*If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.*

In the Claims:

1. (previously presented) A computer system comprising:

a processing unit;

circuitry coupled to the processing unit, said circuitry configured to provide to said processing unit:

a sleep voltage;

a first operating voltage; and

a second operating voltage that is less than the first operating voltage;

wherein said computer system has a first transition time for transitioning from said sleep voltage to said first operating voltage;

wherein said computer system has a second transition time for transitioning from said sleep voltage to said second operating voltage;

wherein said second transition time is within an allowed time for transitioning from a sleep state to an operating state; and

wherein said first transition time is greater than said allowed time.

2. (original) A computer system as recited in Claim 1 wherein said allowed time is based on a configuration of said computer system.

3. (original) A computer system as recited in Claim 1 wherein said allowed time is based on timing requirements of said computer system.

4. (original) A computer system as recited in Claim 3, wherein said timing requirements are based on interrupt response times.

5. (original) A computer system as recited in Claim 1 wherein said first and second transition times are based on respective first and second voltage ramp times.

6. (original) A computer system as recited in Claim 1 wherein said sleep voltage is sufficient to maintain state of said processing unit but is not sufficient to maintain processing activity in said processing unit.

7. (original) A method of operating a computer processor, said method comprising:

transitioning from providing a sleep voltage to said computer processor to providing a first operating voltage to said computer processor within an allowed time for transitioning from a sleep state to an operating state; and

transitioning from said providing said first operating voltage to said computer processor to providing a second operating voltage to said computer processor, wherein a transition time for changing from said sleep voltage directly to said second operating voltage is greater than said allowed time for transitioning from said sleep state to said operating state.

8. (original) A method in accordance with Claim 7 wherein said second operating voltage is greater than said first operating voltage.

9. (original) A method in accordance with Claim 7 further comprising:

enabling a system clock to said computer processor when providing said first operating voltage to said computer processor; and

disabling said system clock to said computer processor when providing said sleep voltage to said computer processor.

10. (original)A method in accordance with Claim 7, wherein said sleep voltage is sufficient to maintain state of said computer processor but is not sufficient to maintain processing activity in said computer processor.

11. (currently amended) A computer system comprising:

a processor;

an adjustable voltage supply configured to output to said processor:

a first and a second sleep voltage; ~~and~~

a first operating voltage ~~that, based on a rate of transitioning from said sleep voltage to said first operating voltage, is not achievable from said sleep voltage within an allowed time for transitioning from a sleep state to an operating state~~ responsive to a transition from said first sleep voltage; and

a second operating voltage responsive to a transition from said second sleep voltage.

wherein said adjustable voltage supply is configured to generate a voltage transition from said second sleep voltage to said first operating

voltage in a time period greater than a time period allowed for transition from a sleep state to an operating state of said computer system.

12. (original) A computer system as recited in Claim 11, wherein said adjustable voltage supply is further configured to output to said processor a second operating voltage that, based on a rate of transitioning from said sleep voltage to said second operating voltage, is achievable from said sleep voltage within said allowed time for transitioning from said sleep state to said operating state.

13. (original) A computer system as recited in Claim 11 wherein said allowed time is based on a configuration of said computer system.

14. (original) A computer system as recited in Claim 11 wherein said adjustable voltage supply comprises a voltage regulator.

15. (currently amended) A computer system comprising:

a processing unit;

circuitry coupled to the processing unit, said circuitry configured to provide to said processing unit:

a first sleep voltage and a second sleep voltage;

a first operating voltage when transitioning from said first sleep voltage; ~~and~~

a second operating voltage when transitioning from said second sleep voltage.

wherein said first operating voltage is greater than said second operating voltage and wherein said first sleep voltage is greater than said second sleep voltage; and

wherein a voltage transition from said second sleep voltage to said first operating voltage is greater than a time allowed for transition from a sleep state to an operating state of said computer system.

16. (original) A computer system as recited in Claim 15, wherein said circuitry is further configured to provide to said processing unit:

said first sleep voltage when transitioning from said first operating voltage; and

said second sleep voltage when transitioning from said second operating voltage.

17. (original) A computer system as recited in Claim 15 wherein a voltage difference between said first operating voltage and said first sleep voltage is approximately equal to a voltage difference between said second operating voltage and said second sleep voltage.

18-19 (cancelled).

20. (currently amended) A computer system comprising:

means for processing;

means for supplying a voltage coupled to said processing means for providing to said processing means:

a first and a second sleep voltage;

a first operating voltage responsive to a transition from said first sleep voltage; and

a second operating voltage responsive to a transition from said second sleep voltage.

wherein said means for supplying a voltage comprises means to generate a voltage transition from said second sleep voltage to said first operating voltage in a time period greater than a time period allowed for transition from a sleep state to an operating state of said computer system.

21. (previously presented)The computer system of Claim 20 wherein:

said means for supplying a voltage are further for providing to said means for processing:

said first sleep voltage re responsive to a transition from said first operating voltage; and

said second sleep voltage responsive to a transition from said second operating voltage.

22. (previously presented) The computer system of Claim 20 wherein a voltage difference between said first operating voltage and said first sleep voltage is

approximately equal to a voltage difference between said second operating voltage and said second sleep voltage.

23. (previously presented) The computer system of Claim 20 wherein said first operating voltage is greater than said second operating voltage and wherein said first sleep voltage is greater than said second sleep voltage.

24. (cancelled)

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
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# NOTICE OF ALLOWANCE AND FEE(S) DUE

7590 09/03/2010

MURABITO, HAO & BARNES LLP
Third Floor
Two North Market Street
San Jose, CA 95113

| EXAMINER | |
|---|---|
| CAO, CHUN | |
| ART UNIT | PAPER NUMBER |
| 2115 | |

DATE MAILED: 09/03/2010

| APPLICATION NO. | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. | CONFIRMATION NO. |
|---|---|---|---|---|
| 11/894,991 | 08/21/2007 | Andrew Read | TRAN-P470 | 9781 |

TITLE OF INVENTION: SAVING POWER WHEN IN OR TRANSITIONING TO A STATIC MODE OF A PROCESSOR

| APPLN. TYPE | SMALL ENTITY | ISSUE FEE DUE | PUBLICATION FEE DUE | PREV. PAID ISSUE FEE | TOTAL FEE(S) DUE | DATE DUE |
|---|---|---|---|---|---|---|
| nonprovisional | NO | $1510 | $300 | $0 | $1810 | 12/03/2010 |

**THE APPLICATION IDENTIFIED ABOVE HAS BEEN EXAMINED AND IS ALLOWED FOR ISSUANCE AS A PATENT. PROSECUTION ON THE MERITS IS CLOSED. THIS NOTICE OF ALLOWANCE IS NOT A GRANT OF PATENT RIGHTS. THIS APPLICATION IS SUBJECT TO WITHDRAWAL FROM ISSUE AT THE INITIATIVE OF THE OFFICE OR UPON PETITION BY THE APPLICANT. SEE 37 CFR 1.313 AND MPEP 1308.**

**THE ISSUE FEE AND PUBLICATION FEE (IF REQUIRED) MUST BE PAID WITHIN THREE MONTHS FROM THE MAILING DATE OF THIS NOTICE OR THIS APPLICATION SHALL BE REGARDED AS ABANDONED. THIS STATUTORY PERIOD CANNOT BE EXTENDED. SEE 35 U.S.C. 151. THE ISSUE FEE DUE INDICATED ABOVE DOES NOT REFLECT A CREDIT FOR ANY PREVIOUSLY PAID ISSUE FEE IN THIS APPLICATION. IF AN ISSUE FEE HAS PREVIOUSLY BEEN PAID IN THIS APPLICATION (AS SHOWN ABOVE), THE RETURN OF PART B OF THIS FORM WILL BE CONSIDERED A REQUEST TO REAPPLY THE PREVIOUSLY PAID ISSUE FEE TOWARD THE ISSUE FEE NOW DUE.**

**HOW TO REPLY TO THIS NOTICE:**

I. Review the SMALL ENTITY status shown above.

If the SMALL ENTITY is shown as YES, verify your current SMALL ENTITY status:

A. If the status is the same, pay the TOTAL FEE(S) DUE shown above.

B. If the status above is to be removed, check box 5b on Part B - Fee(s) Transmittal and pay the PUBLICATION FEE (if required) and twice the amount of the ISSUE FEE shown above, or

If the SMALL ENTITY is shown as NO:

A. Pay TOTAL FEE(S) DUE shown above, or

B. If applicant claimed SMALL ENTITY status before, or is now claiming SMALL ENTITY status, check box 5a on Part B - Fee(s) Transmittal and pay the PUBLICATION FEE (if required) and 1/2 the ISSUE FEE shown above.

II. PART B - FEE(S) TRANSMITTAL, or its equivalent, must be completed and returned to the United States Patent and Trademark Office (USPTO) with your ISSUE FEE and PUBLICATION FEE (if required). If you are charging the fee(s) to your deposit account, section "4b" of Part B - Fee(s) Transmittal should be completed and an extra copy of the form should be submitted. If an equivalent of Part B is filed, a request to reapply a previously paid issue fee must be clearly made, and delays in processing may occur due to the difficulty in recognizing the paper as an equivalent of Part B.

III. All communications regarding this application must give the application number. Please direct all communications prior to issuance to Mail Stop ISSUE FEE unless advised to the contrary.

**IMPORTANT REMINDER: Utility patents issuing on applications filed on or after Dec. 12, 1980 may require payment of maintenance fees. It is patentee's responsibility to ensure timely payment of maintenance fees when due.**



PTOL-85 (Rev. 08/07) Approved for use through 08/31/2010.

## PART B - FEE(S) TRANSMITTAL

**Complete and send this form, together with applicable fee(s), to: Mail** **Mail Stop ISSUE FEE**
**Commissioner for Patents**
**P.O. Box 1450**
**Alexandria, Virginia 22313-1450**
**or Fax (571)-273-2885**

INSTRUCTIONS: This form should be used for transmitting the ISSUE FEE and PUBLICATION FEE (if required). Blocks 1 through 5 should be completed where appropriate. All further correspondence including the Patent, advance orders and notification of maintenance fees will be mailed to the current correspondence address as indicated unless corrected below or directed otherwise in Block 1, by (a) specifying a new correspondence address; and/or (b) indicating a separate "FEE ADDRESS" for maintenance fee notifications.

CURRENT CORRESPONDENCE ADDRESS (Note: Use Block 1 for any change of address)

7590 09/03/2010

MURABITO, HAO & BARNES LLP
Third Floor
Two North Market Street
San Jose, CA 95113

Note: A certificate of mailing can only be used for domestic mailings of the Fee(s) Transmittal. This certificate cannot be used for any other accompanying papers. Each additional paper, such as an assignment or formal drawing, must have its own certificate of mailing or transmission.

**Certificate of Mailing or Transmission**

I hereby certify that this Fee(s) Transmittal is being deposited with the United States Postal Service with sufficient postage for first class mail in an envelope addressed to the Mail Stop ISSUE FEE address above, or being facsimile transmitted to the USPTO (571) 273-2885, on the date indicated below.

(Depositor's name)

(Signature)

(Date)

| APPLICATION NO. | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. | CONFIRMATION NO. |
|---|---|---|---|---|
| 11/894,991 | 08/21/2007 | Andrew Read | TRAN-P470 | 9781 |

TITLE OF INVENTION: SAVING POWER WHEN IN OR TRANSITIONING TO A STATIC MODE OF A PROCESSOR

| APPLN. TYPE | SMALL ENTITY | ISSUE FEE DUE | PUBLICATION FEE DUE | PREV. PAID ISSUE FEE | TOTAL FEE(S) DUE | DATE DUE |
|---|---|---|---|---|---|---|
| nonprovisional | NO | $1510 | $300 | $0 | $1810 | 12/03/2010 |

| EXAMINER | ART UNIT | CLASS-SUBCLASS |
|---|---|---|
| CAO, CHUN | 2115 | 713-320000 |

1. Change of correspondence address or indication of "Fee Address" (37 CFR 1.363).

❑ Change of correspondence address (or Change of Correspondence Address form PTO/SB/122) attached.

❑ "Fee Address" indication (or "Fee Address" Indication form PTO/SB/47; Rev 03-02 or more recent) attached. **Use of a Customer Number is required.**

2. For printing on the patent front page, list

(1) the names of up to 3 registered patent attorneys or agents OR, alternatively,

(2) the name of a single firm (having as a member a registered attorney or agent) and the names of up to 2 registered patent attorneys or agents. If no name is listed, no name will be printed.

1 _____

2 _____

3 _____

3. ASSIGNEE NAME AND RESIDENCE DATA TO BE PRINTED ON THE PATENT (print or type)

PLEASE NOTE: Unless an assignee is identified below, no assignee data will appear on the patent. If an assignee is identified below, the document has been filed for recordation as set forth in 37 CFR 3.11. Completion of this form is NOT a substitute for filing an assignment.

(A) NAME OF ASSIGNEE

(B) RESIDENCE: (CITY and STATE OR COUNTRY)

Please check the appropriate assignee category or categories (will not be printed on the patent) : ❑ Individual ❑ Corporation or other private group entity ❑ Government

4a. The following fee(s) are submitted:

❑ Issue Fee

❑ Publication Fee (No small entity discount permitted)

❑ Advance Order - # of Copies _____

4b. Payment of Fee(s): **(Please first reapply any previously paid issue fee shown above)**

❑ A check is enclosed.

❑ Payment by credit card. Form PTO-2038 is attached.

❑ The Director is hereby authorized to charge the required fee(s), any deficiency, or credit any overpayment, to Deposit Account Number _____ (enclose an extra copy of this form).

5. **Change in Entity Status** (from status indicated above)

❑ a. Applicant claims SMALL ENTITY status. See 37 CFR 1.27.

❑ b. Applicant is no longer claiming SMALL ENTITY status. See 37 CFR 1.27(g)(2).

NOTE: The Issue Fee and Publication Fee (if required) will not be accepted from anyone other than the applicant; a registered attorney or agent; or the assignee or other party in interest as shown by the records of the United States Patent and Trademark Office.

Authorized Signature _____ Date _____

Typed or printed name _____ Registration No. _____

This collection of information is required by 37 CFR 1.311. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, Virginia 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, Virginia 22313-1450.

Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

| APPLICATION NO. | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. | CONFIRMATION NO. |
|---|---|---|---|---|
| 11/894,991 | 08/21/2007 | Andrew Read | TRAN-P470 | 9781 |

7590 09/03/2010

MURABITO, HAO & BARNES LLP
Third Floor
Two North Market Street
San Jose, CA 95113

| EXAMINER | |
|---|---|
| CAO, CHUN | |
| ART UNIT | PAPER NUMBER |
| 2115 | |

DATE MAILED: 09/03/2010

**Determination of Patent Term Adjustment under 35 U.S.C. 154 (b)**
(application filed on or after May 29, 2000)

The Patent Term Adjustment to date is 235 day(s). If the issue fee is paid on the date that is three months after the mailing date of this notice and the patent issues on the Tuesday before the date that is 28 weeks (six and a half months) after the mailing date of this notice, the Patent Term Adjustment will be 235 day(s).

If a Continued Prosecution Application (CPA) was filed in the above-identified application, the filing date that determines Patent Term Adjustment is the filing date of the most recent CPA.

Applicant will be able to obtain more detailed information by accessing the Patent Application Information Retrieval (PAIR) WEB site (http://pair.uspto.gov).

Any questions regarding the Patent Term Extension or Adjustment determination should be directed to the Office of Patent Legal Administration at (571)-272-7702. Questions relating to issue and publication fee payments should be directed to the Customer Service Center of the Office of Patent Publication at 1-(888)-786-0101 or (571)-272-4200.



PTOL-85 (Rev. 08/07) Approved for use through 08/31/2010.

| Notice of Allowability | Application No. | Applicant(s) | |
|---|---|---|---|
| | 11/894,991 | READ ET AL. | |
| | Examiner | Art Unit | |
| | Chun Cao | 2115 | |

***-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--***

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to *amendment filed on 8/25/10*.

2. ☒ The allowed claim(s) is/are *1-17 and 20-23*.

3. ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
   a) ☐ All b) ☐ Some* c) ☐ None of the:
      1. ☐ Certified copies of the priority documents have been received.
      2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
      3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

   * Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
**THIS THREE-MONTH PERIOD IS NOT EXTENDABLE**.

4. ☐ A SUBSTITUTE OATH OR DECLARATION must be submitted. Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL PATENT APPLICATION (PTO-152) which gives reason(s) why the oath or declaration is deficient.

5. ☐ CORRECTED DRAWINGS ( as "replacement sheets") must be submitted.
   (a) ☐ including changes required by the Notice of Draftsperson's Patent Drawing Review ( PTO-948) attached
      1) ☐ hereto or 2) ☐ to Paper No./Mail Date _____.
   (b) ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.

   **Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).**

6. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

**Attachment(s)**

1. ☐ Notice of References Cited (PTO-892)
2. ☐ Notice of Draftperson's Patent Drawing Review (PTO-948)
3. ☐ Information Disclosure Statements (PTO/SB/08), Paper No./Mail Date _____
4. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material
5. ☐ Notice of Informal Patent Application
6. ☐ Interview Summary (PTO-413), Paper No./Mail Date _____ .
7. ☐ Examiner's Amendment/Comment
8. ☐ Examiner's Statement of Reasons for Allowance
9. ☐ Other _____.

/Chun Cao/
Primary Examiner, Art Unit 2115

| Index of Claims | Application/Control No. | Applicant(s)/Patent Under Reexamination |
|---|---|---|
| | 11894991 | READ ET AL. |
| | Examiner | Art Unit |
| | Chun Cao | 2115 |

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| ✓ | Rejected | - | Cancelled | N | Non-Elected | A | Appeal |
| = | Allowed | ÷ | Restricted | I | Interference | O | Objected |

☐ Claims renumbered in the same order as presented by applicant ☐ CPA ☐ T.D. ☐ R.1.47

| CLAIM | | DATE | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|
| Final | Original | 06/30/2009 | 01/20/2010 | 06/23/2010 | 08/31/2010 | | | | | |
| 1 | 1 | ✓ | = | = | = | | | | | |
| 2 | 2 | ✓ | = | = | = | | | | | |
| 3 | 3 | ✓ | = | = | = | | | | | |
| 4 | 4 | ✓ | = | = | = | | | | | |
| 5 | 5 | ✓ | = | = | = | | | | | |
| 6 | 6 | ✓ | = | = | = | | | | | |
| 7 | 7 | ✓ | = | = | = | | | | | |
| 8 | 8 | ✓ | = | = | = | | | | | |
| 9 | 9 | ✓ | = | = | = | | | | | |
| 10 | 10 | ✓ | = | = | = | | | | | |
| 11 | 11 | ✓ | ✓ | ✓ | = | | | | | |
| 12 | 12 | ✓ | ✓ | ✓ | = | | | | | |
| 13 | 13 | ✓ | ✓ | ✓ | = | | | | | |
| 14 | 14 | ✓ | ✓ | ✓ | = | | | | | |
| 15 | 15 | ✓ | ✓ | ✓ | = | | | | | |
| 16 | 16 | ✓ | ✓ | ✓ | = | | | | | |
| 17 | 17 | ✓ | ✓ | ✓ | = | | | | | |
| | 18 | ✓ | ✓ | ✓ | - | | | | | |
| | 19 | ✓ | O | O | - | | | | | |
| 18 | 20 | | ✓ | ✓ | = | | | | | |
| 19 | 21 | | ✓ | ✓ | = | | | | | |
| 20 | 22 | | ✓ | ✓ | = | | | | | |
| 21 | 23 | | ✓ | ✓ | = | | | | | |
| | 24 | | O | O | - | | | | | |

**EAST Search History**

**EAST Search History (Prior Art)**

| Ref # | Hits | Search Query | DBs | Default Operator | Plurals | Time Stamp |
|---|---|---|---|---|---|---|
| S112 | 3140 | 713/320.ccls. | US-PGPUB; USPAT; USOCR | OR | OFF | 2010/08/31 08:36 |
| S113 | 1905 | 713/323.ccls. | US-PGPUB; USPAT; USOCR | OR | OFF | 2010/08/31 08:37 |
| S114 | 1432 | 713/322.ccls. | US-PGPUB; USPAT; USOCR | OR | OFF | 2010/08/31 08:37 |
| S115 | 212 | "core voltage" with regulator with (cpu or processor or microprocessor) | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | OFF | 2010/08/31 08:38 |
| S116 | 40718 | ("central processing unit" or cpu or processor or microprocessor) near4 (stop$3 or disable $1) | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | OFF | 2010/08/31 09:12 |
| S117 | 9 | ((deep near1 sleep) or deep-sleep) with "core voltage" | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | OFF | 2010/08/31 09:13 |
| S118 | 344 | (("core voltage") same (cpu or processor or microprocessor)) same (low or sleep) | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | OFF | 2010/08/31 09:16 |
| S119 | 33 | (("core voltage") same (cpu or processor or microprocessor)) same ((low or sleep) adj voltage) | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | OFF | 2010/08/31 09:27 |
| S120 | 10 | S119 and g06f$.ipc. | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | OFF | 2010/08/31 09:29 |
| S121 | 154 | S116 same (voltage near2 regulator$1) | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | OFF | 2010/08/31 09:37 |

| | | | | | | |
|---|---|---|---|---|---|---|
| S123 | 85 | S121 and g06f$.ipc. | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | OFF | 2010/08/31 09:53 |

**8/31/10 12:42:24 PM**
**C:\Documents and Settings\ccao\My Documents\EAST\Workspaces\11894991.wsp**

| Issue Classification | Application/Control No. | Applicant(s)/Patent Under Reexamination |
|---|---|---|
| | 11894991 | READ ET AL. |
| | Examiner | Art Unit |
| | Chun Cao | 2115 |

| ORIGINAL | | INTERNATIONAL CLASSIFICATION | | | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| CLASS | SUBCLASS | CLAIMED | | | | | NON-CLAIMED | | | | | | | | | |
| 713 | 320 | G | 0 | 6 | F | 1 / 32 (2006.01.01) | | | | | | | | | | |

| CROSS REFERENCE(S) | | | | | |
|---|---|---|---|---|---|
| CLASS | SUBCLASS (ONE SUBCLASS PER BLOCK) | | | | |
| 713 | 323 | | | | |

☐ Claims renumbered in the same order as presented by applicant ☐ CPA ☐ T.D. ☐ R.1.47

| Final | Original | Final | Original | Final | Original | Final | Original | Final | Original | Final | Original | Final | Original | Final | Original |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 1 | 1 | 17 | 17 | | | | | | | | | | | | |
| 2 | 2 | | 18 | | | | | | | | | | | | |
| 3 | 3 | | 19 | | | | | | | | | | | | |
| 4 | 4 | 18 | 20 | | | | | | | | | | | | |
| 5 | 5 | 19 | 21 | | | | | | | | | | | | |
| 6 | 6 | 20 | 22 | | | | | | | | | | | | |
| 7 | 7 | 21 | 23 | | | | | | | | | | | | |
| 8 | 8 | | | | | | | | | | | | | | |
| 9 | 9 | | | | | | | | | | | | | | |
| 10 | 10 | | | | | | | | | | | | | | |
| 11 | 11 | | | | | | | | | | | | | | |
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| 15 | 15 | | | | | | | | | | | | | | |
| 16 | 16 | | | | | | | | | | | | | | |

| NONE | | Total Claims Allowed: | |
|---|---|---|---|
| (Assistant Examiner) | (Date) | 21 | |
| /Chun Cao/<br>Primary Examiner.Art Unit 2115 | 08/31/2010 | O.G. Print Claim(s) | O.G. Print Figure |
| (Primary Examiner) | (Date) | 1 | 5 |

| Search Notes | Application/Control No. | Applicant(s)/Patent Under Reexamination |
|---|---|---|
| | 11894991 | READ ET AL. |
| | Examiner | Art Unit |
| | Chun Cao | 2115 |

| SEARCHED | | | |
|---|---|---|---|
| Class | Subclass | Date | Examiner |
| 713 | 320, 323 | 8/31/10 | cc |

| SEARCH NOTES | | |
|---|---|---|
| Search Notes | Date | Examiner |
| Inventor name search, East search | 6/30/09 | cc |
| East updated search | 8/31/10 | cc |

| INTERFERENCE SEARCH | | | |
|---|---|---|---|
| Class | Subclass | Date | Examiner |
| 713 | 320, 323 | 8/31/10 | cc |
| | PGPUB text search | 8/31/10 | cc |

OK TO ENTER: /cc/ 08/31/2010

TRAN-P470 PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of: Read et al.

| | | | |
|---|---|---|---|
| Serial: | 11/894,991 | Group Art Unit: | 2115 |
| Filed: | August 21, 2007 | Examiner: | Chun Cao |
| For: | SAVING POWER WHEN IN OR TRANSITIONING TO A STATIC MODE OF A PROCESSOR (as filed) | | |

AMENDMENT and RESPONSE

Honorable Commissioner for Patents
PO Box 1450
Alexandria, VA 22313-1450

Dear Sir:

In response to the Office Action mailed June 25, 2010 in the above captioned Patent Application, Applicants respectfully request the Examiner to enter the following amendments and to consider the following remarks.

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

# BIB DATA SHEET

**CONFIRMATION NO. 9781**

| SERIAL NUMBER | FILING or 371(c) DATE | CLASS | GROUP ART UNIT | ATTORNEY DOCKET NO. |
|---|---|---|---|---|
| 11/894,991 | 08/21/2007<br>RULE | 713 | 2115 | TRAN-P470 |

**APPLICANTS**

Andrew Read, Sunnyvale, CA;
Sameer Halepete, San Jose, CA;
Keith Klayman, Sunnyvale, CA;

**** CONTINUING DATA **************************

This application is a DIV of 09/694,433 10/23/2000 PAT 7,260,731

**** FOREIGN APPLICATIONS **************************

**** IF REQUIRED, FOREIGN FILING LICENSE GRANTED ****

09/10/2007

| Foreign Priority claimed ☐ Yes ☑ No<br>35 USC 119(a-d) conditions met ☐ Yes ☐ No<br>Verified and Acknowledged /CHUN CAO/ Examiner's Signature | ☐ Met after Allowance<br>Initials | STATE OR COUNTRY | SHEETS DRAWINGS | TOTAL CLAIMS | INDEPENDENT CLAIMS |
|---|---|---|---|---|---|
| | | CA | 2 | 19 | 4 |

**ADDRESS**

MURABITO, HAO & BARNES LLP
Third Floor
Two North Market Street
San Jose, CA 95113
UNITED STATES

**TITLE**

Saving power when in or transitioning to a static mode of a processor

| FILING FEE RECEIVED | | |
|---|---|---|
| 1680 | FEES: Authority has been given in Paper<br>No._____ to charge/credit DEPOSIT ACCOUNT<br>No._____ for following: | ☐ All Fees<br>☐ 1.16 Fees (Filing)<br>☐ 1.17 Fees (Processing Ext. of time)<br>☐ 1.18 Fees (Issue)<br>☐ Other _____<br>☐ Credit |

BIB (Rev. 05/07).

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Alexandria, Virginia 22313-1450
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Bib Data Sheet

**CONFIRMATION NO. 9781**

| SERIAL NUMBER | FILING OR 371(c) DATE | CLASS | GROUP ART UNIT | ATTORNEY DOCKET NO. |
|---|---|---|---|---|
| 11/894,991 | 08/21/2007<br>RULE | 713 | 2115 | TRAN-P470 |

**APPLICANTS**

Andrew Read, Sunnyvale, CA;
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Keith Klayman, Sunnyvale, CA;

**** CONTINUING DATA ***************************

This application is a DIV of 09/694,433 10/23/2000 PAT 7,260,731

**** FOREIGN APPLICATIONS ********************

**IF REQUIRED, FOREIGN FILING LICENSE GRANTED**
** 09/10/2007

| Foreign Priority claimed | STATE OR COUNTRY | SHEETS DRAWING | TOTAL CLAIMS | INDEPENDENT CLAIMS |
|---|---|---|---|---|
| ☐ yes ☐ no | CA | 2 | 19 | 4 |
| 35 USC 119 (a-d) conditions met ☐ yes ☐ no ☐ Met after Allowance | | | | |
| Verified and Acknowledged Examiner's Signature Initials | | | | |

**ADDRESS**

MURABITO, HAO & BARNES LLP
Third Floor
Two North Market Street
San Jose, CA95113

**TITLE**

TRANSITIONING TO AND FROM A SLEEP STATE OF A PROCESSOR

| FILING FEE RECEIVED | | |
|---|---|---|
| 1680 | FEES: Authority has been given in Paper No. _____ to charge/credit DEPOSIT ACCOUNT No. _____ for following: | ☐ All Fees<br>☐ 1.16 Fees ( Filing )<br>☐ 1.17 Fees ( Processing Ext. of time )<br>☐ 1.18 Fees ( Issue )<br>☐ Other _____<br>☐ Credit |

# PART B - FEE(S) TRANSMITTAL

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**Commissioner for Patents**
**P.O. Box 1450**
**Alexandria, Virginia 22313-1450**
**or Fax (571) 273-2885**

INSTRUCTIONS: This form should be used for transmitting the ISSUE FEE and PUBLICATION FEE (if required). Blocks 1 through 5 should be completed where appropriate. All further correspondence including the Patent, advance orders and notification of maintenance fees will be mailed to the current correspondence address as indicated unless corrected below or directed otherwise in Block 1, by (a) specifying a new correspondence address; and/or (b) indicating a separate "FEE ADDRESS" for maintenance fee notifications.

CURRENT CORRESPONDENCE ADDRESS (Note: Use Block 1 for any change of address)

MURABITO, HAO & BARNES LLP
2 N. MARKET STREET
3RD FLOOR
SAN JOSE, CA 95113

Note: A certificate of mailing can only be used for domestic mailings of the Fee(s) Transmittal. This certificate cannot be used for any other accompanying papers. Each additional paper, such as an assignment or formal drawing, must have its own certificate of mailing or transmission.

**Certificate of Mailing or Transmission**

I hereby certify that this Fee(s) Transmittal is being deposited with the United States Postal Service with sufficient postage for first class mail in an envelope addressed to the Mail Stop ISSUE FEE address above, or being facsimile transmitted to the USPTO (571) 273-2885, on the date indicated below.

| | |
|---|---|
| /Donna Petford/ | (Depositor's name) |
| Donna Petford | (Signature) |
| 12-03-2010 | (Date) |

| APPLICATION NO. | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. | CONFIRMATION NO. |
|---|---|---|---|---|
| 11/894,991 | 08/21/2007 | Andrew Read | TRAN-P059D2 | 9781 |

TITLE OF INVENTION:

| APPLN. TYPE | SMALL ENTITY | ISSUE FEE | PUBLICATION FEE | TOTAL FEE(S) DUE | DATE DUE |
|---|---|---|---|---|---|
| nonprovisional | NO | $1510 | $300 | $1810 | 12/03/2010 |

| EXAMINER | ART UNIT | CLASS-SUBCLASS |
|---|---|---|
| | | |

1. Change of correspondence address or indication of "Fee Address" (37 CFR 1.363).

☐ Change of correspondence address (or Change of Correspondence Address form PTO/SB/122) attached.

☐ "Fee Address" indication (or "Fee Address" Indication form PTO/SB/47; Rev 03-02 or more recent) attached. **Use of a Customer Number is required.**

2. For printing on the patent front page, list

(1) the names of up to 3 registered patent attorneys or agents OR, alternatively, 1_

(2) the name of a single firm (having as a member a registered attorney or agent) and the names of up to 2 registered patent attorneys or agents. If no name is listed, no name will be printed. 2_ 3_

3. ASSIGNEE NAME AND RESIDENCE DATA TO BE PRINTED ON THE PATENT (print or type)

PLEASE NOTE: Unless an assignee is identified below, no assignee data will appear on the patent. If an assignee is identified below, the document has been filed for recordation as set forth in 37 CFR 3.11. Completion of this form is NOT a substitute for filing an assignment.

(A) NAME OF ASSIGNEE (B) RESIDENCE: (CITY and STATE OR COUNTRY)

Please check the appropriate assignee category or categories (will not be printed on the patent) : ☐ Individual ☐ Corporation or other private group entity ☐ Government

4a. The following fee(s) are enclosed:

☑ Issue Fee

☑ Publication Fee (No small entity discount permitted)

☐ Advance Order - # of Copies _

4b. Payment of Fee(s):

☐ A check in the amount of the fee(s) is enclosed.

☐ Payment by credit card. Form PTO-2038 is attached.

☑ The Director is hereby authorized by charge the required fee(s), or credit any overpayment, to Deposit Account Number 504160 .

5. **Change in Entity Status** (from status indicated above)

☐ a. Applicant claims SMALL ENTITY status. See 37 CFR 1.27.

☐ b. Applicant is no longer claiming SMALL ENTITY status. See 37 CFR 1.27(g)(2).

The Director of the USPTO is requested to apply the Issue Fee and Publication Fee (if any) or to re-apply any previously paid issue fee to the application identified above.
NOTE: The Issue Fee and Publication Fee (if required) will not be accepted from anyone other than the applicant; a registered attorney or agent; or the assignee or other party in interest as shown by the records of the United States Patent and Trademark Office.

Authorized Signature /Anthony C. Murabito/ Date 12/03/2010

Typed or printed name Anthony C. Murabito Registration No. 35295

This collection of information is required by 37 CFR 1.311. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, Virginia 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, Virginia 22313-1450.

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**The Privacy Act of 1974 (P.L. 93-579)** requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether disclosure of these records is required by the Freedom of Information Act.
2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.
3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.
4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).
5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.
6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).
7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.
8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspection or an issued patent.
9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

# Electronic Patent Application Fee Transmittal

| | |
|---|---|
| **Application Number:** | 11894991 |
| **Filing Date:** | 21-Aug-2007 |
| **Title of Invention:** | TRANSITIONING TO AND FROM A SLEEP STATE OF A PROCESSOR |
| **First Named Inventor/Applicant Name:** | Andrew Read |
| **Filer:** | Anthony C. Murabito/Donna Petford |
| **Attorney Docket Number:** | TRAN-P470 |

Filed as Large Entity

## Utility under 35 USC 111(a) Filing Fees

| Description | Fee Code | Quantity | Amount | Sub-Total in USD($) |
|---|---|---|---|---|
| **Basic Filing:** | | | | |
| **Pages:** | | | | |
| **Claims:** | | | | |
| **Miscellaneous-Filing:** | | | | |
| **Petition:** | | | | |
| **Patent-Appeals-and-Interference:** | | | | |
| **Post-Allowance-and-Post-Issuance:** | | | | |
| Utility Appl issue fee | 1501 | 1 | 1510 | 1510 |
| Publ. Fee- early, voluntary, or normal | 1504 | 1 | 300 | 300 |

| Description | Fee Code | Quantity | Amount | Sub-Total in USD($) |
|---|---|---|---|---|
| **Extension-of-Time:** | | | | |
| **Miscellaneous:** | | | | |
| | | **Total in USD ($)** | | **1810** |

| Electronic Acknowledgement Receipt | |
|---|---|
| **EFS ID:** | 8963659 |
| **Application Number:** | 11894991 |
| **International Application Number:** | |
| **Confirmation Number:** | 9781 |
| **Title of Invention:** | TRANSITIONING TO AND FROM A SLEEP STATE OF A PROCESSOR |
| **First Named Inventor/Applicant Name:** | Andrew Read |
| **Correspondence Address:** | MURABITO, HAO & BARNES LLP<br>-<br>Third Floor<br>Two North Market Street<br>San Jose CA 95113<br>US 4089389060<br>- |
| **Filer:** | Anthony C. Murabito/Donna Petford |
| **Filer Authorized By:** | Anthony C. Murabito |
| **Attorney Docket Number:** | TRAN-P470 |
| **Receipt Date:** | 03-DEC-2010 |
| **Filing Date:** | 21-AUG-2007 |
| **Time Stamp:** | 15:15:53 |
| **Application Type:** | Utility under 35 USC 111(a) |

## Payment information:

| | |
|---|---|
| Submitted with Payment | yes |
| Payment Type | Electronic Funds Transfer |
| Payment was successfully received in RAM | $1810 |

| | |
|---|---|
| RAM confirmation Number | 1508 |
| Deposit Account | |
| Authorized User | |

## File Listing:

| Document Number | Document Description | File Name | File Size(Bytes)/ Message Digest | Multi Part /.zip | Pages (if appl.) |
|---|---|---|---|---|---|
| 1 | Issue Fee Payment (PTO-85B) | TRAN-P059D2_ISSUEFEE_12-03-2010.pdf | 231989<br>a84cd7992e2d7e60d6e3db8d30fbd5ba9eab98cf | no | 2 |
| **Warnings:** | | | | | |
| **Information:** | | | | | |
| 2 | Fee Worksheet (PTO-875) | fee-info.pdf | 31812<br>31a378a054039c2dd574878f8763aecee602fbf2 | no | 2 |
| **Warnings:** | | | | | |
| **Information:** | | | | | |
| | | **Total Files Size (in bytes):** | 263801 | | |

**This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.**

**New Applications Under 35 U.S.C. 111**
**If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.**

**National Stage of an International Application under 35 U.S.C. 371**
**If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.**

**New International Application Filed with the USPTO as a Receiving Office**
**If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.**

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

| APPLICATION NO. | ISSUE DATE | PATENT NO. | ATTORNEY DOCKET NO. | CONFIRMATION NO. |
|---|---|---|---|---|
| 11/894,991 | 01/11/2011 | 7870404 | TRAN-P470 | 9781 |

7590 12/22/2010

MURABITO, HAO & BARNES LLP
Third Floor
Two North Market Street
San Jose, CA 95113

# ISSUE NOTIFICATION

The projected patent number and issue date are specified above.

**Determination of Patent Term Adjustment under 35 U.S.C. 154 (b)**
(application filed on or after May 29, 2000)

The Patent Term Adjustment is 378 day(s). Any patent to issue from the above-identified application will include an indication of the adjustment on the front page.

If a Continued Prosecution Application (CPA) was filed in the above-identified application, the filing date that determines Patent Term Adjustment is the filing date of the most recent CPA.

Applicant will be able to obtain more detailed information by accessing the Patent Application Information Retrieval (PAIR) WEB site (http://pair.uspto.gov).

Any questions regarding the Patent Term Extension or Adjustment determination should be directed to the Office of Patent Legal Administration at (571)-272-7702. Questions relating to issue and publication fee payments should be directed to the Application Assistance Unit (AAU) of the Office of Data Management (ODM) at (571)-272-4200.

APPLICANT(s) (Please see PAIR WEB site http://pair.uspto.gov for additional applicants):

Andrew Read, Sunnyvale, CA;
Sameer Halepete, San Jose, CA;
Keith Klayman, Sunnyvale, CA;

PTO/SB/44 (09-07)
Approved for use through 08/31/2010. OMB 0651-0033
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.
(Also Form PTO-1050)

# UNITED STATES PATENT AND TRADEMARK OFFICE
## CERTIFICATE OF CORRECTION



PATENT NO. : 7,870,404 B2

APPLICATION NO.: 11/894,991

ISSUE DATE : January 11, 2011

INVENTOR(S) : Read et al.

It is certified that an error appears or errors appear in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

Page 2, item (56), under “Other Publications”, in Column 2, Line 3, delete “Mhz” and insert - - MHZ - -.

Column 8, line 27, in Claim 11, delete “voltage:” and insert - - voltage; - -.

Column 8, line 60, in Claim 15, delete “voltage:” and insert - - voltage; - -.

Column 10, line 7, in Claim 19, delete “re responsive” and insert - - responsive - -.

MAILING ADDRESS OF SENDER (Please do not use customer number below):

_____
_____
_____
_____
_____

## Privacy Act Statement

The **Privacy Act of 1974 (P.L. 93-579)** requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether disclosure of these records is required by the Freedom of Information Act.
2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.
3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.
4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).
5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.
6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).
7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (*i.e.*, GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.
8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspection or an issued patent.
9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

| Electronic Patent Application Fee Transmittal | |
|---|---|
| **Application Number:** | 11894991 |
| **Filing Date:** | 21-Aug-2007 |
| **Title of Invention:** | TRANSITIONING TO AND FROM A SLEEP STATE OF A PROCESSOR |
| **First Named Inventor/Applicant Name:** | Andrew Read |
| **Filer:** | Blayne Donnis Green/Lindsey Hunt |
| **Attorney Docket Number:** | TRAN-P470 |

Filed as Large Entity

**Utility under 35 USC 111(a) Filing Fees**

| Description | Fee Code | Quantity | Amount | Sub-Total in USD($) |
|---|---|---|---|---|
| **Basic Filing:** | | | | |
| **Pages:** | | | | |
| **Claims:** | | | | |
| **Miscellaneous-Filing:** | | | | |
| **Petition:** | | | | |
| **Patent-Appeals-and-Interference:** | | | | |
| **Post-Allowance-and-Post-Issuance:** | | | | |
| Certificate of correction | 1811 | 1 | 100 | 100 |
| **Extension-of-Time:** | | | | |

| Description | Fee Code | Quantity | Amount | Sub-Total in USD($) |
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| **Miscellaneous:** | | | | |
| | | **Total in USD ($)** | | **100** |

| Electronic Acknowledgement Receipt | |
|---|---|
| **EFS ID:** | 9991567 |
| **Application Number:** | 11894991 |
| **International Application Number:** | |
| **Confirmation Number:** | 9781 |
| **Title of Invention:** | TRANSITIONING TO AND FROM A SLEEP STATE OF A PROCESSOR |
| **First Named Inventor/Applicant Name:** | Andrew Read |
| **Correspondence Address:** | MURABITO, HAO & BARNES LLP<br>-<br>Third Floor<br>Two North Market Street<br>San Jose CA 95113<br>US 4089389060<br>- |
| **Filer:** | Blayne Donnis Green/Lindsey Hunt |
| **Filer Authorized By:** | Blayne Donnis Green |
| **Attorney Docket Number:** | TRAN-P470 |
| **Receipt Date:** | 29-APR-2011 |
| **Filing Date:** | 21-AUG-2007 |
| **Time Stamp:** | 18:05:28 |
| **Application Type:** | Utility under 35 USC 111(a) |

## Payment information:

| | |
|---|---|
| Submitted with Payment | yes |
| Payment Type | Credit Card |
| Payment was successfully received in RAM | $100 |

| | |
|---|---|
| RAM confirmation Number | 4973 |
| Deposit Account | |
| Authorized User | |

## File Listing:

| Document Number | Document Description | File Name | File Size(Bytes)/ Message Digest | Multi Part /.zip | Pages (if appl.) |
|---|---|---|---|---|---|
| 1 | Request for Certificate of Correction | CoC_7870404.pdf | 80875<br>2e6e1638251a69e2a71a59a39ae94f1cfd5f7744 | no | 2 |
| **Warnings:** | | | | | |
| **Information:** | | | | | |
| 2 | Fee Worksheet (PTO-875) | fee-info.pdf | 29705<br>a94a1dee4bc9dfc33b52b20a7ae0c11d31fe62e9 | no | 2 |
| **Warnings:** | | | | | |
| **Information:** | | | | | |
| | | **Total Files Size (in bytes):** | 110580 | | |

**This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.**

**<u>New Applications Under 35 U.S.C. 111</u>**
**If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.**

**<u>National Stage of an International Application under 35 U.S.C. 371</u>**
**If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.**

**<u>New International Application Filed with the USPTO as a Receiving Office</u>**
**If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.**

UNITED STATES PATENT AND TRADEMARK OFFICE

# CERTIFICATE OF CORRECTION



| | |
|---|---|
| PATENT NO. | : 7,870,404 B2 |
| APPLICATION NO. | : 11/894991 |
| DATED | : January 11, 2011 |
| INVENTOR(S) | : Read et al. |

It is certified that error appears in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

Page 2, item (56), under "Other Publications", in Column 2, Line 3, delete "Mhz" and insert -- MHZ --.

Column 8, line 27, in Claim 11, delete "voltage:" and insert -- voltage; --.

Column 8, line 60, in Claim 15, delete "voltage:" and insert -- voltage; --.

Column 10, line 7, in Claim 19, delete "re responsive" and insert -- responsive --.

Signed and Sealed this
Thirty-first Day of May, 2011

David J. Kappos

David J. Kappos
*Director of the United States Patent and Trademark Office*

# PATENT ASSIGNMENT COVER SHEET

Electronic Version v1.1
Stylesheet Version v1.2

EPAS ID: PAT6027515

| | |
|---|---|
| **SUBMISSION TYPE:** | NEW ASSIGNMENT |
| **NATURE OF CONVEYANCE:** | NUNC PRO TUNC ASSIGNMENT |
| **EFFECTIVE DATE:** | 01/10/2020 |
| **SEQUENCE:** | 2 |

**CONVEYING PARTY DATA**

| Name | Execution Date |
|---|---|
| INTELLECTUAL VENTURES ASSETS 156 LLC | 01/10/2020 |

**RECEIVING PARTY DATA**

| | |
|---|---|
| **Name:** | INNOVATIVE SILICON SOLUTIONS, LLC |
| **Street Address:** | 2382 ROCKFIELD BLVD. |
| **Internal Address:** | SUITE 170 |
| **City:** | LAKE FOREST |
| **State/Country:** | CALIFORNIA |
| **Postal Code:** | 92630 |

**PROPERTY NUMBERS Total: 10**

| Property Type | Number |
|---|---|
| **Patent Number:** | 7260731 |
| **Patent Number:** | 7870404 |
| **Patent Number:** | 9436264 |
| **Patent Number:** | 9690366 |
| **Patent Number:** | 7302619 |
| **Patent Number:** | 7600166 |
| **Patent Number:** | 7334173 |
| **Patent Number:** | 7634701 |
| **Patent Number:** | 7810002 |
| **Patent Number:** | 6774033 |

**CORRESPONDENCE DATA**

**Fax Number:**

***Correspondence will be sent to the e-mail address first; if that is unsuccessful, it will be sent using a fax number, if provided; if that is unsuccessful, it will be sent via US Mail.***

**Phone:** 949-791-9366
**Email:** fahim@hongdungroup.com
**Correspondent Name:** FAHIM AFTAB
**Address Line 1:** 2382 ROCKFIELD BLVD.

| | |
|---|---|
| **Address Line 2:** | SUITE 170 |
| **Address Line 4:** | LAKE FOREST, CALIFORNIA 92630 |
| **ATTORNEY DOCKET NUMBER:** | JG032320-2 |
| **NAME OF SUBMITTER:** | FAHIM AFTAB |
| **SIGNATURE:** | /Fahim Aftab/ |
| **DATE SIGNED:** | 03/23/2020 |
| | This document serves as an Oath/Declaration (37 CFR 1.63). |

**Total Attachments: 3**
source=IV Assignment A-2#page1.tif
source=IV Assignment A-2#page2.tif
source=IV Assignment A-2#page3.tif

*Exhibit A-2*

## ASSIGNMENT OF PATENT RIGHTS

For good and valuable consideration, the receipt of which is hereby acknowledged, Intellectual Ventures Assets 156 LLC, a Delaware limited liability company, with an address at 251 Little Falls Drive, Wilmington, DE 19808 ("***Assignor***"), does hereby sell, assign, transfer, and convey unto Innovative Silicon Solutions, LLC, a Texas limited liability company having an address at 5900 Balcones Drive, STE 100, Austin, TX 78731 ("***Assignee***"), all of Assignor's right, title, and interest in and to the following (collectively, the "***Assigned Patent Rights***"):

(a) the patents and patent applications listed in the table below (the "***Patents***");

**Active Patent(s) – (Filed; Granted)**

| Patent/Application Number | Country | Issue Date/ Filing Date | Title of Patent and First Named Inventor |
|---|---|---|---|
| 7260731<br><br>(09/694433) | US | 2007-08-21<br><br>(2000-10-23) | Saving Power When In Or Transitioning To A Static Mode Of A Processor<br><br>Andrew Read |
| 7870404<br><br>(11/894991) | US | 2011-01-11<br><br>(2007-08-21) | Transitioning To And From A Sleep State Of A Processor<br><br>Andrew Read |
| 9436264<br><br>(12/987423) | US | 2016-09-06<br><br>(2011-01-10) | Saving Power When In Or Transitioning To A Static Mode Of A Processor<br><br>Andrew Read |
| 9690366<br><br>(15/241690) | US | 2017-06-27<br><br>(2016-08-19) | Saving Power When In Or Transitioning To A Static Mode Of A Processor By Using Feedback-Configured Voltage Regulator<br><br>Andrew Read |
| 7302619<br><br>(10/885356) | US | 2007-11-27<br><br>(2004-07-06) | Error Correction In A Cache Memory<br><br>Joseph Tompkins |
| 7600166<br><br>(11/169403) | US | 2009-10-06<br><br>(2005-06-28) | Method And System For Providing Trusted Access To A JTAG Scan Interface In A Microprocessor<br><br>David Dunn |
| 7334173<br><br>(11/241104) | US | 2008-02-19<br><br>(2005-09-29) | Method And System For Protecting Processors From Unauthorized Debug Access |

| Patent/Application Number | Country | Issue Date/ Filing Date | Title of Patent and First Named Inventor |
|---|---|---|---|
| | | | Morgan, Andrew |
| TWI325534 (TW095136358) | TW | 2010-06-01 (2006-09-29) | Securing Scan Test Architecture Morgan, Andrew |
| 7634701 (12/033864) | US | 2009-12-15 (2008-02-19) | Method And System For Protecting Processors From Unauthorized Debug Access Morgan, Andrew |
| 7810002 (12/544145) | US | 2010-10-05 (2009-08-19) | Providing Trusted Access To A Jtag Scan Interface In A Microprocessor David Dunn |
| 6774033 (10/287258) | US | 2004-08-10 (2002-11-04) | Metal Stack For Local Interconnect Layer Ben-Tzur, Mira |

(b) any future reissues, reexaminations, extensions, continuations, continuing prosecution application, requests for continuing examinations, divisions, and registrations of any of the Patents;

(c) rights to apply in any or all countries of the world for future patents, certificates of invention, utility models, industrial design protections, design patent protections, or other future governmental grants or issuances of any type related to the Patents; and

(d) causes of action and enforcement rights of any kind under, or on account of, any of the Patents and/or any of the items described in either of the foregoing categories (b) or (c), including, without limitation, all causes of action, enforcement rights and all other rights to seek and obtain any other remedies of any kind for past, current and future infringement.

Assignor hereby authorizes the respective patent office or governmental agency in each jurisdiction to issue any and all future patents, certificates of invention, utility models or other governmental grants or issuances that may be granted upon any of the Assigned Patent Rights in the name of Assignee, as the assignee to the entire interest therein. This Assignment of Patent Rights will inure for the benefit of any permitted successors or assigns of Assignee.

Assignor will, at the reasonable request of Assignee, take all reasonable steps necessary and proper, to confirm the assignment to Assignee of the Assigned Patent Rights pursuant to this Assignment of Patent Rights, including without limitation, the execution, acknowledgment, and recordation of specific assignments, oaths, declarations, and other documents on a country-by-country basis, to assist Assignee in obtaining and perfecting the Assigned Patent Rights.

IN WITNESS WHEREOF this Assignment of Patent Rights is executed on January 10, 2020 to be effective as of January 10, 2020.

**ASSIGNOR:**

INTELLECTUAL VENTURES ASSETS 156 LLC
By: _____
Name: Jim Weisfield
Title: Authorized Person

# PATENT ASSIGNMENT COVER SHEET

Electronic Version v1.1
Stylesheet Version v1.2

EPAS ID: PAT6036476

| | |
|---|---|
| **SUBMISSION TYPE:** | CORRECTIVE ASSIGNMENT |
| **NATURE OF CONVEYANCE:** | Corrective Assignment to correct the RE-RECORD ASSIGNMENT PREVIOUSLY RECORDED UNDER 052199/0838 TO CORRECT ADDRESS OF RECEIVING PARTY. previously recorded on Reel 052199 Frame 0838. Assignor(s) hereby confirms the NUNC PRO TUNC ASSIGNMENT. |
| **SEQUENCE:** | 2 |

**CONVEYING PARTY DATA**

| Name | Execution Date |
|---|---|
| INTELLECTUAL VENTURES ASSETS 156 LLC | 01/10/2020 |

**RECEIVING PARTY DATA**

| | |
|---|---|
| **Name:** | INNOVATIVE SILICON SOLUTIONS, LLC |
| **Street Address:** | 5900 BALCONES DRIVE |
| **City:** | AUSTIN |
| **State/Country:** | TEXAS |
| **Postal Code:** | 78731 |

**PROPERTY NUMBERS Total: 10**

| Property Type | Number |
|---|---|
| **Patent Number:** | 7260731 |
| **Patent Number:** | 7870404 |
| **Patent Number:** | 9436264 |
| **Patent Number:** | 9690366 |
| **Patent Number:** | 7302619 |
| **Patent Number:** | 7600166 |
| **Patent Number:** | 7334173 |
| **Patent Number:** | 7634701 |
| **Patent Number:** | 7810002 |
| **Patent Number:** | 6774033 |

**CORRESPONDENCE DATA**

**Fax Number:**

***Correspondence will be sent to the e-mail address first; if that is unsuccessful, it will be sent using a fax number, if provided; if that is unsuccessful, it will be sent via US Mail.***

**Phone:** 9497919366
**Email:** fahim@hongdungroup.com
**Correspondent Name:** FAHIM AFTAB

| | |
|---|---|
| **Address Line 1:** | 23832 ROCKFIELD BLVD. |
| **Address Line 2:** | SUITE 170 |
| **Address Line 4:** | LAKE FOREST, CALIFORNIA 92630 |

| | |
|---|---|
| **ATTORNEY DOCKET NUMBER:** | JG032320-2 CORRECTED |
| **NAME OF SUBMITTER:** | FAHIM AFTAB |
| **SIGNATURE:** | /Fahim Aftab/ |
| **DATE SIGNED:** | 03/28/2020 |
| | This document serves as an Oath/Declaration (37 CFR 1.63). |

**Total Attachments: 6**
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*Electronic Patent Assignment System*

# Confirmation Receipt

**Your assignment has been received by the USPTO.**
**The coversheet of the assignment is displayed below:**

## PATENT ASSIGNMENT COVER SHEET

Electronic Version v1.1
Stylesheet Version v1.2

| | |
|---|---|
| **SUBMISSION TYPE:** | NEW ASSIGNMENT |
| **NATURE OF CONVEYANCE:** | NUNC PRO TUNC ASSIGNMENT |
| **EFFECTIVE DATE:** | 01/10/2020 |
| **SEQUENCE:** | 2 |

**CONVEYING PARTY DATA**

| Name | Execution Date |
|---|---|
| INTELLECTUAL VENTURES ASSETS 156 LLC | 01/10/2020 |

**RECEIVING PARTY DATA**

| | |
|---|---|
| **Name:** | INNOVATIVE SILICON SOLUTIONS, LLC |
| **Street Address:** | 2382 ROCKFIELD BLVD. |
| **Internal Address:** | SUITE 170 |
| **City:** | LAKE FOREST |
| **State/Country:** | CALIFORNIA |
| **Postal Code:** | 92630 |

**PROPERTY NUMBERS Total: 10**

| Property Type | Number (Issue Date) | |
|---|---|---|
| **Patent Number:** | 7260731 8/21/2007 | 09/694,433 |

Fee Paid

| | | | | | |
|---|---|---|---|---|---|
| Patent Number: | 7870404 | 01/11/2011 | 11/894,991 | expires | 01/11/22 |
| Patent Number: | 9436264 | 9/6/2016 | 12/987,423 | Fees Due | 9/6/23 |
| Patent Number: | 9690366 | 6/27/2017 | 15/241,690 | Fees Due | 6/27/2020 |
| Patent Number: | 7302619 | 11/27/2001 | 10/885,356 | Fees Paid | 3.5yr |
| Patent Number: | 7600166 | 10/06/2009 | 11/169,403 | Fees due | 10/04/2020 |
| Patent Number: | 7334173 | 02/19/2008 | 11/241,104 | Fees Paid | |
| Patent Number: | 7634701 | 12/15/2009 | 12/033,864 | Fees Due | 12/15/2020 |
| Patent Number: | 7810002 | 10/05/2010 | 12/544,145 | Fees Due | 10/05/2021 |
| Patent Number: | 6774033 | 08/10/2004 | 10/287,255 | Fees Paid | |

11.5yr window

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| Date: | 03/23/2020 |
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**Total Attachments: 3**
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source=IV Assignment A-2#page2.tif
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*Exhibit A-2*

## ASSIGNMENT OF PATENT RIGHTS

For good and valuable consideration, the receipt of which is hereby acknowledged, Intellectual Ventures Assets 156 LLC, a Delaware limited liability company, with an address at 251 Little Falls Drive, Wilmington, DE 19808 ("***Assignor***"), does hereby sell, assign, transfer, and convey unto Innovative Silicon Solutions, LLC, a Texas limited liability company having an address at 5900 Balcones Drive, STE 100, Austin, TX 78731 ("***Assignee***"), all of Assignor's right, title, and interest in and to the following (collectively, the "***Assigned Patent Rights***"):

(a) the patents and patent applications listed in the table below (the "***Patents***");

**Active Patent(s) – (Filed; Granted)**

| Patent/Application Number | Country | Issue Date/ Filing Date | Title of Patent and First Named Inventor |
|---|---|---|---|
| 7260731<br><br>(09/694433) | US | 2007-08-21<br><br>(2000-10-23) | Saving Power When In Or Transitioning To A Static Mode Of A Processor<br><br>Andrew Read |
| 7870404<br><br>(11/894991) | US | 2011-01-11<br><br>(2007-08-21) | Transitioning To And From A Sleep State Of A Processor<br><br>Andrew Read |
| 9436264<br><br>(12/987423) | US | 2016-09-06<br><br>(2011-01-10) | Saving Power When In Or Transitioning To A Static Mode Of A Processor<br><br>Andrew Read |
| 9690366<br><br>(15/241690) | US | 2017-06-27<br><br>(2016-08-19) | Saving Power When In Or Transitioning To A Static Mode Of A Processor By Using Feedback-Configured Voltage Regulator<br><br>Andrew Read |
| 7302619<br><br>(10/885356) | US | 2007-11-27<br><br>(2004-07-06) | Error Correction In A Cache Memory<br><br>Joseph Tompkins |
| 7600166<br><br>(11/169403) | US | 2009-10-06<br><br>(2005-06-28) | Method And System For Providing Trusted Access To A JTAG Scan Interface In A Microprocessor<br><br>David Dunn |
| 7334173<br><br>(11/241104) | US | 2008-02-19<br><br>(2005-09-29) | Method And System For Protecting Processors From Unauthorized Debug Access |

| Patent/Application Number | Country | Issue Date/ Filing Date | Title of Patent and First Named Inventor |
|---|---|---|---|
| | | | Morgan, Andrew |
| TWI325534<br>(TW095136358) | TW | 2010-06-01<br>(2006-09-29) | Securing Scan Test Architecture<br>Morgan, Andrew |
| 7634701<br>(12/033864) | US | 2009-12-15<br>(2008-02-19) | Method And System For Protecting Processors From Unauthorized Debug Access<br>Morgan, Andrew |
| 7810002<br>(12/544145) | US | 2010-10-05<br>(2009-08-19) | Providing Trusted Access To A Jtag Scan Interface In A Microprocessor<br>David Dunn |
| 6774033<br>(10/287258) | US | 2004-08-10<br>(2002-11-04) | Metal Stack For Local Interconnect Layer<br>Ben-Tzur, Mira |

(b) any future reissues, reexaminations, extensions, continuations, continuing prosecution application, requests for continuing examinations, divisions, and registrations of any of the Patents;

(c) rights to apply in any or all countries of the world for future patents, certificates of invention, utility models, industrial design protections, design patent protections, or other future governmental grants or issuances of any type related to the Patents; and

(d) causes of action and enforcement rights of any kind under, or on account of, any of the Patents and/or any of the items described in either of the foregoing categories (b) or (c), including, without limitation, all causes of action, enforcement rights and all other rights to seek and obtain any other remedies of any kind for past, current and future infringement.

Assignor hereby authorizes the respective patent office or governmental agency in each jurisdiction to issue any and all future patents, certificates of invention, utility models or other governmental grants or issuances that may be granted upon any of the Assigned Patent Rights in the name of Assignee, as the assignee to the entire interest therein. This Assignment of Patent Rights will inure for the benefit of any permitted successors or assigns of Assignee.

Assignor will, at the reasonable request of Assignee, take all reasonable steps necessary and proper, to confirm the assignment to Assignee of the Assigned Patent Rights pursuant to this Assignment of Patent Rights, including without limitation, the execution, acknowledgment, and recordation of specific assignments, oaths, declarations, and other documents on a country-by-country basis, to assist Assignee in obtaining and perfecting the Assigned Patent Rights.

IN WITNESS WHEREOF this Assignment of Patent Rights is executed on January 10, 2020 to be effective as of January 10, 2020.

**ASSIGNOR:**

INTELLECTUAL VENTURES ASSETS 156 LLC
By: _____
Name: Jim Weisfield
Title: Authorized Person

*Exhibit B-2*

## ASSIGNMENT OF RIGHTS IN CERTAIN ASSETS

For good and valuable consideration, the receipt of which is hereby acknowledged, Intellectual Ventures Assets 156 LLC, a Delaware limited liability company, with an address at 251 Little Falls Drive, Wilmington, DE 19808 ("***Assignor***"), does hereby sell, assign, transfer, and convey unto Innovative Silicon Solutions, LLC, a Texas limited liability company having an address at 5900 Balcones Drive, STE 100, Austin, TX 78731 ("***Assignee***"), its right, title, and interest in and to any and all of the following provisional patent applications, patent applications, patents, and other governmental grants or issuances of any kind (the "***Certain Assets***"):

**Inactive Patent(s) – (Abandoned; Lapsed; Expired)**

| Patent/Application Number | Country | Issue Date/ Filing Date | Title of Patent and First Named Inventor |
|---|---|---|---|
| (PCT/US2001/050801) | WO | (2001-10-18) | Method And Apparatus For Reducing Static Power Loss<br><br>Andrew Read |
| (PCT/US2006/038168) | WO | (2006-09-28) | Securing Scan Test Architecture<br><br>Morgan, Andrew |

Assignor assigns to Assignee all of its rights to the inventions, invention disclosures, and discoveries in the assets listed above, together, with its rights, if any, to revive prosecution of claims under such assets and to sue or otherwise enforce any claims under such assets for past, present or future infringement.

Assignor hereby authorizes the respective patent office or governmental agency in each jurisdiction to make available to Assignee all records regarding the Certain Assets.

The terms and conditions of this Assignment of Rights in Certain Assets will inure to the benefit of Assignee, its successors, assigns, and other legal representatives and will be binding upon Assignor, its successors, assigns, and other legal representatives.

EXECUTED this 10th day of January 2020, to be effective as of January 10, 2020.

**ASSIGNOR:**

**INTELLECTUAL VENTURES ASSETS 156 LLC**
By: _____
Name: Jim Weisfield
Title: Authorized Person

# PATENT ASSIGNMENT COVER SHEET

Electronic Version v1.1
Stylesheet Version v1.2

EPAS ID: PAT6398647

| | |
|---|---|
| **SUBMISSION TYPE:** | NEW ASSIGNMENT |
| **NATURE OF CONVEYANCE:** | CHANGE OF NAME |

**CONVEYING PARTY DATA**

| Name | Execution Date |
|---|---|
| INNOVATIVE SILICON SOLUTIONS LLC | 11/12/2020 |

**RECEIVING PARTY DATA**

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| **State/Country:** | TEXAS |
| **Postal Code:** | 78731 |

**PROPERTY NUMBERS Total: 12**

| Property Type | Number |
|---|---|
| **Patent Number:** | 7302619 |
| **Patent Number:** | 6774033 |
| **Patent Number:** | 7154299 |
| **Patent Number:** | 6748577 |
| **Patent Number:** | 7260731 |
| **Patent Number:** | 9436264 |
| **Patent Number:** | 9690366 |
| **Patent Number:** | 7870404 |
| **Patent Number:** | 7600166 |
| **Patent Number:** | 7810002 |
| **Patent Number:** | 7634701 |
| **Patent Number:** | 7334173 |

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| | This document serves as an Oath/Declaration (37 CFR 1.63). |
| **Total Attachments: 1**<br>source=Certificate of Filing of HD Silicon#page1.tif | |

Corporations Section
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Ruth R. Hughs
Secretary of State

# Office of the Secretary of State

## CERTIFICATE OF FILING
## OF

HD Silicon Solutions LLC
803500718

[formerly: Innovative Silicon Solutions, LLC]

The undersigned, as Secretary of State of Texas, hereby certifies that a Certificate of Amendment for the above named entity has been received in this office and has been found to conform to the applicable provisions of law.

ACCORDINGLY, the undersigned, as Secretary of State, and by virtue of the authority vested in the secretary by law, hereby issues this certificate evidencing filing effective on the date shown below.

Dated: 11/10/2020

Effective: 11/10/2020

Ruth R. Hughs
Secretary of State