i486™ MICROPROCESSOR

- Binary Compatible with Large Software Base
 - MS-DOS*, OS/2**, Windows UNIX*** System V/386

 - iRMX[®], iRMK™ Kernels
- High Integration Enables On-Chip -8 Kbyte Code and Data Cache
 - Floating Point Unit
 - Paged, Virtual Memory Management
- Easy To Use
 - -Built-In Self Test
 - Hardware Debugging Support
 - -Intel Software Support
 - Extensive Third Party Software Support

- High Performance Design - Frequent Instructions Execute in One Clock
 - 25 MHz and 33 MHz Clock **Frequencies**
 - 106 Mbyte/Sec Burst Bus
 - CHMOS IV Process Technology
- Complete 32-Bit Architecture — Address and Data Busses
 - Registers
- Multiprocessor Support
 - Multiprocessor Instructions
 - Cache Consistency Protocols
 - -Support for Second Level Cache

The i486™ CPU offers the highest performance for DOS, OS/2, Windows and UNIX System V/386 applications. It is 100% binary compatible with the 386TM CPU. One million transistors integrate cache memory, floating point hardware and memory management on-chip while retaining binary compatibility with previous members of the 86 architectural family. Frequently used instructions execute in one cycle resulting in RISC performance levels. An 8 Kbyte unified code and data cache combined with a 106 Mbyte/Sec burst bus at 33.3 MHz ensure high system throughput even with inexpensive DRAMs.

New features enhance multiprocessing systems. New instructions speed manipulation of memory based semaphores. On-chip hardware ensures cache consistency and provides hooks for multilevel caches.

The built in self test extensively tests on-chip logic, cache memory and the on-chip paging translation cache. Debug features include breakpoint traps on code execution and data accesses.



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