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Moody et al.

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[45] **Date of Patent: * Jul. 19, 1994**

[54] **SWITCHED-CAPACITOR NOTCH FILTER WITH PROGRAMMABLE NOTCH WIDTH AND DEPTH**

[75] Inventors: **Kristaan L. Moody**, Nottingham; **Paul W. Latham, II**, Lee, both of N.H.

[73] Assignee: **Allegro Microsystems, Inc.**, Worcester, Mass.

[*] Notice: The portion of the term of this patent subsequent to Sep. 14, 2010 has been disclaimed.

[21] Appl. No.: **912,382**

[22] Filed: **Jul. 13, 1992**

[51] **Int. Cl.**^{5} **H03K 5/00**

[52] **U.S. Cl.** **307/521**; 328/167

[58] **Field of Search** 307/520, 521, 524; 328/167

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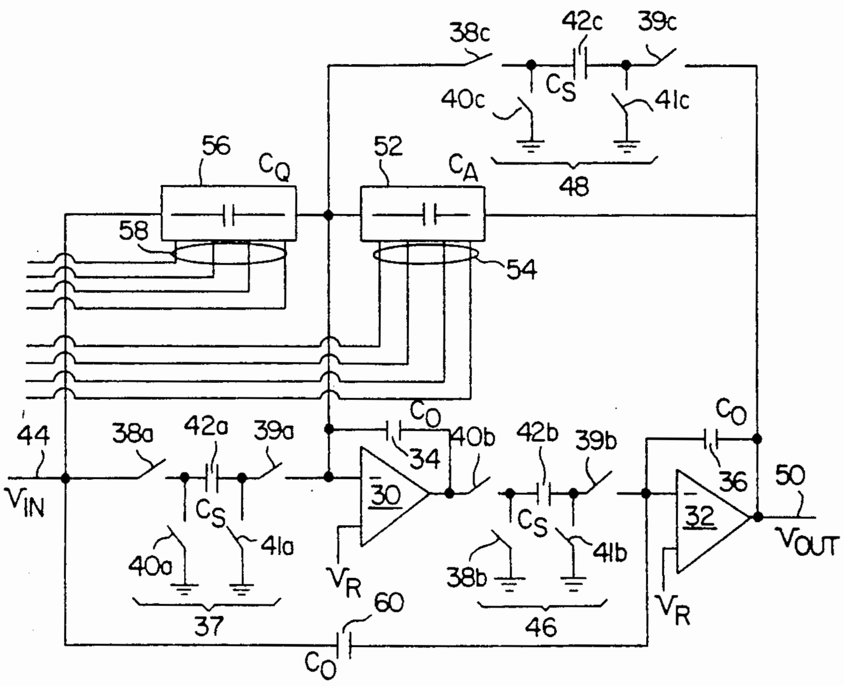
Primary Examiner—Richard A. Bertsch
Assistant Examiner—David W. Scheuermann

[57] **ABSTRACT**

A notch filter circuit includes first and second operational amplifiers, each having a capacitor connected from the amplifier output to the input. A third capacitor is connected between the second-amplifier input and the filter circuit input. A first switched-capacitor resistor is connected between the filter circuit input and the first-amplifier input. A second switched-capacitor resistor is connected between the first amplifier output and the second amplifier input. The second-amplifier output is connected to the filter circuit output. A third switched-capacitor resistor is connected between said filter circuit output and said first amplifier input; First and second programmable capacitor arrays are connected respectively in parallel with the third switched-capacitor resistor and in parallel with the first switched-capacitor resistor, so that a change only in the capacitance of the second capacitor array causes a corresponding change in the filter notch depth and a change only in the capacitance of the first capacitor array causes a corresponding change in the filter notch width. The first and second capacitor arrays each have a group of digital programming terminals that may be connected together for making fixed the ratio of the capacitance values of the two arrays. A digitally programmable voltage divider circuit connected in series with the second programmable capacitor array permits the independent programing of notch depth, i.e. without affecting notch width.

5 Claims, 3 Drawing Sheets



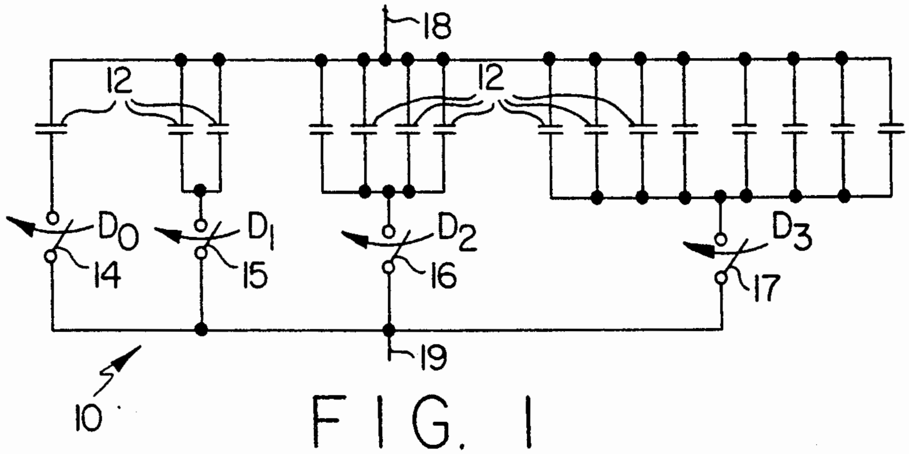


FIG. 1
PRIOR ART

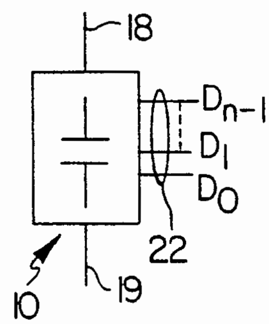


FIG. 2

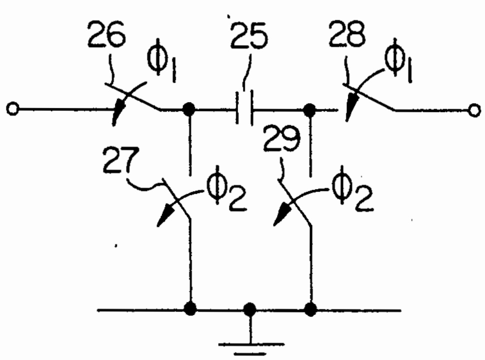


FIG. 3
PRIOR ART

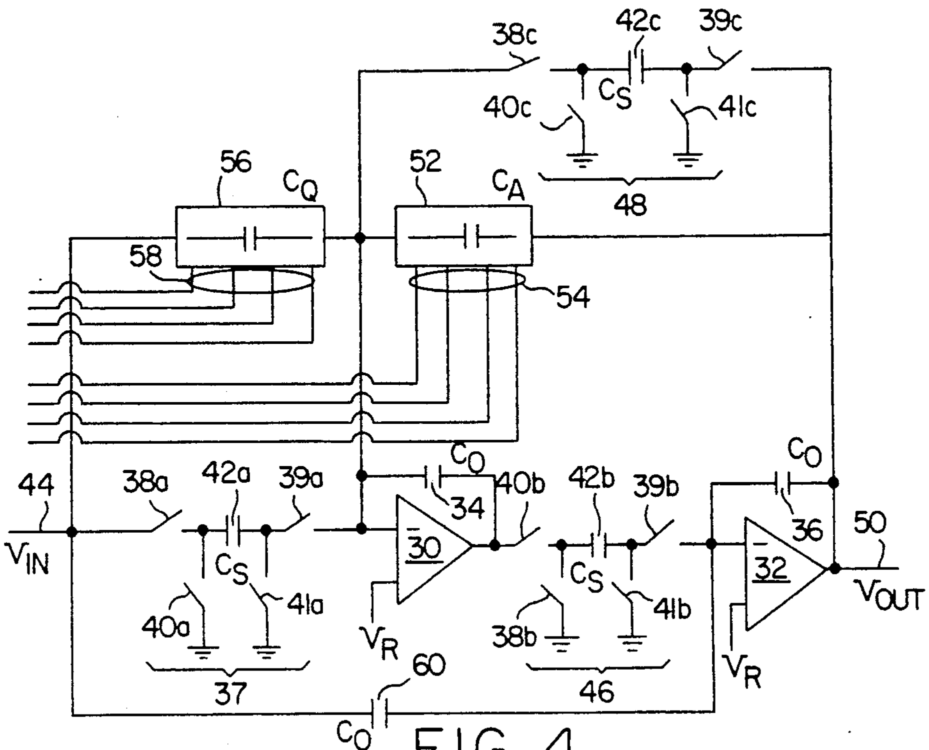


FIG. 4

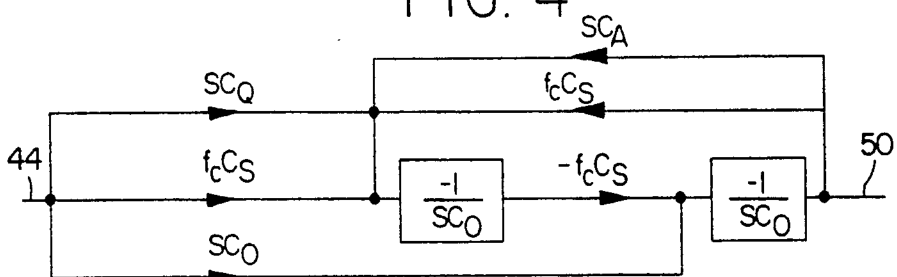


FIG. 5

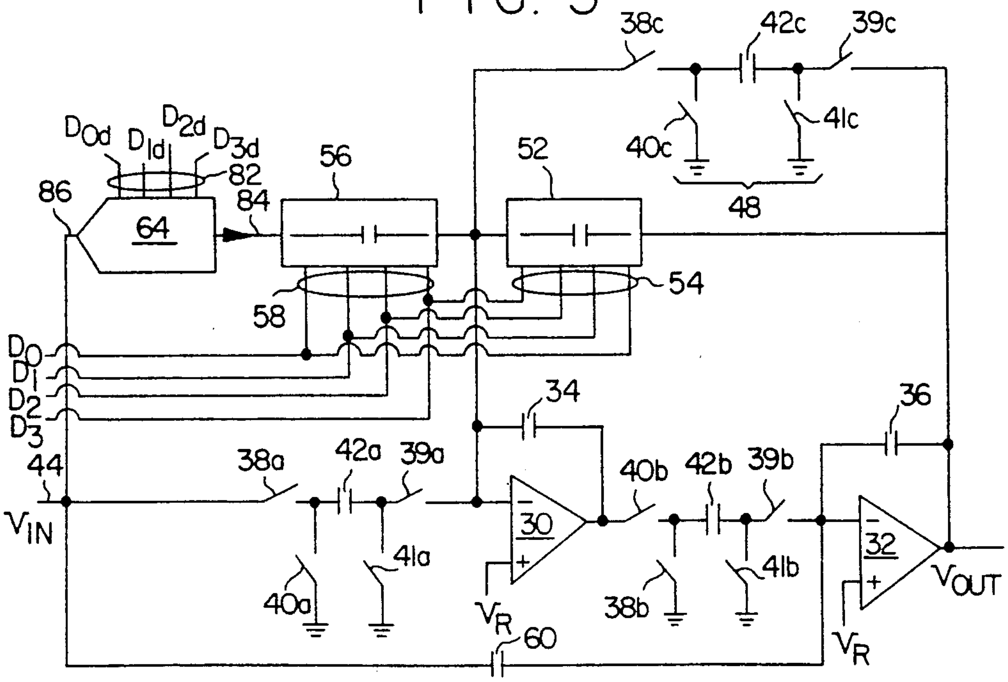


FIG. 6

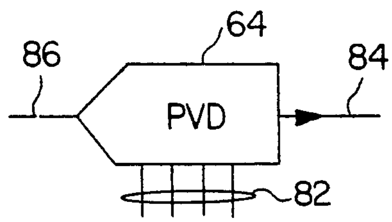


FIG. 7

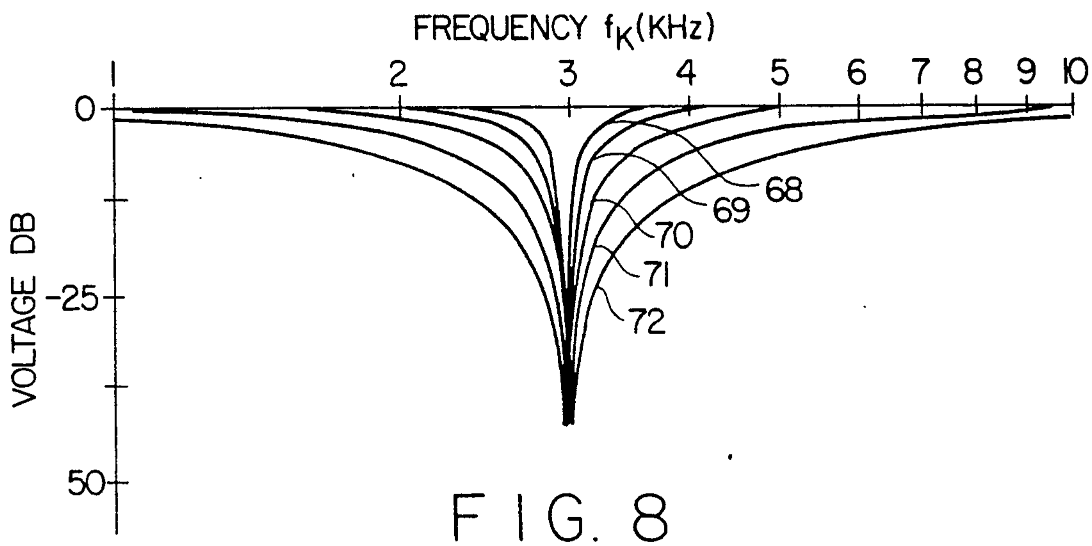


FIG. 8

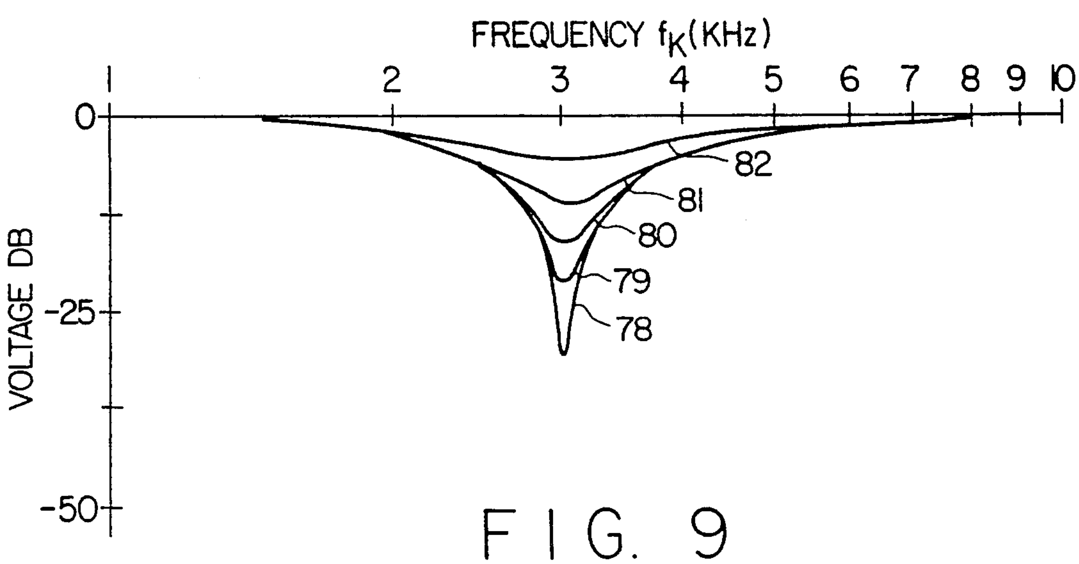


FIG. 9

SWITCHED-CAPACITOR NOTCH FILTER WITH PROGRAMMABLE NOTCH WIDTH AND DEPTH

BACKGROUND

This invention relates to an active notch filter circuit employing switched-capacitor resistors and more particularly to such filter circuits that include simultaneously-digitally-programmable capacitor arrays for controlling notch width and notch depth.

Notch filters are used in analog-signal manipulating circuits for rejecting a particular signal frequency, or narrow range of frequencies. Conventional notch filters have a center or primary rejection frequency w, and a quality factor Q, which when high corresponds to a narrow filter bandwidth and when low corresponds to a relatively wide bandwidth. A high and low Q value also corresponds respectively to a narrow notch and a wide notch, as is further explained below. The transfer function of the conventional notch filter is expressed as

$$\frac{Vout}{Vin} = \frac{S^2 + w^2}{S^2 + \frac{w}{Q} S + w^2}.$$

Notch filters of this kind are described by Alan B. Grebene in his book Bipolar And MOS Analog Integrated Circuit Design, 1984, pages 736–739.

Notch width and notch depth are typically established by the filter manufacturer and are not controllable by the filter user.

It is an object of this invention to provide a notch filter circuit that is programmable with respect to notch width and depth.

It is a further object of this invention to provide such a filter wherein notch width and notch depth are independently programmable by the user.

SUMMARY OF THE INVENTION

A programmable notch filter includes first and second tandem connected operational amplifiers, each with a capacitor connected output to input across it. The tandem connection is effected by one switched-capacitor resistor between the output of the first amplifier to the input of the second. Another switched-capacitor resistor is connected between the notch filter input and the input of the first amplifier. The filter output is the output of the second amplifier. Yet another switched capacitor resistor is connected between the notch filter output and the input of the first amplifier. A feed forward capacitor is connected between the input of the notch filter and the input of the second amplifier.

A notch-width programming circuit consists of a circuit branch, that includes a first digitally-programmable capacitor array, which array has a first group of digital programming terminals and which array is connected in parallel with the yet another switched-capacitor resistor for determining the capacitance of the first array, and thus the notch width, in response to a digital programming signal that may be applied to the first group of digital programming terminals.

A notch-depth programming circuit consists of a circuit branch, that includes a second digitally-programmable capacitor array, which array has a second group of digital programming terminals and which array is connected in parallel with the another switched-capacitor resistor. This second digitally-programmable capacitor array is for determining notch depth, in response to a digital programming signal that may be applied to the second group of digital programming terminals.

In another aspect of this invention, the first and second groups of digital terminals of the capacitor arrays are connected to each other; and a digitally programmable voltage divider circuit, has a third group of digital programming terminals, is connected in the notch-depth circuit branch, has an input connected to the notch filter input, and has an output connected to the second capacitor array for determining the divider ratio of the programmable voltage divider and thus the notch depth without affecting the notch width, in response to a digital programming signal that may be applied to the third group of digital programming terminals.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. **1** shows a circuit diagram of a digitally programmable capacitor array suitable for use in a notch filter circuit of this invention.

FIG. **2** shows a block-diagram representation of the capacitor array of FIG. **1**.

FIG. **3** shows a circuit diagram of a switched capacitor resistor.

FIG. **4** shows a first preferred embodiment of a notch filter circuit of this invention.

FIG. **5** shows a current flow diagram corresponding to the circuit of FIG. **4**.

FIG. **6** shows a second preferred embodiment of a notch filter circuit of this invention.

FIG. **7** shows a block diagram of a reverse-connected DAC for use as a digitally controlled voltage divider.

FIG. **8** shows, for different values of the programmable capacitance ratio Co/C_Q, plots of the transfer function Vout/Vin, or "gain", as a function of the frequency f_k of the input signal, for the circuit of FIG. **5**.

FIG. **9** shows, for different values of the programmable voltage divider ratio, A, a plot of the transfer function Vout/Vin, or "gain", as a function of the frequency f_k of the input signal, for the circuit of FIG. **5**.

DESCRIPTION OF THE PREFERRED EMBODIMENTS

A digitally programmable capacitor array **10** in FIG. **1** is binary weighted, i.e. all of the capacitors **12** have the same capacitance value, C, and they are connected in binary groups of **1**, **2**, **4**, etc. Electrically programmable switches **14**, **15**, **16** and **17** determine which groups of capacitors **12** contribute to the capacitance C_A of the array **10** as measured between terminals **18** and **19**.

The digital-signal-activated switches **14**, **15**, **16** and **17** are preferably implemented as MOS transistors (not shown). A switch to which a binary zero is applied opens, and a switch to which a binary **1** is applied closes to connect the switch-associated group of capacitors **12** between terminals **18** and terminal **19**. Thus for example, when the digital programming signal is 1/0/0/1, only switches **14** and **17** contribute to the array capacitance C_A which is illustrated in the block diagram of FIG. **2**. The corresponding decimal number is $N = D0 + 2D1 + 4D2 + 8D3 = 1 \cdot 1 + 2.0 + 4.0 + 8.1 = \mathbf{9}$. Thus $C_A = (D0 + 2D1 + 4D2 + 8D3)C$, or $C_A = MC$, wherein M is the decimal number corresponding to the digital programming signal that sets the switches **14** through **17**.

For greater simplicity and clarity of presentation, the number of programming bits shown in the drawing, m,

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