SOCIETY FOR INFORMATION DISPLAY

SID

APPLICATIONS NOTES

MAY 19-21, 1992
TUESDAY-THURSDAY
SHERATON BOSTON HOTEL
BOSTON, MASSACHUSETTS

21.3: Fault Identification on TFT-LCD Substrates Using Transfer Admittance Measurement

H. Hall

GenRad, Inc., Concord, MA

Abstract

Identifying faults as to type on TFT-LCD substrates is necessary to determine if they can be repaired and to provide information to improve product quality. Fast fault detection and determining fault type require different test strategies. Transfer admittance measuring techniques can be used effectively for both purposes.

Introduction

The primary reason manufacturers need to test TFT-LCD panels at the substrate level is to avoid putting more value into bad substrates which eventually will have to be scrapped after final visual tests. A second reason is to find faults so that bad panels can be repaired, thus saving the value already put into them. Many types of faults can be repaired, but not all. Moreover, of those that can be repaired, different types of faults are repaired by different processes. Thus identification of faults is necessary for repair and for the savings that it can provide. Still another important reason for testing is to improve the manufacturing processes. This also requires fault identification in order to determine what the problem is. This could give the biggest savings of all.

This paper examines the capability of an electrical test procedure for identifying faults as well as detecting and locating them.

Review of the Test Method

The method discussed is the so-called "Transfer Admittance Method" [1] that applies voltages to the gate (or control) lines, and to the storage capacitor network, "Cs Bus", (if there is one), and detects currents on drain (data) lines (see figure 1).

In the preferred configuration, all gate and drain lines are probed to allow good guarding and many detectors are used simultaneously to get good test throughput. The system measures the complex admittance, output current divided by input voltage, and separates this into conductance and capacitance. A dc voltage is also applied to the active gate line to turn the TFTs in that row both on and off and measurements are made under both conditions. The differences between these two capacitance and two conductance

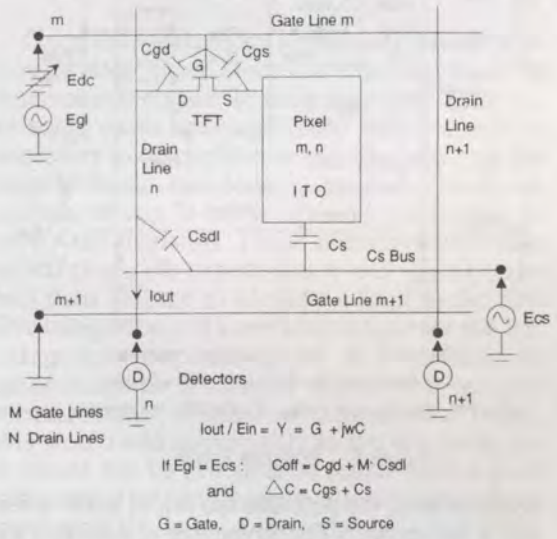

Figure 1 Test Method

measurements, Δ C and Δ G, are calculated because they provide the most sensitive means of detection and identification of most fault types.

If a protective guard ring is present, this method requires that the resistances between the line test pads and the guard ring be high enough to allow the application of the dc voltage necessary to turn the TFTs on and to allow the detection of the output currents without excessive attenuation and noise. If this requirement is considered at the design stage, these resistances can be made high enough for good "testability" without impairing the ability of the guard ring to protect the substrate from damage from electrostatic voltages. The method puts no restrictions on the active area of the substrate and makes no contact to this area.

Types of faults

There are a wide variety of possible faults as shown in figure 2. Any line can be open and any two points can be shorted together. The circuit in this diagram has a separate Cs bus. There are fewer types of faults on substrates in which the storage capacitors are connected to the adjacent gate line (m+1) or which have no added Cs capacitor at all. This figure also shows the shorthand nomenclature used to name the faults. Note that we call the TFT

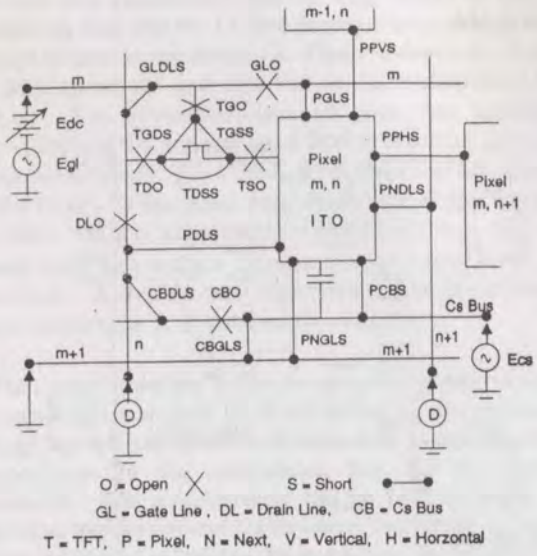

Figure 2 Possible Faults

connection to the data line the drain, while some call it the source. (The advantage of calling it the drain is that the "D" can represent both data and drain).

Most "hard" faults, true opens or shorts, are easily detected and located. All of the hard faults have "soft" versions; opens that are not quite open, and, more common, high resistance shorts due to leakage resistance. The most important of these is leakage across the storage capacitor and from the pixel to gate line because these affect the ability of Cs to hold a charge. Other soft faults are low TFT "on" conductance (or a "weak" TFT) and high TFT "off" conductance (a "leaky" TFT). The ability to detect soft faults depends on how small their effect is and on the sensitivity of the system. The latter is limited by noise and can be improved by taking more time to make the measurements.

Many substrates use parallel TFTs for redundancy. A short in either TFT is a hard fault, but an open in one has a small effect and perhaps should not be called a fault at all. However, we can usually detect an open in one TFT and can often determine whether the open is in the gate, drain or source by measuring the effective Cgs (gate-source) capacitance.

Means of detection

All faults affect either Δ C or Δ G so that these measured values are tested against limits. To do this we have to know the normal values and assign limits which we want to be as tight as possible to help catch soft faults. Even though the Δ C and Δ G values are quite constant over the panel area, they can vary because of attenuation and phase shift along the gate and drain lines. Thus a local normal value must be determined if tight limits are to be set. One way to do this is to measure a block of pixels, exclude bad pixels that exceed broad limits and average the values of the remaining ones.

Detection requires good precision, but not high accuracy because, for testing, we are looking for differences between pixels, not actual pixel parameter values. The detectors must have equal sensitivities so that equal pixels on different drain lines will not give different measurements. Each detector has a precision conductance standard and these are used for calibration before each substrate is measured. Moreover, these standards can be calibrated easily with an external test fixture.

Detection is optimized by choosing the test conditions. For sensitive detection of capacitance values we want a high frequency to increase the output current because the capacitive current is proportional to frequency (Iout = Ein2πfC). However, too high a frequency will result in large phase shifts that will give conductance errors proportional to capacitance and visa versa. Generally testing is done at a higher frequency than that used for measurements which require absolute accuracy .

The ac level should be as high as possible to improve the signal to noise ratio. However, if it is large, the dc bias voltages, both positive and negative, must be large enough to prevent the large ac from turning the TFTs on or off or from causing excess distortion. The dc bias should be high enough to turn the TFTs on, but not so full on that even weak TFTs conduct so well that they can't be detected. Ac and dc voltages and frequency are programmable so that their values may be optimized for a specific substrate type.

Methods of Fault Identification

The system stores the location of faults that are detected by the foot screening test discussed above, but it does not store the test date. Therefore, the first step of fault identification is to repeat the measurements of each failed pixel.

No pass/fail test is made, instead the new data for each pixel are subjected to a series of tests that categorize those hard faults whose characteristics are easily detected. This is very fast because these tests are just numerical comparisons. Their order is important (see categories 1 to 5 in Table 1). The first tests are for gross shorts (large Goff and Δ G) because these can overload the detector giving meaningless Δ C values which would cause erroneous diagnostic decisions. These are followed by several tests of Δ C with the most easily detected faults first to reduce the possibility of erroneous classification.

Table 1
Simplified Identification Program (Preliminary)
when have Cs Bus and Redundant TFTs

```
1.  IF Goff Very High MEASURE Goff with Ecs = 0
      IF Goff high: GLDS or TGDS (in parallel)
      IF NOT: CBDLS
2.  IF Δ G Very High MEASURE Δ G with Ecs = 0
      IF Δ G high: TGSS or PGLS (in parallel)
      IF NOT: PCBS (Cs shorted)
3.  IF Δ C ~ 0 MEASURE Δ C of pixel to right.
      IF Δ C = 0: Possible GLO
            VERIFY by testing more pixels.
      IF NOT MEASURE Δ C of adjacent up or down.
            IF Δ C = 0: Possible DLO
                  VERIFY by measuring more pixels.
            IF NOT MEASURE with ac on Next Gate Line.
                  IF Δ G high: PNGL
                  IF NOT MEASURE Coff above and below.
                        IF Coff high: TDSS or PDLS (parallel)
                        IF NOT MEASURE Coff right and left.
                              IF Coff high: PNDLS.
                              IF NOT TDO or TGO (both TFTs open)
4.  IF Δ C ~ Cgs MEASURE Δ C left & right.
      IF Δ C ~ Cgs for both: CBO
      IF NOT: TSO (both TFTs open)
5.  IF Δ C High MEASURE Δ C above & below
      IF Δ C either high: PPVS

    [[Measure Pixel N Times and Average]]

6.  IF Δ Slightly Low Test Δ C Gs (series value)
      IF Δ Cs Low MEASURE Δ C with Ecs = 0
            IF Δ C high: RTDO (R = redundant)
            IF Δ C Normal: RTSO or WkTFT (Wk = weak)
            IF Δ C Low: MEASURE Goff
                  IF Goff high: TDSLk (Lk = leakage)
                  IF NOT: RTGO
      IF Δ Gs NOT low MEASURE Δ C left & right
            IF Δ C low: CBGLS
                  VERIFY by Measuring Δ C along gate line
            IF NOT: possible PPHS, continue program
7.  IF Δ G High MEASURE Δ G with Ecs = 0
      IF Δ G low: PCBLk (cs has leakage)
      IF NOT: TGSLk or PGLLk (parallel leakage)
8.  IF Goff High MEASURE Goff with Ecs = 0
      IF Goff High: GLDLLk, TGDLk or TDSLk
      IF NOT: CBDLk
```

The pixels that pass these first tests are those with soft faults, or with hard faults that are difficult to detect, and good pixels that failed the initial pass/fail test because of measurement imprecision. More precision is needed to separate out the good pixels and to identify the faults of the bad. Therefore the next step is to repeat the measurements several times and average the results, with the number of averaged can be chosen to optimize the trade-off between accuracy and speed. This improved data is then used to test for the final categories of faults.

Once categorized to a group of faults with similar data, more electrical tests are made to determine the specific fault type (see Table 1). In some cases only one more measurement is necessary to determine the specific fault type but usually more than one is needed. Often, an additional test is made after identification to verify the decision. These measurements take added time. We expect that it will usually take less than 100 ms to identify a fault in the first five categories and somewhat longer for the last categories depending on the number of measurements averaged (about 10 ms per measurement). If there are thousands of faults, this would add appreciably to the test time, but it would not be practical to repair such a poor substrate. The test program allows a maximum number of faults to be set and testing is aborted if this number is exceeded.

The type and location of all faults is stored and can be printed out or sent to a remote computer. This is necessary for the repair operation. The number of occurrences of each fault type is also listed for quality control purposes.

Some of the special tests made are listed below and in the test program of Table 1.

- Testing with one ac source removed.

Several categories use a test with ac only on the gate line because it distinguishes between shorts or leakage resistances to the gate line and those to the Cs bus. Thus this test is used when Goff or Δ G is high. Testing with ac only on the Cs bus would also distinguish between these faults and this test could be used for verification.

Testing with ac only on the gate line gives a better measurement of Cgs because Δ C = Cgs in this case, not Cgs + Cs. Thus, we want to use this test when we want to measure Cgs accurately to locate an open in a redundant TFT.

- Testing for Δ C = 0 in Adjacent Pixels

Testing the adjacent pixels, above, below, left and right, can distinguish line opens from

single pixel faults. If Δ C = 0, the cause could be a open gate or drain line (GLO or DLO), but if the pixels above and below are normal it can't be a DLO and if those to both sides are normal it can't be a GLO. However, if Δ C for an adjacent pixel does equal zero, it does not prove that there is an open because that could be the result of some other type of fault. A line open should be verified by testing more pixels along the line in question.

- Testing Coff along Drain Lines.

The cause of a Δ C = 0 measurement could also be a TFT D-S short (TDSS or PDLS). This will also make Coff high for this pixel (by Δ C) and for all pixels along its drain line. Testing Coff for the pixel measured should identify this fault and testing pixels above and below for a high Coff can verify it. Similarly a short from the pixel to the next drain line (PNDLS) will cause a very low Δ C but will cause a high Coff for all measurements on the next drain line (n+1).

- Applying a Signal to the Next Gate line

A very low Δ C can be the result of a short from the pixel to the next gate line (PNGLS). This can be easily found by applying a signal (ac only) to that gate line which will give a large Δ G if that fault is present. This is a test connection normally only used in testing substrates that have the Cs tied to the next gate line.

- Testing Equivalent Series Δ G

An unusual test is made to find weak TFTs or an open TFT in parallel with a good one. In this case we want to determine abnormally low TFT "on" conductance. The TFT conductance is in series with the capacitance Cs + Cgs which is the normal Δ C capacitance if the TFT is fully on. If low, this TFT conductance makes Δ C slightly low and Δ G slightly high. This combination can be difficult to recognize because both conditions are caused by other types of faults. Converting to equivalent series conductance, Δ Gs, makes this fault much more apparent.

The Δ G and Δ C normally measured are equivalent parallel quantities being obtained from the real and imaginary parts of admittance. If we convert them into equivalent series quantities we should measure the TFT conductance and the normal Δ C which are series [2]. This works well and the abnormal series value, Δ Gs, of a weak TFT is markedly lower than that for a good pixel particularly if the effect is exaggerated by reducing the dc bias voltage.

- Testing at a Lower Frequency

Soft faults due to leakage resistance give slightly high Goff or Δ G values. These high resistance values can be measured more accurately using a lower frequency to reduce phase shift errors. However, absolute accuracy is not required for identification of these faults if the measured values of normal pixels are known, and testing at the a lower frequency usually does not improve precision.

Summary

A procedure for identifying faults on TFT-LCD substrates has been outlined that determines the type of any specific fault from a larger number of possible fault types. This first categorizes the fault into one of several groups by testing the measurement data against various limits. Then, depending on this initial classification, more measurements of different types are made that lead to an exact diagnoses in most cases. The order of these tests and measurements is important in optimizing the accuracy of identification and reducing the time required.

This fault identification capability should be very valuable to substrate manufacturers because it allows them to decide if a fault can be repaired and aids in improving their fabrication process.

References:

1. Hall, H.P. and Pilotte, P.R.
"Testing TFT-LCD Substrates with a Transfer Admittance Method"
Paper 32.6, S.I.D. '91 Digest of Papers

2. Pilotte, P.R.
"Modeling and Characterization of TFT-LCDs Using a Transfer Admittance
Method" Paper 21.2, S.I.D. '92 Digest of Papers