CUSTOMER NO.	38327

CONTINUATION/DIVISIONAL APPLICATION TRANSMITTAL

(Rule 53(b) Continuation or Divisional) ☐ DUPLICATE

Address to: **Commissioner of Patents**
P.O. Box 1450
Alexandria, VA 22313-1450

Attorney Docket No.:	HARU-0126
First Named Inventor:	Nakayoshi
Total Pages:	126

This requests a ☒ Continuation or ☐ Divisional application under 37 CFR §1.53(b) of prior application:

Application. No.:	14/942,120	Group Art Unit:	2871
Filed on:	November 16, 2015	Examiner:	Lucy P. Chen
Entitled:	LIQUID CRYSTAL DISPLAY DEVICE, DISPLAY DEVICE AND MANUFACTURING METHOD THEREOF		

☒ 1. The entire disclosure of the pending, prior application is hereby incorporated by reference.

☐ 2. Submitted herewith is a copy of the complete prior application as filed.

☐ 3. This application is filed by fewer than all the inventors named in the prior nonprovisional application, 37 CFR 1.53(b)(1). **DELETE** the following inventor(s): _____.

☒ 4. Submitted herewith is a copy of the signed Oath/Declaration from the prior application.

☐ 5. Small entity status was established in the prior application, and is still proper and desired.

☐ 6. A _____ month Petition for Extension of Time is filed concurrently in the prior application.

☒ 7. The Commissioner is authorized to credit any overpayment and charge any deficiency in any fees required under 37 CFR § 1.16 and/or 1.17 to Deposit Account No. 60-0155.

☒ 8. The amount of $1,600.00 for filing fee is being submitted herewith via the EFS payment system.

☒ 9. The prior application is assigned of record to: Japan Display Inc. and Panasonic Liquid Crystal Display Co., Ltd.

☒ 10. Priority is claimed based on U.S. App. No. 14/942,120 filed November 16, 2015, which claims priority to U.S. App. No. 14/708,348 filed May 11, 2015, which claims priority to U.S. App No. 14/285,006 filed May 22, 2014, which claims priority of U.S. App. No. 13/927,539 filed June 26, 2013, which claims priority of U.S. App. No. 13/650,203 filed October 12, 2012, which claims priority of U.S. App. No. 13/364,092 filed February 1, 2012, which claims priority of U.S. Appl. No. 12/926,735 filed December 7, 2010, which claims priority of U.S. App. No. 12/292,728 filed November 25, 2008, which claims priority of U.S. App. No. 11/976,884 filed October 29, 2007, which claims priority of U.S. App. No. 11/409,076 filed on April 24, 2006, which claims priority to U.S. App. No. 11/211,574 filed Aug. 26, 2005, which claims priority to U.S. App. No. 10/237,911 filed Sep. 10, 2002, which claims priority to Japanese Patent Application No. 2001-317147 filed on Oct. 15, 2001, and which is hereby incorporated by reference.

☐ 11. A Preliminary Amendment is enclosed.

☒ 12. Other: Information Disclosure Statement with Form PTO-1449.

THE FILING FEE IS CALCULATED AS FOLLOWS:				BASIC FEE (FILING, EXAMINATION & SEARCH FEES):	$1,600.00
Total Claims:	13	-20 =	0	× $80 =	
Independent claims:	1	-3 =	0	× $420 =	
				Multiple Dependent Claim (Add $780.00):	
			Total Pages	126 (# × .75 – 100 = extra 50s =) × 400	0.00
				Subtotal:	1,600.00
				Reduction if Small Entity Status:	0.00
				Total:	1,600.00

Marquez IP Law Office, PLLC
1629 K Street, NW, Suite 300
Washington, DC 20006
Tel. No. 202-349-1690
Fax No. 202-754-9829
Customer No. 38327

Date:	Name:	Signature:	Reg. No.
September 21, 2016	Juan Carlos A. Marquez	***/juan.carlos.a.marquez/***	34,072

PTO/AIA/14 (11-15)
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Application Data Sheet 37 CFR 1.76	Attorney Docket Number	HARU-0126
	Application Number	
Title of Invention	LIQUID CRYSTAL DISPLAY DEVICE, DISPLAY DEVICE AND MANUFACTURING METHOD THEREOF	

The application data sheet is part of the provisional or nonprovisional application for which it is being submitted. The following form contains the bibliographic data arranged in a format specified by the United States Patent and Trademark Office as outlined in 37 CFR 1.76.
This document may be completed electronically and submitted to the Office in electronic format using the Electronic Filing System (EFS) or the document may be printed and included in a paper filed application.

Secrecy Order 37 CFR 5.2:

☐ Portions or all of the application associated with this Application Data Sheet may fall under a Secrecy Order pursuant to 37 CFR 5.2 (Paper filers only. Applications that fall under Secrecy Order may not be filed electronically.)

Inventor Information:

Inventor 1 Remove

Legal Name

Prefix	Given Name	Middle Name	Family Name	Suffix
	Yoshiaki		NAKAYOSHI	

Residence Information (Select One) US Residency ● Non US Residency Active US Military Service

City	Country of Residence [i]
Ooamishirasato	JP

Mailing Address of Inventor:

Address 1	c/o Japan Display Inc.
Address 2	3-7-1, Nishi-Shinbashi, Minato-ku
City	Tokyo
State/Province	
Postal Code	105-003
Country [i]	JP

Inventor 2 Remove

Legal Name

Prefix	Given Name	Middle Name	Family Name	Suffix
	Kazuhiko		YANAGAWA	

Residence Information (Select One) ● US Residency ◯ Non US Residency Active US Military Service

City	State/Province	Country of Residence [i]
Mobara		JP

Mailing Address of Inventor:

Address 1	c/o Japan Display Inc.
Address 2	3-7-1, Nishi-Shinbashi, Minato-ku
City	Tokyo
State/Province	
Postal Code	105-003
Country [i]	JP

All Inventors Must Be Listed - Additional Inventor Information blocks may be generated within this form by selecting the **Add** button. Add

Correspondence Information:

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Application Data Sheet 37 CFR 1.76	Attorney Docket Number	HARU-0126
	Application Number	
Title of Invention	LIQUID CRYSTAL DISPLAY DEVICE, DISPLAY DEVICE AND MANUFACTURING METHOD THEREOF	

Enter either Customer Number or complete the Correspondence Information section below.
For further information see 37 CFR 1.33(a).

☐ **An Address is being provided for the correspondence Information of this application.**

Customer Number	38327		
Email Address	juancarlos@marqueziplaw.com	Add Email	Remove Email

Application Information:

Title of the Invention	LIQUID CRYSTAL DISPLAY DEVICE, DISPLAY DEVICE AND MANUFACTURING METHOD THEREOF		
Attorney Docket Number	HARU-0126	**Small Entity Status Claimed**	☐
Application Type	Nonprovisional		
Subject Matter	Utility		
Total Number of Drawing Sheets (if any)	63	**Suggested Figure for Publication (if any)**	

Filing By Reference:

Only complete this section when filing an application by reference under 35 U.S.C. 111(c) and 37 CFR 1.57(a). Do not complete this section if application papers including a specification and any drawings are being filed. Any domestic benefit or foreign priority information must be provided in the appropriate section(s) below (i.e., "Domestic Benefit/National Stage Information" and "Foreign Priority Information").

For the purposes of a filing date under 37 CFR 1.53(b), the description and any drawings of the present application are replaced by this reference to the previously filed application, subject to conditions and requirements of 37 CFR 1.57(a).

Application number of the previously filed application	Filing date (YYYY-MM-DD)	Intellectual Property Authority or Country

Publication Information:

☐ Request Early Publication (Fee required at time of Request 37 CFR 1.219)

☐ **Request Not to Publish.** I hereby request that the attached application not be published under 35 U.S.C. 122(b) and certify that the invention disclosed in the attached application **has not and will not** be the subject of an application filed in another country, or under a multilateral international agreement, that requires publication at eighteen months after filing.

Representative Information:

Representative information should be provided for all practitioners having a power of attorney in the application. Providing this information in the Application Data Sheet does not constitute a power of attorney in the application (see 37 CFR 1.32).
Either enter Customer Number or complete the Representative Name section below. If both sections are completed the customer Number will be used for the Representative Information during processing.

Please Select One:	● Customer Number	US Patent Practitioner	○ Limited Recognition (37 CFR 11.9)
Customer Number	38327		

Application Data Sheet 37 CFR 1.76	Attorney Docket Number	HARU-0126
	Application Number	
Title of Invention	LIQUID CRYSTAL DISPLAY DEVICE, DISPLAY DEVICE AND MANUFACTURING METHOD THEREOF	

Domestic Benefit/National Stage Information:

This section allows for the applicant to either claim benefit under 35 U.S.C. 119(e), 120, 121, 365(c), or 386(c) or indicate National Stage entry from a PCT application. Providing benefit claim information in the Application Data Sheet constitutes the specific reference required by 35 U.S.C. 119(e) or 120, and 37 CFR 1.78.
When referring to the current application, please leave the "Application Number" field blank.

Prior Application Status	Pending				Remove
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)		
	Continuation of	14942120	2015-11-16		
Prior Application Status	Patented				Remove
Application Number	Continuity Type	Prior Application Number	Filing Date (YYYY-MM-DD)	Patent Number	Issue Date (YYYY-MM-DD)
14942120	Continuation of	14708348	2015-05-11	9213204	2015-12-15
Prior Application Status	Patented				Remove
Application Number	Continuity Type	Prior Application Number	Filing Date (YYYY-MM-DD)	Patent Number	Issue Date (YYYY-MM-DD)
14708348	Continuation of	14285006	2014-05-22	9086600	2015-07-21
Prior Application Status	Patented				Remove
Application Number	Continuity Type	Prior Application Number	Filing Date (YYYY-MM-DD)	Patent Number	Issue Date (YYYY-MM-DD)
14285006	Continuation of	13927539	2013-06-26	8760609	2014-06-24
Prior Application Status	Patented				Remove
Application Number	Continuity Type	Prior Application Number	Filing Date (YYYY-MM-DD)	Patent Number	Issue Date (YYYY-MM-DD)
13927539	Continuation of	13650203	2012-10-12	8493522	2013-07-23
Prior Application Status	Patented				Remove
Application Number	Continuity Type	Prior Application Number	Filing Date (YYYY-MM-DD)	Patent Number	Issue Date (YYYY-MM-DD)
13650203	Continuation of	13364092	2012-02-01	8310641	2012-11-13
Prior Application Status	Patented				Remove
Application Number	Continuity Type	Prior Application Number	Filing Date (YYYY-MM-DD)	Patent Number	Issue Date (YYYY-MM-DD)
13364092	Continuation of	12926735	2010-12-07	8248549	2012-08-21
Prior Application Status	Patented				Remove
Application Number	Continuity Type	Prior Application Number	Filing Date (YYYY-MM-DD)	Patent Number	Issue Date (YYYY-MM-DD)
12926735	Continuation of	12292728	2008-11-25	7872696	2011-01-18

Application Data Sheet 37 CFR 1.76	Attorney Docket Number	HARU-0126
	Application Number	
Title of Invention	LIQUID CRYSTAL DISPLAY DEVICE, DISPLAY DEVICE AND MANUFACTURING METHOD THEREOF	

Prior Application Status	Patented				Remove
Application Number	Continuity Type	Prior Application Number	Filing Date (YYYY-MM-DD)	Patent Number	Issue Date (YYYY-MM-DD)
12292728	Division of	11976884	2007-10-29	7605876	2009-10-20
Prior Application Status	Patented				Remove
Application Number	Continuity Type	Prior Application Number	Filing Date (YYYY-MM-DD)	Patent Number	Issue Date (YYYY-MM-DD)
11976884	Division of	11409076	2006-04-24	7307673	2007-12-11
Prior Application Status	Patented				Remove
Application Number	Continuity Type	Prior Application Number	Filing Date (YYYY-MM-DD)	Patent Number	Issue Date (YYYY-MM-DD)
11409076	Division of	11211574	2005-08-26	7423701	2008-09-09
Prior Application Status	Patented				Remove
Application Number	Continuity Type	Prior Application Number	Filing Date (YYYY-MM-DD)	Patent Number	Issue Date (YYYY-MM-DD)
11211574	Division of	10237911	2002-09-10	6970222	2005-11-29

Additional Domestic Benefit/National Stage Data may be generated within this form by selecting the **Add** button. Add

Foreign Priority Information:

This section allows for the applicant to claim priority to a foreign application. Providing this information in the application data sheet constitutes the claim for priority as required by 35 U.S.C. 119(b) and 37 CFR 1.55. When priority is claimed to a foreign application that is eligible for retrieval under the priority document exchange program (PDX)[i] the information will be used by the Office to automatically attempt retrieval pursuant to 37 CFR 1.55(i)(1) and (2). Under the PDX program, applicant bears the ultimate responsibility for ensuring that a copy of the foreign application is received by the Office from the participating foreign intellectual property office, or a certified copy of the foreign priority application is filed, within the time period specified in 37 CFR 1.55(g)(1).

Remove

Application Number	Country[i]	Filing Date (YYYY-MM-DD)	Access Code[i] (if applicable)
2001-317149	JP	2001-10-15	

Additional Foreign Priority Data may be generated within this form by selecting the **Add** button. Add

Statement under 37 CFR 1.55 or 1.78 for AIA (First Inventor to File) Transition Applications

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Application Data Sheet 37 CFR 1.76	Attorney Docket Number	HARU-0126
	Application Number	
Title of Invention	LIQUID CRYSTAL DISPLAY DEVICE, DISPLAY DEVICE AND MANUFACTURING METHOD THEREOF	

☐ This application (1) claims priority to or the benefit of an application filed before March 16, 2013 and (2) also contains, or contained at any time, a claim to a claimed invention that has an effective filing date on or after March 16, 2013.
NOTE: By providing this statement under 37 CFR 1.55 or 1.78, this application, with a filing date on or after March 16, 2013, will be examined under the first inventor to file provisions of the AIA.

PTO/AIA/14 (11-15)
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Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it contains a valid OMB control number.

Application Data Sheet 37 CFR 1.76	Attorney Docket Number	HARU-0126
	Application Number	
Title of Invention	LIQUID CRYSTAL DISPLAY DEVICE, DISPLAY DEVICE AND MANUFACTURING METHOD THEREOF	

Authorization or Opt-Out of Authorization to Permit Access:

When this Application Data Sheet is properly signed and filed with the application, applicant has provided written authority to permit a participating foreign intellectual property (IP) office access to the instant application-as-filed (see paragraph A in subsection 1 below) and the European Patent Office (EPO) access to any search results from the instant application (see paragraph B in subsection 1 below).

Should applicant choose not to provide an authorization identified in subsection 1 below, applicant **must opt-out** of the authorization by checking the corresponding box A or B or both in subsection 2 below.

NOTE: This section of the Application Data Sheet is **ONLY** reviewed and processed with the **INITIAL** filing of an application. After the initial filing of an application, an Application Data Sheet cannot be used to provide or rescind authorization for access by a foreign IP office(s). Instead, Form PTO/SB/39 or PTO/SB/69 must be used as appropriate.

1. Authorization to Permit Access by a Foreign Intellectual Property Office(s)

A. Priority Document Exchange (PDX) - Unless box A in subsection 2 (opt-out of authorization) is checked, the undersigned hereby **grants the USPTO authority** to provide the European Patent Office (EPO), the Japan Patent Office (JPO), the Korean Intellectual Property Office (KIPO), the State Intellectual Property Office of the People's Republic of China (SIPO), the World Intellectual Property Organization (WIPO), and any other foreign intellectual property office participating with the USPTO in a bilateral or multilateral priority document exchange agreement in which a foreign application claiming priority to the instant patent application is filed, access to: (1) the instant patent application-as-filed and its related bibliographic data, (2) any foreign or domestic application to which priority or benefit is claimed by the instant application and its related bibliographic data, and (3) the date of filing of this Authorization. See 37 CFR 1.14(h)(1).

B. Search Results from U.S. Application to EPO - Unless box B in subsection 2 (opt-out of authorization) is checked, the undersigned hereby **grants the USPTO authority** to provide the EPO access to the bibliographic data and search results from the instant patent application when a European patent application claiming priority to the instant patent application is filed. See 37 CFR 1.14(h)(2).

The applicant is reminded that the EPO's Rule 141(1) EPC (European Patent Convention) requires applicants to submit a copy of search results from the instant application without delay in a European patent application that claims priority to the instant application.

2. Opt-Out of Authorizations to Permit Access by a Foreign Intellectual Property Office(s)

☐ A. Applicant **DOES NOT** authorize the USPTO to permit a participating foreign IP office access to the instant application-as-filed. If this box is checked, the USPTO will not be providing a participating foreign IP office with any documents and information identified in subsection 1A above.

☐ B. Applicant **DOES NOT** authorize the USPTO to transmit to the EPO any search results from the instant patent application. If this box is checked, the USPTO will not be providing the EPO with search results from the instant application.

NOTE: Once the application has published or is otherwise publicly available, the USPTO may provide access to the application in accordance with 37 CFR 1.14.

PTO/AIA/14 (11-15)
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U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE

Application Data Sheet 37 CFR 1.76	Attorney Docket Number	HARU-0126
	Application Number	
Title of Invention	LIQUID CRYSTAL DISPLAY DEVICE, DISPLAY DEVICE AND MANUFACTURING METHOD THEREOF	

Applicant Information:

Providing assignment information in this section does not substitute for compliance with any requirement of part 3 of Title 37 of CFR to have an assignment recorded by the Office.

Applicant 1 — Remove

If the applicant is the inventor (or the remaining joint inventor or inventors under 37 CFR 1.45), this section should not be completed. The information to be provided in this section is the name and address of the legal representative who is the applicant under 37 CFR 1.43; or the name and address of the assignee, person to whom the inventor is under an obligation to assign the invention, or person who otherwise shows sufficient proprietary interest in the matter who is the applicant under 37 CFR 1.46. If the applicant is an applicant under 37 CFR 1.46 (assignee, person to whom the inventor is obligated to assign, or person who otherwise shows sufficient proprietary interest) together with one or more joint inventors, then the joint inventor or inventors who are also the applicant should be identified in this section.

Clear

● Assignee	Legal Representative under 35 U.S.C. 117	Joint Inventor
Person to whom the inventor is obligated to assign.	Person who shows sufficient proprietary interest	

If applicant is the legal representative, indicate the authority to file the patent application, the inventor is:

Name of the Deceased or Legally Incapacitated Inventor:

If the Applicant is an Organization check here. ☒

Organization Name	Japan Display Inc.

Mailing Address Information For Applicant:

Address 1	8-7-1, Nishi-Shinbashi, Minato-ku		
Address 2			
City	Tokyo	**State/Province**	
Country	JP	Postal Code	105-003
Phone Number		Fax Number	
Email Address			

Additional Applicant Data may be generated within this form by selecting the Add button. Add

PTO/AIA/14 (11-15)
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Application Data Sheet 37 CFR 1.76	Attorney Docket Number	HARU-0126
	Application Number	
Title of Invention	LIQUID CRYSTAL DISPLAY DEVICE, DISPLAY DEVICE AND MANUFACTURING METHOD THEREOF	

Applicant 2 — Remove

If the applicant is the inventor (or the remaining joint inventor or inventors under 37 CFR 1.45), this section should not be completed. The information to be provided in this section is the name and address of the legal representative who is the applicant under 37 CFR 1.43; or the name and address of the assignee, person to whom the inventor is under an obligation to assign the invention, or person who otherwise shows sufficient proprietary interest in the matter who is the applicant under 37 CFR 1.46. If the applicant is an applicant under 37 CFR 1.46 (assignee, person to whom the inventor is obligated to assign, or person who otherwise shows sufficient proprietary interest) together with one or more joint inventors, then the joint inventor or inventors who are also the applicant should be identified in this section.

Clear

◉ Assignee	Legal Representative under 35 U.S.C. 117	Joint Inventor
Person to whom the inventor is obligated to assign.	Person who shows sufficient proprietary interest	

If applicant is the legal representative, indicate the authority to file the patent application, the inventor is:

Name of the Deceased or Legally Incapacitated Inventor:

If the Applicant is an Organization check here. ☒

Organization Name	Panasonic Liquid Crystal Display Co., Ltd.		
Mailing Address Information For Applicant:			
Address 1	1-6 Megahida-cho, Shikama-ku		
Address 2	Himeji-shi		
City	Hyogo-ken	**State/Province**	
Country	JP	Postal Code	
Phone Number		Fax Number	
Email Address			

Additional Applicant Data may be generated within this form by selecting the Add button. Add

Assignee Information including Non-Applicant Assignee Information:

Providing assignment information in this section does not substitute for compliance with any requirement of part 3 of Title 37 of CFR to have an assignment recorded by the Office.

Assignee 1

Complete this section if assignee information, including non-applicant assignee information, is desired to be included on the patent application publication. An assignee-applicant identified in the "Applicant Information" section will appear on the patent application publication as an applicant. For an assignee-applicant, complete this section only if identification as an assignee is also desired on the patent application publication.

Remove

If the Assignee or Non-Applicant Assignee is an Organization check here. ☐

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Application Data Sheet 37 CFR 1.76	Attorney Docket Number	HARU-0126
	Application Number	
Title of Invention	LIQUID CRYSTAL DISPLAY DEVICE, DISPLAY DEVICE AND MANUFACTURING METHOD THEREOF	

Prefix	**Given Name**	Middle Name	**Family Name**	Suffix

Mailing Address Information For Assignee including Non-Applicant Assignee:

Address 1			
Address 2			
City		**State/Province**	
Country i		Postal Code	
Phone Number		Fax Number	
Email Address			

Additional Assignee or Non-Applicant Assignee Data may be generated within this form by selecting the Add button. Add

Signature:

Remove

NOTE: This Application Data Sheet must be signed in accordance with 37 CFR 1.33(b). **However, if this Application Data Sheet is submitted with the INITIAL filing of the application and either box A or B is not checked in subsection 2 of the "Authorization or Opt-Out of Authorization to Permit Access" section, then this form must also be signed in accordance with 37 CFR 1.14(c).**

This Application Data Sheet **must** be signed by a patent practitioner if one or more of the applicants is a **juristic entity** (e.g., corporation or association). If the applicant is two or more joint inventors, this form must be signed by a patent practitioner, **all** joint inventors who are the applicant, or one or more joint inventor-applicants who have been given power of attorney (e.g., see USPTO Form PTO/AIA/81) on behalf of **all** joint inventor-applicants.

See 37 CFR 1.4(d) for the manner of making signatures and certifications.

Signature	/juan.carlos.a.marquez/			Date (YYYY-MM-DD)	2016-09-21
First Name	Juan Carlos	Last Name	Marquez	Registration Number	34072

Additional Signature may be generated within this form by selecting the Add button. Add

This collection of information is required by 37 CFR 1.76. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 23 minutes to complete, including gathering, preparing, and submitting the completed application data sheet form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

Privacy Act Statement

The Privacy Act of 1974 (P.L. 93-579) requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1 The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C. 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether the Freedom of Information Act requires disclosure of these records.

2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.

3 A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.

4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).

5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent CooperationTreaty.

6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).

7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.

8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspections or an issued patent.

9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

LIQUID CRYSTAL DISPLAY DEVICE, DISPLAY DEVICE AND MANUFACTURING METHOD THEREOF

CROSS-REFERENCE TO RELATED APPLICATION

[0001] This application is a Continuation of U.S. App. Serial No. 14/942,120 filed November 16, 2015, which is a Continuation of U.S. App. Serial No. 14/708,348 filed May 11, 2015, which is a Continuation of U.S. App. Serial No. 14/285,006 filed May 22, 2014, which is a Continuation of U.S. App. Serial No. 13/927,539 filed June 26, 2013, which is a Continuation of U.S. App. Serial No. 13/650,203 filed October 12, 2012, which is a Continuation of U.S. App. Serial No. 13/364,092 filed February 1, 2012, which is a Continuation of U.S. App. Serial No. 12/926,735 filed December 7, 2010, which is a Continuation of U.S. App. Serial No. 12/292,728 filed November 25, 2008, which is a Divisional of U.S. App. Serial No. 11/976,884 filed October 29, 2007, which is a Divisional of U.S. App. Serial No. 11/409,076 filed April 24, 2006, which is a Divisional of U.S. App. Serial No. 11/211,574 filed Aug. 26, 2005, which is a Divisional of U.S. App. Serial No. 10/237,911 filed Sep. 10, 2002. Priority is claimed based on U.S. App, Serial No. 14/708,348 filed May 11, 2015, which claims priority of U.S. App. Serial No. 14/285,006 filed May 22, 2014, which claims priority of U.S. App. Serial No. 13/927,539 filed June 26, 2013, which claims priority of U.S. App. Serial No. 13/650,203 filed October 12, 2012, which claims priority of U.S. App. Serial No. 13/364,092 filed February 1, 2012, which claims priority of U.S. Appl. Serial No. 12/926,735 filed December 7, 2010, which claims priority of U.S. App. Serial No. 12/292,728 filed November 25, 2008, which claims priority of U.S. App. Serial No. 11/976,884 filed October 29, 2007, which claims priority of U.S. App. Serial No. 11/409,076 filed on April 24, 2006, which claims priority to U.S. App. Serial No. 11/211,574 filed Aug. 26, 2005, which claims priority to U.S. App. Serial No. 10/237,911 filed Sep. 10, 2002, which claims priority to Japanese Patent Application No. 2001-317147 filed on Oct. 15, 2001, and which is hereby incorporated by reference.

BACKGROUND OF THE INVENTION

[0002] 1. Field of the Invention

[0003] The present invention relates to a liquid crystal display device, and more particularly to an active matrix type liquid crystal display device which can reduce holding capacity for holding lighting of pixels for a given time and feeding resistance thereof thus enhancing numerical aperture.

[0004] 2. Description of the Related Art

[0005] An active matrix type liquid crystal display device generally adopts a system in which liquid crystal is sandwiched between a pair of substrates which face each other in an opposed manner and pixels are selected by pixel electrodes which are driven by a large number of switching elements represented by thin film transistors formed on one of the above-mentioned pair of

substrates. One type of the liquid crystal display device adopting such a system is a so-called vertical field type in which on the other substrate (second substrate) which faces one substrate (first substrate) of the above-mentioned pair of substrates, color filters and common electrodes are formed or the color filters are also formed on the first substrate.

[0006] As another system, there exists a so-called IPS system in which counter electrodes which correspond to the common electrodes are formed on the above-mentioned first substrate side. Also with respect to this system, there has been known a system which forms color filters on either the first substrate side or the second substrate side.

[0007] The vertical field type liquid crystal display device includes a plurality of gate lines which extend in the first direction (usually horizontal scanning direction) and are arranged parallel to each other and a plurality of drain lines which extend in the second direction which crosses the gate lines (usually vertical scanning direction) and are arranged parallel to each other. The liquid crystal display device further includes switching elements such as thin film transistors or the like in the vicinity of respective crossing portions of the gate lines and drain lines and pixel electrodes which are driven by the switching elements.

[0008] In this vertical field type liquid crystal display device, the common electrodes are formed on the second substrate such that the common electrodes face the pixel electrodes in an opposed manner, an electric field is generated between the common electrodes and the selected pixel electrodes in the direction which approximately crosses a surface of the substrate at a right angle, and lighting of the pixels is performed by changing the orientation of liquid crystal molecules sandwiched between the pixel electrode and the common electrodes.

[0009] On the other hand, in the IPS type liquid crystal display device, gate lines, drain lines, and switching elements similar to those of the vertical field type liquid crystal display device are formed on an inner surface of the above-mentioned first substrate, comb-shaped pixel electrodes are formed on the same substrate, and counter electrodes are formed close to the pixel electrodes on the same substrate. Then, an electric field is generated between the selected pixel electrodes and the counter electrodes in the direction approximately parallel to a surface of the substrate, and lighting of the pixels is performed by changing the orientation direction of liquid crystal molecules arranged between the pixel electrodes and the counter electrodes. As a liquid crystal display device which has developed this type, there exists a liquid crystal display device which adopts a matted electrode as the counter electrodes and forms comb-shaped pixel electrodes as a layer above or below the counter electrodes.

[0010] In both of the above-mentioned type liquid crystal display devices, the charge storing capacity for holding the lighting time of `the pixels which are lit due to selection at a given value (hereinafter, simply referred to as "holding capacity") is formed in regions where the pixel electrodes and the gate lines are overlapped or regions where other electrode lines which are formed such that the other electrode lines transverse the pixel electrode forming region and the

pixel electrodes, and feeding paths for storing charge in the holding capacity is formed of either the gate lines or the above-mentioned electrode lines.

SUMMARY OF INVENTION

[0011] In this manner, one electrode which forms the holding capacity is a linear electrode and the feeding is limited to one direction (extending direction of the electrode) and hence, the feeding resistance is large. Further, corresponding to the increase of the distance between the electrode and a feeding end, the voltage drop is remarkably increased so that there arises a case that the required charge cannot be fed. Further, since the above-mentioned gate line usually crosses the drain line, a crossing capacity is increased. As a result, this has been one of causes which make the rapid driving of liquid crystal display device difficult. As a countermeasure to cope with such a problem, there has been proposed a liquid crystal display device which uses the above-mentioned other electrode line. However, when the holding capacity is formed in the pixel electrode forming region, numerical aperture is reduced as a matter of course.

[0012] Further, along with the demand for high definition, the size of pixels per one pixel is reduced so that there has been a task that it is difficult to form the sufficient holding capacity.

[0013] Further, although it is effective to reduce the size of the holding capacity to enhance the numerical aperture, this brings about the reduction of the holding capacity. That is, there has been a task that there exists a trade-off relationship between the enhancement of numerical aperture and the assurance of holding capacity.

[0014] Accordingly, it is an object of the present invention to provide an active matrix liquid crystal display device which can reduce resistance of feeding electrodes which constitute holding capacities. It is another object of the present invention to provide a rapid driving active matrix type liquid crystal display device having high brightness by obviating the reduction of numerical aperture of pixels.

[0015] It is still another object of the present invention to realize an active matrix type liquid crystal display device which can satisfy both of the assurance of holding capacity and the enhancement of numerical aperture simultaneously.

[0016] Other objects and advantages of the present invention will be apparent from the explanation made hereinafter.

0017] The typical constitution of the present invention lies in that on a switching element forming substrate of the liquid crystal display device, a transparent conductive layer (reference layer) having a large area which covers at least a major portion or a whole area of a pixel electrode forming region is formed, and switching elements (active elements), other electrodes and lines are formed over the transparent conductive layer by way of an insulation layer. Due to such a constitution, the feeding resistance with respect to the holding capacity can be largely reduced. Further, a trade-off between the enhancement of numerical aperture and the increase of holding

capacity can be eliminated. Representative constitutions of the present invention are described hereinafter.

1):

[0018] In a liquid crystal display device in which liquid crystal is sandwiched between a first substrate and a second substrate which face each other in an opposed manner, and at least a plurality of gate lines which extend in the first direction and are arranged parallel to each other, a plurality of drain lines which extend in the second direction which crosses the gate lines and are arranged parallel to each other, a plurality of switching elements which are arranged at crossing portions of the gate lines and the drain lines, and pixel electrodes which are driven by the switching elements are formed on an inner surface of the first substrate,

[0019] having an electrode forming layer which include the gate lines, the drain lines, the switching elements and the pixel electrodes,

[0020] having a reference electrode layer arranged between the first substrate and the electrode forming layer with first insulation layer between the reference electrode layer and the electrode forming layer, and

[0021] holding capacities of the pixels are formed between the pixel electrodes and the reference electrode layer.

[0022] Due to such a constitution, the feeding resistance with respect to the storage capacity is largely reduced so that it is possible to realize the liquid crystal display device which can realize both of the enhancement of numerical aperture of pixels and the assurance of holding capacity.

(2):

[0023] In the constitution (1), the electrode forming layer includes the gate lines, a gate insulation layer, the semiconductor layers, the drain lines, a passivation layer and the pixel electrodes in this order over the first insulation layer, and the holding capacity of the pixel is formed between the pixel electrodes and the reference electrode layer.

[0024] Since the holding capacity is constituted of the passivation layer, the gate insulation layer and the first insulation layer which are formed between the pixel electrode and the reference electrode layer, the distance to the reference electrode layer as viewed from the liquid crystal layer can be largely increased so that the influence of the electric field of the reference electrode layer on the electric field for driving liquid crystal can be attenuated.

3):

[0025] In the constitution (1), the reference electrode layer is arranged in the extension direction of the gate lines such that the reference electrode layer is arranged parallel to the gate lines and overlaps regions where the pixel electrodes are formed.

[0026] Due to such a constitution, the parasitic capacity between the gate line and the reference electrode layer can be reduced and the potential can be made stable.

(4):

[0027] In the constitution (1), the reference electrode layer is provided to a region of the first substrate which includes regions in which the gate lines, the drain lines and the pixel electrodes are formed.

[0028] Due to such a constitution, the reference electrode layer forms a so-called matted electrode so that the feeding resistance can be further reduced and the limitation imposed on the feeding direction can be eliminated.

(5):

[0029] In the constitution (1), the passivation layer is formed over the gate insulation layer, the pixel electrodes are formed over the passivation layer, and the whole or a portion of the pixel electrodes penetrate the passivation layer and are brought into contact with the gate insulation layer.

[0030] Due to such a constitution, holding capacity formed between the conductive layers and the pixel electrodes can be adjusted by changing the area that the pixel electrodes penetrate the passivation layer.

(6):

[0031] In the constitution (1), the passivation layer is formed over the gate insulation layer, the pixel electrodes are formed over the passivation layer, and the whole or a portion of the pixel electrodes in the pixel regions penetrate the passivation layer and the gate insulation layer and are brought into contact with the first insulation layer.

[0032] Due to such a constitution, holding capacity formed between the reference electrode layer and the pixel electrodes can be adjusted by changing the area that the pixel electrodes penetrate the passivation layer and the gate insulation layer.

(7):

[0033] In the constitution (1), the passivation layer is formed over the gate insulation layer, the pixel electrodes are formed over the passivation layer, and the switching elements include source electrodes on the gate insulation layer which are connected to the pixel electrodes via through holes formed in the passivation layer and extension portions which extend along the gate lines or the drain lines at one portions of the source electrodes.

[0034] Due to such a constitution, holding capacity can be adjusted by changing the length or the width of the extension portions of the source electrodes, that is, by changing the area that the source electrodes overlap the pixel electrodes.

(8):

[0035] In the constitution (1), the first insulation layer is formed of an organic insulation layer.

[0036] Due to such a constitution, the electric distance between the reference electrode layer and the electrode forming layer can be increased compared to a case in which the insulation layer is provided. Further, parasitic capacity between the reference electrode layer and the gate lines as well as the drain lines can be reduced.

(9):

[0037] In the constitution (1), the liquid crystal display device includes a light shielding layer which perform light shielding of gaps defined between the vicinities in the extension direction of the drain lines and the pixel electrodes.

[0038] Due to such a constitution, leaking of light can be prevented.

(10):

[0039] In the constitution (1), common electrodes which constitute pixels together with the pixel electrodes are formed on an inner surface of the second substrate.

(11):

[0040] In a liquid crystal display device in which liquid crystal is sandwiched between a first substrate and a second substrate which face each other in an opposed manner, and at least a plurality of gate lines which extend in the first direction and are arranged parallel to each other, a plurality of drain lines which extend in the second direction which crosses the gate lines and are arranged parallel to each other, a plurality of switching elements which are arranged at crossing portions of the gate lines and the drain lines, and pixel electrodes which are driven by the switching elements are formed on an inner surface of the first substrate,

[0041] having an electrode forming layer which include the gate lines, the drain lines, the switching elements and the pixel electrodes,

[0042] having a reference electrode layer arranged between the first substrate and the electrode forming layer with first insulation layer between the reference electrode layer and the electrode forming layer, and

[0043] the electrode forming layer includes the gate insulation layer, the passivation layer, a second insulation layer and the pixel electrodes in this order over the first insulation layer, and

[0044] holding capacities of the pixels are formed between the pixel electrodes and the reference electrode layer.

[0045] Due to such a constitution, the numerical aperture of the pixels can be enhanced. Since the area of the conductive layers is large, the feeding resistance can be reduced. Further, since the holding capacity is formed by the passivation layer, the gate insulation layer and the first insulation layer which are formed between the pixel electrodes and the reference electrode layer, the holding capacity can be easily controlled. Further, since the organic insulation layer is also formed over the switching elements, the pixel electrodes and the drain lines can overlap each other so that the numerical aperture is further enhanced. When the pixel electrodes and the drain lines overlap each other, it is possible to eliminate light shielding layers between the vicinities of the extension direction of the drain lines and the pixel electrodes so that the numerical aperture is further enhanced.

(12):

[0046] In the constitution (11), the reference electrode layer is arranged in the extension direction of the gate lines such that the reference electrode layer is arranged parallel to the gate lines and

overlaps regions where the pixel electrodes are formed.

[0047] Due to such a constitution, the capacity between the gate lines and the reference electrode layers can be reduced so that the increase of holding capacity can be suppressed and the potential can be made stable.

(13):

[0048] In the constitution (11), the reference electrode layer is provided to a region of the first substrate which includes regions in which the gate lines, the drain lines and the pixel electrodes are formed.

[0049] Due to such a constitution, the reference electrode layer forms a so-called matted electrode so that the feeding resistance can be further reduced and the limitation imposed on the feeding direction can be eliminated.

(14):

[0050] In the constitution (11), the first organic insulation layer is formed of color filters.

[0051] Due to such a constitution, the numerical aperture of the pixels is enhanced. Since the area of the conductive layers is large, the feeding resistance can be reduced. Further, since the holding capacity is formed by the passivation layer, the gate insulation layer and the color filter layer which is made of organic material and exhibits small dielectric constant between the pixel electrodes and the reference electrode layer, the increase of parasitic capacity between lines can be suppressed. Still further, since the color filter layer is formed over the first substrate, the tolerance of alignment of the first substrate with the second substrate is increased.

(15):

[0052] In the constitution (14), the reference electrode layer is arranged in the extension direction of the gate lines such that the reference electrode layer is arranged parallel to the gate lines and overlaps regions where the pixel electrodes are formed.

0053] Due to such a constitution, the capacity between the gate lines and the conductive layer can be reduced and the potential can be made stable.

(16):

[0054] In the constitution (14), the reference electrode layer is provided to a region of the first substrate which includes regions in which the gate lines, the drain lines and the pixel electrodes are formed.

[0055] Due to such a constitution, the reference electrode layer forms a so-called matted electrode so that the feeding resistance can be further reduced and the limitation imposed on the feeding direction can be eliminated.

(17):

[0056] In the constitution (11), the first insulation layer is an organic insulation layer.

0057] Due to such a constitution, the electric distance between the reference electrode layer and the electrode forming layer can be increased compared to a case in which the insulation layer is

provided. Further, the parasitic capacity between the reference electrode layer and the gate line as well as the drain line can be reduced.

(18):

[0058] In the constitution (11), the liquid crystal display device includes a light shielding layer which performs light shielding of gaps defined between the vicinities in the extension direction of the drain lines and the pixel electrodes.

[0059] Due to such a constitution, leaking of light can be prevented.

(19):

[0060] In the constitution (11), common electrodes which constitute pixels together with the pixel electrodes are formed on an inner surface of the second substrate.

(20):

[0061] In a liquid crystal display device in which liquid crystal is sandwiched between a first substrate and a second substrate which face each other in an opposed manner, and at least a plurality of gate lines which extend in the first direction and are arranged parallel to each other, a plurality of drain lines which extend in the second direction which crosses the gate lines and are arranged parallel to each other, a plurality of switching elements which are arranged at crossing portions of the gate lines and the drain lines, and pixel electrodes which are driven by the switching elements are formed on an inner surface of the first substrate, and pixel regions are formed of a plurality of pixel electrodes,

[0062] having an electrode forming layer which include the gate lines, the drain lines, the switching elements and the pixel electrodes,

[0063] having a reference electrode layer arranged between the first substrate and the electrode forming layer with first insulation layer between the reference electrode layer and the electrode forming layer, and

[0064] the electrode forming layer includes the gate insulation layer, the passivation layer and the pixel electrode in this order over the first insulation layer and further includes a capacitive electrode layer which is formed over the first insulation layer and is connected to the pixel electrodes, and

[0065] holding capacities of the pixels are formed among the pixel electrodes, the reference electrode layer and the capacitive electrode layer.

[0066] Due to such a constitution, the numerical aperture of the pixels can be enhanced. Since the area of the conductive layers is large, the feeding resistance can be reduced. Further, since the holding capacity can be adjusted by changing the area and size of the capacitive electrode layer, it is possible to realize both of the enhancement of numerical aperture and the assurance of holding capacity. Still further, when the organic insulation layer is formed between the passivation layer and the pixel electrodes, it is possible to make the pixel electrodes and the drain lines overlap each other and hence, the numerical aperture is further enhanced. When the pixel electrodes and the

drain lines overlap each other, it is possible to eliminate light shielding layers between the vicinities of the extension direction of the drain lines and the pixel electrodes so that the numerical aperture is further enhanced.

(21):

[0067] In the constitution (20), the reference electrode layer is arranged in the extension direction of the gate lines such that the reference electrode layer is arranged parallel to the gate lines and overlaps regions where the pixel electrodes are formed.

[0068] Due to such a constitution, the capacity between the gate lines and the reference electrode layer can be reduced and the potential can be made stable.

(22):

[0069] In the constitution (20), the reference electrode layer is provided to a region of the first substrate which includes regions in which the gate lines, the drain lines and the pixel electrodes are formed.

[0070] Due to such a constitution, the reference electrode layer forms a so-called matted electrode so that the feeding resistance can be further reduced and the limitation imposed on the feeding direction can be eliminated.

(23):

[0071] In the constitution (20), the switching elements include source electrodes over the gate insulation layer which are connected to the pixel electrodes via through holes formed in the passivation layer, and the capacitive electrode layer is connected to the source electrodes and is provided to regions of the pixel electrodes.

[0072] Due to such a constitution, the holding capacity can be adjusted by changing the size of the capacitive electrode layer.

(24):

[0073] In the constitution (20), the first insulation layer is formed of color filters.

[0074] Due to such a constitution, the numerical aperture of the pixels can be enhanced. Since the area of the conductive layers is large, the feeding resistance can be reduced. Further, since the color filter layer is formed over the first substrate, the tolerance of alignment of the first substrate with the second substrate can be increased.

(25):

[0075] In the constitution (20), the capacitive electrode layer is formed over the passivation layer, the organic insulation layer is formed over the passivation layer, the pixel electrodes are formed over the organic insulation layer and are connected to the capacitive electrode layer via through holes formed in the organic insulation layer.

[0076] Due to such a constitution, the holding capacity can be adjusted by changing the size of the capacitive electrode layer.

(26):

[0077] In the constitution (20), the capacitive electrode layer is formed over the gate insulation layer, and the pixel electrodes are connected to the capacitive electrode layer via through holes formed in the passivation layer.

[0078] Due to such a constitution, the holding capacity can be adjusted by changing the size of the capacitive electrode layer.

(27):

[0079] In the constitution (20), the capacitive electrode layer is formed over the first insulation layer, and the pixel electrodes penetrate the passivation layer and are connected to the capacitive electrode layer via through holes formed in the gate insulation layer.

[0080] Due to such a constitution, the holding capacity formed between the conductive layer and the pixel electrodes can be adjusted by changing the area that the pixel electrodes penetrate the passivation layer and the gate insulation layer.

(28):

[0081] In the constitution (20), the first insulation layer is formed of an organic insulation layer.

[0082] Due to such a constitution, the electric distance between the reference electrode layer and the electrode forming layer can be increased compared to a case in which the insulation layer is provided. Further, parasitic capacity between the reference electrode layer and the gate lines as well as the drain lines can be reduced.

(29):

[0083] In the constitution (20), the liquid crystal display device includes a light shielding layer which performs light shielding of gaps defined between the vicinities in the extension direction of the drain lines and the pixel electrodes.

[0084] Due to such a constitution, leaking of light can be prevented.

(30):

[0085] In the constitution (20), common electrodes which constitute pixels together with the pixel electrodes are formed on an inner surface of the second substrate.

(31):

[0086] In a liquid crystal display device in which liquid crystal is sandwiched between a first substrate and a second substrate which face each other in an opposed manner, and at least a plurality of gate lines which extend in the first direction and are arranged parallel to each other, a plurality of drain lines which extend in the second direction which crosses the gate lines and are arranged parallel to each other, a plurality of switching elements which are arranged at crossing portions of the gate lines and the drain lines, and pixel electrodes which are driven by the switching elements are formed on an inner surface of the first substrate, and pixel regions are formed of a plurality of pixel electrodes,

[0087] the improvement is characterized in that between an electrode forming layer which is constituted of the gate lines, the drain lines, the switching elements and the pixel electrodes

including the pixel regions of the first substrate and the first substrate side, a reference electrode layer which is insulated by a first insulation layer with respect to the electrode forming layer is formed,

[0088] wherein having an electrode forming layer which include the gate lines, the drain lines, the switching elements and the pixel electrodes,

[0089] having a reference electrode layer arranged between the first substrate and the electrode forming layer with first insulation layer between the reference electrode layer and the electrode forming layer, and

[0090] the electrode forming layer includes the gate insulation layer, the passivation layer and the pixel electrode in this order over the first insulation layer and further includes a capacitive electrode layer which is connected to the pixel electrodes between the first insulation layer and the passivation layer, and

[0091] holding capacities of the pixels are formed among the pixel electrodes, the reference electrode layer and the capacitive electrode layer.

[0092] Due to such a constitution, the numerical aperture of pixels can be enhanced. Further, since the area of the reference electrode layer is large, the feeding resistance can be reduced. Still further, the holding capacity can be adjusted by changing the area and the shape of the capacitive electrode layer.

(32):

[0093] In the constitution (31), the reference electrode layer is arranged in the extension direction of the gate lines such that the reference electrode layer is arranged parallel to the gate lines and overlaps regions where the pixel electrodes are formed.

[0094] Due to such a constitution, the capacity between the gate lines and the reference electrode layer can be reduced. The increase of parasitic capacity between lines can be suppressed. Further, the potential can be made stable.

(33):

[0095] In the constitution (31), the reference electrode layer is provided to a region of the first substrate which includes regions in which the gate lines, the drain lines and the pixel electrodes are formed.

[0096] Due to such a constitution, the reference electrode layer forms a so-called matted electrode so that the feeding resistance can be further reduced and the limitation imposed on the feeding direction can be eliminated.

(34):

[0097] In the constitution (31), the organic insulation layer is formed of color filters.

[0098] Due to such a constitution, the numerical aperture of the pixels is enhanced. Since the area of the reference electrode layers is large, the feeding resistance can be reduced. Further, since the color filters are formed of organic films, the parasitic capacitance between lines can be reduced.

Still further, since the color filter layer is formed over the first substrate, the tolerance of alignment of the first substrate with the second substrate is increased.

(35):

[0099] In the constitution (31), the first insulation layer is formed of an organic insulation layer.

[0100] Due to such a constitution, the electric distance between the reference electrode layer and the electrode forming layer can be increased compared to a case in which the insulation layer is provided. Further, the parasitic capacity between the reference electrode layer and the gate lines as well as the drain lines can be reduced.

(36):

[0101] In the constitution (31), the liquid crystal display device includes a light shielding layer which performs light shielding of gaps defined between the vicinities in the extension direction of the drain lines and the pixel electrodes.

[0102] Due to such a constitution, leaking of light can be prevented.

(37):

[0103] In the constitution (31), the capacitive electrode layer is formed over the first insulation layer, and the capacitive electrode layer is connected to the reference electrode layer via through holes which penetrate the first insulation layer.

[0104] Due to such a constitution, the holding capacity formed between the reference electrode layer and the pixel electrodes can be adjusted by changing the area of the capacitive electrode layer connected to the reference electrode layer.

(38):

[0105] In the constitution (31), the capacitive electrode layer is formed over the gate insulation layer, and the capacitive electrode layer is connected to the reference electrode layer via through holes which penetrate the gate insulation layer.

[0106] Due to such a constitution, the holding capacity formed between the reference electrode layer and the pixel electrodes can be adjusted by changing the area of the capacitive electrode layer connected to the reference electrode layer.

(39):

[0107] In the constitution (31), the capacitive electrode layer is formed over the passivation layer, and the capacitive electrode layer is connected to the reference electrode layer via through holes which penetrate the passivation layer, the gate insulation layer and the first insulation layer.

[0108] Due to such a constitution, the holding capacity formed between the reference electrode layer and the pixel electrodes can be adjusted by changing the area of the capacitive electrode layer connected to the reference electrode layer.

(40):

[0109] In the constitution (31), the capacitive electrode layer is formed over the gate insulation layer, a second capacitive electrode layer is formed over the first insulation layer, the pixel

electrode is connected to the capacitive electrode layer via through holes formed in the passivation layer, and the second capacitive electrode layer is connected to the reference electrode layer via through holes formed in the first insulation layer.

[0110] Due to such a constitution, the holding capacity can be easily adjusted by changing the areas of the capacitive electrode layer and the second capacitive electrode layer. Further, the holding capacity can be further increased.

(41):

[0111] In the constitution (31), the first insulation layer is formed of an organic insulation layer.

[0112] Due to such a constitution, the electric distance between the reference electrode layer and the electrode forming layer can be increased compared to a case that the insulation layer is provided. Further, the parasitic capacity among the reference electrode layer, the gate lines and the drain lines can be reduced.

(42):

[0113] In the constitution (31), the liquid crystal display device includes a light shielding layer which performs light shielding of gaps defined between the vicinities in the extension direction of the drain lines and the pixel electrodes.

[0114] Due to such a constitution, leaking of light can be prevented.

(43):

[0115] In the constitution (31), common electrodes which constitute pixels together with the pixel electrodes are formed on an inner surface of the second substrate.

(44):

[0116] In a liquid crystal display device in which liquid crystal is sandwiched between a first substrate and a second substrate which face each other in an opposed manner, and at least a plurality of gate lines which extend in the first direction and are arranged parallel to each other, a plurality of drain lines which extend in the second direction which crosses the gate lines and are arranged parallel to each other, a plurality of switching elements which are arranged at crossing portions of the gate lines and the drain lines, pixel electrodes which are driven by the switching elements, and counter electrodes which generate an electric field for driving pixels between the pixel electrodes and the counter electrodes are formed on an inner surface of the first substrate,

[0117] having an electrode forming layer which include the gate lines, the drain lines, the switching elements and the pixel electrodes,

[0118] having a reference electrode layer arranged between the first substrate and the electrode forming layer with first insulation layer between the reference electrode layer and the electrode forming layer, and

[0119] holding capacities of the pixels are formed among the pixel electrodes and the reference electrode layer.

[0120] Due to such a constitution, the liquid crystal display device can achieve both of the large

numerical aperture and the large holding capacity. Further, since it is unnecessary to increase the areas of the pixel electrodes and the lines for forming the holding capacity, the numerical aperture is enhanced. Still further, since the area of the reference electrode layer is large, the feeding resistance can be reduced.

(45):

[0121] In the constitution (44), the counter electrodes are formed over the organic insulation layer, and the counter electrodes are connected to the reference electrode layer via through holes formed in the first insulation layer.

[0122] Due to such a constitution, the area of the reference electrode layer can be increased and hence, the feeding resistance to the counter electrodes can be reduced.

(46):

[0123] In the constitution (44), the counter electrodes are formed over the gate insulation layer, and the counter electrodes are connected to the reference electrode layer via through holes formed in the gate insulation layer and the first insulation layer.

[0124] Due to such a constitution, the area of the reference electrode layer can be increased and hence, the feeding resistance can be reduced.

(47):

[0125] In the constitution (44), the counter electrodes are formed over the passivation layer, and the counter electrodes are connected to the reference electrode layer via through holes formed in the passivation layer, the gate insulation layer and the first insulation layer.

[0126] Due to such a constitution, the area of the reference electrode layer can be increased and hence, the feeding resistance can be reduced.

(48):

[0127] In the constitution (44), the reference electrode layer is arranged in the extension direction of the gate lines such that the reference electrode layer is arranged parallel to the gate lines and overlaps regions where the pixel electrodes are formed.

[0128] Due to such a constitution, the parasitic capacity formed between the gate lines and the reference electrode layer can be reduced and the potential can be made stable.

(49):

[0129] In the constitution (44), the reference electrode layer is provided to a region of the first substrate which includes regions in which the gate lines, the drain lines and the pixel electrodes are formed.

[0130] Due to such a constitution, the reference electrode layer forms a so-called matted electrode so that the feeding resistance can be further reduced and the limitation imposed on the feeding direction can be eliminated.

(50):

[0131] In the constitution (44), the counter electrodes are formed over the first insulation layer,

the counter electrodes extend to the neighboring pixel regions by crossing the drain lines and are connected to the reference electrode layers of the neighboring pixel regions via through holes formed in the first insulation layer.

[0132] Due to such a constitution, even when the through holes are formed insufficiently, the feeding of electricity is performed through the counter electrodes from the neighboring pixel sides. Further, when the through holes which connect each counter electrode and each reference electrode are formed in a plural number for every pixel, the reliability of connection between the electrode layers can be enhanced.

(51):

[0133] In the constitution (44), the counter electrodes are formed over an organic insulation layer, conductive layers which extend to the neighboring pixel regions by crossing the drain lines are formed over the gate insulation layer, the counter electrodes are connected to the conductive layers via through holes formed in the gate insulation layer, and the conductive layers are connected to the reference electrode layer via through holes formed in the first insulation layer.

[0134] Due to such a constitution, even when the through holes are formed insufficiently, the feeding of electricity is performed through the conductive layers from the neighboring pixel sides. Further, when the through holes which connect each counter electrode and each reference electrode are formed in a plural number for every pixel, the reliability of connection between the electrode layers can be enhanced.

(52):

[0135] In the constitution (44), the counter electrodes are formed over a passivation layer, conductive layers which extend to the neighboring pixel regions by crossing the drain lines are formed over the gate insulation layer, the counter electrodes are connected to the conductive layers via through holes formed in the passivation layer and the gate insulation layer, and the conductive layers are connected to the reference electrode layer via through holes formed in the first insulation layer.

[0136] Due to such a constitution, even when the through holes are formed insufficiently, the feeding of electricity is performed through the conductive layers from the neighboring pixel sides. Further, when the through holes which connect each counter electrode and each reference electrode are formed in a plural number for every pixel, the reliability of connection between the electrode layers can be enhanced.

(53):

[0137] In the constitution (44), a color filter layer is formed between the reference electrode which is formed below the first insulation layer and the first substrate.

[0138] Due to such a constitution, it is possible to isolate the color filter layer from the liquid crystal layer with the use of the reference electrodes and hence, it is possible to prevent the liquid crystal from being contaminated by constituent materials of the color filter layer.

(54):

[0139] In the constitution (44), the counter electrodes are formed over the first insulation layer parallel to the extension direction of the gate lines, the counter electrodes extends over the pixel region, and the counter electrodes are connected to the reference electrodes in respective pixel regions via through holes formed in the first insulation layer.

[0140] Due to such a constitution, holding capacity is formed at portions where the counter electrodes and the pixel electrodes overlap each other, and the gate insulation layer functions as a dielectric of the holding capacity and hence, the constitution is suitable for increasing the holding capacity.

(55):

[0141] In the constitution (44), the counter electrodes are connected to the reference electrodes in respective pixel regions via through holes formed in the first insulation layer and the gate insulation layer in a penetrating manner, and holding capacities are formed at overlapping portions of the counter electrodes and the pixel electrodes.

(56):

[0142] In the constitution (44), the pixel electrodes are formed over the gate insulation layer, the counter electrodes are formed below the gate insulation layers, the counter electrodes are connected to the reference electrodes via through holes formed in the first insulation layer, and holding capacities are formed by the counter electrodes and the pixel electrodes.

(57):

[0143] In the constitution (44), the pixel electrodes and the counter electrodes are formed on the same layer.

(58):

[0144] In the constitution (44), the counter electrodes are formed over the pixel electrodes and are connected to the reference electrodes by way of through holes formed in a gate insulation film and a first insulation film.

(59):

[0145] In the constitution (44), the first insulation layer is formed of an organic insulation layer.

(60):

[0146] In a liquid crystal display device in which liquid crystal is sandwiched between a first substrate and a second substrate which face each other in an opposed manner, and at least a plurality of gate lines which extend in the first direction and are arranged parallel to each other, a plurality of drain lines which extend in the second direction which crosses the gate lines and are arranged parallel to each other, a plurality of switching elements which are arranged at crossing portions of the gate lines and the drain lines, and pixel electrodes which are driven by the switching elements are formed on an inner surface of the first substrate,

[0147] having an electrode forming layer which include the gate lines, the drain lines, the switching

elements and the pixel electrodes,

[0148] having a counter electrode layer arranged between the first substrate and the electrode forming layer with first insulation layer between the reference electrode layer and the electrode forming layer, and the reference electrode layer overlapped substantially all region of the pixel electrode and function as a counter electrode, and

[0149] holding capacities of the pixels are formed between the pixel electrodes and the counter electrode layer.

[0150] Due to such a constitution, the feeding resistance with respect to the holding capacity can be largely reduced so that the image quality is enhanced. Further, it is possible to realize both of the enhancement of numerical aperture and the assurance of holding capacity.

(61):

[0151] In the constitution (60), the counter electrode layer is arranged in the extension direction of the gate lines such that the counter electrode layer is arranged parallel to the gate lines and overlaps regions where the pixel electrodes are formed.

[0152] Due to such a constitution, an independent reference electrode layer is unnecessary, the parasitic capacity between the gate lines and the conductive layers can be reduced, and the potential can be made stable.

(62):

[0153] In the constitution (60), the counter electrode layer is provided to a region of the first substrate which includes regions in which the gate lines, the drain lines and the pixel electrodes are formed.

[0154] Due to such a constitution, the counter electrode layer forms a so-called matted electrode so that the feeding resistance can be further reduced and the limitation imposed on the feeding direction can be eliminated.

(63):

[0155] In the constitution (60), the whole or a portion of the layer constitution of insulation layers below the pixel electrodes and the whole or a portion of the region are removed.

[0156] Due to such a constitution, the strength of electric field generated between the pixel electrodes and the counter electrodes is increased so that the driving voltage can be reduced.

(64):

[0157] In the constitution (60), over the counter electrode layer, connection lines which are arranged parallel to the extension direction of the gate lines and are connected to counter electrodes which are disposed close to the counter electrode are formed.

(65):

[0158] In the constitution (60), below the counter electrode layer, connection lines which are arranged parallel to the extension direction of the gate lines and are connected to counter electrodes which are disposed close to the counter electrode are formed.

[0159] Due to the above-mentioned constitution (64) or (65), even when the through holes are formed insufficiently, the feeding of electricity is performed through the connection lines from the neighboring pixel sides. Further, when the through holes which connect each counter electrode with each reference electrode are formed in a plural number for every pixel, the reliability of connection of the electrode layers can be enhanced.

(66):

[0160] In the constitution (60), the first insulation layer is removed at portions of the pixel regions.

0161] Due to such a constitution, a plurality of regions which differ in driving voltage can be formed in the pixel region so that the multi-domain effect can be obtained.

(67):

[0162] In the constitution (60), a color filter layer is formed between the reference electrodes which are arranged below the first insulation layer and the first substrate.

(68):

[0163] In the constitution (60), the first insulation layer is formed of an organic insulation layer.

(69):

[0164] In the constitution (68), the organic insulation layer is formed of color filters.

(70):

[0165] In a liquid crystal display device, liquid crystal sandwiched between a first substrate and a second substrate which face each other in an opposed manner;

[0166] a plurality of gate lines which extend in the first direction and are arranged parallel to each other;

0167] a plurality of drain lines which extend in the second direction which crosses the gate lines and are arranged parallel to each other;

[0168] a plurality of switching elements which are arranged at crossing portions of the gate lines and the drain lines;

[0169] pixel electrodes which are driven by the switching elements are formed on an inner surface of the first substrate,

[0170] counter electrodes which generate an electric field for driving pixels between the pixel electrodes formed on an inner surface of the first;

[0171] having an electrode forming layer which include the gate lines, the drain lines, the switching elements and the pixel electrodes,

[0172] having a reference electrode layer arranged between the first substrate and the electrode forming layer with first insulation layer between the reference electrode layer and the electrode forming layer,

[0173] the electrode forming layer is formed by laminating the gate insulation layer, the passivation layer, an organic insulation layer and counter electrodes in this order over the first insulation layer,

[0174] the counter electrode layer is shared by a pixel region which is arranged close to the pixel region in the extension direction of the gate lines and a pixel region which is arranged close to the pixel region in the extension direction of the drain lines,

[0175] the counter electrode layer is connected to the reference electrode layer via through holes which electrically penetrate the organic insulation layer, the passivation layer, the gate insulation layer and the first insulation layer, and

[0176] holding capacities of the pixels are formed between the pixel electrodes and the reference electrode layer.

(71):

[0177] In the constitution (70), the liquid crystal display device includes a capacitive electrode layer which is disposed below the pixel electrodes and is formed between the first insulation layer and the gate insulation layer, and the capacitive electrode layer is connected to the reference electrode layer via through holes.

[0178] Due to such a constitution, the holding capacity can be increased and adjusted by the capacitive electrode layer.

(72):

[0179] In the constitution (70), removing regions are formed in the first insulation layer disposed below the pixel electrodes.

[0180] Due to such a constitution, the holding capacity formed between the pixel electrode and the reference electrode layer can be increased.

(73):

[0181] In the constitution (70), the first insulation layer is formed of an organic insulation layer.

(74):

[0182] In the constitution (73), the organic insulation layer is formed of color filters.

(75):

[0183] In an image display device in which at least a plurality of gate lines which extend in the first direction and are arranged parallel to each other, a plurality of drain lines which extend in the second direction which crosses the gate lines and are arranged parallel to each other, a plurality of switching elements which are arranged at crossing portions of the gate lines and the drain lines, and pixel electrodes which are driven by the switching elements are formed on an inner surface of the first substrate,

[0184] having an electrode forming layer which include the gate lines, the drain lines, the switching elements and the pixel electrodes,

[0185] having a reference electrode layer arranged between the first substrate and the electrode forming layer with first insulation layer between the reference electrode layer and the electrode forming layer, and

[0186] the reference electrode layer is substantially formed over the whole surface of the pixel

regions and shared by a plurality of pixels.

(76):

[0187] In the constitution (75), a semiconductor layer which constitutes the switching element has crystalline property.

(77):

[0188] An image display device being characterized in that a reference electrode layer formed between a substrate and a semiconductor having crystalline property, and having insulation layer between the reference electrode layer and the semiconductor, and the reference electrode layer is formed over substantially the whole surface of a pixel region and is shared by a plurality of pixels.

(78):

[0189] In the constitution (77), the reference electrode layer is formed of a transparent electrode.

(79):

[0190] A manufacturing method of an image display device comprises at least a first step in which a reference electrode layer which is shared by a plurality of pixels is formed on a substantially whole surface of a pixel region on a substrate, a second step in which an insulation layer is formed, and a third step in which a semiconductor layer is formed in this order, and thereafter, further comprise a fourth step in which laser beams are irradiated to the semiconductor layer.

(80):

[0191] A manufacturing method of an image display device comprises at least a first step in which a reference electrode layer which is shared by a plurality of pixels is formed on a substantially whole surface of a pixel region on a substrate, a second step in which an insulation layer is formed, and a third step in which a semiconductor layer is formed in this order, and thereafter, further comprises a fourth step in which ions are implanted into the semiconductor layer.

[0192] The present invention is not limited to the above-mentioned respective constitutions and the constitutions of embodiments which will be explained later and various modifications are considered without departing from the technical concept of the present invention.

BRIEF DESCRIPTION OF THE DRAWINGS

[0193] FIG. 1 is a plan view of the vicinity of one pixel of a liquid crystal display device for schematically explaining the pixel constitution of one embodiment of the present invention.

[0194] FIG. 2 is a cross-sectional view taken along a line I-I in FIG. 1.

[0195] FIG. 3 is a cross-sectional view taken along a line II-II in FIG. 1.

[0196] FIG. 4 is a plan view of the vicinity of one pixel of a liquid crystal display device for schematically explaining the pixel constitution of another embodiment of the present invention.

[0197] FIG. 5 is a cross-sectional view taken along a line I-I in FIG. 4.

[0198] FIG. 6 is a cross-sectional view taken along a line II-II in FIG. 4.

[0199] FIG. 7 is a plan view of the vicinity of one pixel of a liquid crystal display device for

schematically explaining the pixel constitution of still another embodiment of the present invention.

[0200] FIG. 8 is a cross-sectional view taken along a line I-I in FIG. 7.

[0201] FIG. 9 is a cross-sectional view taken along a line I-I in FIG. 8 showing the vicinity of one pixel of a liquid crystal display device for schematically explaining the pixel constitution of still another embodiment of the present invention.

[0202] FIG. 10 is a plan view of the vicinity of one pixel of a liquid crystal display device for schematically explaining the pixel constitution of still another embodiment of the present invention.

[0203] FIG. 11 is a plan view of the vicinity of one pixel of a liquid crystal display device for schematically explaining the pixel constitution of still another embodiment of the present invention.

[0204] FIG. 12 is a plan view of the vicinity of one pixel of a liquid crystal display device for schematically explaining the pixel constitution of still another embodiment of the present invention.

[0205] FIG. 13 is a cross-sectional view taken along a line I-I in FIG. 12.

[0206] FIG. 14 is across-sectional view taken along a line II-II in FIG. 12.

[0207] FIG. 15 is a plan view of the vicinity of one pixel of a liquid crystal display device for schematically explaining the pixel constitution of still another embodiment of the present invention.

[0208] FIG. 16 is a cross-sectional view taken along a line I-I in FIG. 15.

[0209] FIG. 17 is across-sectional view taken along a line II-II in FIG. 15.

[0210] FIG. 18 is a cross-sectional view taken along a line I-I in FIG. 15 of a liquid crystal display device for schematically explaining the pixel constitution of another embodiment of the present invention.

[0211] FIG. 19 is across-sectional view taken along a line II-II in FIG. 18.

[0212] FIG. 20 is a plan view of the vicinity of one pixel of a liquid crystal display device for schematically explaining the pixel constitution of still another embodiment of the present invention.

[0213] FIG. 21 is a cross-sectional view taken along a line III-III in FIG. 20.

[0214] FIG. 22 is a cross-sectional view taken along the line III-III in FIG. 20 for schematically explaining the pixel constitution of another embodiment of the present invention.

[0215] FIG. 23 is a cross-sectional view taken along the line III-III in FIG. 20 for schematically explaining the pixel constitution of another embodiment of the present invention.

[0216] FIG. 24 is a plan view of the vicinity of one pixel of a liquid crystal display device for schematically explaining the pixel constitution of still another embodiment of the present invention.

[0217] FIG. 25 is a cross-sectional view taken along a line III-III in FIG. 24.

[0218] FIG. 26 is a cross-sectional view taken along a line III-III in FIG. 24 of the vicinity of one pixel of the liquid crystal display device for schematically explaining the pixel constitution of still another embodiment of the present invention.

[0219] FIG. 27 is a cross-sectional view taken along a line III-III in FIG. 24 of the vicinity of one pixel of the liquid crystal display device for schematically explaining the pixel constitution of still another embodiment of the present invention.

[0220] FIG. 28 is a plan view of the vicinity of one pixel of a liquid crystal display device for schematically explaining the pixel constitution of still another embodiment of the present invention.
[0221] FIG. 29 is a cross-sectional view taken along a line III-III in FIG. 28.
[0222] FIG. 30 is a cross-sectional view taken along a line III-III in FIG. 28 of the vicinity of one pixel of the liquid crystal display device for schematically explaining the pixel constitution of still another embodiment of the present invention.
[0223] FIG. 31 is a plan view of the vicinity of one pixel of a liquid crystal display device for schematically explaining the pixel constitution of still another embodiment of the present invention.
[0224] FIG. 32 is a cross-sectional view taken along a line III-III in FIG. 31.
[0225] FIG. 33 is a cross-sectional view taken along a line III-III in FIG. 31 of the vicinity of one pixel of the liquid crystal display device for schematically explaining the pixel constitution of still another embodiment of the present invention.
[0226] FIG. 34 is a plan view of the vicinity of one pixel of a liquid crystal display device for schematically explaining the pixel constitution of still another embodiment of the present invention.
[0227] FIG. 35 is a cross-sectional view taken along a line III-III in FIG. 34.
[0228] FIG. 36 is a cross-sectional view taken along a line III-III in FIG. 34 of the vicinity of one pixel of the liquid crystal display device for schematically explaining the pixel constitution of still another embodiment of the present invention.
[0229] FIG. 37 is a cross-sectional view taken along a line III-III in FIG. 34 of the vicinity of one pixel of the liquid crystal display device for schematically explaining the pixel constitution of still another embodiment of the present invention.
[0230] FIG. 38 is a plan view of the vicinity of one pixel of a liquid crystal display device for schematically explaining the pixel constitution of still another embodiment of the present invention.
[0231] FIG. 39 is a cross-sectional view taken along a line III-III in FIG. 38.
[0232] FIG. 40 is a cross-sectional view taken along a line III-III in FIG. 38 of the vicinity of one pixel of the liquid crystal display device for schematically explaining the pixel constitution of still another embodiment of the present invention.
[0233] FIG. 41 is a cross-sectional view taken along a line III-III in FIG. 38 of the vicinity of one pixel of the liquid crystal display device for schematically explaining the pixel constitution of still another embodiment of the present invention.
[0234] FIG. 42 is a plan view of the vicinity of one pixel of a liquid crystal display device for schematically explaining the pixel constitution of still another embodiment of the present invention.
[0235] FIG. 43 is a cross-sectional view taken along a line III-III in FIG. 38.
[0236] FIG. 44 is a cross-sectional view taken along a line III-III in FIG. 42 of the vicinity of one pixel of the liquid crystal display device for schematically explaining the pixel constitution of still another embodiment of the present invention.
[0237] FIG. 45 is a plan view of a through hole and a metal light shielding film in still another

embodiment of the present invention.

[0238] FIGs. 46A – 46D are cross-sectional views of an essential part for explaining still another embodiment of the present invention.

[0239] FIG. 47 is a plan view of the vicinity of one pixel of a liquid crystal display device for schematically explaining the pixel constitution of still another embodiment of the present invention.

[0240] FIG. 48 is a cross-sectional view taken along a line III-III in FIG. 47.

[0241] FIG. 49 is a cross-sectional view taken along a line IV-IV in FIG. 47 of the vicinity of one pixel of the liquid crystal display device for schematically explaining the pixel constitution of still another embodiment of the present invention.

[0242] FIG. 50 is a cross-sectional view taken along a line IV-IV in FIG. 47 of the vicinity of one pixel of the liquid crystal display device for schematically explaining the pixel constitution of still another embodiment of the present invention.

[0243] FIG. 51 is a plan view of the vicinity of one pixel of a liquid crystal display device for schematically explaining the pixel constitution of still another embodiment of the present invention.

[0244] FIG. 52 is a cross-sectional view taken along a line V-V in FIG. 51.

[0245] FIG. 53 is a cross-sectional view taken along a line V-V in FIG. 51 showing the vicinity of one pixel of a liquid crystal display device for schematically explaining the pixel constitution of still another embodiment of the present invention.

[0246] FIG. 54 is a cross-sectional view taken along a line V-V in FIG. 51 showing the vicinity of one pixel of a liquid crystal display device for schematically explaining the pixel constitution of still another embodiment of the present invention.

[0247] FIG. 55 is a cross-sectional view taken along a line V-V in FIG. 51 showing the vicinity of one pixel of a liquid crystal display device for schematically explaining the pixel constitution of still another embodiment of the present invention.

[0248] FIG. 56 is a plan view of the vicinity of one pixel of a liquid crystal display device for explaining a modification of the embodiments shown in FIG. 47 to FIG. 55.

[0249] FIG. 57 is a plan view of the vicinity of one pixel of a liquid crystal display device for schematically explaining the pixel constitution of still another embodiment of the present invention.

[0250] FIG. 58 is a cross-sectional view taken along a line VI-VI in FIG. 57.

[0251] FIG. 59 is a cross-sectional view taken along a line VI-VI in FIG. 57 showing the vicinity of one pixel of a liquid crystal display device for schematically explaining the pixel constitution of still another embodiment of the present invention.

[0252] FIG. 60 is a plan view of the vicinity of one pixel of a liquid crystal display device for schematically explaining the pixel constitution of still another embodiment of the present invention.

[0253] FIG. 61 is a cross-sectional view taken along a line VII-VII in FIG. 60.

[0254] FIG. 62 is a cross-sectional view taken along a line VIII-VIII in FIG. 60.

[0255] FIG. 63 is a cross-sectional view taken along a line VII-VII in FIG. 60 showing the vicinity

of one pixel of a liquid crystal display device for schematically explaining the pixel constitution of still another embodiment of the present invention.

[0256] FIG. 64 is a plan view of a portion of a thin film transistor TFT of a liquid crystal display device for schematically explaining an essential part of the pixel constitution of still another embodiment of the present invention.

[0257] FIG. 65 is a plan view of the vicinity of one pixel of a liquid crystal display device for schematically explaining an essential part of the pixel constitution of still another embodiment of the present invention.

[0258] FIG. 66 is a cross sectional view taken along a line IX-IX in FIG. 65.

[0259] FIG. 67 is a cross-sectional view taken along a line IX-IX in FIG. 65 showing the vicinity of one pixel of a liquid crystal display device for schematically explaining an essential part of the pixel constitution of still another embodiment of the present invention.

[0260] FIG. 68 is a plan view of the vicinity of one pixel of a liquid crystal display device for schematically explaining an essential part of the pixel constitution of still another embodiment of the present invention.

[0261] FIG. 69 is a cross sectional view taken along a line X-X in FIG. 68.

[0262] FIG. 70 is a cross-sectional view taken along a line X-X in FIG. 68 showing the vicinity of one pixel of a liquid crystal display device for schematically explaining an essential part of the pixel constitution of still another embodiment of the present invention.

[0263] FIG. 71 is a plan view of the vicinity of one pixel of a liquid crystal display device for schematically explaining an essential part of the pixel constitution of still another embodiment of the present invention.

[0264] FIG. 72 is a cross sectional view taken along a line XI-XI in FIG. 71.

[0265] FIG. 73 is a cross-sectional view taken along a line XI-XI in FIG. 68 showing the vicinity of one pixel of a liquid crystal display device for schematically explaining an essential part of the pixel constitution of still another embodiment of the present invention.

[0266] FIG. 74 is a plan view of the vicinity of one pixel of a liquid crystal display device for schematically explaining an essential part of the pixel constitution of still another embodiment of the present invention.

[0267] FIG. 75 is a cross sectional view taken along a line XII-XII in FIG. 74.

[0268] FIG. 76 is across-sectional view taken along a line XII-XII in FIG. 74 showing the vicinity of one pixel of a liquid crystal display device for schematically explaining an essential part of the pixel constitution of still another embodiment of the present invention.

[0269] FIG. 77 is a cross-sectional view taken along a line XII-XII in FIG. 74 showing the vicinity of one pixel of a liquid crystal display device for schematically explaining an essential part of the pixel constitution of still another embodiment of the present invention.

[0270] FIG. 78 is a cross-sectional view taken along a line XII-XII in FIG. 74 showing the vicinity

of one pixel of a liquid crystal display device for schematically explaining an essential part of the pixel constitution of still another embodiment of the present invention.

[0271] FIG. 79 is a cross-sectional view taken along a line XII-XII in FIG. 74 showing the vicinity of one pixel of a liquid crystal display device for schematically explaining an essential part of the pixel constitution of still another embodiment of the present invention.

[0272] FIG. 80 is an explanatory view for explaining the constitution of a substrate of the liquid crystal display device of the present invention.

[0273] FIG. 81 is an explanatory view showing a state in which a tape carrier package on which a driving circuit is formed is mounted on the first substrate at a terminal region.

[0274] FIG. 82 is an explanatory view showing a state in which a driving circuit chip is directly mounted on the first substrate at the terminal region.

[0275] FIG. 83 is an explanatory view of an example of layout of a liquid crystal filling port for allowing liquid crystal to be filled and sealed between two substrates.

[0276] FIG. 84 is a schematic cross-sectional view of the liquid crystal display device of the present invention.

[0277] FIGs. 85A - 85C are plan views for schematically explaining a terminal region of a gate driving circuit mounted in a tape carrier package method

[0278] FIGs. 86A - 86B are plan views for schematically explaining a terminal region on which a driving circuit chip is mounted in a FCA method.

[0279] FIGs. 87A – 87B are plan views for schematically explaining a terminal region when a method in which electricity is supplied to a flexible printed circuit board or the like from a reference potential generation circuit disposed in a control circuit of the liquid crystal display device is adopted.

[0280] FIG. 88 is a schematic plan view of the liquid crystal display device for explaining a first example in which a feeding terminal to a reference electrode is formed.

[0281] FIG. 89 is a schematic plan view of the liquid crystal display device for explaining a second example in which feeding terminal to a reference electrode is formed.

[0282] FIG. 90 is a cross-sectional view of an essential part showing a portion A of FIG. 89 in an enlarged manner.

[0283] FIG. 91 is a schematic cross-sectional view of the liquid crystal display device for explaining a third example in which a feeding terminal to a reference electrode is formed.

[0284] FIG. 92 is a cross-sectional view of an essential part showing the feeding terminal portion of FIG. 91 in an enlarged manner.

[0285] FIG. 93 is a schematic cross-sectional view of the liquid crystal display device for explaining a fourth example in which a feeding terminal to a reference electrode is formed.

[0286] FIG. 94 is a schematic cross-sectional view of a liquid crystal display device for explaining a constitutional example of an outer periphery of an effective display region when an organic

insulation layer formed on the first substrate is constituted of color filters.

[0287] FIG. 95 is a schematic cross-sectional view of a liquid crystal display device for explaining another constitutional example of the outer periphery of the effective display region when the organic insulation layer formed on the first substrate is constituted of color filters.

[0288] FIG. 96 is a schematic cross-sectional view of a liquid crystal display device for explaining a constitutional example in which color filters are formed on all of a seal, an outer peripheral portion thereof and an effective display region.

[0289] FIGs. 97A – 97B are explanatory views of an alignment method when driving circuits are mounted on various lead terminals and feeding terminals which are formed on the first substrate.

[0290] FIG. 98 is a schematic cross-sectional view of a liquid crystal display device which is configured to prevent electrolytic corrosion of a reference electrode layer formed on the first substrate.

[0291] FIG. 99 is a schematic plan view for explaining an example in which color filters are formed when an organic insulation layer which is formed on the first substrate is constituted of the color filters.

[0292] FIG. 100 is a schematic plan view for explaining a constitutional example when an organic insulation layer which is formed on the first substrate is constituted of color filters.

[0293] FIG. 101 is a schematic plan view for explaining another constitutional example when an organic insulation layer which is formed on the first substrate is constituted of color filters.

[0294] FIG. 102 is a schematic plan view for explaining still another constitutional example when an organic insulation layer which is formed on the first substrate is constituted of color filters.

[0295] FIG. 103 is a schematic cross-sectional view showing an example of arrangement when the liquid crystal display device of the present invention is used as a transmission-type display module.

[0296] FIG. 104 is a schematic cross-sectional view for explaining another example of arrangement when the liquid crystal display device of the present invention is used as transmission-type display module.

[0297] FIG. 105 is a schematic cross-sectional view for explaining an example of arrangement when the liquid crystal display device of the present invention is used as a reflection-type display module.

[0298] FIG. 106 is a schematic cross-sectional view for explaining another example of arrangement when the liquid crystal display device of the present invention is used as a reflection-type display module.

[0299] FIG. 107 is a schematic cross-sectional view for explaining still another example of arrangement when the liquid crystal display device of the present invention is used as a reflection-type display module.

[0300] FIG. 108 is a schematic cross-sectional view for explaining still another example of arrangement when the liquid crystal display device of the present invention is used as a reflection-

type display module.

[0301] FIG. 109 is a schematic cross-sectional view for explaining still another example of arrangement when the liquid crystal display device of the present invention is used as a reflection-type display module.

[0302] FIG. 110 is a schematic cross-sectional view for explaining an example of arrangement when the liquid crystal display device of the present invention is used as a transmission/reflection-type display module.

[0303] FIG. 111 is a schematic cross-sectional view for explaining another example of arrangement when the liquid crystal display device of the present invention is used as a transmission/reflection-type display module.

EXPLANATION OF SYMBOLS

[0304] SUB1 . . . first substrate, SUB2 . . . second substrate, CF . . . color filter, BM . . . black matrix, CT . . . common electrode (or counter electrode), LC . . . liquid crystal (or liquid crystal layer), AL . . . orientation film, PAS . . . passivation layer, O-PAS(O-PAS1, O-PAS2) . . . organic insulation layer (first organic insulation layer, second organic insulation layer), SD1 . . . source electrode, SD2 . . . drain electrode, DL . . . drain line (or drain line layer), GL . . . gate line (or gate line layer), GI . . . gate insulation layer, SM . . . metal shield, ST . . . reference electrode (or reference electrode layer), PX . . . pixel electrode (or pixel electrode layer), TH (TH1, TH2) . . . through hole, AS . . . semiconductor layer, Cstg . . . holding capacity or a storage capacity, NGI . . . gate insulation layer removed region, OC . . . overcoat layer, TED . . . second reference electrode, ML . . . metal layer, XP . . . organic insulation layer removed region, CT/ST . . . counter/reference electrode layer, BL . . . backlight, FL . . . front light

DESCRIPTION OF THE PREFERRED EMBODIMENTS

[0305] Preferred embodiments of the present invention are explained in detail hereinafter in conjunction with drawings which show the embodiments.

[0306] FIG. 1 is a plan view of the vicinity of one pixel of a vertical field type liquid crystal display device for schematically explaining the pixel constitution of the first embodiment of the present invention. In the drawings, reference symbol PX indicates a pixel electrode, DL indicates drain lines (video signal lines or data lines), GL indicates gate lines (scanning lines), SM indicates a light shielding film (metal shield) which performs light shielding between the pixel electrode and the drain line, ST indicates a reference electrode layer (also referred to as a conductive layer), SD1 indicates a source electrode, SD2 indicates a drain electrode, AS indicates a semiconductor layer, and TH indicates a through hole. Here, the above-mentioned gate lines, drain lines and respective electrodes are referred to as electrode layers when they are explained in conjunction with cross sections.

[0307] FIG. 2 is a cross-sectional view taken along a line I-I in FIG. 1 and FIG. 3 is also a cross-sectional view taken along a line II-II in FIG. 1. Reference symbol SUB1 indicates a first substrate, ST indicates a reference electrode layer, O-PAS indicates an organic insulation layer, PAS indicates a passivation layer, AL indicates orientation films, CT indicates a common electrode, CF indicates color filters, BM indicates a black matrix, and SUB2 indicates a second substrate.

[0308] In FIG. 1 to FIG. 3, in the liquid crystal display device, liquid crystal (also referred to as a liquid crystal layer hereinafter) LC is filled in a gap defined between the first substrate SUB1 and the second substrate SUB2 which face each other in an opposed manner. On an inner surface of the first substrate SUB1, a plurality of gate lines GL which extend in the first direction and are arranged parallel to each other and a plurality of drain lines GL which extend in the second direction crossing the gate lines and are arranged parallel to each other are formed.

[0309] Thin film transistors TFT which constitute switching elements are provided to crossing portions of the gate lines GL and drain lines DL. Each thin film transistor TFT is constituted of the gate electrode which is formed of the gate line GL, the drain electrode SD2 which extends from the drain line DL, the semiconductor layer AS and the source electrode SD1. In the embodiment described hereinafter, the explanation of the thin film transistor TFT is omitted.

[0310] The source electrode SD1 of the thin film transistor TFT is connected to the pixel electrode layer PX via the through hole TH. The pixel electrode layer PX is formed on the substantially whole portion of a pixel region thus constituting a display region of the liquid crystal display device. A multi-layered portion which forms the gate line GL, the drain line DL, the thin film transistor TFT and the pixel electrode PX including the pixel regions of the first substrate SUB1 is referred to as an electrode forming layer. Between this electrode forming layer and the first substrate side SUB1, the reference electrode layer ST which insulates the electrode forming layer with the organic insulation layer O-PAS is provided.

[0311] Here, including respective embodiments which will be explained later, an inorganic insulation layer may be used in place of the organic insulation layer as O-PAS. By adopting the organic insulation layer, the parasitic capacity between the reference electrode layer and the gate line GL as well as the drain line DL can be further reduced.

[0312] With respect to the above-mentioned electrode forming layer, above the organic insulation layer O-PAS, the gate line layer GL, the gate insulation layer GI, the drain line layer DL, the thin film transistor TFT, the passivation layer PAS and the pixel electrode layer PX are formed in this order. Then, a holding capacity of the pixel (so-called Cstg) is formed between the pixel electrode layer PX and the reference electrode layer ST. That is, the holding capacity is formed between the pixel electrode layer PX and the reference electrode layer ST using the passivation layer PAS, the gate insulation layer GI and the organic insulation layer O-PAS as dielectrics. The reference electrode layer ST is formed over a wide area such that the reference electrode layer ST covers the whole pixel region.

[0313] As material of the organic insulation layer O-PAS, polysilazane can be used, for example. This material is coated using a SOG (Spin-On-Glass) method. The organic film material having low dielectric constant is effective for reducing the parasitic capacitance between lines. For example, various organic material such as, polyimide, polyamide, polyimide amide, acrylic resin, polyacrylic resin and benzocyclobutene can be used. Further, since it is necessary to make the transmission-type liquid crystal display device have the sufficient light transmitting characteristics, it is desirable to increase the light transmissivity. It is effective to utilize existing material layers to effectively enhance the light transmissivity. That is, when the color filter layers are utilized as the above-mentioned organic insulation layer, the light transmissivity is hardly impeded. To reduce the formation process of the organic insulation layer, it is desirable that the layer material has photosensitivity. The same goes for respective embodiments described later with respect to this point.

[0314] This is because that with the constitution which forms the through hole below the gate insulation layer, the number of photolithography processes can be reduced. Further, when the through hole is formed in the organic insulation layer at a position equal to the position of the through hole formed in the gate insulation layer, at the time of forming the thorough hole from the gate insulation layer or the insulation layer arranged above the gate insulation layer, patterning or collective forming which uses the upper insulation layer as a mask can be adopted and hence, it is not always necessary to make the layer material photosensitive. However, products of various constitutions are usually manufactured using the same process and the same material and hence, to produce a large kinds of products using the same manufacturing line, it is desirable to use material having photosensitivity. The same goes for respective embodiments which will be explained later with respect to this point as well.

[0315] Further, the film thickness of the organic insulation layer O-PAS can be easily set for each constitution by performing simulation based on disclosed contents of embodiments described later by those who are skilled in the art. That is, the film thickness can be calculated based on characteristics curves obtained from values on the planar structure or the cross-sectional structure of the substrates, the dielectric constant of the organic insulation layer and the like. By utilizing the calculated film thickness, the actual film thickness can be set by selecting the film thickness for each product or the range corresponding to the design concept with respect to the wiring resistance, the performance of peripheral driving circuits, using liquid crystal material, the target quality and the like. The same goes for respective embodiment which will be explained later.

[0316] Due to such a constitution, the feeding resistance with respect to the holding capacity is largely reduced so that it is possible to obtain the liquid crystal display device which satisfies both of the enhancement of the numerical aperture of the pixel and the assurance of the holding capacity. Since it is unnecessary to provide the feeding line to the pixel region, the numerical aperture of the pixel can be enhanced. Further, storage capacities can be formed by the passivation layer formed

between the pixel electrode and the reference electrode layer, the gate insulation layer and the organic insulation layer which exhibits the small dielectric constant. Compared to a case in which only the organic insulation layer is formed, the distance from the liquid crystal layer to the reference electrode layer can be largely increased and hence, the influence of the electric field of the reference electrode layer to the electric field for driving the liquid crystal can be reduced.

[0317] Further, in this embodiment, the reference electrode layer ST may be configured such that the reference electrode layer ST extends parallel to the extending direction of the gate line GL and is overlapped to the region where the pixel electrode is formed. Due to such a constitution, the capacity between the gate line GL and the reference electrode layer can be reduced so that the increase of the parasitic capacity is suppressed and the potential can be stabilized.

[0318] FIG. 4 is a plan view of the vicinity of one pixel of a vertical field type liquid crystal display device for schematically explaining the pixel constitution of the second embodiment of the present invention, FIG. 5 is a cross-sectional view taken along a line I-I in FIG. 4, and FIG. 6 is a cross-sectional view taken along a line II-II in FIG. 4. Reference symbols in the drawings which are equal to those of the previous embodiment indicate identical functioning portions.

[0319] In this embodiment, the reference electrode layer ST has a region which includes regions where the gate line layer GL, the drain line DL and the pixel electrode layer PX of the first substrate SUB1 are formed. The holding capacity is formed between the pixel electrode layer PX and the reference electrode layer ST. According to this embodiment, since the reference electrode layer ST is formed below the gate line layer GL, it is desirable to set the thickness of the organic insulation layer O-PAS to equal to or more than 1 μm, for example, by taking the parasitic capacity of both electrode layers into account.

[0320] Due to such a constitution, in addition to advantageous effects similar to those of the first embodiment, since the reference electrode layer ST is formed of a so-called matted electrode, the feeding resistance can be further reduced and the limitation imposed on the feeding direction can be eliminated.

[0321] FIG. 7 is a plan view of the vicinity of one pixel of a vertical field type liquid crystal display device for schematically explaining the pixel constitution of the third embodiment of the present invention and FIG. 8 is a cross-sectional view taken along a line I-I in FIG. 7. Reference symbols in the drawings which are equal to those of the previous embodiments indicate identical functioning portions. With respect to the pixel forming layer, over the organic insulation layer O-PAS, the gate line layer GL, the gate insulation layer GI, the drain line layer DL, the thin film transistor TFT, the passivation layer PAS and the pixel electrode PX are formed in this order. The whole or a portion of the pixel electrode PX in the pixel region penetrates the passivation layer PAS and is brought into contact with the gate insulation layer GI.

[0322] Due to such a constitution of this embodiment, in addition to the advantageous effects obtained by respective embodiments, the storage capacity formed between the reference electrode

layer ST and the pixel electrode PX can be adjusted by the area of the pixel electrode PX which penetrates the passivation layer PAS.

[0323] FIG. 9 is a cross-sectional view taken along a line I-I in FIG. 8 of the vicinity of a pixel in a vertical field type liquid crystal display device for schematically explaining the pixel constitution of the fourth embodiment of the present invention. Reference symbols in the drawings which are equal to those of the previous embodiments indicate identical functioning portions.

[0324] With respect to the pixel forming layer, over the organic insulation layer O-PAS, the gate line layer GL, the gate insulation layer GI, the drain line layer DL, the thin film transistor TFT, the passivation layer PAS and the pixel electrode PX are formed in this order. The whole or a portion of the pixel electrode PX in the pixel region penetrates the passivation layer PAS and the gate insulation layer GL and is brought into contact with the organic insulation layer O-PAS.

[0325] Due to such a constitution of this embodiment, the storage capacity formed between the reference electrode layer ST and the pixel electrode PX can be adjusted by the area of the pixel electrode PX which penetrates the passivation layer PAS and the gate insulation layer GI.

[0326] FIG. 10 is a plan view of the vicinity of one pixel of a vertical field type liquid crystal display device for schematically explaining the pixel constitution of the fifth embodiment of the present invention. This embodiment is a modification of the above-mentioned fourth embodiment, wherein the gate insulation layer GI is eliminated at a portion within the region of the pixel electrode PX. Advantageous effects obtained by this embodiment is similar to those obtained by the fourth embodiment. Further, due to devoid of the gate insulation layer GI, the transmissivity is enhanced.

[0327] FIG. 11 is a plan view of the vicinity of one pixel of a vertical field type liquid crystal display device for schematically explaining the pixel constitution of the sixth embodiment of the present invention. In this embodiment, the thin film transistor TFT includes the source electrode SD1 over the gate insulation layer GI, wherein the source electrode SD1 is connected to the pixel electrode PX via the through hole TH formed in the passivation layer PAS and a portion of the source electrode SD1 is expanded to the inside of the region of the pixel electrode PX. It is preferable to expand the source electrode SD1 as an extension portion SD1E which extends along the gate line GL or the drain line DL.

[0328] Due to the constitution of this embodiment, in addition to the advantageous effects obtained by respective embodiments, it is possible to adjust the storage capacity by changing the length or the width of the extension portion SD1E of the source electrode SD1, that is, by changing the area of the source electrode SD1 which overlaps the pixel electrode PX.

[0329] FIG. 12 is a plan view of the vicinity of one pixel of a vertical field type liquid crystal display device for schematically explaining the pixel constitution of the seventh embodiment of the present invention, FIG. 13 is a cross-sectional view taken along a line I-I in FIG. 12, and FIG. 14 is a cross-sectional view taken along a line II-II in FIG. 12. Reference symbols in the drawings

which are equal to those of the previous embodiments indicate identical functioning portions.

[0330] With respect to the liquid crystal display device of this embodiment, between the electrode forming layer which is constituted of the gate line layer GL, the drain line layer DL, the thin film transistor TFT and the pixel electrode PX including the pixel regions of the first substrate SUB1 and the first substrate SUB1 side, the reference electrode layer ST which is insulated by the first organic insulation layer O-PAS1 with respect to the electrode forming layer is provided. The pixel forming layer is configured such that the gate line layer GL, the gate insulation layer GI, the drain line layer DL, the thin film transistor TFT, the passivation layer PAS, the second organic insulation layer O-PAS2 and the pixel electrode PX are formed over the organic insulation layer O-PAS1 in this order. The holding capacity of the pixel is formed between the pixel electrode PX and the reference electrode layer ST.

[0331] Due to such a constitution of this embodiment, the numerical aperture of the pixel is enhanced and the feeding resistance can be reduced because of the large area of the conductive layer. Further, when the organic insulation layer is also formed over the switching element, it is possible to overlap the pixel electrode and the drain line to each other so that the numerical aperture is further enhanced. When the pixel electrode and the drain line overlap each other, it is possible to eliminate a light shielding layer between the vicinity in the extension direction of the drain line and the pixel electrode so that the numerical aperture is still further enhanced.

[0332] Further, the above-mentioned reference electrode layer ST is formed in the extension direction of the gate line layer GL such that the reference electrode layer ST is arranged parallel to the gate line layer GL and overlaps the region where the pixel electrode layer PX is formed. Accordingly, the parasitic capacity between the gate line layer and the conductive layer is reduced and the potential can be made stable.

[0333] Still further, the reference electrode layer is provided to the region of the above-mentioned first substrate SUB1 which includes the region where the gate line layer GL, the drain line layer DL and the pixel electrode layer PX are formed. Due to such a constitution, since the reference electrode layer ST is formed of a so-called matted electrode, the feeding resistance can be further reduced and the limitation imposed on the feeding direction can be eliminated.

[0334] FIG. 15 is a plan view of the vicinity of one pixel of a vertical field type liquid crystal display device for schematically explaining the pixel constitution of the eighth embodiment of the present invention, FIG. 16 is across-sectional view taken along a line I-I in FIG. 15, and FIG. 17 is a cross-sectional view taken along a line II-II in FIG. 15. Reference symbols in the drawings which are equal to those of the previous embodiments indicate identical functioning portions.

[0335] In this embodiment, the above-mentioned first organic insulation layer is constituted of the color filters CF. Accordingly, the holding capacity is formed by the organic insulation layer O-PAS, the passivation layer PAS, the gate insulation layer DI and the color filter layers CF which are formed between the pixel electrode layer PX and the reference electrode layer ST and hence,

the increase of the parasitic capacity between the reference electrode layer and the gate line as well as the drain line can be suppressed. Further, since the color filter layers CF are formed on the first substrate SUB1, the tolerance of alignment of the first substrate SUB1 with the second substrate SUB2 is increased whereby the numerical aperture of the pixel is enhanced and the feeding resistance can be reduced due to large area of the conductive layer.

[0336] FIG. 18 is a cross-sectional view taken along a line I-I in FIG. 15 of a vertical field type liquid crystal display device for schematically explaining the pixel constitution of the ninth embodiment of the present invention and FIG. 19 is a cross-sectional view taken along a line II-II in FIG. 18. Reference symbols in the drawings which are equal to those of the previous embodiments indicate identical functioning portions.

[0337] In the embodiment shown in FIG. 17, the black matrix BM which performs light-shielding of boundaries of the color filters CF is formed on the second substrate SUB2 side. In this embodiment, the black matrix BM is formed on the first substrate SUB1 side.

[0338] Further, in the eighth embodiment and the ninth embodiment, the above-mentioned reference electrode layer ST is formed in the extension direction of the gate line layer GL such that the reference electrode layer ST is arranged parallel to the gate line layer GL and overlaps the region where the pixel electrode layer PX is formed.

[0339] Due to such a constitution, the parasitic capacity formed between the gate line layer GL and the reference electrode layer ST can be reduced. Further, it is possible to stabilize the potential.

[0340] Further, by forming the reference electrode layer ST as a so-called matted electrode which is provided to a region of the first substrate SUB1 which includes a region where the gate line layer GL, the drain line layer DL and the pixel electrode layer PX are formed, the feeding resistance can be further reduced and the limitation imposed on the feeding direction can be eliminated.

[0341] Further, an overcoat layer which levels the color filter layers CF may be formed between the color filter layers CF and the gate insulation layer GI. Here, the reference electrode layer ST may be formed between the color filter layers CF and the gate insulation layer GI.

[0342] FIG. 20 is a plan view of the vicinity of one pixel of a vertical field type liquid crystal display device for schematically explaining the pixel constitution of the tenth embodiment of the present invention and FIG. 21 is a cross-sectional view taken along a line III-III in FIG. 20. Reference symbols in the drawings which are equal to those of the previous embodiments indicate identical functioning portions.

[0343] In this embodiment, between the electrode forming layer which is constituted of the gate line layer GL, the drain line layer DL, the thin film transistor TFT, and the pixel electrode layer PX including the pixel regions of the first substrate SUB1 and the first substrate side SUB1, the first reference electrode layer ST which is insulated by the first organic insulation layer O-PAS1 with respect to the electrode forming layer is formed. Further, over the first organic insulation layer O-PAS1, the gate line layer GL, the gate insulation layer GI, the drain line layer DL, the thin

film transistor TFT, the passivation layer PAS, the second organic insulation layer O-PAS2, and the pixel electrode layer PX are formed in this order. A capacitive electrode layer TED which is connected to the pixel electrode PX is formed between the second organic insulation layer O-PAS2 and the passivation layer PAS.

[0344] FIG. 22 is a cross-sectional view taken along a line III-III in FIG. 20 for schematically explaining the pixel constitution of the eleventh embodiment of the present invention Reference symbols in the drawings which are equal to those of the previous embodiments indicate identical functioning portions. In this embodiment, the capacitive electrode layer TED shown in FIG. 21 is formed above the gate insulation layer GI and below the second organic insulation layer O-PAS2.

[0345] FIG. 23 is a cross-sectional view taken along a line III-III in FIG. 20 for schematically explaining the pixel constitution of the twelfth embodiment of the present invention. Reference symbols in the drawings which are equal to those of the previous embodiments indicate identical functioning portions. In this embodiment, the capacitive electrode layer TED shown in FIG. 21 or FIG. 22 is formed above the first organic insulation layer O-PAS1 and below the gate insulation layer GI.

[0346] Due to the constitutions of the above-mentioned tenth, eleventh and twelfth embodiments, the numerical aperture of the pixel can be enhanced and the feeding resistance can be reduced because of the large area of conductive layer. Further, the storage capacity can be adjusted by the area and shape of the capacitive electrode layer TED. Further, when the organic insulation layer is also formed above the thin film transistor, it is possible to make the pixel electrode and the drain line overlap each other so that the numerical aperture can be further enhanced. When the pixel electrode and the drain line overlap each other, a light shielding layer formed between the vicinity in the extension direction of the drain line and the pixel electrode can be eliminated so that the numerical aperture can be further enhanced.

[0347] Here, the first reference electrode layer ST can be formed in the extension direction of the gate line layer GL such that the first reference electrode layer ST is arranged parallel to the gate line layer GL and overlaps the region where the pixel electrode layer PX is formed. Due to such a constitution, the parasitic capacity formed between the gate line layer GL and the first reference electrode layer ST can be reduced whereby the increase of storage capacity can be suppressed or the potential can be stabilized.

[0348] Further, the first reference electrode layer ST may be formed on a region of the first substrate SUB1 which includes the region where the gate line layer GL, the drain line layer DL and the pixel electrode layer PX are formed. Due to such a constitution, since the first reference electrode layer ST is constituted of a so-called matted electrode, the feeding resistance is further reduced and the limitation imposed on the feeding direction can be eliminated.

[0349] FIG. 24 is a plan view of the vicinity of one pixel of a vertical field type liquid crystal display device for schematically explaining the pixel constitution of the thirteenth embodiment of

the present invention and FIG. 25 is a cross-sectional view taken along a line III-III in FIG. 24. Reference symbols in the drawings which are equal to those of the previous embodiments indicate identical functioning portions. In this embodiment, for example, the capacitive electrode layer TED explained in conjunction with FIG. 20 to FIG. 23 is formed between the passivation layer PAS and the second organic insulation layer O-PAS in the pixel region and is connected to the pixel electrode layer PX via the through hole TH2.

[0350] That is, the thin film transistor TFT includes the source electrode which is connected to the pixel electrode PX via the through hole TH1 formed in the passivation layer PAS on the gate insulation layer GI, and the capacitive electrode layer TED is connected to the source electrode SD1 and is provided to the region where the pixel electrode PX is formed.

[0351] Due to such a constitution, the holding capacity can be adjusted by changing the size of the above-mentioned capacitive electrode layer TED. Here, the first organic insulation layer O-PAS may be formed of color filters.

[0352] Due to such a constitution, the numerical aperture of the pixel can be enhanced and the feeding resistance can be reduced because of the large area of the conductive layer. Further, when the holding capacity is formed by the organic insulation layer O-PAS having small dielectric constant, the passivation layer PAS, the gate insulation layer GI and the color filter layer CF formed between the pixel electrode PX and the reference electrode layer ST, the increase of parasitic capacity can be suppressed. Further, since the color filter layers CF are formed on the first substrate SUB1, the tolerance of alignment of the first substrate SUB1 with the second substrate SUB2 can be increased.

[0353] FIG. 26 is a cross-sectional view taken along a line III-III in FIG. 24 of the vicinity of one pixel of a vertical field type liquid crystal display device for schematically explaining the pixel constitution of the fourteenth embodiment of the present invention. Reference symbols in the drawings which are equal to those of the previous embodiments indicate identical functioning portions. In this embodiment, the capacitive electrode layer TED is provided over the gate insulation layer GI. The pixel electrode PX is connected to the capacitive electrode layer TED via the through hole TH2 formed in the second organic insulation layer O-PAS2 and the passivation layer PAS.

[0354] FIG. 27 is a cross-sectional view taken along a line III-III in FIG. 24 of the vicinity of one pixel of a vertical field type liquid crystal display device for schematically explaining the pixel constitution of the fifteenth embodiment of the present invention. Reference symbols in the drawings which are equal to those of the previous embodiments indicate identical functioning portions. In this embodiment, the capacitive electrode layer TED is provided over the first organic insulation layer O-PAS. The pixel electrode PX is connected to the capacitive electrode layer TED via the through hole TH2 which is formed such that the through hole TH2 penetrates the second organic insulation layer O-PAS2, the passivation layer PAS and the gate insulation layer GI.

[0355] Due to the constitutions of the above-mentioned thirteenth to fifteenth embodiments, the holding capacity formed between the conductive layer and the pixel electrode PX can be adjusted by changing the area of the capacitive electrode layer TED.

[0356] Further, the first organic insulation layer O-PAS1 in the thirteenth to fifteenth embodiments may be formed of color filters.

[0357] Due to such a constitution, the numerical aperture of the pixel can be enhanced and the feeding resistance can be reduced because of the large area of the conductive layer. Further, when the color filter layers CF are formed on the first substrate SUB1, the tolerance of alignment of the first substrate SUB1 with the second substrate SUB2 can be increased.

[0358] FIG. 28 is a plan view of the vicinity of one pixel of a vertical field type liquid crystal display device for schematically explaining the pixel constitution of the sixteenth embodiment of the present invention and FIG. 29 is a cross-sectional view taken along a line III-III in FIG. 28. Reference symbols in the drawings which are equal to those of the previous embodiments indicate identical functioning portions. In this embodiment, between the electrode forming layer which is constituted of the gate line GL, the drain line DL, the switching element or thin film transistor TFT, and the pixel electrode PX including the pixel regions of the first substrate SUB1 and the first substrate SUB1 side, the first reference electrode layer ST which is insulated by the organic insulation layer O-PAS with respect to the electrode forming layer is formed.

[0359] Further, with respect to the above-mentioned electrode forming layer, over the above-mentioned organic insulation layer O-PAS, the gate line layer GL, the gate insulation layer GI, the drain line layer DL, the thin film transistor TFT, the passivation layer PAS, and the pixel electrode layer PX are formed in this order. A capacitive electrode layer TED which is connected to the pixel electrode layer PX is formed between the organic insulation layer O-PAS and the passivation layer PAS. Still further, the holding capacity of the pixel is formed between the pixel electrode layer PX and the first reference electrode layer ST as well as the capacitive electrode layer TED.

[0360] As shown in FIG. 29, the capacitive electrode layer TED is provided above the gate insulation layer GI and the source electrode SD1 is connected to the capacitive electrode layer TED. The switching element TFT includes the source electrode SD1 which is connected to the pixel electrode PX via the through hole TH formed in the passivation layer PAS over the gate insulation layer GI, and the capacitive electrode layer TED is formed in the pixel region in such a manner that the capacitive electrode layer TED is connected to the source electrode SD1.

[0361] Due to such a constitution, the storage capacity can be adjusted by changing the size of the above-mentioned capacitive electrode layer TED. Further, the organic insulation layer O-PAS may be formed of color filter layers.

[0362] Due to such a constitution of this embodiment, the numerical aperture of the pixel can be enhanced and the feeding resistance can be reduced because of the large area of the conductive layer. The holding capacity can be adjusted by changing the size of the capacitive electrode layer

TED. Further, when the color filter layers CF are formed on the first substrate SUB1, the tolerance of alignment of the first substrate SUB1 with the second substrate SUB2 can be increased.

[0363] FIG. 30 is a cross-sectional view taken along a line III-III in FIG. 28 of the vicinity of one pixel of a vertical field type liquid crystal display device for schematically explaining the pixel constitution of the seventeenth embodiment of the present invention. Reference symbols in the drawings which are equal to those of the previous embodiments indicate identical functioning portions. In this embodiment, the capacitive electrode layer TED is provided over the organic insulation layer O-PAS and the source electrode SD1 is connected to the capacitive electrode layer TED via the through hole TH which penetrates the gate insulation layer GI.

[0364] Due to such a constitution, the holding capacity formed between the capacitive electrode layer TED and the pixel electrode PX can be adjusted based on the area of pixel electrode PX which penetrates the passivation layer PAS and the gate insulation layer GI. Further, the organic insulation layer O-PAS may be formed of color filter layers.

0365] Due to such a constitution of this embodiment, the numerical aperture of the pixel can be enhanced and the feeding resistance can be reduced because of the large area of the first reference electrode layer. Further, when the organic insulation layer is formed of color filter layers, the tolerance of alignment of the first substrate SUB1 with the second substrate SUB2 can be increased.

[0366] FIG. 31 is a plan view of the vicinity of one pixel of a vertical field type liquid crystal display device for schematically explaining the pixel constitution of the eighteenth embodiment of the present invention and FIG. 32 is a cross-sectional view taken along a line III-III in FIG. 31. Reference symbols in the drawings which are equal to those of the previous embodiments indicate identical functioning portions. In this embodiment, the capacitive electrode layer TED is provided over the gate insulation layer GI and the pixel electrode layer PX is connected to the capacitive electrode layer TED via the through hole TH2 which penetrates the passivation layer PAS. Further, the organic insulation layer O-PAS may also be formed of color filter layers.

[0367] Due to such a constitution of this embodiment, the holding capacity formed between the first reference electrode layer ST and the pixel electrode layer PX can be adjusted by changing the area of the capacitive electrode layer TED. Further, the organic insulation layer O-PAS may be also formed of color filter layers.

[0368] FIG. 33 is a cross-sectional view taken along a line III-III in FIG. 31 of the vicinity of one pixel of a vertical field type liquid crystal display device for schematically explaining the pixel constitution of the nineteenth embodiment of the present invention. Reference symbols in the drawings which are equal to those of the previous embodiments indicate identical functioning portions. In this embodiment, the capacitive electrode layer TED is provided over the organic insulation layer O-PAS and the pixel electrode layer PX is connected to the capacitive electrode layer TED via the through hole TH2 which penetrates the passivation layer PAS and the gate insulation layer GI.

[0369] Due to such a constitution of this embodiment, the holding capacity formed between the first reference electrode layer ST and the pixel electrode layer PX can be adjusted by changing the area of the capacitive electrode layer TED. Further, the organic insulation layer O-PAS may be also formed of color filter layers.

[0370] FIG. 34 is a plan view of the vicinity of one pixel of a vertical field type liquid crystal display device for schematically explaining the pixel constitution of the twentieth embodiment of the present invention and FIG. 35 is a cross-sectional view taken along a line III-III in FIG. 34. Reference symbols in the drawings which are equal to those of the previous embodiments indicate identical functioning portions. In this embodiment, the capacitive electrode layer TED is provided over the first organic insulation layer O-PAS and the capacitive electrode layer TED is connected to the first reference electrode layer ST via the through hole TH2 which penetrates the first organic insulation layer O-PAS1.

[0371] Due to such a constitution, the storage capacity is adjusted by changing the area of capacitive electrode layer TED which is connected to the first reference electrode layer ST. Further, when color filter layers CF are formed on the first substrate SUB1, the tolerance of alignment of the first substrate SUB1 with the second substrate SUB2 can be increased.

[0372] FIG. 36 is a cross-sectional view taken along a line III-III in FIG. 34 of the vicinity of one pixel of a vertical field type liquid crystal display device for schematically explaining the pixel constitution of the twenty-first embodiment of the present invention. Reference symbols in the drawings which are equal to those of the previous embodiments indicate identical functioning portions. In this embodiment, the capacitive electrode layer TED is provided over the gate insulation layer GI and the capacitive electrode layer TED is connected to the first reference electrode layer ST via the through hole TH2 which penetrates the gate insulation layer GI.

[0373] Due to such a constitution of this embodiment, the storage capacity can be adjusted by changing the area of the capacitive electrode layer which is connected to the first reference electrode layer ST. Further, when the color filter layers CF are formed on the first substrate SUB1, the tolerance of alignment of the first substrate SUB1 with the second substrate SUB2 can be increased.

[0374] FIG. 37 is a cross-sectional view taken along a line III-III in FIG. 34 of the vicinity of one pixel of a vertical field type liquid crystal display device for schematically explaining the pixel constitution of the twenty-second embodiment of the present invention. Reference symbols in the drawings which are equal to those of the previous embodiments indicate identical functioning portions. In this embodiment, the capacitive electrode layer TED is provided over the passivation layer PAS and the capacitive electrode layer TED is connected to the first reference electrode layer ST via the through hole TH2 which penetrates the passivation layer PAS, the gate insulation layer GI and the first organic insulation layer O-PAS1.

[0375] Due to such a constitution of this embodiment, the storage capacity which is formed

between the conductive layer and the pixel electrode PX can be adjusted by changing the area of the capacitive electrode layer TED which is connected to the first reference electrode layer ST. Further, when the color filter layers CF are formed on the first substrate SUB1, the tolerance of alignment of the first substrate SUB1 with the second substrate SUB2 can be increased.

[0376] Further, due to such a constitution of this embodiment, the numerical aperture can be enhanced and the feeding resistance can be reduced because of the large area of the conductive layer. Further, when the first organic insulation layer O-PAS1 is formed of color filters, the tolerance of alignment of the first substrate SUB1 with the second substrate SUB2 can be increased.

[0377] FIG. 38 is a plan view of the vicinity of one pixel of a vertical field type liquid crystal display device for schematically explaining the pixel constitution of the twenty-third embodiment of the present invention and FIG. 39 is a cross-sectional view taken along a line III-III in FIG. 38. Reference symbols in the drawings which are equal to those of the previous embodiments indicate identical functioning portions. In this embodiment, the capacitive electrode layer TED is provided over the gate insulation layer GI and the capacitive electrode layer TED is connected to the first reference electrode layer ST via the through hole TH2 which penetrates the gate insulation layer GI and the organic insulation layer O-PAS.

[0378] Due to such a constitution of this embodiment, the holding capacity which is formed between the first reference electrode layer ST and the pixel electrode layer PX can be adjusted by changing the area of the capacitive electrode layer TED which is connected to the first reference electrode layer ST. Further, when the color filter layers CF are formed on the first substrate SUB1, the tolerance of alignment of the first substrate SUB1 with the second substrate SUB2 can be increased.

[0379] FIG. 40 is a cross-sectional view taken along a line III-III in FIG. 38 of the vicinity of one pixel of a vertical field type liquid crystal display device for schematically explaining the pixel constitution of the twenty-fourth embodiment of the present invention. Reference symbols in the drawings which are equal to those of the previous embodiments indicate identical functioning portions. In this embodiment, the capacitive electrode layer TED is provided over the organic insulation layer O-PAS and the capacitive electrode layer TED is connected to the first reference electrode layer ST via the through hole TH2 which penetrates the organic insulation layer O-PAS.

[0380] Due to such a constitution of this embodiment, the holding capacity which is formed between the first reference electrode layer ST and the pixel electrode layer PX can be adjusted by changing the area of the capacitive electrode layer TED which is connected to the first reference electrode layer ST. Further, when the color filter layers CF are formed on the first substrate SUB1, the tolerance of alignment of the first substrate SUB1 with the second substrate SUB2 can be increased.

[0381] FIG. 41 is a cross-sectional view taken along a line III-III in FIG. 38 of the vicinity of one pixel of a vertical field type liquid crystal display device for schematically explaining the pixel

constitution of the twenty-fifth embodiment of the present invention. Reference symbols in the drawings which are equal to those of the previous embodiments indicate identical functioning portions. In this embodiment, the capacitive electrode layer TED is provided over the gate insulation layer GI and, at the same time, the second capacitive electrode layer TEDD is formed on the organic insulation layer O-PAS. The pixel electrode PX is connected to the capacitive electrode layer TED by way of the through hole TH2 formed in the passivation layer PAS and, at the same time, the second capacitive electrode layer TEDD is connected to the first reference electrode layer ST via through hole TH3 formed in the organic insulation layer O-PAS.

[0382] Due to such a constitution of this embodiment, the holding capacity which is formed between the first reference electrode layer ST and the pixel electrode layer PX can be adjusted by changing the area of the capacitive electrode layer TED and the area of the second capacitive electrode layer TEDD. Further, when the color filter layers CF are formed on the first substrate SUB1, the tolerance of alignment of the first substrate SUB1 with the second substrate SUB2 can be increased.

[0383] FIG. 42 is a plan view of the vicinity of one pixel of a vertical field type liquid crystal display device for schematically explaining the pixel constitution of the twenty-sixth embodiment of the present invention and FIG. 43 is a cross-sectional view taken along a line III-III in FIG. 42. Reference symbols in the drawings which are equal to those of the previous embodiments indicate identical functioning portions. This embodiment describes a case in which the capacitive electrode layer TED in the above-mentioned respective embodiments is provided to the first substrate SUB1 and the organic insulation layer is formed of the color filter layers CF.

[0384] When the color filter layers CF are formed on the first substrate SUB1, since the color filters CF are not present at portions of the first substrate SUB1 corresponding to the through hole TH2, leaking of light is generated at this portions. To prevent such leaking of light, a metal-shielding film ML is formed over the through hole TH2 which connects the capacitive electrode TED with the first reference electrode layer ST and the capacitive electrode layer TED is connected to the first reference electrode layer ST through the metal light-shielding film ML.

[0385] FIG. 44 is a cross-sectional view taken along a line III-III in FIG. 42 of the vicinity of one pixel of a vertical field type liquid crystal display device for schematically explaining the pixel constitution of the twenty-seventh embodiment of the present invention. In this embodiment, the metal light-shielding film ML according to the above-mentioned twenty-sixth embodiment is provided over the capacitive electrode layer TED.

[0386] FIG. 45 is a plan view of the through hole TH2 and the metal light-shielding film ML according to the twenty-sixth embodiment or the twenty-seventh embodiment of the present invention. Respective sides of the metal light-shielding film ML are larger than corresponding sides of an opening portion of the through hole TH2 and are set to the size of at least equal to or more than 1 μm. Here, the same goes for a case in which an overcoat layer is formed on the color

filter layers CF.

[0387] FIGs. 46A – 46D are cross-sectional views of an essential part served for explaining the twenty-eighth embodiment of the present invention and for showing the cross-sectional structure of the through hole TH1 and the metal light-shielding film ML. In this embodiment, color filters CF are used as the organic insulation layer, the capacitive electrode layer TED is formed on the gate insulation layer which is, in turn, formed on the same layer as the source electrode SD1, and the source electrode SD1 is formed of the metal light-shielding film ML. This provision is made to cope with leaking of light at the through hole portion using the metal light-shielding film formed on the through hole portion. One example of such a constitution is explained taking a TH2 portion in FIG. 42 as an example. It is needless to say that other through holes may be used for performing light-shielding of through hole portions.

[0388] In FIG. 46A, the metal light-shielding film ML is formed such that the metal light-shielding film ML penetrates the through hole TH1 from the source electrode SD1 and is connected to the first reference electrode layer ST such that the capacitive electrode TED is formed over the source electrode SD1. In FIG. 46B, after forming the capacitive electrode layer TED in the through hole TH2, the metal light-shielding film ML is formed in the through hole TH1 from the source electrode SD1. In FIG. 46C, after forming the metal light-shielding film ML in the through hole TH1, the first reference electrode layer ST is connected to the reference electrode layer TED via the SD layer.

[0389] Further, in FIG. 46D, the metal light-shielding film ML is formed in the through hole TH and, after connecting the light-shielding metal film ML with the reference electrode layer ST, metal light-shielding film ML and the reference electrode layer TED are connected to each other.

[0390] In the above-mentioned respective embodiments, by forming the reference electrode layer (or the first reference electrode layer) ST in the extending direction of the gate line GL such that the layer is arranged parallel to the gate line GL and overlaps the region where the pixel electrode PX is formed, the increase of the parasitic capacity between the gate line layer GL and the reference electrode layer (or the first reference electrode layer) can be suppressed and the potential can be stabilized.

[0391] Further, in the above-mentioned respective embodiments, by forming the reference electrode layer (or the first reference electrode layer) ST in the region of the first substrate SUB1 which includes the region where the gate line GL, the drain line DL and the pixel electrode PX are formed, the reference electrode layer ST is formed of a so-called matted electrode and hence, the feeding resistance can be further reduced and the limitation imposed on the feeding direction can be eliminated.

[0392] Further, in the above-mentioned respective embodiments, by providing the light-shielding layer ML which performs light-shielding between the vicinity in the extension direction of the drain line DL and the pixel electrode PX, it is possible to prevent leaking of light between the drain

line DL and the pixel electrode PX.

[0393] FIG. 47 is a plan view of the vicinity of one pixel of an IPS type liquid crystal display device for schematically explaining the pixel constitution of the twenty-ninth embodiment of the present invention and FIG. 48 is a cross-sectional view taken along a line III-III in FIG. 47. Reference symbols in the drawings which are equal to those of the previous embodiments indicate identical functioning portions. In this embodiment, liquid crystal is inserted in a gap defined between a first substrate SUB1 and a second substrate SUB2 which face each other in an opposed manner. On an inner surface of the first substrate SUB1, a plurality of gate lines GL which extend in the first direction and are arranged parallel to each other and a plurality of drain lines GL which extend in the second direction which crosses the gate lines GL and are arranged parallel to each other, a plurality of thin film transistors which are arranged at crossing portions of the gate lines GL and the drain lines DL1 comb-shaped pixel electrodes PX which are driven by the thin film transistors TFT, and comb-shaped counter electrodes CT which generate electric fields for driving pixels between the counter electrodes CT and the pixel electrodes PX are formed.

[0394] The pixel electrodes PX and the counter electrodes CT may be formed on the same layer.

[0395] Further, between an electrode forming layer which is constituted of the gate line GL, the drain line DL, the thin film transistor TFT and the pixel electrode PS including a pixel region of the first substrate SUB1 and the first substrate SUB1 side, a reference electrode layer ST which is insulated by an organic insulation layer O-PAS with respect to the electrode forming layer is provided and holding capacity of the pixel is formed between the pixel electrode PX and the reference electrode layer ST.

[0396] Further, the counter electrode CT is formed over the organic insulation layer O-PAS and the counter electrode CT is connected to the reference electrode layer ST via a through hole TH formed in the organic insulation layer O-PAS.

[0397] Due to such a constitution of this embodiment, it is possible to form the sufficient holding capacity and hence, the image quality can be stabilized and enhanced. Further, since it is unnecessary to increase the area of the pixel electrode PX for forming the holding capacity, the numerical aperture can be enhanced. Still further, since the area of the reference electrode layer ST is large, the feeding resistance can be reduced.

[0398] FIG. 49 is a cross-sectional view taken along a line IV-IV in FIG. 47 of the vicinity of one pixel of the IPS type liquid crystal display device for schematically explaining the pixel constitution of the thirtieth embodiment of the present invention. The counter electrode CT is formed over a gate insulation layer GI and the counter electrode CT is connected to the reference electrode layer ST via the through hole TH formed in the gate insulation layer GI and the organic insulation layer O-PAS.

[0399] Due to such a constitution of this embodiment, holding capacity is formed between the pixel electrode PX and the reference electrode layer ST via the organic insulation layer O-PAS

having small dielectric constant. Since it is unnecessary to increase the area of the pixel electrode PX for forming the holding capacity, the numerical aperture is enhanced. Further, since the area of the reference electrode layer ST is large, the feeding resistance can be reduced.

[0400] FIG. 50 is across-sectional view taken along a line IV-IV in FIG. 47 of the vicinity of one pixel of the IPS type liquid crystal display device for schematically explaining the pixel constitution of the thirty-first embodiment of the present invention. In this embodiment, the counter electrode CT is formed over a passivation layer PAS and the counter electrode CT is connected to the reference electrode layer ST via a through hole TH formed in the passivation layer PAS, the gate insulation layer GI and the organic insulation layer O-PAS.

[0401] Due to such a constitution of this embodiment, holding capacity is formed between the pixel electrode PX and the reference electrode layer ST via the organic insulation layer O-PAS having small dielectric constant. Since it is unnecessary to increase the area of the pixel electrode PX for forming the holding capacity, the numerical aperture is enhanced. Further, since the area of the reference electrode layer ST is large, the feeding resistance can be reduced.

[0402] Further, in the above-mentioned twenty-ninth embodiment and the thirtieth embodiment, the reference electrode layer ST may be formed in the extension direction of the gate line GL such that the reference electrode layer ST is arranged parallel to the gate line GL and overlaps the region where the pixel electrode PX and the counter electrode CT are formed.

[0403] Due to such a constitution, the parasitic capacity formed between the gate line layer GL and the reference electrode layer ST can be reduced, the increase of the holding capacity is suppressed, and the potential can be stabilized.

[0404] Further, in the above-mentioned twenty-ninth embodiment and the thirtieth embodiment, the reference electrode layer ST may be formed in a region of the first substrate SUB1 which includes the region where the gate line layer GL, the drain line layer DL, the pixel electrode PX and the counter electrode CT are formed.

[0405] Due to such a constitution, since the reference electrode layer ST is formed of a so-called matted electrode, the feeding resistance can be further reduced and the limitation imposed on the feeding direction can be eliminated. Further, by increasing a layer thickness of the organic insulation layer O-PAS, the influence of the reference electrode layer ST to the liquid crystal driving electric field can be reduced. Color filters may be used in place of the organic insulation layer O-PAS. Further, when an overcoat layer is formed over the color filters, it is desirable to form the reference electrode layer ST below the color filter layer.

[0406] FIG. 51 is a plan view of the vicinity of one pixel of an IPS type liquid crystal display device for schematically explaining the pixel constitution of the thirty-second embodiment of the present invention and FIG. 52 is a cross-sectional view taken along a line V-V in FIG. 51. In this embodiment, a counter electrode CT is formed over an organic insulation layer O-PAS and extends to a neighboring pixel region by crossing the drain line DL and is connected to a reference

electrode layer of the neighboring pixel region via a through hole TH formed in the organic insulation layer O-PAS.

[0407] Due to such a constitution of this embodiment, even when the through hole TH is insufficiently formed, feeding electricity is performed through the reference electrode layer ST from the neighboring pixel side.

[0408] FIG. 53 is a cross-sectional view taken along a line V-V in FIG. 51 of the vicinity of one pixel of an IPS type liquid crystal display device for schematically explaining the pixel constitution of the thirty-third embodiment of the present invention. In this embodiment, a counter electrode CT is formed over a gate insulation layer GI and a capacitive electrode layer TED which crosses one drain line DL and extends to a neighboring pixel region is formed over the organic insulation layer O-PAS. The counter electrode layer CT is connected to a first reference electrode layer ST via a through hole TH formed in the gate insulation layer GI and the organic insulation layer O-PAS.

[0409] Due to such a constitution of this embodiment, even when the through hole TH is insufficiently formed, feeding of electricity is performed from the neighboring pixel side to the first reference electrode layer ST through the capacitive electrode layer TED. Further, by forming the through holes which connect each counter electrode and each reference electrode in a plural number for every pixel, the reliability of connection between electrode layers can be enhanced.

[0410] FIG. 54 is a cross-sectional view taken along a line V-V in FIG. 51 of the vicinity of one pixel of an IPS type liquid crystal display device for schematically explaining the pixel constitution of the thirty-fourth embodiment of the present invention. In this embodiment, a counter electrode CT is formed over a passivation layer PAS and a capacitive electrode layer TED which crosses one drain line DL and extends to a neighboring pixel region is formed over the organic insulation layer O-PAS. The counter electrode layer CT is connected to a first reference electrode layer ST via a through hole TH formed in the passivation layer PAS, the gate insulation layer GI and the organic insulation layer O-PAS.

[0411] Due to such a constitution of this embodiment, even when the through hole TH is insufficiently formed, feeding of electricity is performed from the neighboring pixel side through the capacitive electrode layer TED.

[0412] FIG. 55 is a cross-sectional view taken along a line V-V in FIG. 51 of the vicinity of one pixel of an IPS type liquid crystal display device for schematically explaining the pixel constitution of the thirty-fifth embodiment of the present invention. In this embodiment, a color filter layer CF is formed below the first reference electrode layer ST of the thirty-fourth embodiment shown in FIG. 54 and over the above-mentioned first substrate SUB1.

[0413] Due to such a constitution, in addition to the advantageous effects obtained by the previous embodiment, the color filter layer CF is isolated from the liquid crystal layer due to the first reference electrode layer ST and hence, the contamination of the liquid crystal due to constituent

material of the color filter layer CF can be prevented.

[0414] FIG. 56 is a plan view of the vicinity of one pixel of an IPS type liquid crystal display device for explaining a modification of the embodiments shown in FIG. 47 to FIG. 55. That is, the through holes TH which connect the counter electrode CT and the reference electrode ST of each pixel are formed in a plural number for each pixel so that the reliability of connection between these electrode layers can be enhanced.

[0415] FIG. 57 is a plan view of the vicinity of one pixel of an IPS type liquid crystal display device for schematically explaining the pixel constitution of the thirty-sixth embodiment of the present invention and FIG. 58 is a cross-sectional view taken along a line VI-VI in FIG. 57. In this embodiment, a counter electrode CT is formed over an organic insulation layer O-PAS such that the counter electrode CT is arranged parallel to the extension direction of a gate line GL and extends over a neighboring pixel region. Further, in each pixel region, the counter electrode CT is connected to a reference electrode ST in each pixel region via a through hole TH formed in the organic insulation layer O-PAS.

[0416] Due to such a constitution, holding capacity is formed at a portion where the counter electrode CT and the pixel electrode PX overlap each other and the gate insulation layer GI constitutes a dielectric of the holding capacity. This constitution is suitable for increasing the holding capacity.

[0417] FIG. 59 is a cross-sectional view taken along a line VI-VI in FIG. 57 of the vicinity of one pixel of an IPS type liquid crystal display device for schematically explaining the pixel constitution of the thirty-seventh embodiment of the present invention. In this embodiment, a counter electrode CT is formed over a gate insulation layer, for example, and a capacitive electrode layer TED is formed over an organic insulation layer O-PAS such that the capacitive electrode layer TED is arranged parallel to the extension direction of a gate line GL and extends over a pixel region disposed close to the organic insulation layer O-PAS. In each pixel region, the counter electrode CT is connected to a reference electrode layer ST via a through hole TH formed in the organic insulation layer O-PAS and a gate insulation layer GI in a penetrating manner. Further, holding capacity is formed at a portion where the capacitive electrode layer TED and the pixel electrode layer PX overlap each other.

[0418] Due to such a constitution, the gate insulation layer GI constitutes a dielectric of the holding capacity and forms a comb-shaped pixel electrode.

[0419] FIG. 60 is a plan view of the vicinity of one pixel of a modified IPS type liquid crystal display device for schematically explaining the pixel constitution of the thirty-eighth embodiment of the present invention, FIG. 61 is a cross-sectional view taken along a line VII-VII in FIG. 60, and FIG. 62 is a cross-sectional view taken along a line VIII-VIII in FIG. 60. In this embodiment, a pixel electrode PX is formed over a gate insulation layer GI in a so-called herringbone shape. A source electrode SD1 is formed over the gate insulation layer GI and a pixel electrode overlaps the

source electrode SD1. A counter electrode CT is formed over an organic insulation layer O-PAS and is connected to a reference electrode layer ST via a through hole TH2 thus forming holding capacity between the counter electrode CT and the above-mentioned pixel electrode PX.

[0420] Due to such a constitution of this embodiment, the gate insulation layer GI constitutes a dielectric of the holding capacity and hence, the reduction of holding capacity brought about by forming the pixel electrode in a herringbone shape can be increased.

[0421] FIG. 63 is a cross-sectional view taken along a line VII-VII in FIG. 60 of the vicinity of one pixel of a modified IPS type liquid crystal display device for schematically explaining the pixel constitution of the thirty-ninth embodiment of the present invention. In this embodiment, a source electrode SD1 is formed over a gate insulation layer GI and is connected to a pixel electrode PX formed over a passivation layer PAS via a through hole TH1. This embodiment is similar to the embodiment shown in FIG. 61 with respect to other constitutions.

[0422] Due to such a constitution, the gate insulation layer GI constitutes a dielectric of holding capacity.

0423] FIG. 64 is a plan view of a thin film transistor TFT portion of a modified IPS type liquid crystal display device for schematically explaining an essential part of the pixel constitution of the fortieth embodiment of the present invention. In this embodiment, holding capacity can be adjusted by changing an area of a source electrode SD1 of the thin film transistor TFT formed over a gate insulation layer GI.

[0424] The holding capacity can be adjusted in other embodiments of the present invention using such a concept.

[0425] FIG. 65 is a plan view of the vicinity of one pixel of a modified IPS type liquid crystal display device for schematically explaining an essential part of the pixel constitution of the forty-first embodiment of the present invention and FIG. 66 is a cross-sectional view taken along a line IX-IX in FIG. 65. In this embodiment, a pixel electrode PX Is formed over a gate insulation layer GI in a so-called herringbone shape. A source electrode SD1 is formed over the gate insulation layer GI and a pixel electrode overlaps the source electrode SD1. A reference electrode is formed below an organic insulation layer O-PAS and this reference electrode constitutes a reference/counter electrode layer ST/CT which also functions as a counter electrode. Holding capacity is formed between the reference/counter electrode layer ST/CT and the pixel electrode PX.

[0426] Due to such a constitution of this embodiment, it is possible to obtain a liquid crystal display device which can render the formation of the counter electrode layer CT unnecessary, can largely reduce the feeding resistance with respect to the holding capacity and prevents the reduction of numerical aperture of the pixel.

[0427] Further, the reference/counter electrode layer ST/CT is formed in the extension direction of the gate line GL such that the reference/counter electrode layer ST/CT is arranged parallel to

the gate line GL, for example, and overlaps a region where the pixel electrode PX is formed.

[0428] Due to such a constitution, it is unnecessary to provide an independent reference/counter electrode layer for every pixel so that capacity between the gate line layer GL and the reference/counter electrode layer ST/CT can be reduced, the increase of parasitic capacity can be suppressed, and the potential can be stabilized.

[0429] Further, the reference/counter electrode layer ST/CT is formed over the whole region of the first substrate SUB1 including a region where the gate line GL, the drain line DL and the pixel electrode PX are formed.

[0430] Due to such a constitution, the reference/counter electrode layer ST/CT constitutes a so-called matted electrode and hence, feeding resistance is further reduced and the limitation imposed on the feeding direction can be eliminated.

[0431] FIG. 67 is a cross-sectional view taken along a line IX-IX in FIG. 65 of the vicinity of one pixel of a modified IPS type liquid crystal display device for schematically explaining an essential part of the pixel constitution of the forty-second embodiment of the present invention. In this embodiment, a pixel electrode PX is formed over a gate insulation layer GI in a so-called herringbone shape. A source electrode SD1 is formed over the gate insulation layer GI and a pixel electrode overlaps the source electrode SD1. This embodiment corresponds to a constitution which is formed by wholly or partially removing an organic insulation layer O-PAS below the pixel electrode PX from the constitution shown in FIG. 66.

[0432] Due to such a constitution, the strength of an electric field generated between the pixel electrode PX and the reference/counter electrode layer ST/CT can be increased so that the driving voltage can be reduced.

[0433] FIG. 68 is a plan view of the vicinity of one pixel of a modified IPS type liquid crystal display device for schematically explaining an essential part of the pixel constitution of the forty-third embodiment of the present invention and FIG. 69 is a cross-sectional view taken along a line X-X in FIG. 68. In this embodiment, a counter electrode layer CT is formed over an organic insulation layer O-PAS and a connection line GLL which is arranged parallel to the extension direction of a gate line GL and is connected to a pixel electrode PX disposed close to the counter electrode CT is formed over the counter electrode layer CT.

[0434] FIG. 70 is a cross-sectional view taken along a line X-X in FIG. 68 of the vicinity of one pixel of a modified IPS type liquid crystal display device for schematically explaining an essential part of the pixel constitution of the forty-fourth embodiment of the present invention. In this embodiment, a connection line GLL which is arranged parallel to the extension direction of a gate line GL and is connected to a pixel electrode layer PX disposed close to a counter electrode layer CT is formed between the counter electrode layer CT and an organic insulation layer O-PAS.

[0435] Due to such constitutions of the forty-third embodiment and the forty-fourth embodiment, even when a through hole TH is formed insufficiently, feeding of electricity is performed from a

neighboring pixel side through a conductive layer. Further, by forming the through holes TH which connect each counter electrode layer CT and the each reference electrode ST in a plural number for every pixel, the reliability of connection between these electrode layers can be enhanced.

[0436] FIG. 71 is a plan view of the vicinity of one pixel of a modified IPS type liquid crystal display device for schematically explaining an essential part of the pixel constitution of the forty-fifth embodiment of the present invention and FIG. 72 is a cross-sectional view taken along a line XI-XI in FIG. 71. In this embodiment, the liquid crystal display device is provided with a reference/counter electrode layer ST/CT which functions as a reference electrode layer and also as a counter electrode and a portion of an organic insulation layer O-PAS in a pixel region is removed.

[0437] FIG. 73 is a cross-sectional view taken along a line XI-XI in FIG. 71 of the vicinity of one pixel of a modified IPS type liquid crystal display device for schematically explaining an essential part of the pixel constitution of the forty-sixth embodiment of the present invention. In this embodiment, a counter electrode CT is formed over an organic insulation layer O-PAS and a portion of the organic insulation layer O-PAS within a pixel region is removed.

[0438] Due to the constitutions of the forty-fifth embodiment and the forty-sixth embodiment, it is possible to form a plurality of regions which differ in driving voltage within the pixel region so that the liquid crystal display device can obtain a multi-domain effect.

[0439] FIG. 74 is a plan view of the vicinity of one pixel of another modified IPS type liquid crystal display device for schematically explaining an essential part of the pixel constitution of the forty-seventh embodiment of the present invention and FIG. 75 is a cross-sectional view taken along a line XII-XII in FIG. 74.

[0440] In this embodiment, the liquid crystal display device is constituted as follows. That is, liquid crystal is filled in a gap which is defined by a first substrate SUB1 and a second substrate SUB2 which face each other in an opposed manner. On an inner surface of the first substrate, at least a plurality of gate lines which extend in the first direction and are arranged in parallel to each other, a plurality of drain lines which extend in the second direction crossing the gate lines and are arranged parallel to each other, a plurality of switching element which are provided to crossing portions of the gate lines and drain lines, pixel electrode which are driven by the switching elements, and counter electrodes which generate electric fields for driving pixels between the pixel electrodes and the counter electrodes are formed. Pixel regions are constituted of a plurality of pixel electrodes.

[0441] Further, with respect to the shapes of these electrodes, the pixel electrode PX may be formed in a planar shape and the counter electrode CT may be formed in a herringbone shape. That is, in this embodiment, the electrodes may be configured to have shapes opposite to the shapes of electrodes shown in FIG. 60, FIG. 65, FIG. 68 or FIG. 71. In this case, it is possible to shield a leaked electric field from the gate line GL and the drain line DL by the counter electrode CT so that the further enhancement of image qualities can be realized.

[0442] Further, in this embodiment, between the electrode forming layer which is constituted of the gate line GL, the drain line DL, thin film transistor TFT, and the pixel electrode PX including the pixel regions of the first substrate SUB1 and the first substrate SUB1 side, the reference electrode layer ST which is insulated by the first insulation layer O-PAS1 with respect to the electrode forming layer is formed.

[0443] With respect to the electrode forming layer, over the organic insulation layer O-PAS1, the gate line GL, the gate insulation layer GI, the passivation layer PAS, the second organic insulation layer O-PAS2 and the counter electrode CT are laminated in this order. The counter electrode layer CT is shared by a pixel region disposed close to the pixel region in the extension direction of the gate line GL and a pixel region disposed close to the pixel region in the extension direction of drain line DL. Then, the counter electrode layer CT is connected to the reference electrode layer ST via a through hole TH which penetrates the second organic insulation layer O-PAS2, the passivation layer PAS, the gate insulation layer GI and the first organic insulation layer O-PAS1, thus forming holding capacity of the pixel between the pixel electrode PX and the reference electrode layer ST.

[0444] Due to the constitution of this embodiment, it is possible to shield leaking of electric field from the gate line GL and the drain line DL using the counter electrode CT and hence, the further enhancement of image qualities can be realized.

[0445] FIG. 76 is a cross-sectional view taken along a line XII-XII in FIG. 74 of the vicinity of one pixel of another modified IPS type liquid crystal display device for schematically explaining an essential part of the pixel constitution of the forty-eighth embodiment of the present invention. This embodiment includes a capacitive electrode layer TED which is connected to a reference electrode layer ST via through hole TH below a pixel electrode PX and is arranged between a first organic insulation layer O-PAS1 and a gate insulation layer GI.

[0446] Due to such a constitution, holding capacity can be increased and adjusted by changing an area of the capacitive electrode layer TED.

[0447] FIG. 77 is across-sectional view taken along a line XII-XII in FIG. 74 of the vicinity of one pixel of another modified IPS type liquid crystal display device for schematically explaining an essential part of the pixel constitution of the forty-ninth embodiment of the present invention. In this embodiment, a portion of a first organic insulation layer O-PAS1 which forms holding capacity below a pixel electrode PX is removed.

[0448] In such a constitution, due to devoid of the organic insulation layer having small dielectric constant, the holding capacity formed between the pixel electrode PX and the reference electrode layer ST can be increased.

[0449] FIG. 78 is a cross-sectional view taken along a line XII-XII in FIG. 74 of the vicinity of one pixel of another modified IPS type liquid crystal display device for schematically explaining an essential part of the pixel constitution of the fiftieth embodiment of the present invention. In

this embodiment, a portion of a second organic insulation layer O-PAS2 which is disposed above a pixel electrode PX and below a counter electrode CT is removed.

[0450] Also in this embodiment, due to devoid of the organic insulation layer having small dielectric constant, the holding capacity formed between the pixel electrode PX and the reference electrode layer ST can be increased.

[0451] FIG. 79 is a cross-sectional view taken along a line XII-XII in FIG. 74 of the vicinity of one pixel of another modified IPS type liquid crystal display device for schematically explaining an essential part of the pixel constitution of the fifty-first embodiment of the present invention. In this embodiment, a capacitive electrode layer TED is formed between a gate insulation layer GI and a first organic insulation layer O-PAS1 which are disposed below a pixel electrode PX. This capacitive electrode layer TED is connected to a counter electrode layer CT at a position not shown in the drawing. Further, the capacitive electrode TED may be formed parallel to the extension direction of the gate line GL and is shared in common by the pixels.

[0452] Due to such a constitution, the holding capacity can be increased or adjusted by changing an area of the capacitive electrode TED.

[0453] Embodiments of other constitutional portions of the liquid crystal display device of the present invention are explained hereinafter.

[0454] FIG. 80 is an explanatory view of the substrate constitution of the liquid crystal display device of the present invention. The liquid crystal display device PNL is constituted by laminating the first substrate SUB1 and the second substrate SUB2 having a size smaller than that of the first substrate SUB1 to each other by way of the liquid crystal. On one side of the first substrate SUB1 and another side of the first substrate SUB1 which is disposed close to one side, terminal regions (drain-line-side terminal region TMD, gate-line-side terminal region TMG) are formed. An effective display region is provided to the most portion of the second substrate SUB2 which is overlapped to the first substrate SUB1.

[0455] FIG. 81 is an explanatory view showing a state in which a tape carrier package loading a driving circuit thereon is mounted on the first substrate SUB1 at the terminal regions. A plurality of tape carrier packages TCP (tape carrier packages for driving drain lines which load drain-line driving circuit chips CH2, tape carrier packages for driving gate lines which load gate-line driving circuit chips CH1) are respectively mounted on the drain-line-side terminal region TMD and the gate-line-side terminal region TMG.

[0456] FIG. 82 is an explanatory view showing a state in which driving circuit chips are directly mounted on the first substrate SUB1 at the terminal regions. A plurality of drain-line driving circuit chips CH2 are mounted on the drain-line-side terminal region TMD and a plurality of gate-line driving circuit chips CH1 are mounted on the gate-line-side terminal region TMG. This mounting method is referred to as a FCA method (or a CPG method).

[0457] FIG. 83 is an explanatory view showing an arrangement example of liquid crystal filling

ports through which liquid crystal is filled into a gap defined by two substrates and is sealed thereafter. In this example, two liquid crystal filling ports INJ are formed in a side on which the driving circuit chips are not mounted. The number and mounting positions of the liquid crystal filling ports INJ are determined corresponding to the size of the liquid crystal display device PNL and may be one, three or more.

[0458] FIG. 84 is a schematic cross-sectional view of the liquid crystal display device of the present invention. On an inner surface of the first substrate SUB1, the reference electrode layer ST is formed and the organic insulation layer O-PAS is formed over the reference electrode layer ST. Other layers and electrodes are omitted from the drawing. The liquid crystal LC is sealed between the first substrate SUB1 and the second substrate SUB2 and a periphery of the effective display region is sealed by a sealing member.

[0459] FIGs. 85A -85C are plan views for schematically explaining the terminal regions of the gate driving circuit which is mounted in a tape carrier package method. In FIG. 85A to FIG. 85C, terminals of the driving circuit chip CH1 which are loaded on the tape carrier package TCP are connected to terminal portions of the gate lines which are pulled out to the first substrate SUB1 side. The connection to the reference electrode ST is performed by removing the organic insulation layer O-PAS. Portions where the organic insulation layer O-Pas is removed are indicated by XP. FIG. 85A indicates a state in which the removing portions XP are arranged at the outside of the sealing member SL and below the tape carrier package TCP.

[0460] FIG. 85B shows a state in which the removing portion XP of the organic insulation layer O-PAS is disposed at the outside of the sealing member SL and at positions away from the tape carrier package TCP. Further, FIG. 85C shows a state in which the removing portion XP of the organic insulation layer O-PAS is arranged at the inside of the sealing member SL.

[0461] FIGs. 86A -86B are plan views for schematically explaining the terminal region on which the driving circuit chip is mounted by a FCA method. FIG. 86A indicates a state in which the organic insulation layer O-PAS is removed at the outside of the sealing member SL and a feeding terminal of the driving circuit chip for the reference electrode layer is connected at this removing portion XP. FIG. 86B shows a state in which the organic insulation layer O-PAS is removed at the inside of the seal member SL and the feeding terminal of the driving circuit chip for the reference electrode layer is connected at this removing portion XP. It is desirable that a width of a feeding line to the reference electrode layer is larger than a width of other signal lines for reducing the feeding resistance.

[0462] FIGs. 87A - 87B are plan views for schematically explaining the terminal region when a method in which electricity is fed from a reference potential generation circuit disposed in a control circuit of the liquid crystal display device to a using flexible printed circuit board or the like is adopted. A reference electrode feeding line STL is formed on the flexible printed circuit board FPC and electricity is fed to a terminal of the reference electrode which is pulled out to the first

substrate SUB1 via the flexible printed circuit board FPC from the reference potential generation circuit disposed in the control circuit of the liquid crystal display device. FIG. 87A shows a case in which this feeding method is adopted in the tape carrier package mounting method and FIG. 87B shows a case in which this feeding method is adopted in a FCA method. In this manner, by performing the feeding of electricity to the reference electrode layer ST using the flexible printed circuit board FPC without going through the driving circuit chip CH1 so that the feeding of electricity can be performed with the further lower feeding resistance. In the drawing, GDL indicates a feeding line to the gate line.

[0463] FIG. 88 is a schematic plan view of the liquid crystal display device for explaining the first example for forming the feeding terminal to the reference electrode. In both of the vertical field method and the IPS method (including the modified IPS method and other modified IPS method), a periphery of the reference electrode ST is patterned thus forming lead terminals STT and feeding of electricity to the reference electrode ST is performed using constitutions shown in FIG. 84 to FIG. 87.

[0464] FIG. 89 is a schematic plan view of the liquid crystal display device for explaining a second example for forming feeding terminals to the reference electrode and FIG. 90 is a cross-sectional view of an essential part showing a portion A in FIG. 89 in an enlarged manner. Particularly in the vertical field method having common electrodes at the second substrate SUB2 side, connection portions STC are formed on corner portions of the reference electrode ST by patterning and the common electrode ST is connected to the reference electrode ST at the connection portions STC by means of a conductive paste AG. The feeding of electricity to the reference electrode ST is performed by the common electrode. It is not always necessary to provide the connection portion STC at all corner portions of the reference electrode ST and may be formed atone, two or three corner portions of the reference electrode ST.

[0465] FIG. 91 is a schematic cross-sectional view of the liquid crystal display device for explaining a third example of the formation of a feeding terminal to the reference electrode and FIG. 92 is a cross-sectional view of an essential part which shows the feeding terminal portion in FIG. 91 in an enlarged manner. The feeding terminal STT to the reference electrode ST may be formed separately from the formation of the reference electrode ST. Further, the feeding terminal STT may be pulled out as a line which is connected with other line such as the gate line or the drain line at the inside of the seal SL. Here, the connection resistance of both lines are taken into account. The above-mentioned constitution is suitable when the contact resistance between the feeding terminal STT and the reference electrode ST formed of a transparent electrode made of non-Al-based metal (metal of high melting point such as Cr, Mo, Ti, Ta, W, Zr or the like, or alloy thereof) is low. Here, the feeding terminal STT may be formed of a transparent conductive film (ITO, IZO or the like).

[0466] FIG. 93 is a schematic cross-sectional view of a liquid crystal display device for explaining

a fourth example of the formation of the feeding terminal to the reference electrode. When the contact resistance between the feeding terminal STT and the reference electrode ST is high, it is preferable to connect them using an auxiliary connection line STT'. For example, when the feeding terminal STT is made of Al, the auxiliary connection line STT' made of non-Al-based metal is used. Further, when the auxiliary connection line STT' is also formed of a transparent conductive film and also when the Al-based feeding terminal STT and the reference electrode ST are directly connected to each other, different from usual signal lines, it is possible to perform the multiple-point feeding of electricity and hence, the constitution shown in FIG. 93 is available.

[0467] FIG. 94 is a schematic cross-sectional view of the liquid crystal display device for explaining a constitutional example of an outer periphery of an effective display region when the organic insulation layer formed on the first substrate is formed of a color filter CF. When the organic insulation layer is formed of the color filter CF, the color filter material CF1 of three primary colors (R, G, B) or the color filter material CF1 formed of at least one of these colors and the color filter material CF2 formed of at least other color are laminated to the outer periphery of effective display region. With such a constitution, it is possible to form a light shielding layer on the outer periphery of the effective display region. Further, when two color filter materials are laminated to the outer periphery of the effective display region, one color filter material CF1 is red (R) and the other color filter material CF2 is green (G) or blue (B). The color filter material R absorbs light other than red (R) light. Accordingly, by combining color filter material G or B which absorb red (R) with the color filter material R, the color filter CF can absorb lights of respective colors R, G, B.

[0468] FIG. 95 is a schematic cross-sectional view of the liquid crystal display device for explaining another constitutional example of the outer periphery of the effective display region when the organic insulation layer formed on the first substrate is formed of the color filter. That is, this example shows a case in which the color filter CF2 which is explained in conjunction with FIG. 94 is laminated to the sealing portion SL and an outer peripheral portion thereof. Further, to protect the whole color filter layer including the color filter layers (CF1, CF2) and the effective display region, it is preferable to form an overcoat layer OC over the color filter layer (CF, CF1, CF2).

[0469] FIG. 96 is a schematic cross-sectional view of the liquid crystal display device for explaining a constitutional example in which a color filter is formed over all of a sealing portion, an outer peripheral portion thereof and an effective display region. Also in this case, it is preferable to form an overcoat layer OC over the color filter layer CF which covers all of the sealing portion, the outer peripheral portion thereof and the effective display region.

[0470] FIGs. 97A – 97B are explanatory views of an aligning method in mounting driving circuits to various types of lead terminals and feeding terminals formed on a first substrate. FIG. 97A shows a case in which a tape carrier package is used and FIG. 97B shows a case in which a FCA

method is adopted. In FIG. 97A and FIG. 97B, when a color filter CF is provided also outside the sealing member, it is preferable to form removing portions XP in the color filter CF in the vicinity of alignment marks AM for achieving the alignment of a tape carrier package TCP which mounts a driving circuit chip CH1 thereon or a driving circuit chip CH1 of FCA with various types of lead terminals and feeding terminals formed on the first substrate. Due to such a constitution, the generation of an error at the time of performing the optical recognition of the alignment marks AM is prevented so that the mounting accuracy is ensured.

[0471] FIG. 98 is a schematic cross-sectional view of a liquid crystal display device which is configured to prevent electrolytic corrosion of a reference electrode layer formed on a first substrate. To prevent electrolytic corrosion of the reference electrode layer ST outside a sealing member SL, the reference electrode layer ST including end portions thereof is covered with an organic insulation layer O-PAS.

[0472] FIG. 99 is a schematic plan view for explaining an example of the formation of a color filter when an organic insulation layer formed on a first substrate is made of the color filter. As shown in FIG. 99, the color filter CF may be formed only at an inner side of a sealing member SL. The color filter CF contains a large quantity of pigment or dye to perform a function of selecting wavelength of light. Accordingly, the color filter CF has a tendency of exhibiting higher hygroscopic property compared to a colorless organic insulation layer.

[0473] When the color filter CF is disposed in a region outside the sealing member SL which exhibits high temperature and high humidity, the color filter CF in the region absorbs moisture and swells so that wrinkles are generated and hence, there is a possibility that lead lines and feeding lines which are formed over the color filter CF are disconnected. To prevent such a phenomenon, the color filter CF is formed only at the inside of the sealing member SL.

[0474] FIG. 100 is a schematic plan view served for explaining an example of the formation of a color filter when an organic insulation layer formed on the first substrate is made of the color filter. Compared to the constitution explained in conjunction with FIG. 99, in this example, the reference electrode layer ST is formed such that the reference electrode layer ST is extended to the outside of the sealing member SL. Further, in this example, to prevent the short-circuiting between the reference electrode layer ST and the scanning signal line or the like, portions of the reference electrode layer ST on which the color filter CF is not formed are covered with an overcoat layer OC. Due to such a constitution, the above-mentioned short-circuiting can be surely prevented.

[0475] FIG. 101 is a schematic plan view served for explaining another constitutional example in which the organic insulation layer formed on the first substrate is constituted of the color filter. When the color filter layer CF is formed only in the inside of the effective display region of the first substrate SUB1, the reference electrode layer ST is also formed only in the inside of the effective display region. Here, the reference electrode layer ST may be stuck out from the color filter CF provided that the reference electrode layer ST does not cross other lines.

[0476] FIG. 102 is a schematic plan view served for explaining still another constitutional example in which the organic insulation layer formed on the first substrate is constituted of the color filter. Compared to the case shown in FIG. 101, the reference electrode layer ST is formed such that the reference electrode layer ST is stuck out from the color filter CF without crossing other lines in this example as shown in FIG. 102. Further, as shown in FIG. 102, an overcoat layer OC is formed such that the overcoat layer OC covers the color filter CF and the reference electrode ST.

[0477] FIG. 103 is a schematic cross-sectional view for explaining one arrangement example in which the liquid crystal display device of the present invention is used as a transmission type display module. On a back surface of the first substrate SUB1 of the liquid crystal display device which is formed by laminating the first substrate SUB1 and the second substrate SUB2 to each other, a backlight BL is mounted. This arrangement example is a typical constitution of the transmission type display module. Illumination light L1 from the backlight BL is modulated by the liquid crystal display device when the light L1 passes through the liquid crystal display device and is irradiated from the second substrate SUB2 side.

[0478] FIG. 104 is a schematic cross-sectional view for explaining another arrangement example in which the liquid crystal display device of the present invention is used as a transmission type display module. On a front surface of the second substrate SUB2 of the liquid crystal display device which is formed by laminating the first substrate SUB1 and the second substrate SUB2 to each other, a front light FL is mounted. Illumination light L1 from the front light FL is modulated by the liquid crystal display device when the light L1 passes through the liquid crystal display device and is irradiated from the first substrate SUB1 side.

[0479] FIG. 105 is a schematic cross-sectional view for explaining the first arrangement example in which the liquid crystal display device of the present invention is used as a reflection type display module. A reference electrode ST which is provided to the first substrate SUB1 of the liquid crystal display device which is formed by laminating the first substrate SUB1 and the second substrate SUB2 to each other is formed of a reflective metal layer. An external light L2 which is incident on the second substrate SUB2 is reflected on the reference electrode ST and the light L2 which is irradiated from the second substrate SUB2 side is modulated in accordance with an electronic latent image formed in the liquid crystal display device when the light L2 passes through the inside of the liquid crystal display device.

[0480] FIG. 106 is a schematic cross-sectional view for explaining the second arrangement example in which the liquid crystal display device of the present invention is used as a reflection type display module. On a front surface of the second substrate SUB2 of the liquid crystal display device which is formed by laminating the first substrate SUB1 and the second substrate SUB2 to each other, a front light FL is mounted. Light L2 irradiated from the front light FL is reflected on a reference electrode ST which is constituted of a reflective metal layer provided to an inner surface of the first substrate SUB1 and is irradiated from the second substrate SUB2 side through the front

light FL. The light L2 is modulated by the liquid crystal display device when the light L2 passes through the inside of the liquid crystal display device.

[0481] FIG. 107 is a schematic cross-sectional view for explaining the third arrangement example in which the liquid crystal display device of the present invention is used as a reflection type display module. On a front surface of the second substrate SUB2 of the liquid crystal display device which is formed by laminating the first substrate SUB1 and the second substrate SUB2, a reflection layer RT is mounted. An external light L2 incident from the first substrate SUB1 is reflected on the reflection layer RT and is irradiated from the first substrate SUB1 side. The light L2 is modulated by the liquid crystal display device when the light L2 passes through the inside of the liquid crystal display device.

[0482] FIG. 108 is a schematic cross-sectional view for explaining the fourth arrangement example in which the liquid crystal display device of the present invention is used as a reflection type display module. A common electrode CT which is formed on an inner surface of the second substrate SUB2 of the liquid crystal display device which is formed by laminating the first substrate SUB1 and the second substrate SUB2 is constituted of a reflective metal layer. An external light L2 incident from the first substrate SUB1 is reflected on the common electrode CT and is irradiated from the first substrate SUB1 side. The light L2 is modulated by the liquid crystal display device when the light L2 passes through the inside of the liquid crystal display device.

[0483] FIG. 109 is a schematic cross-sectional view for explaining the fifth arrangement example in which the liquid crystal display device of the present invention is used as a reflection type display module. On a back surface of the first substrate SUB1 of the liquid crystal display device which is formed by laminating the first substrate SUB1 and the second substrate SUB2, a front light FL is mounted. Further, a common electrode CT which is formed on an inner surface of the second substrate SUB2 is constituted of a reflective metal layer. An external light L2 incident on the first substrate SUB1 from the front light FL is reflected on the common electrode CT and is irradiated from the first substrate SUB1 side after passing through the front light FL. The light L2 is modulated by the liquid crystal display device when the light L2 passes through the inside of the liquid crystal display device.

[0484] FIG. 110 is a schematic cross-sectional view for explaining one arrangement example in which the liquid crystal display device of the present invention is used as a transmission/reflection type display module. A reference electrode ST which is provided to the first substrate SUB1 of the liquid crystal display device formed by laminating the first substrate SUB1 and the second substrate SUB2 is constituted of a reflective metal layer and includes partial apertures (slit holes or dot holes) corresponding to respective pixels.

[0485] When the liquid crystal display device is operated in a reflection type mode, an external light L2 incident from the second substrate SUB2 is reflected on the reference electrode ST and is irradiated from the second substrate SUB2. When the liquid crystal display device is operated in a

transmission type mode, light L1 irradiated from the backlight BL mounted on a back surface of the first substrate SUB1 passes through the apertures of the reference electrode ST and is irradiated through the second substrate SUB2. When either one of the light L2 or the light L1 passes through the inside of the liquid crystal display device, the light L2 or L1 is modulated by the liquid crystal display device. Further, a semitransparent reflection layer may be used as the reference electrode ST in place of the reflective metal layer having apertures. Here, it is needless to say the liquid crystal display device can be operated in both modes, that is, the reflection mode and the transmission mode.

[0486] FIG. 111 is a schematic cross-sectional view for explaining another arrangement example in which the liquid crystal display device of the present invention is used as a transmission/reflection type display module. A common electrode CT which is provided to the second substrate SUB2 of the liquid crystal display device formed by laminating the first substrate SUB1 and the second substrate SUB2 is constituted of a reflective metal layer and includes partial apertures (slit holes or dot holes).

[0487] When the liquid crystal display device is operated in a reflection type mode, an external light L2 incident from the first substrate SUB1 is reflected on the common electrode CT and is irradiated from the first substrate SUB1. When the liquid crystal display device is operated in a transmission type mode, light L1 irradiated from the front light FL mounted on a front surface of the second substrate SUB2 passes through the apertures of the common electrode CT and is irradiated through the first substrate SUB1. When either one of the light L2 or the light L1 passes through the inside of the liquid crystal display device, the light L2 or L1 is modulated by an electronic image formed in the liquid crystal display device. Further, a semitransparent reflection layer may be used as the common electrode CT in place of the reflective metal layer having apertures.

[0488] The present invention is not limited to the above-mentioned embodiments and constitutional examples and various liquid crystal display devices can be constituted using the constitution in which the reference electrodes are formed on the substrate side on which the switching elements such as thin film transistors are formed as the basis.

[0489] Further, with respect to the substrates used in the above-mentioned respective substrates, the substrate SUB1 may be formed of a glass substrate.

[0490] Alternatively, the substrate SUB1 may be formed of a plastic substrate or a resin substrate.

[0491] In the present invention, the reference electrode layer ST is formed in advance at the time of producing the substrate or before delivering the substrate and hence, only the non-defective substrate can be applied so that the yield rate is enhanced. Further, since it is unnecessary to form the capacity forming portion with high accuracy, the throughput can be enhanced and the cost can be reduced. Further, the films are formed before forming the TFT layer, a manufacturing method such as a coating method which is liable to generate foreign materials can be used and hence, the

cost can be further reduced.

[0492] Although the structure which is formed by laminating the gate line GL, the gate insulation film GI and the semiconductor layer in this order has been explained in the above-mentioned respective embodiments, the structure may be formed by laminating them in the order of the semiconductor layer, the gate insulation film GI and the gate line GL. Such a structure is suitable in a case that the semiconductor layer is formed of a layer having crystalline property such as polysilicon, CGS, SLS, SELAX or a layer formed of single crystal.

[0493] Further, when the layer having crystalline property is used as the semiconductor layer, further advantages can be realized. In the present invention, between the semiconductor layer and the substrate, the reference electrode layer ST having a large area which extends over the substantially whole pixel region is formed. Although the ion implantation is performed in a step for forming the switching element using the semiconductor layer having the crystalline property, ions are widely implanted covering regions other than the semiconductor layer. According to the present invention, the ion can be shielded with the reference electrode layer ST and hence, it is possible to prevent the ion from reaching the substrate SUB1 whereby the substrate SUB1 is not damaged and the reliability is enhanced.

[0494] In the step for forming the semiconductor layer having crystalline property, there has been known a method in which after forming an amorphous semiconductor, laser beams are partially irradiated to the amorphous semiconductor to perform scanning so that the semiconductor is fused partially due to heat of laser beams and crystallized to impart the crystalline property to the semiconductor. For example, SELAX, SLS and the like have been known. In such a method, since heat at a level which can fuse the semiconductor is added to the semiconductor, the heat of high temperature is transmitted to the periphery of the fused portion. The inventors have found that the strain and thermal stress are accumulated in the substrate SUB1 due to this heat of high temperature. Further, the inventors of the present invention have found a new problem that this stress brings about the disturbance in the polarization state and lowers the contrast ratio.

[0495] According to the present invention, the reference electrode layer ST is formed between the semiconductor layer and the substrate SUB1. Since the reference electrode layer ST is broad enough to cover the most portion of the pixel region, extends over a plurality of pixels and is conductive. Accordingly, the local high heat generated by laser beams can be instantly dispersed so that it is possible to prevent the damage and stress to the above-mentioned substrate and the reduction of contrast whereby high quality and high reliability can be realized.

[0496] This advantageous effect is an advantageous effect which can be realized by providing the conductive layer which extends over the substantially whole pixel region between the crystalline semiconductor layer and the substrate. The present invention also discloses and claims this constitution, that is, an image display device having the conductive layer which extends over the substantially whole pixel region between the crystalline semiconductor layer and the substrate as

the present invention.

[0497] Further, the above-mentioned respective embodiment shave been explained in conjunction with the liquid crystal display device for the sake of explanation. However, as can be clearly understood from the explanation of the above-mentioned respective embodiments, with the use of the technical concept disclosed by the present invention, the constitution arranged above the substrate SUB1 can be applicable to an organic EL, an inorganic EL or other image display device. Accordingly, "liquid crystal display device" in the claims discloses and claims the image display device in a range of equivalence. Further, in the same manner, "sandwiching liquid crystal between a first substrate and a second substrate which face each other in an opposed manner" in claims of this specification means "a first substrate and a second substrate which are arranged to face each other" in the liquid crystal display device which constitutes an equivalent of the liquid crystal display device.

[0498] As has been explained heretofore, according to the present invention, by providing the reference electrode layer functioning as the feeding electrode which forms holding capacity for activated or lit pixels to the substrate side on which the switching elements are formed, the resistance to the feeding electrode can be reduced and, at the same time, the reduction of numerical aperture of the pixels can be obviated thus realizing the active matrix type liquid crystal display device exhibiting high brightness and rapid driving.

[0499] Further, it is possible to provide the image display device which can satisfy both of the assurance of holding capacity and the enhancement of numerical aperture.

[0500] Still further, it is possible to enhance the image qualities and the reliability of the image display device which uses the crystalline semiconductor.

What is claimed is:

1. A liquid crystal display device, comprising:

a first substrate;

a second substrate;

a liquid crystal layer between the first substrate and the second substrate, containing liquid crystal molecules;

a gate line and a drain line;

a pixel electrode and a counter electrode disposed between the first substrate and the liquid crystal layer;

a gate insulation layer formed on the gate line;

an organic insulation layer disposed between the first substrate and the liquid crystal layer;

a switching element, connected to the gate line, including a first electrode connected to the drain line and a second electrode connected to the pixel electrode;

wherein the liquid crystal layer is driven by an electric field generated between the pixel electrode and the counter electrode,

wherein the pixel electrode is formed between the liquid crystal layer and the organic insulation layer, and wherein the counter electrode is a planar shape, and the pixel electrode comprises a slit having a first portion, and the first portion is not parallel with the gate line and the drain line.

2. A liquid crystal display device according to claim 1,

wherein the counter electrode is connected to a common layer and,

wherein the organic insulation layer is formed between the counter electrode and the first substrate.

3. A liquid crystal display device according to claim 2,

wherein the counter electrode is connected to the common layer via a through hole within the organic insulation layer.

4. A liquid crystal display device according to claim 3,

wherein the common layer is a planar shape, and faces a plurality of pixel electrodes.

5. A liquid crystal display device according to claim 2,

wherein a passivation layer is formed between the liquid crystal layer and the pixel electrode contacted the second electrode, and

wherein the passivation layer is formed between the liquid crystal layer and the drain line.

6. A liquid crystal display device according to claim 1,

wherein the counter electrode is a planar shape, and the pixel electrode comprises a slit having the first portion and a second portion, and both of the first portion and the second portion are not parallel with the gate line and the drain line.

7. A liquid crystal display device according to claim 1,

wherein the gate insulation layer is formed between the counter electrode and the drain line.

8. A liquid crystal display device according to claim 1,

wherein the counter electrode connects to a connection line.

9. A liquid crystal display device according to claim 8,

wherein the connection line is made of metal material.

10. A liquid crystal display device according to claim 9,

wherein the connection line is arranged parallel to the extension direction of the gate line.

11. A liquid crystal display device according to claim 10,

wherein the organic insulation layer is formed between the connection line and the first substrate.

12. A liquid crystal display device according to claim 9,

wherein the connection line is directly contacted to the counter electrode.

13. A liquid crystal display device according to claim 12,

wherein the common electrode is disposed between the connection line and the liquid crystal layer.

ABSTRACT OF THE DISCLOSURE

Image display device having an electrode forming layer which includes a plurality of gate lines, a plurality of drain lines, a plurality of switching elements and the a plurality of pixel electrodes, and having reference electrode layer between the electrode forming layer and a substrate where the electrode forming layer formed thereon, and the reference electrode layer and the electrode forming layer are insulated by insulating layer.

FIG. 1

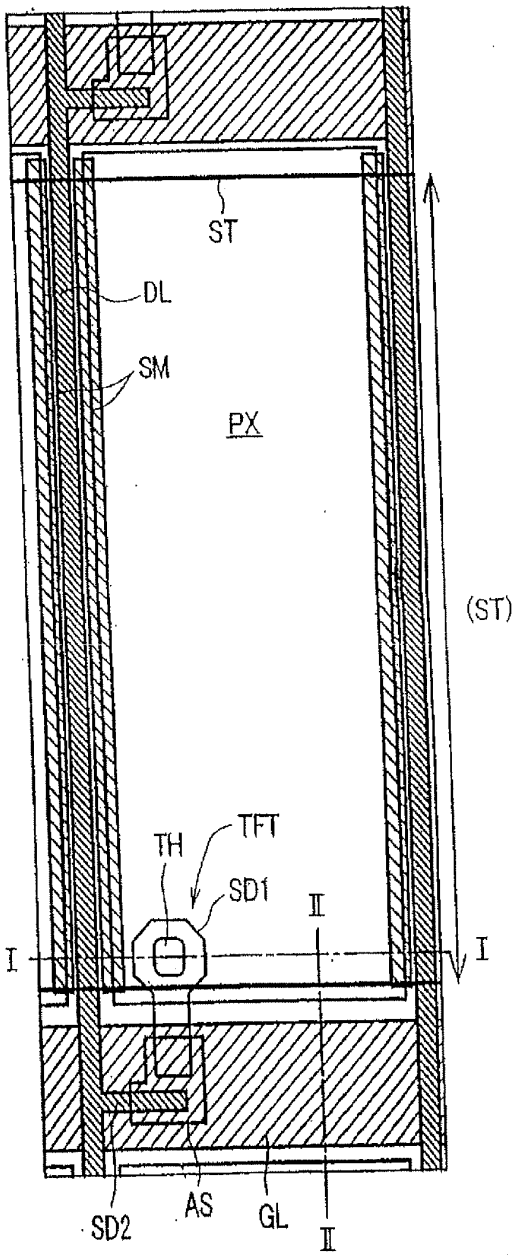


FIG. 2

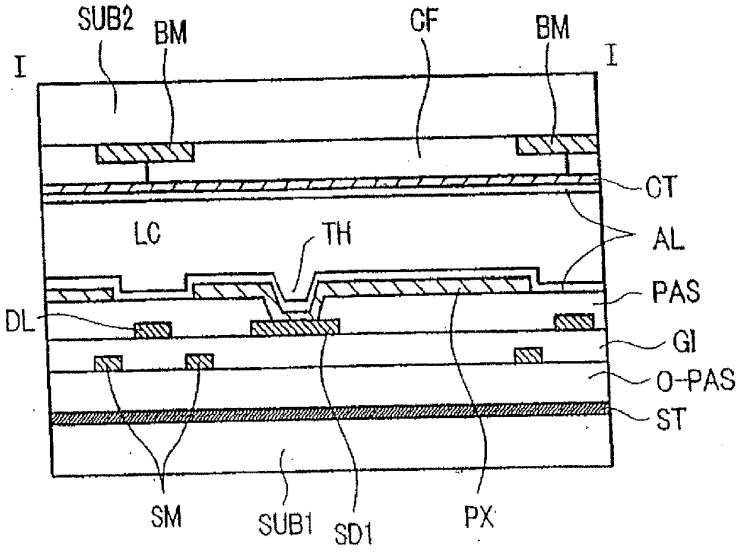
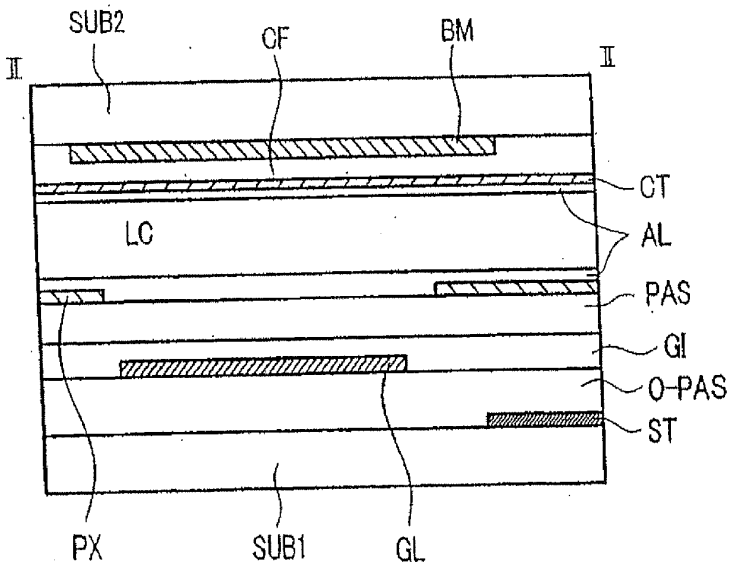

SUB2
BM
CF
BM
I
I
CT
LC
TH
AL
PAS
DL
GI
O-PAS
ST
SM
SUB1
SD1
PX

FIG. 3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II
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PAS
GI
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ST
PX
SUB1
GL

FIG. 4

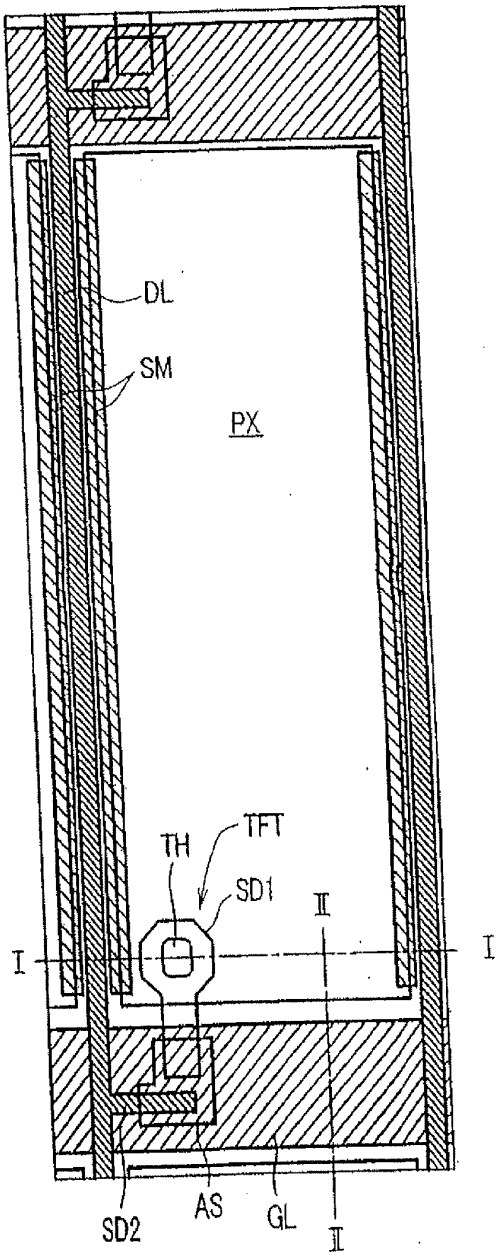

FIG. 5

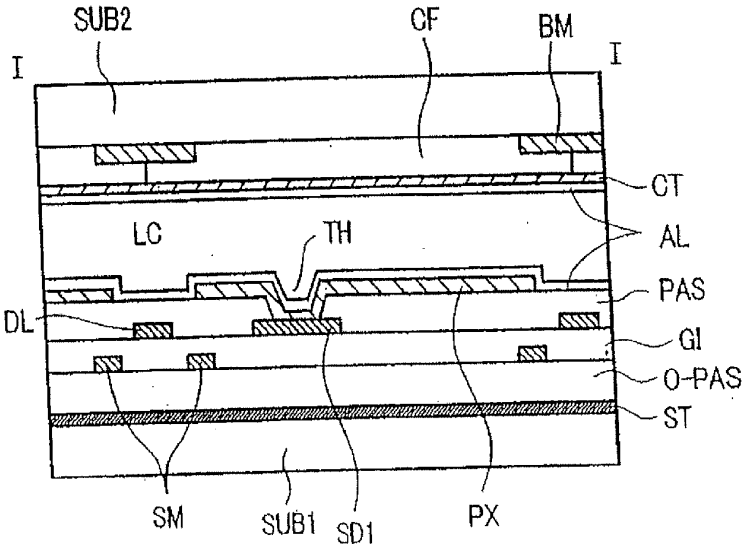
SUB2
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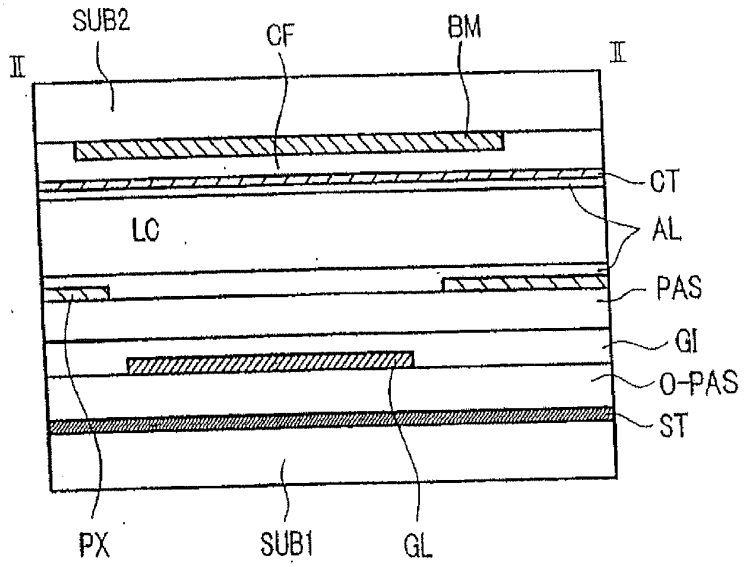
FIG. 6


SUB2
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PAS
GI
O-PAS
ST
PX
SUB1
GL

FIG. 7

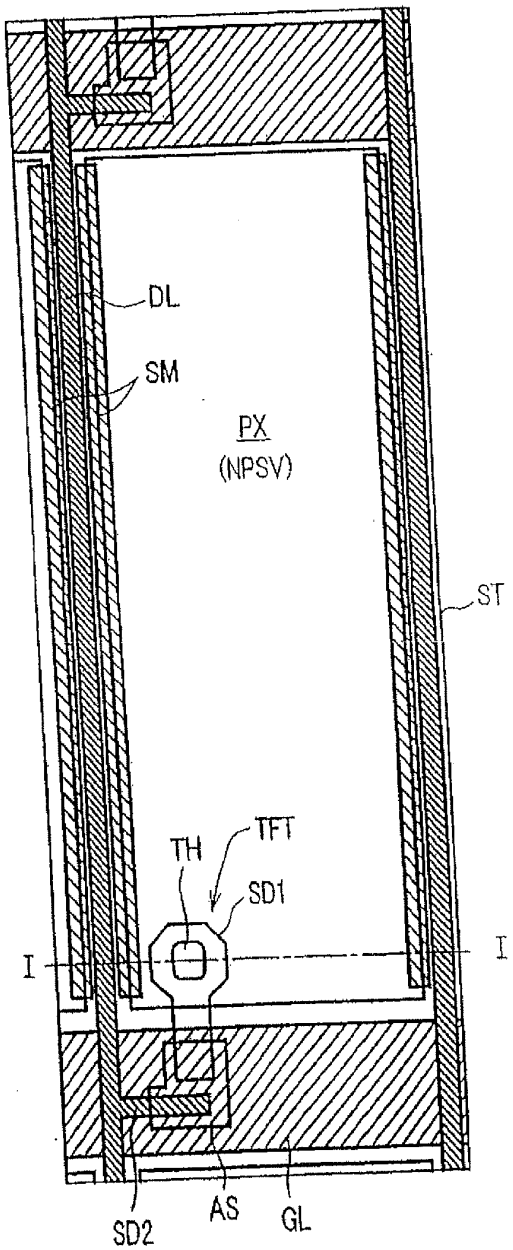
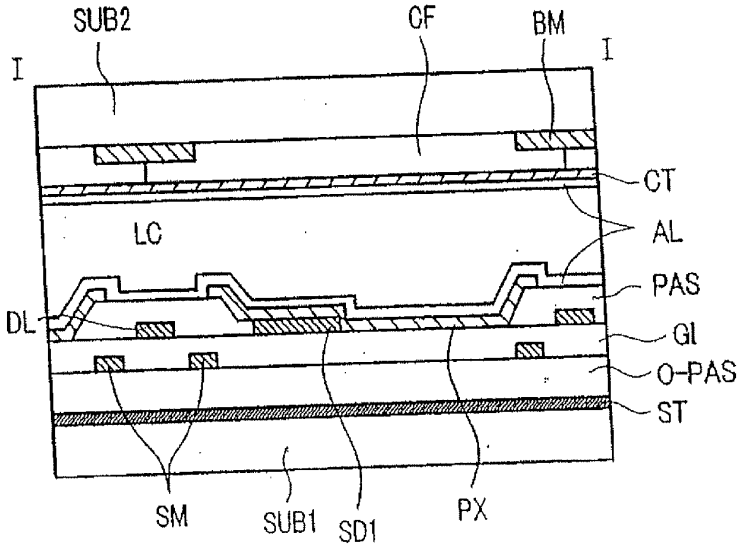


FIG. 8


SUB2
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AL
LC
PAS
DL
GI
O-PAS
ST
SM
SUB1
SD1
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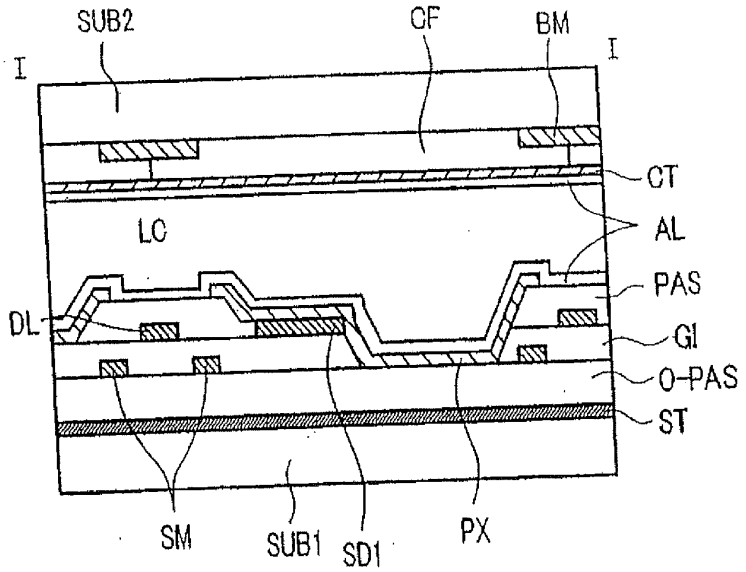
FIG. 9


SUB2
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AL
LC
PAS
DL
GI
O-PAS
ST
SM
SUB1
SD1
PX

FIG. 10

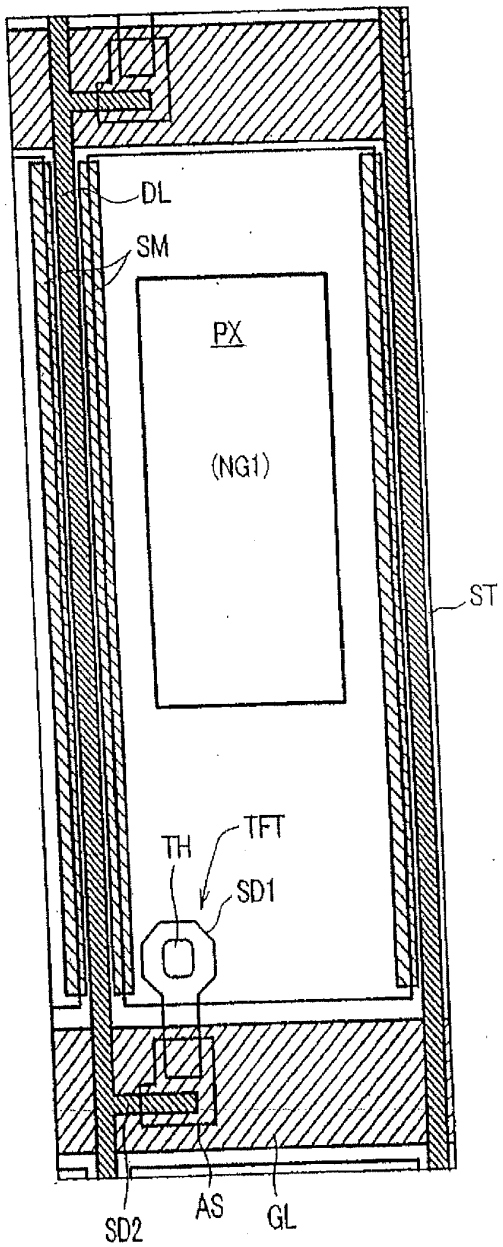

FIG. 11

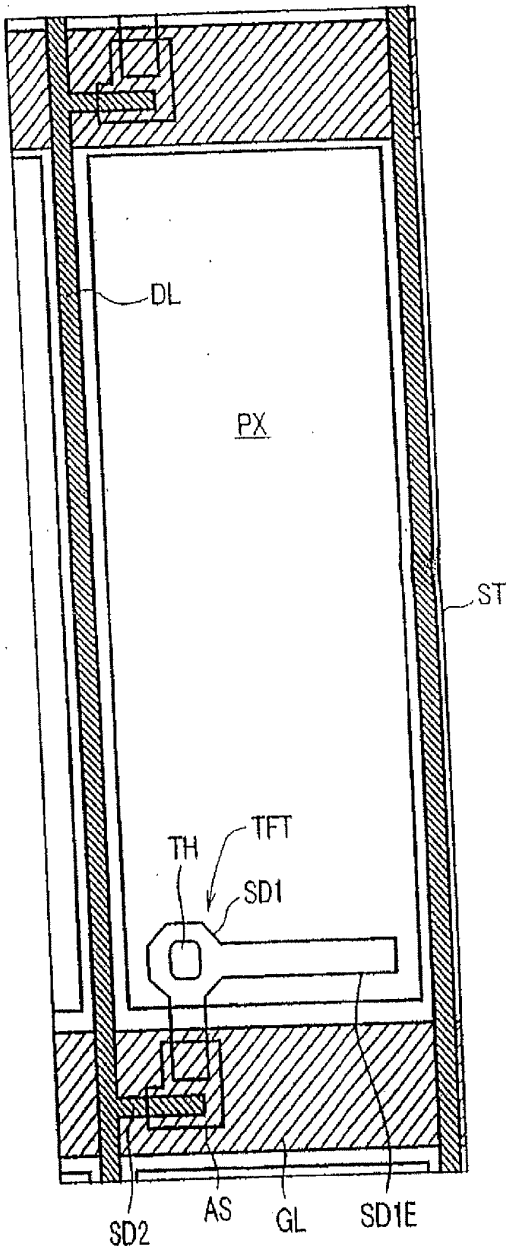

FIG. 12

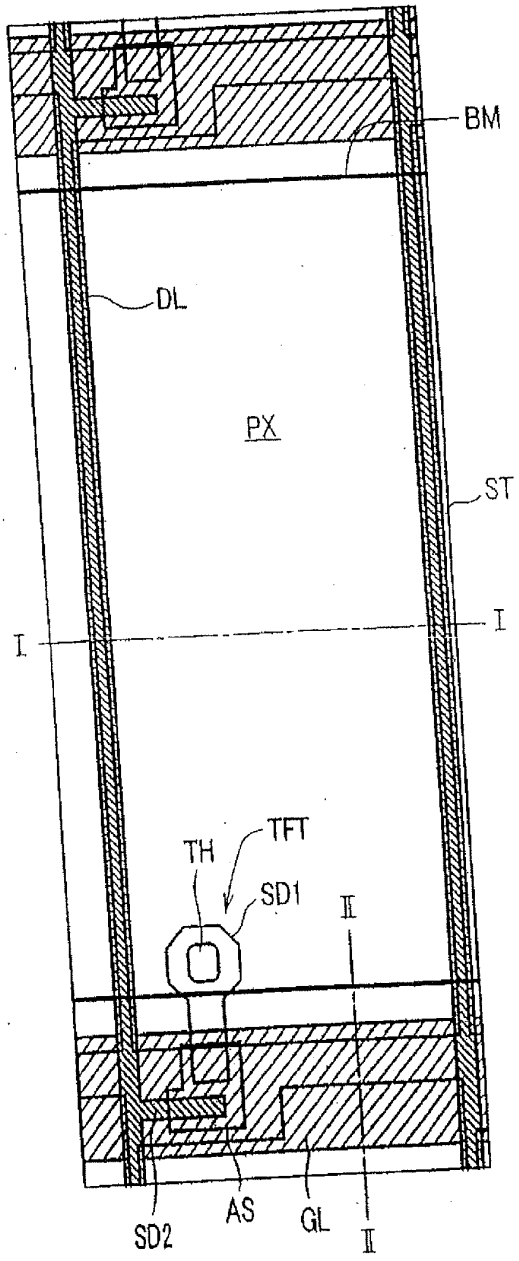

FIG. 13

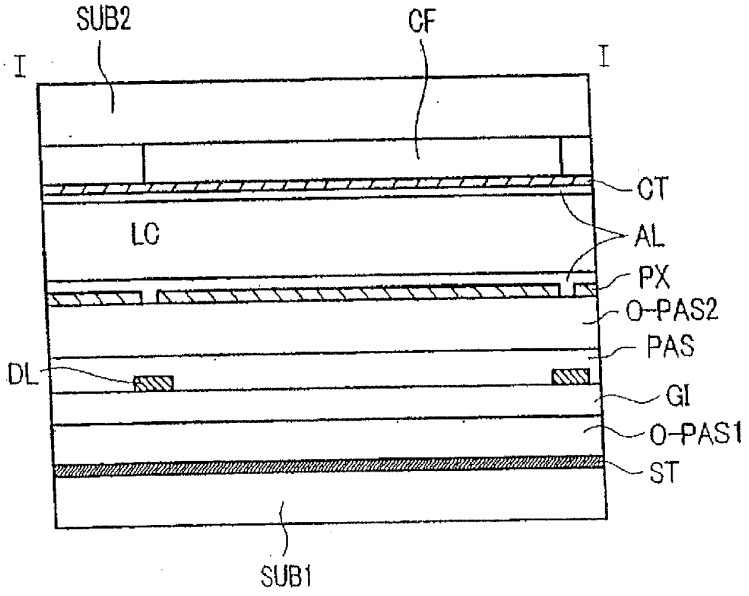
SUB2
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FIG. 14

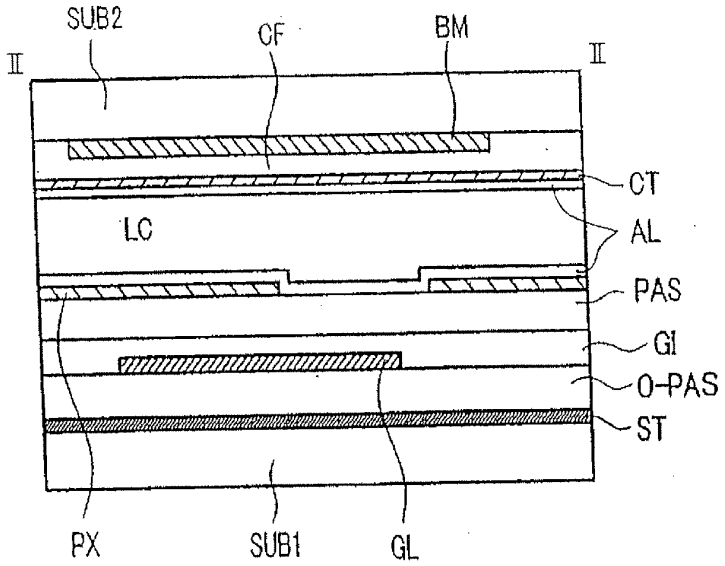
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FIG. 15

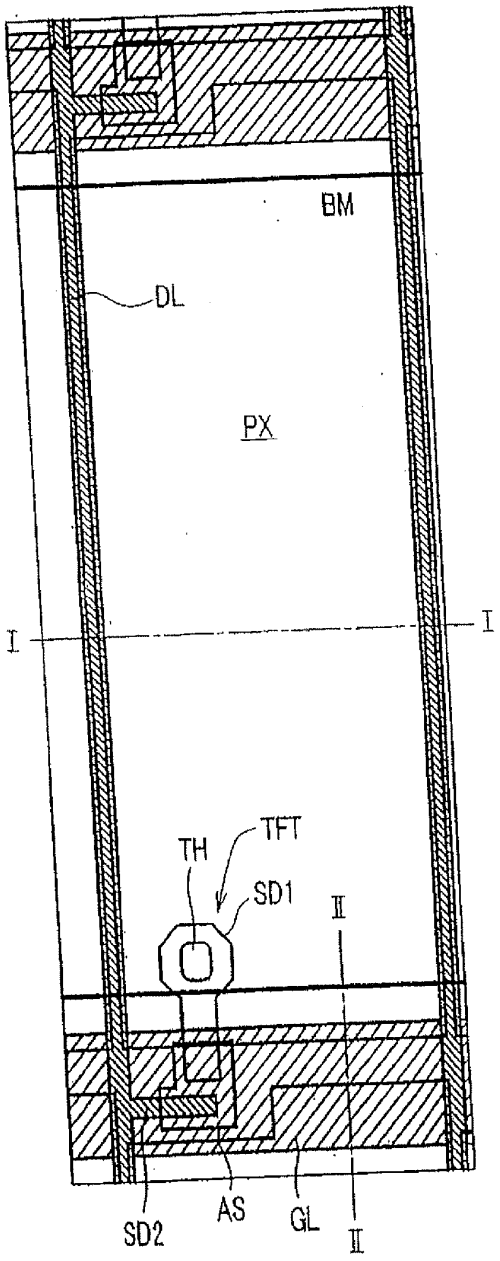

FIG. 16

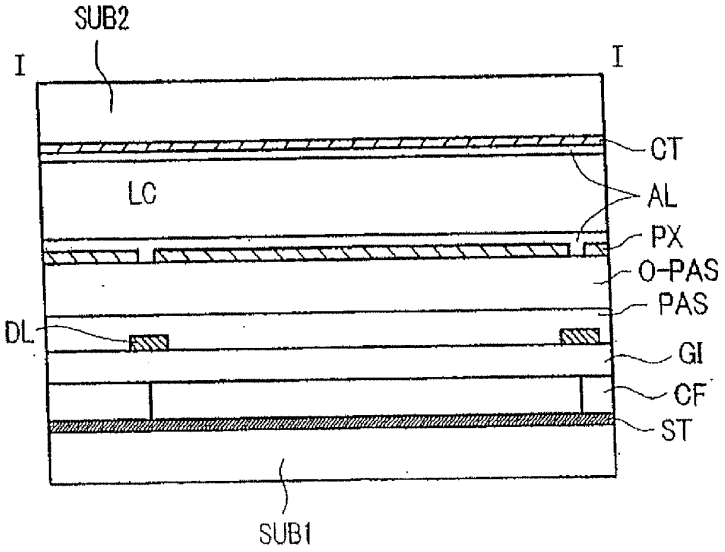
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FIG. 17

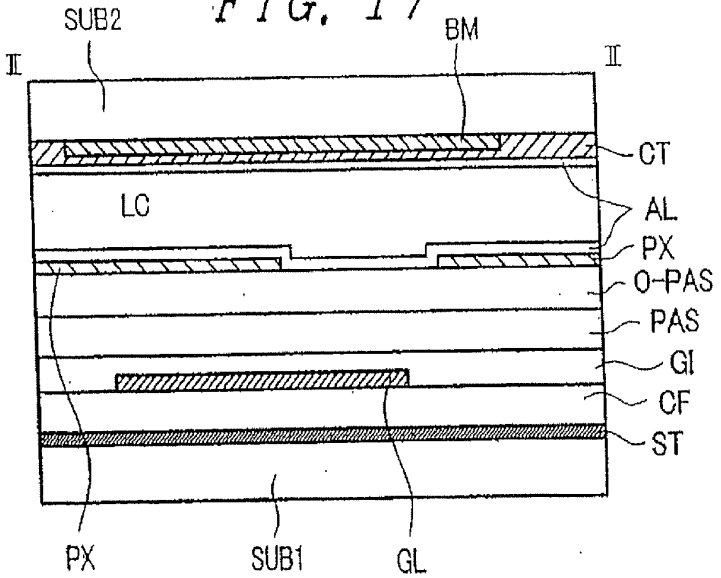
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FIG. 18

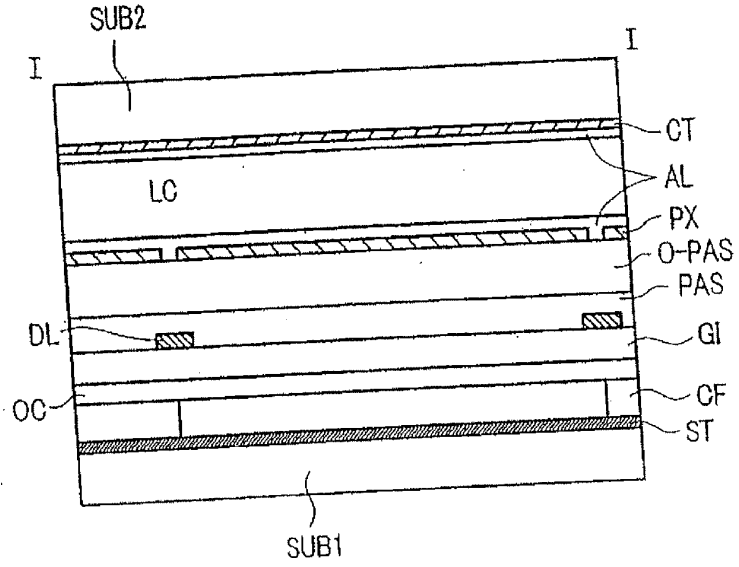
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FIG. 19

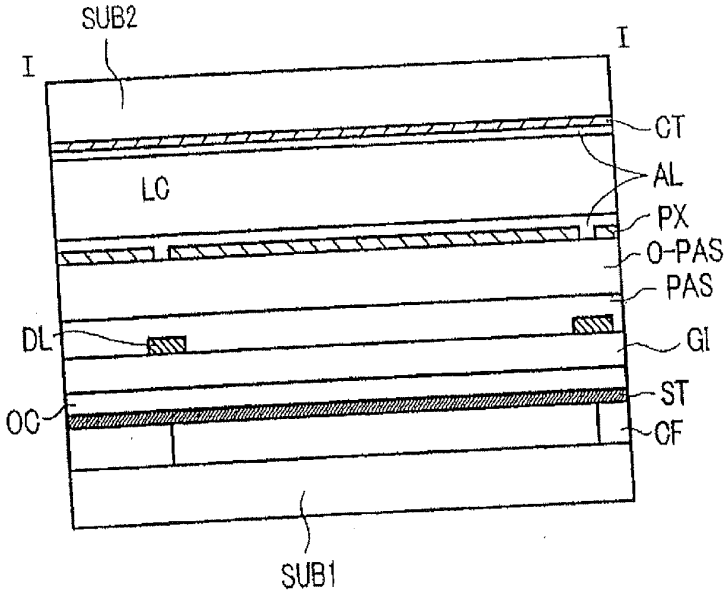
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FIG. 20

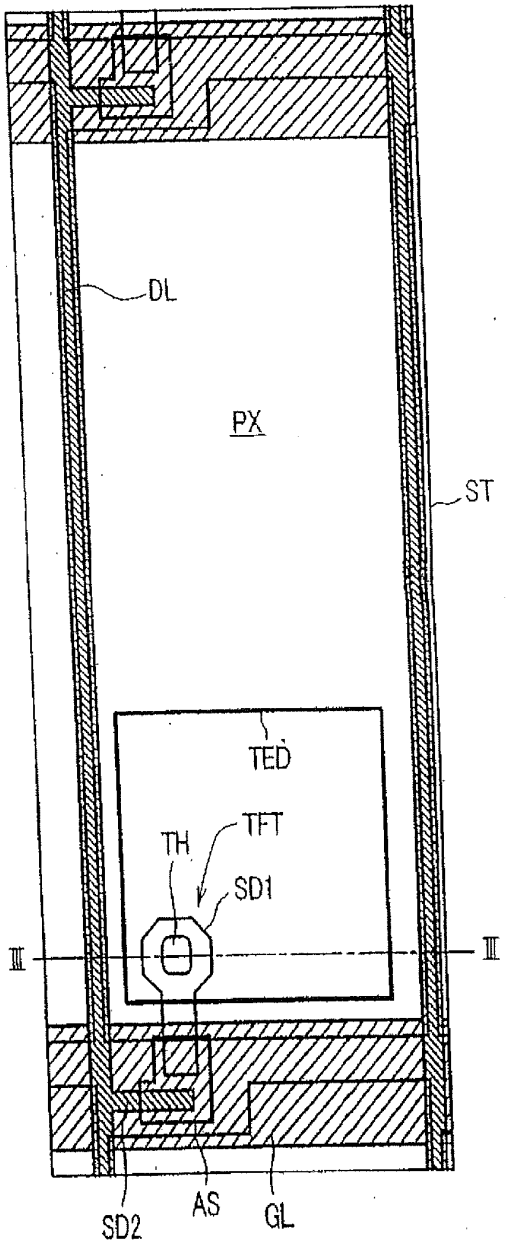

FIG. 21

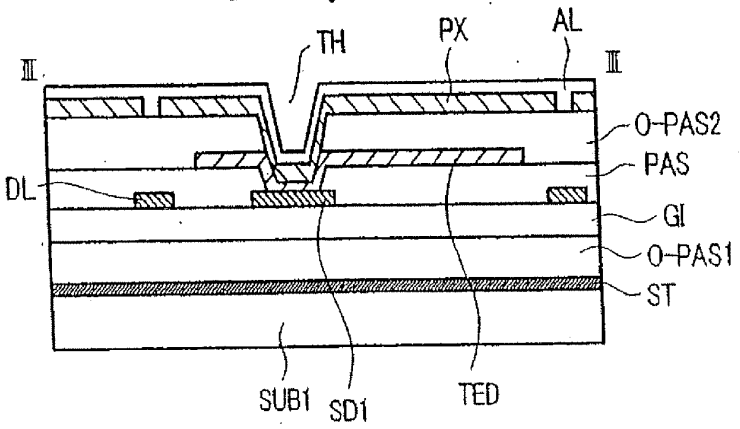

FIG. 22

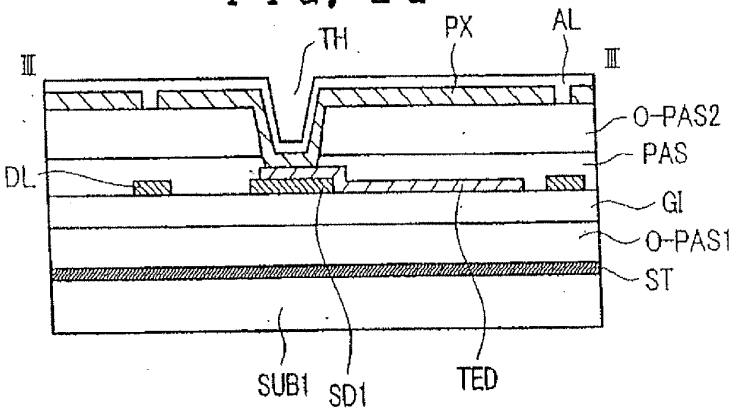

FIG. 23

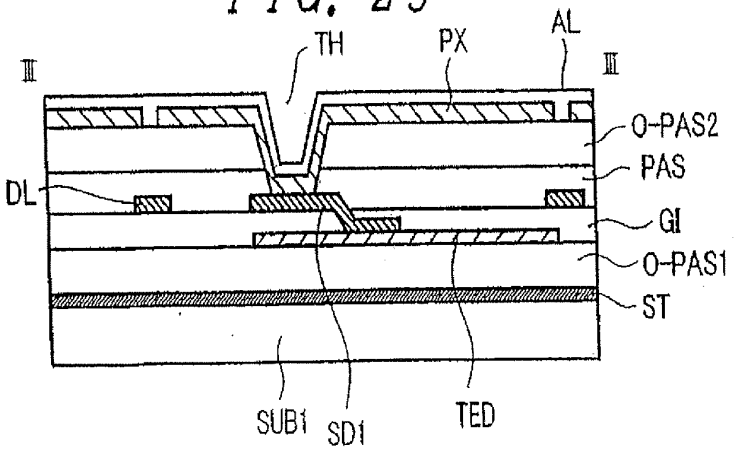

FIG. 24

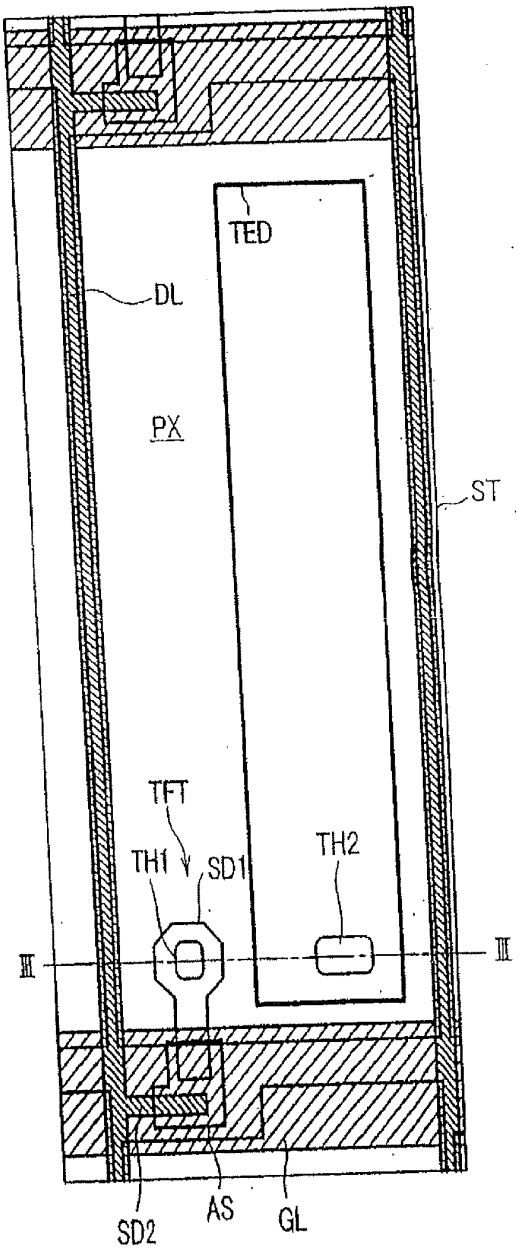

FIG. 25

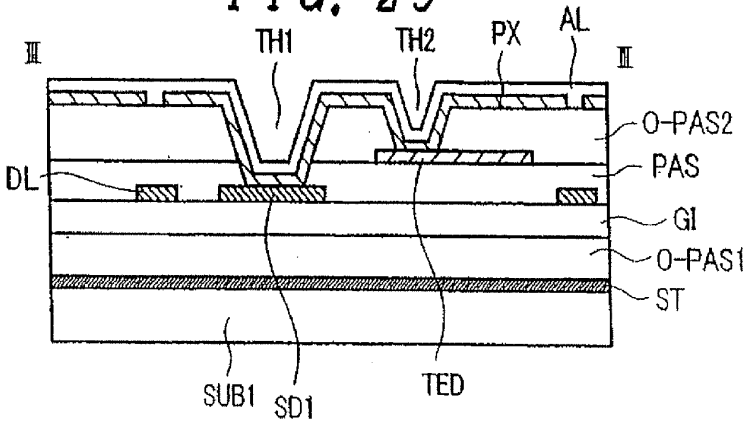

FIG. 26

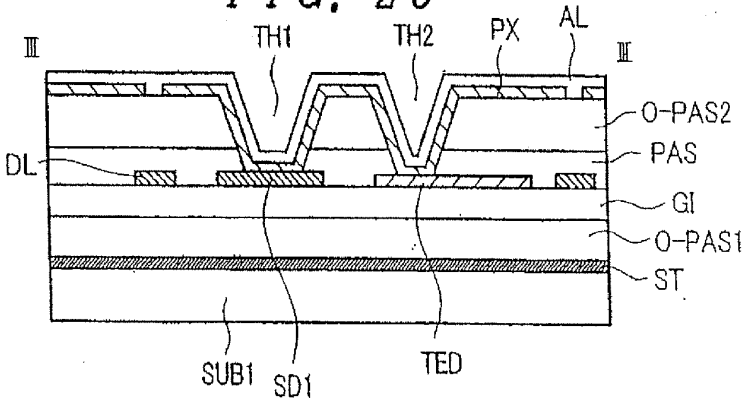

FIG. 27

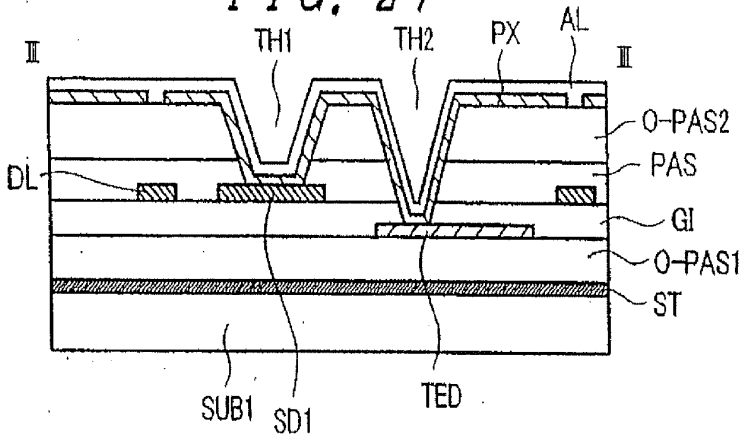

FIG. 28

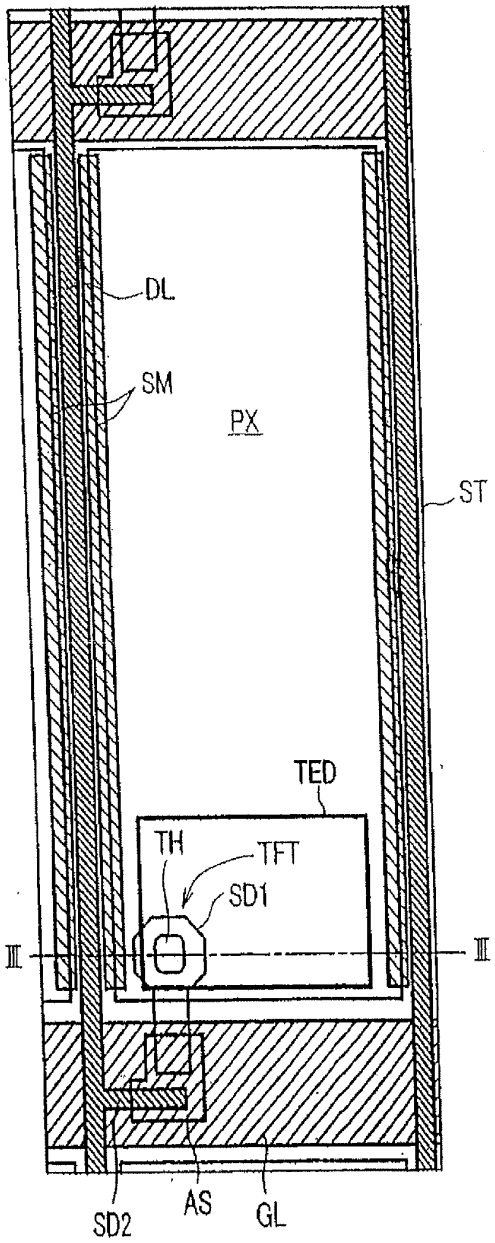

FIG. 29

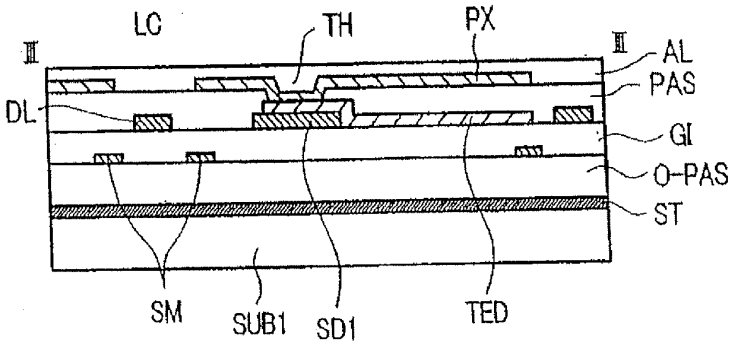
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FIG. 30

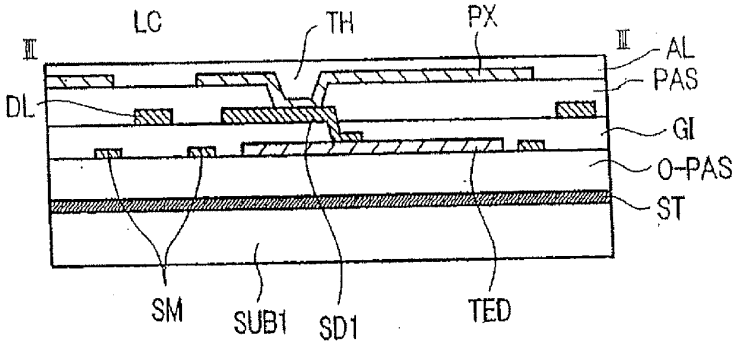
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FIG. 31

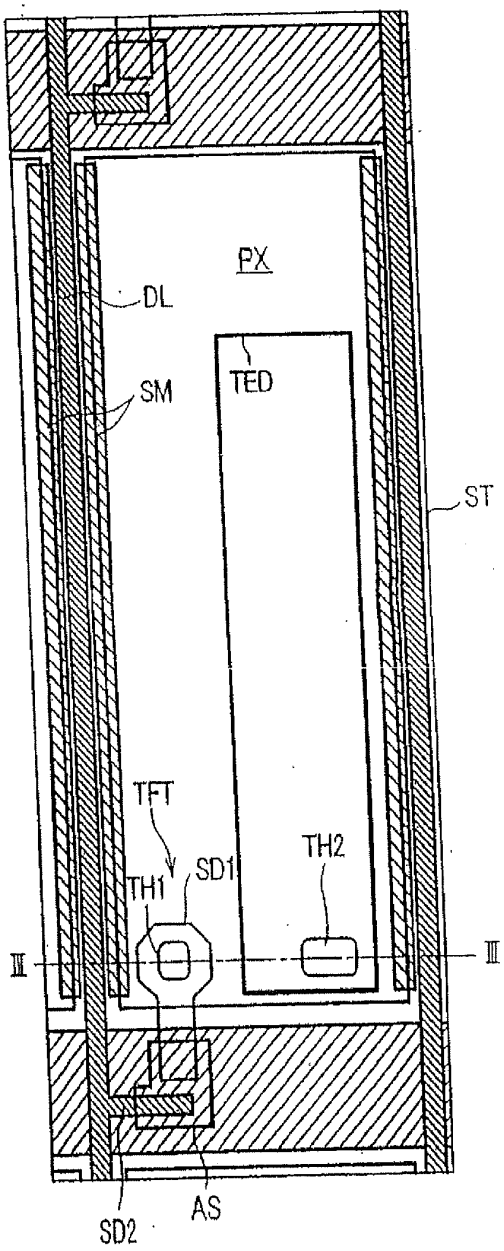

FIG. 32

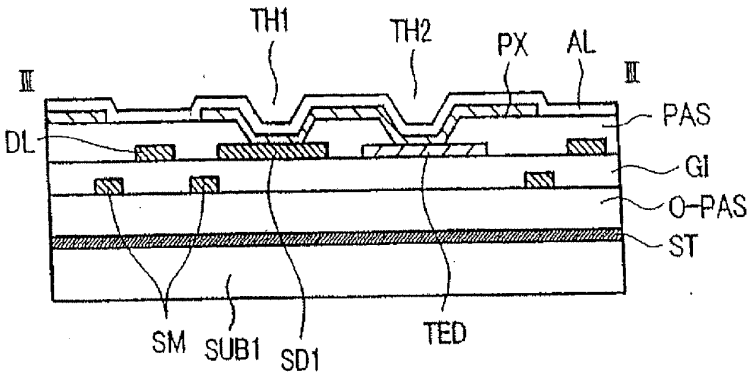
TH1
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FIG. 33

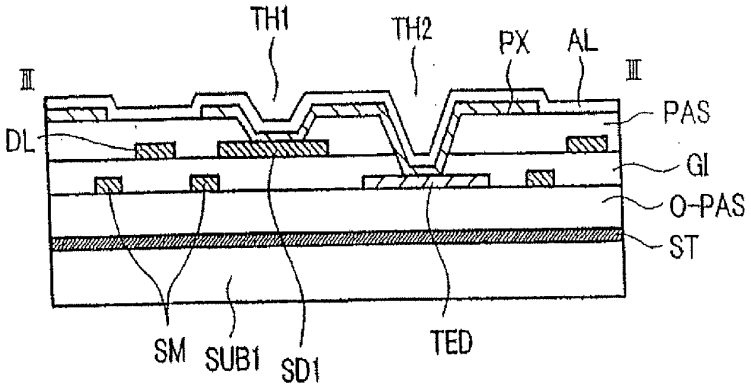
TH1
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FIG. 34

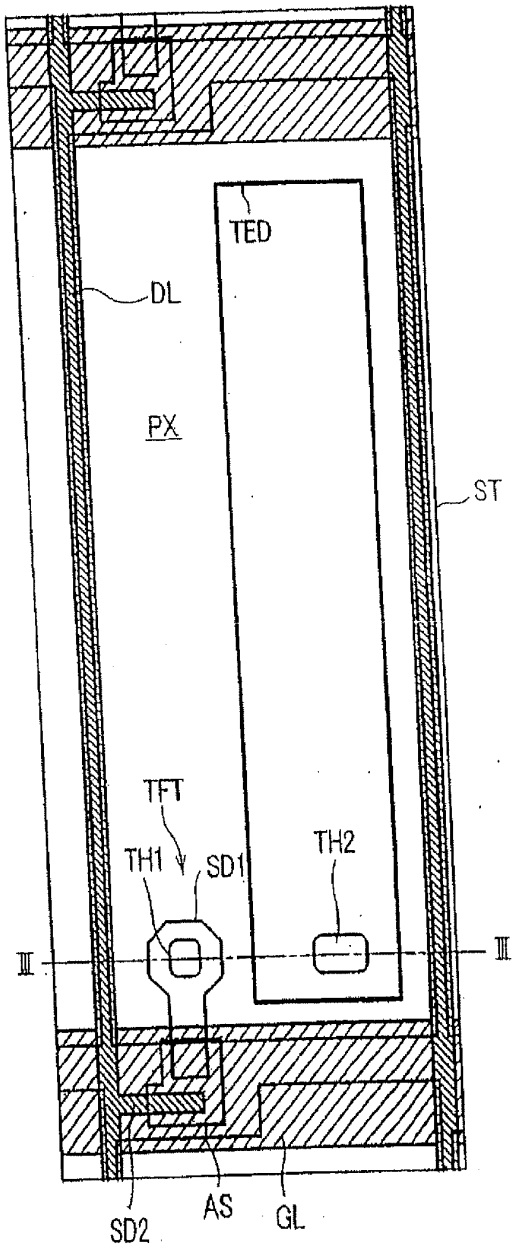

FIG. 35

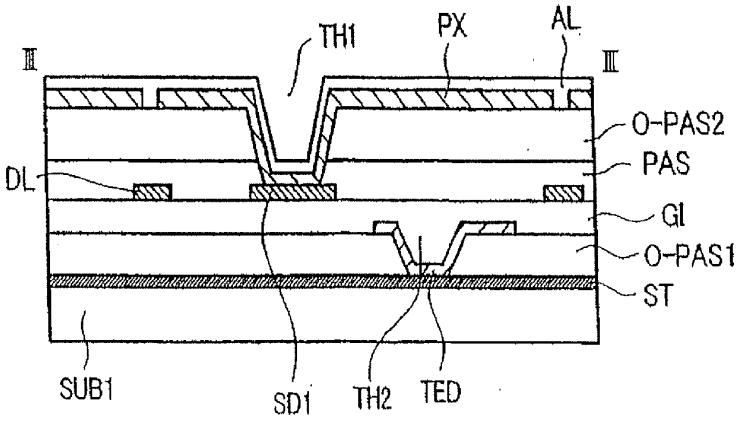

FIG. 36

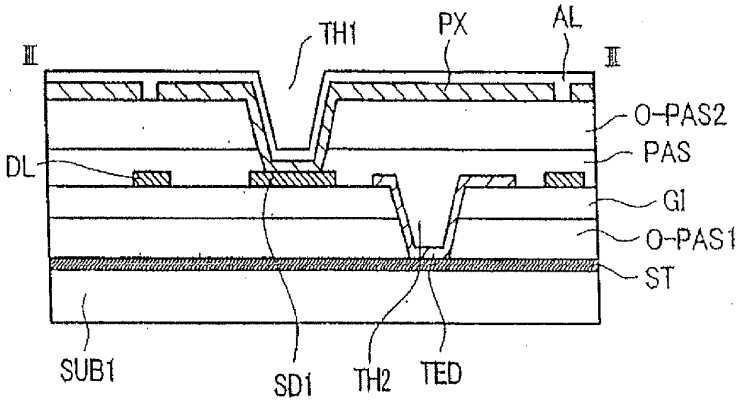

FIG. 37

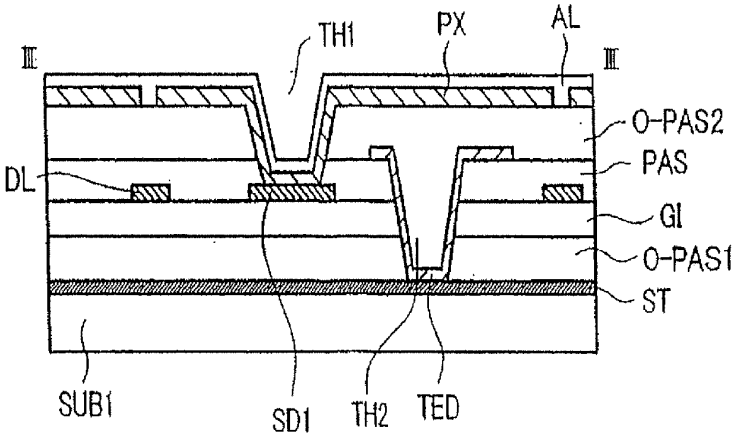

FIG. 38

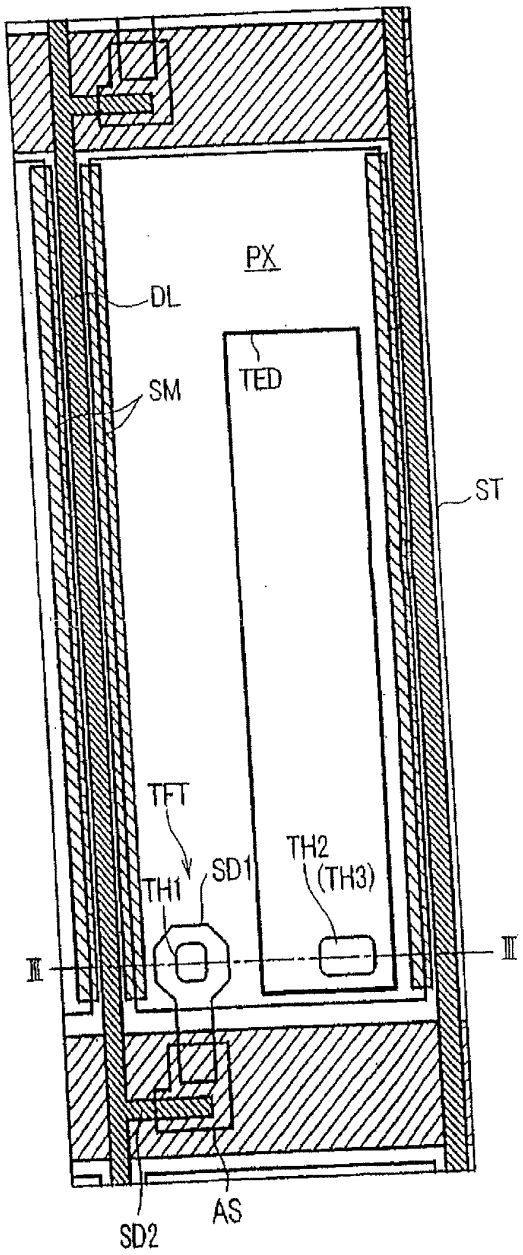

FIG. 39

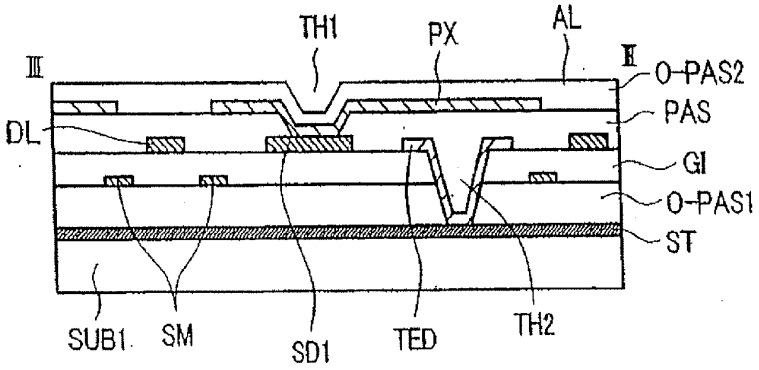

FIG. 40

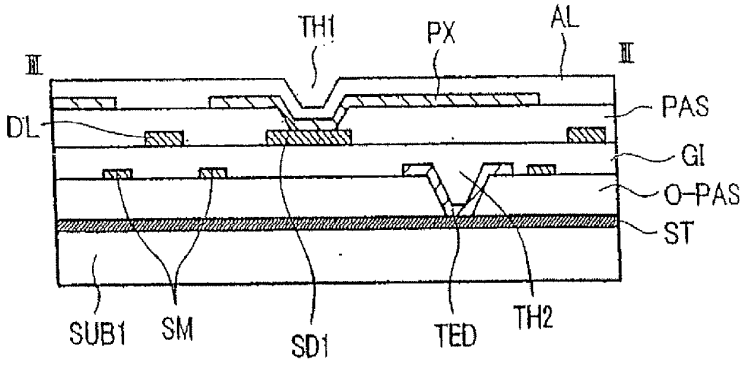

FIG. 41

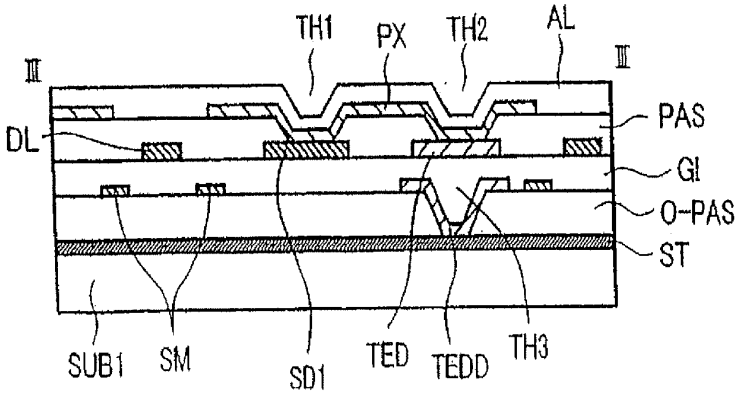

FIG. 42

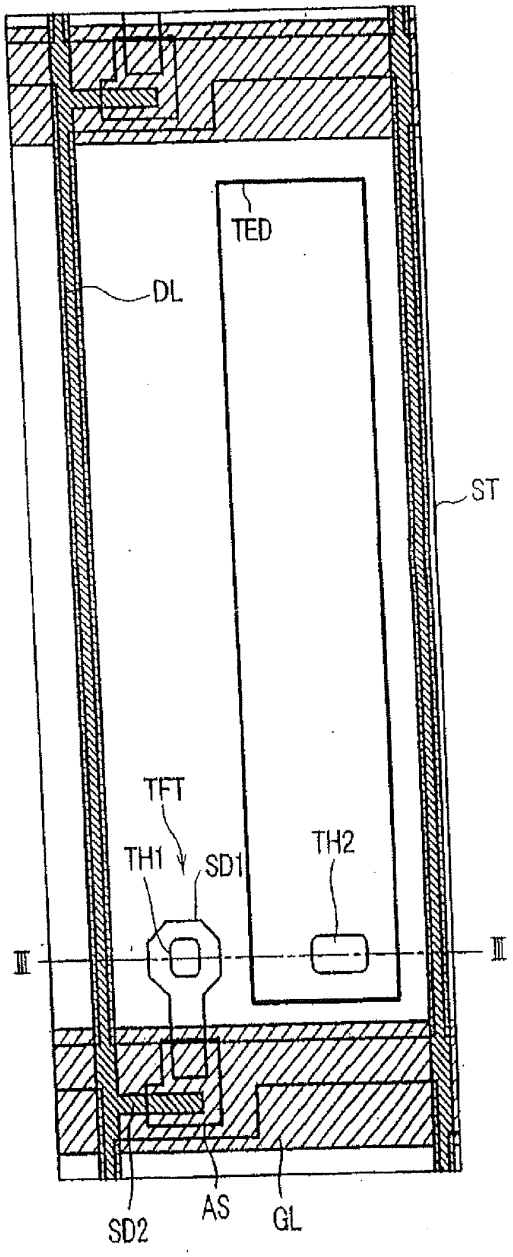

FIG. 43

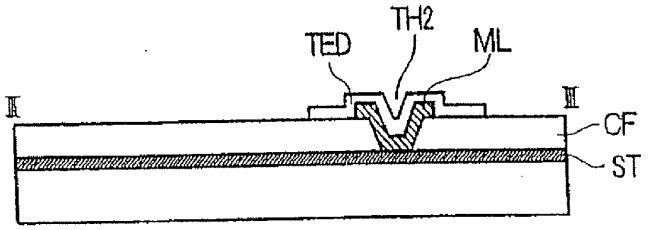

FIG. 44

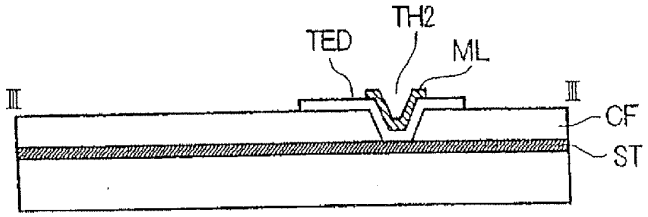

FIG. 45

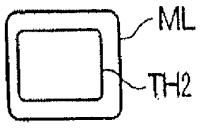

FIG. 46A

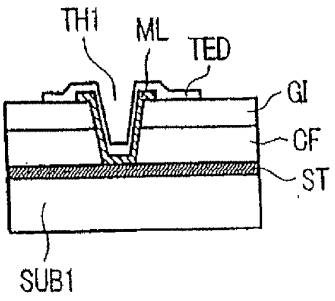

FIG. 46B

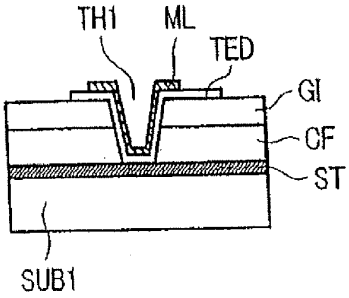

FIG. 46C

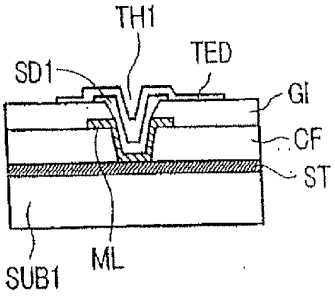

FIG. 46D

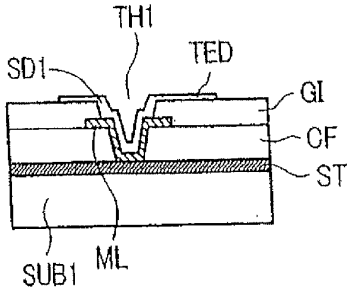

FIG. 47

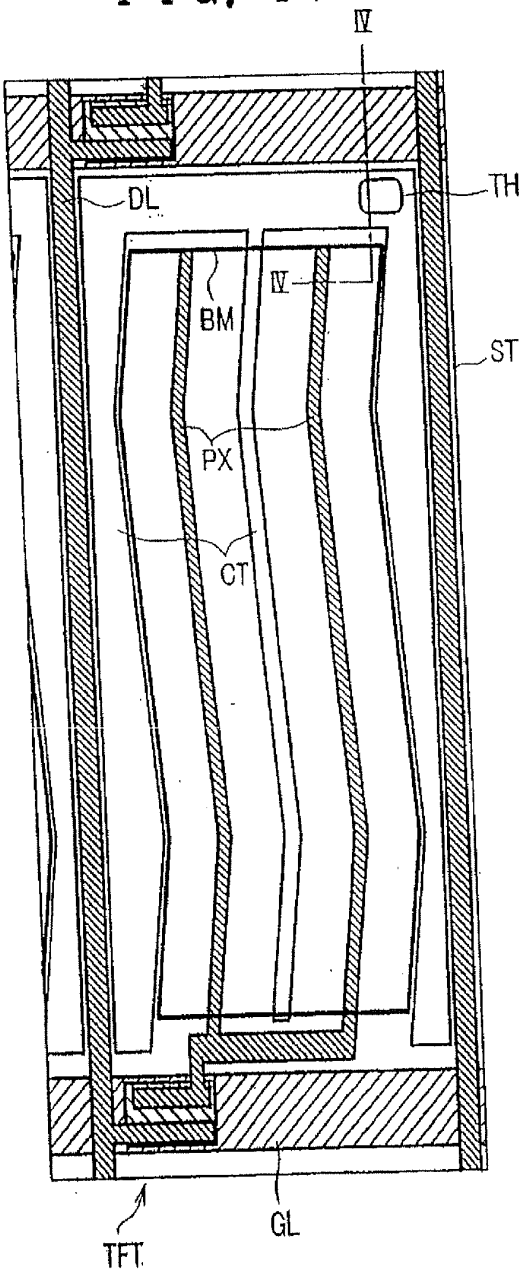

FIG. 48

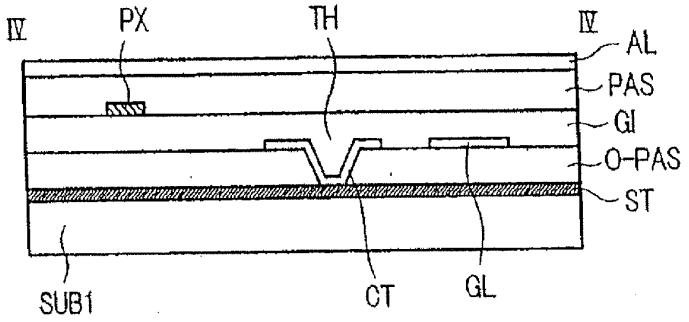

FIG. 49

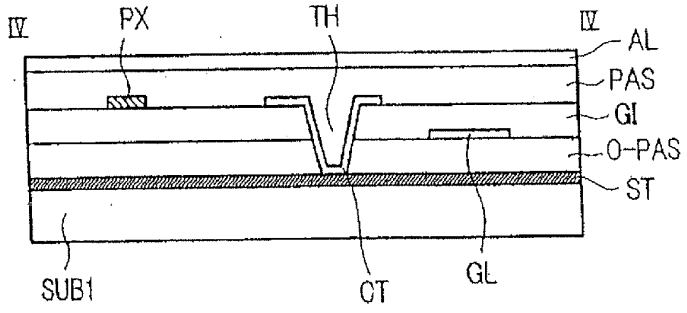

FIG. 50

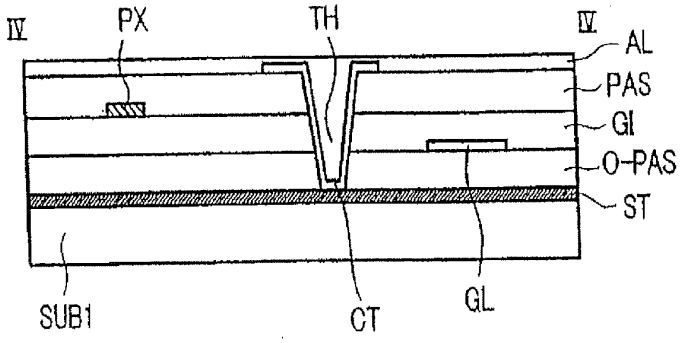

FIG. 51

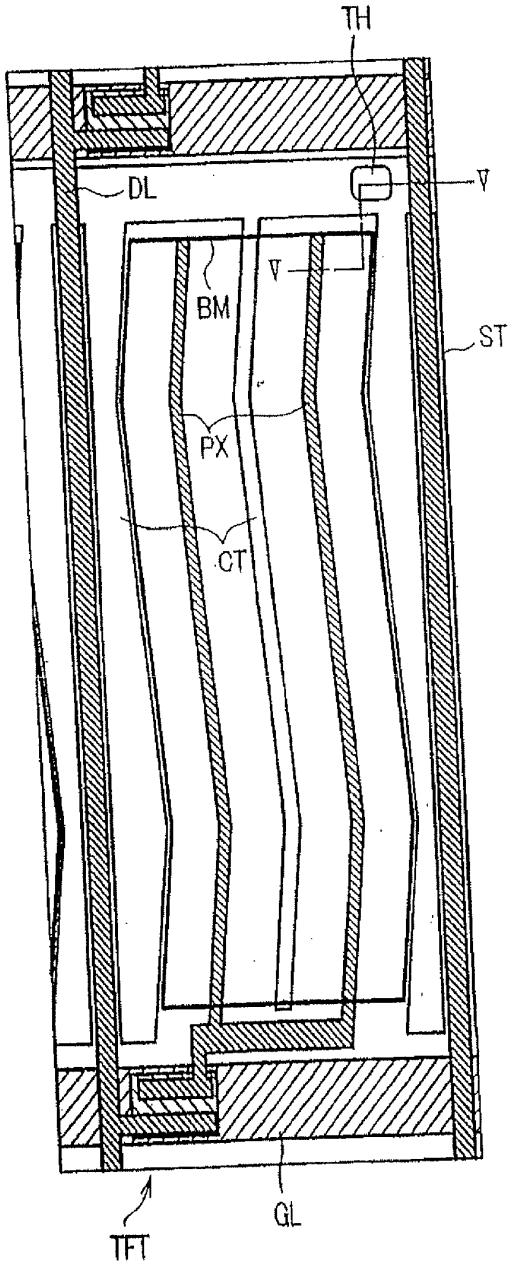

FIG. 52

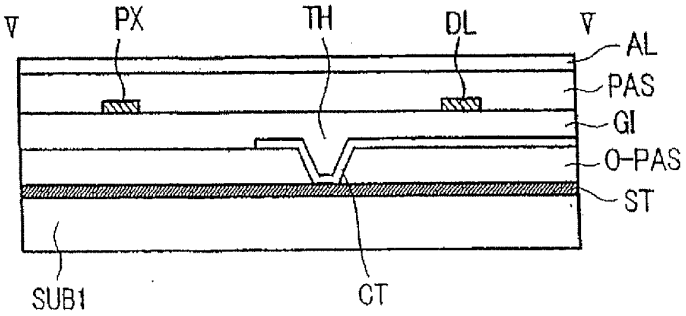
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FIG. 53

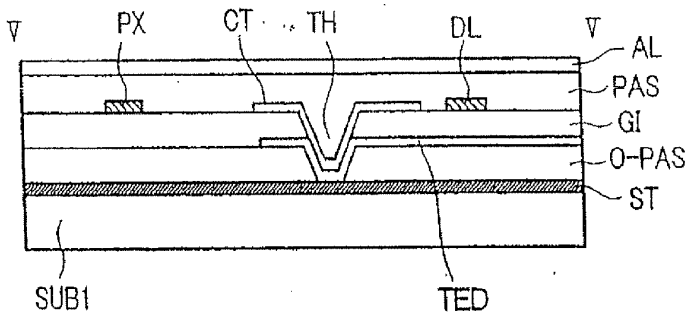
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FIG. 54

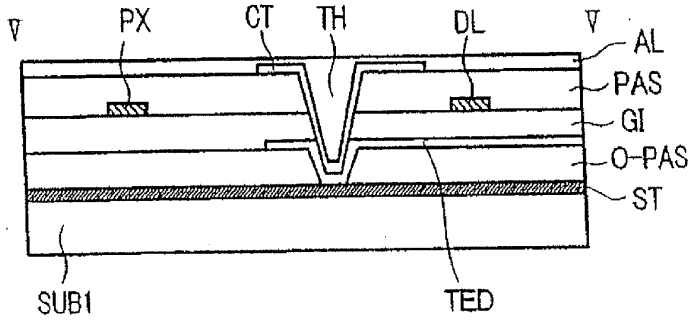
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FIG. 55

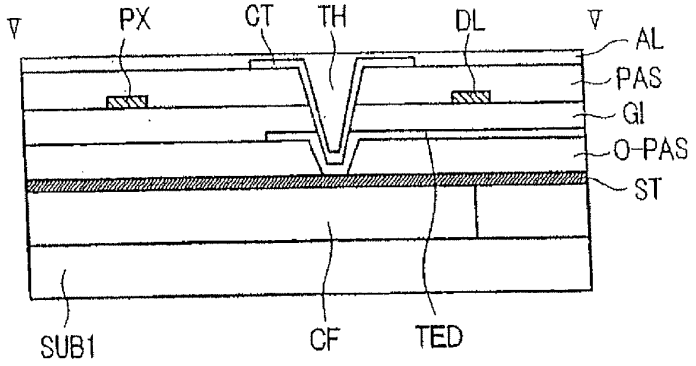
V
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FIG. 56

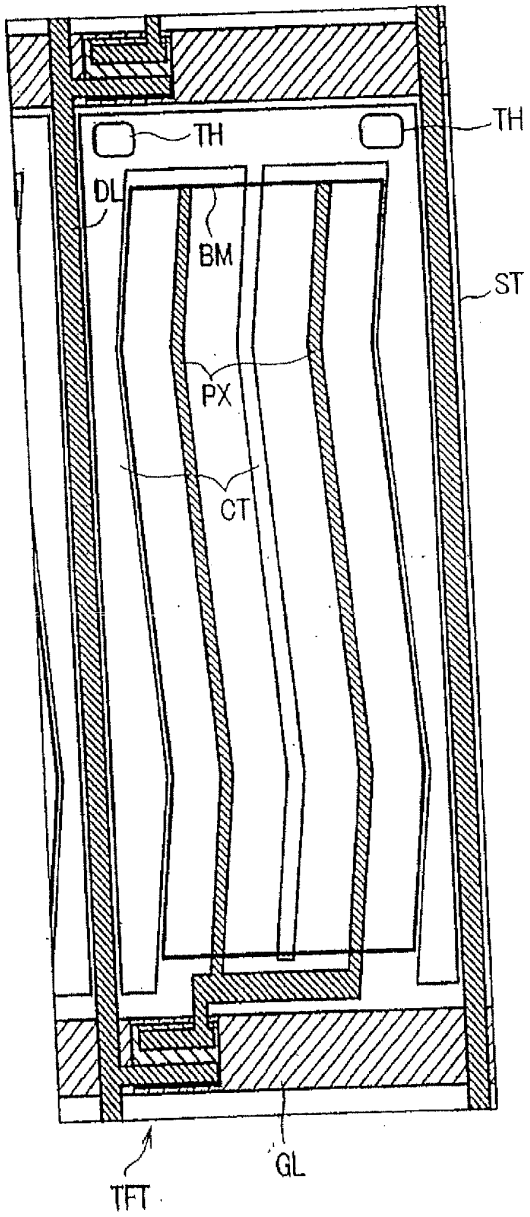

FIG. 57

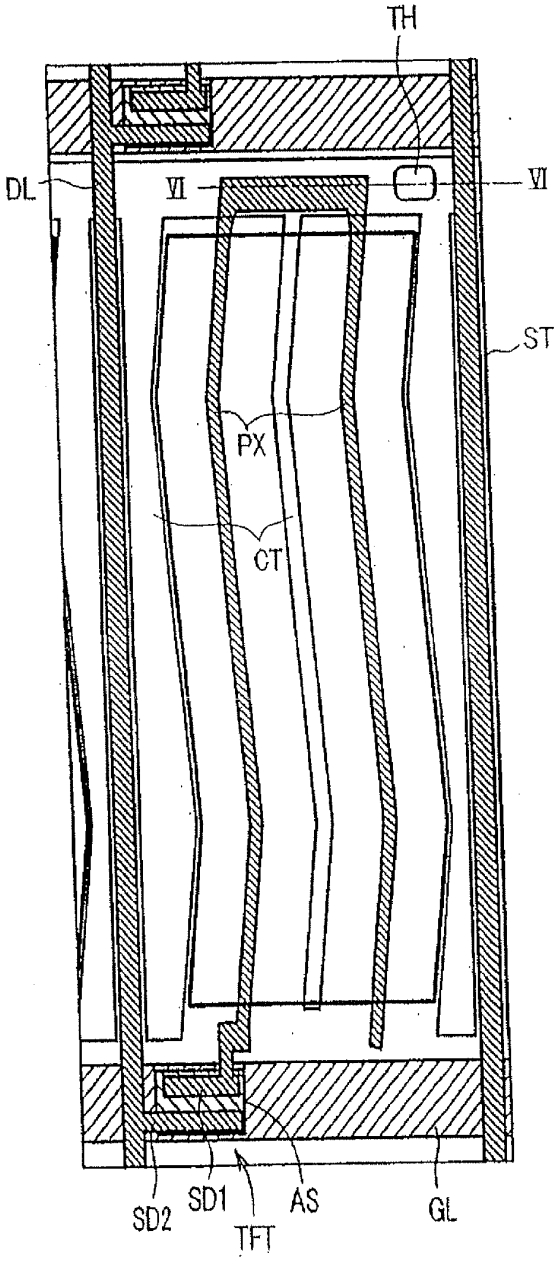

FIG. 58

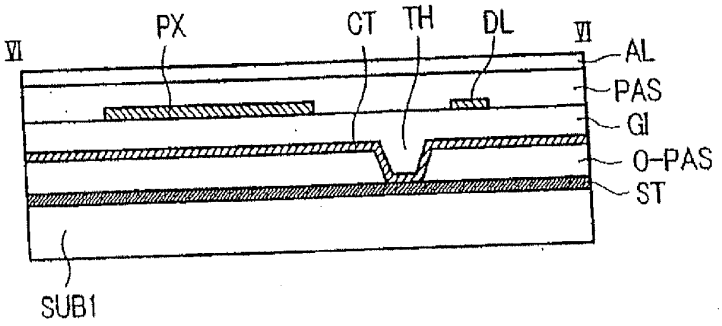
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FIG. 59

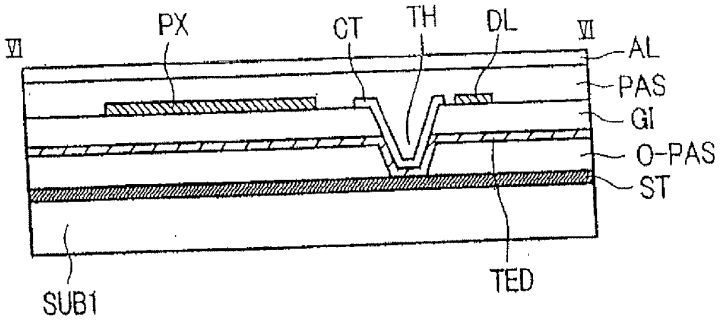
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FIG. 60

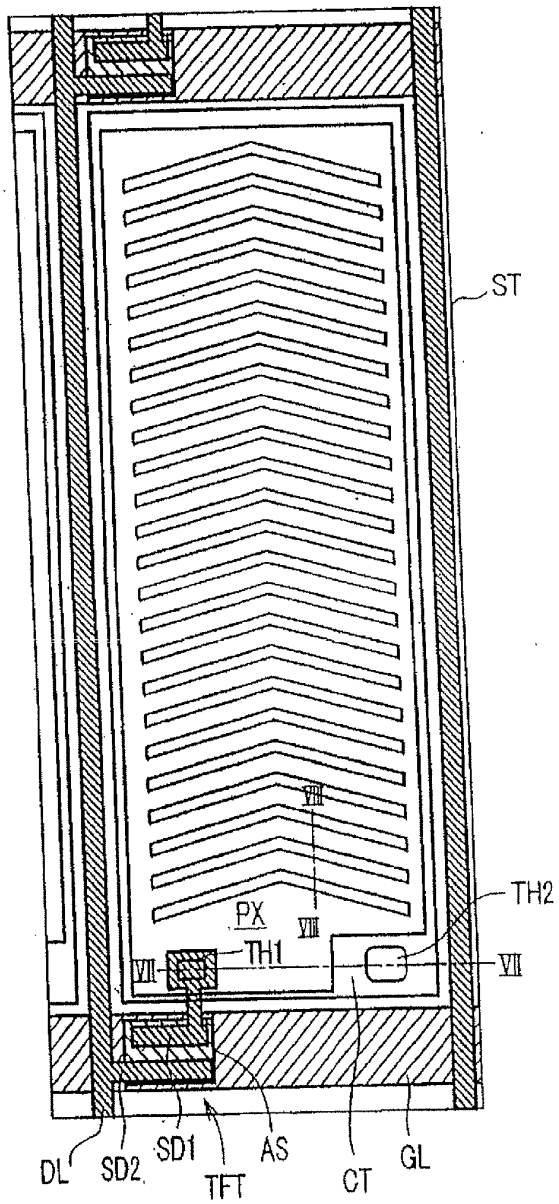


FIG. 61

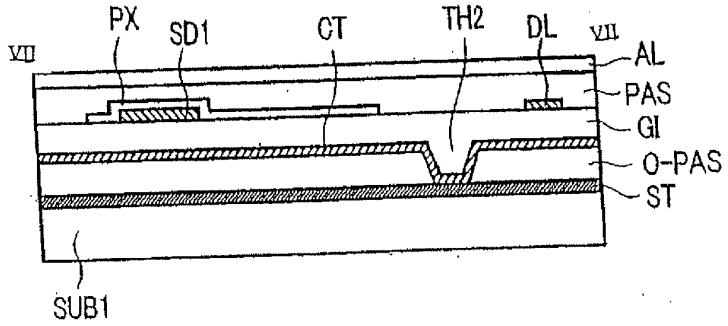

PX
SD1
CT
TH2
DL
VII
VII
AL
PAS
GI
O-PAS
ST
SUB1

FIG. 62

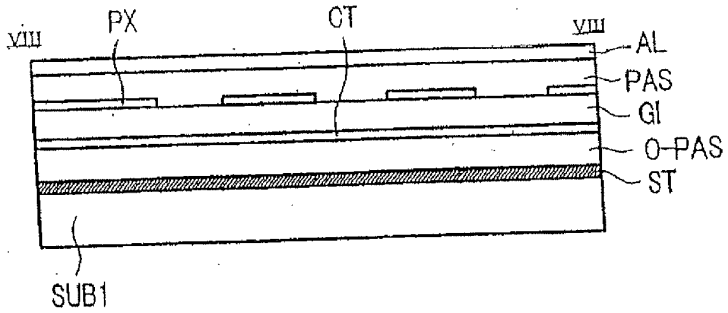

VIII
PX
CT
VIII
AL
PAS
GI
O-PAS
ST
SUB1

FIG. 63

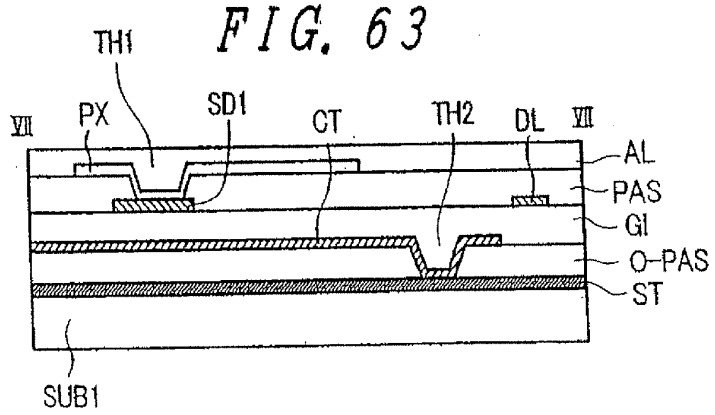

TH1
SD1
CT
TH2
DL
VII
PX
VII
AL
PAS
GI
O-PAS
ST
SUB1

FIG. 64

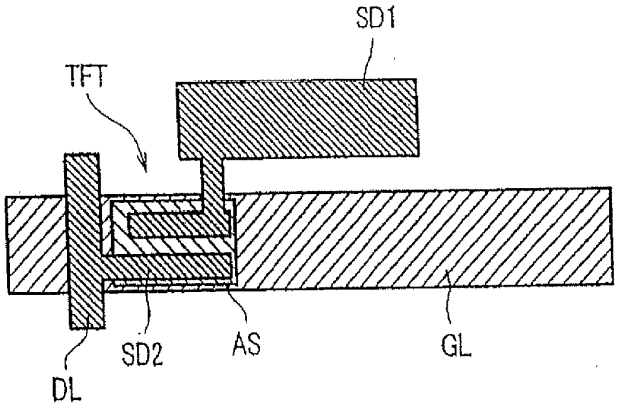

SD1
TFT
SD2
AS
GL
DL

FIG. 65

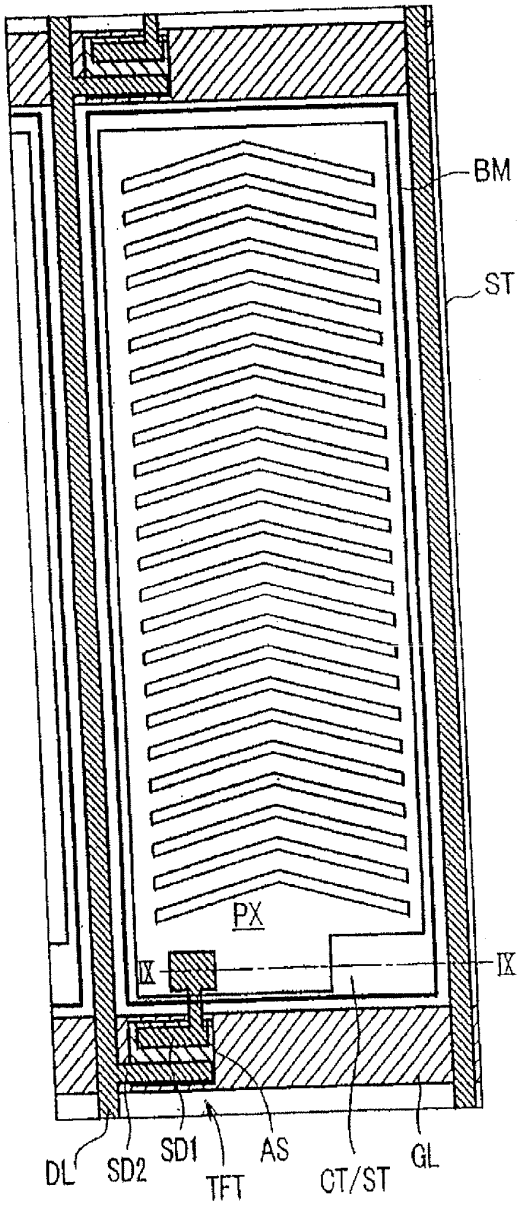


FIG. 66

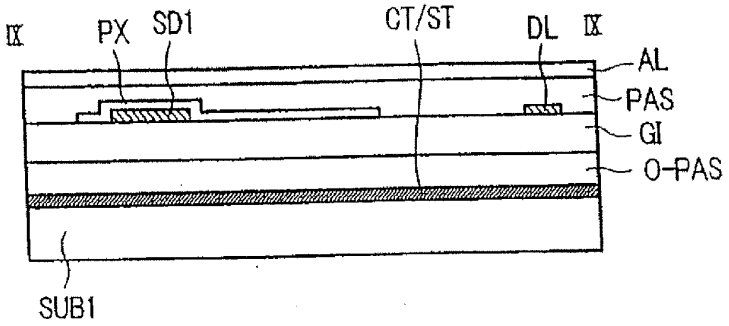

IX
PX
SD1
CT/ST
DL
IX
AL
PAS
GI
O-PAS
SUB1

FIG. 67

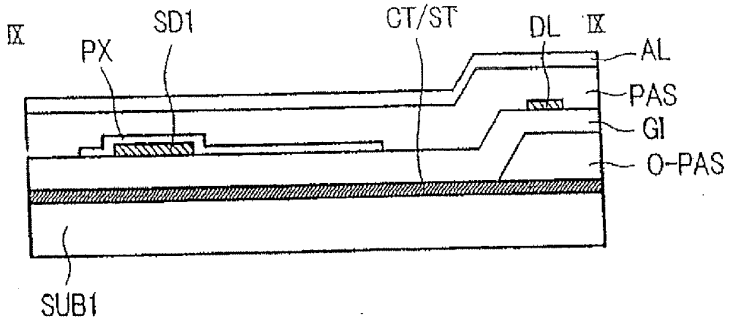

IX
SD1
PX
CT/ST
DL
IX
AL
PAS
GI
O-PAS
SUB1

FIG. 68

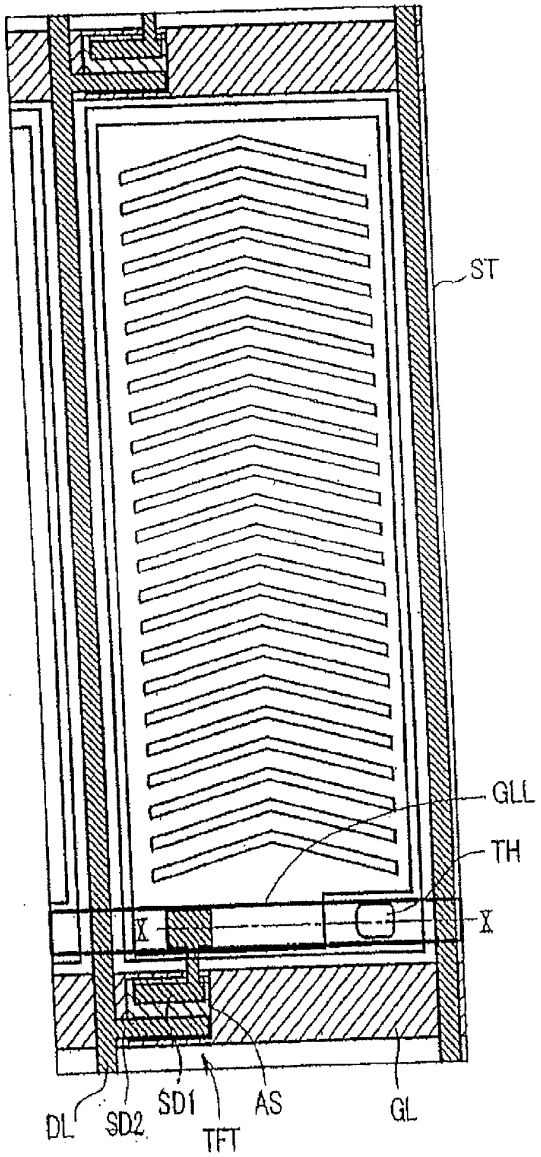


FIG. 69

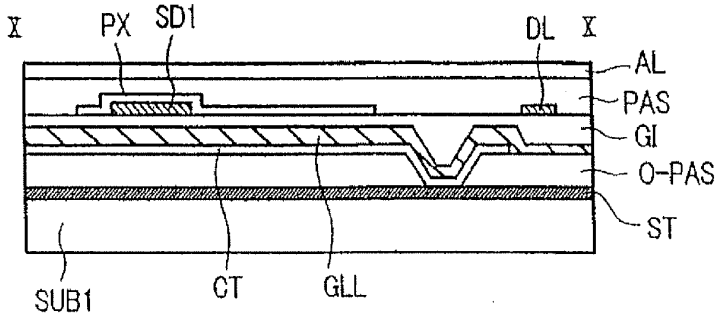

X
PX
SD1
DL
X
AL
PAS
GI
O-PAS
ST
SUB1
CT
GLL

FIG. 70

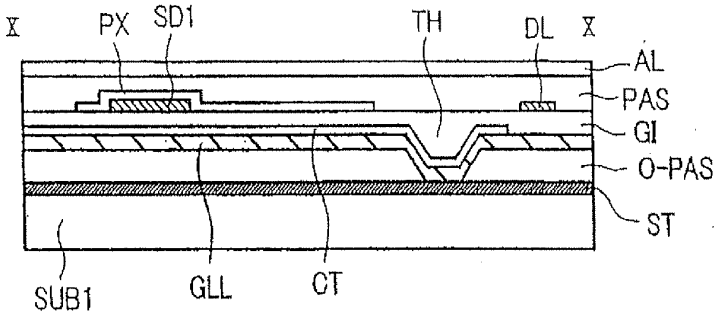

X
PX
SD1
TH
DL
X
AL
PAS
GI
O-PAS
ST
SUB1
GLL
CT

FIG. 71

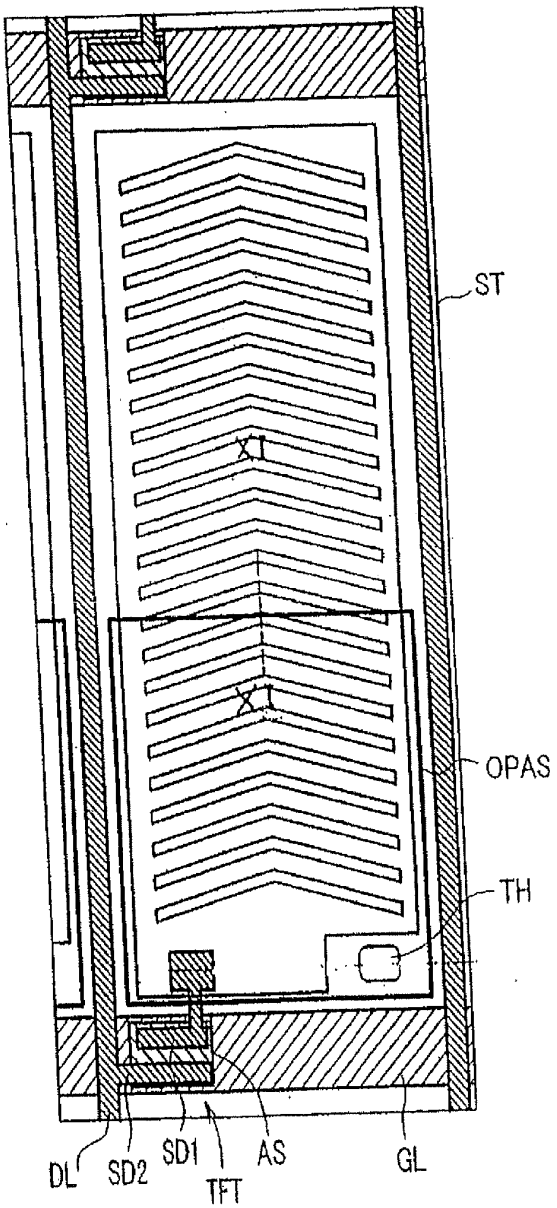


FIG. 72

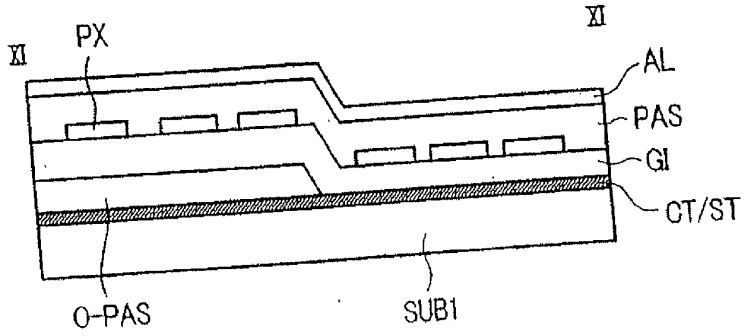

XI
PX
XI
AL
PAS
GI
CT/ST
O-PAS
SUB1

FIG. 73

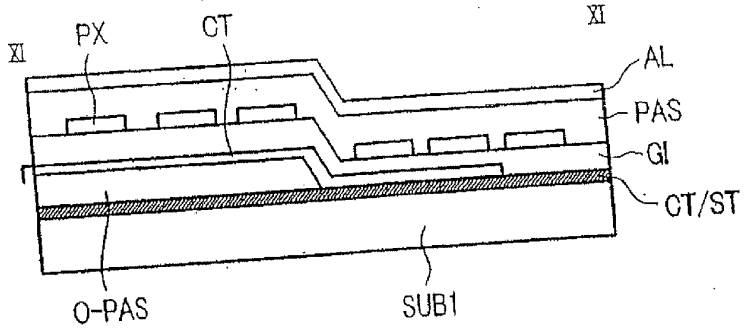

XI
PX
CT
XI
AL
PAS
GI
CT/ST
O-PAS
SUB1

FIG. 74

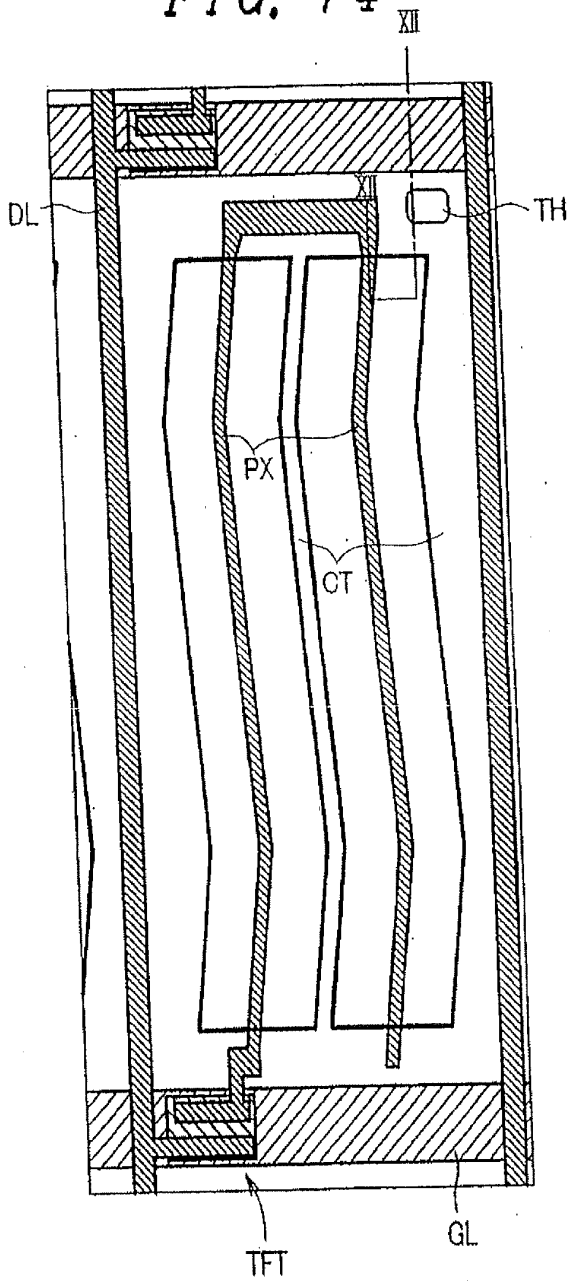


FIG. 75

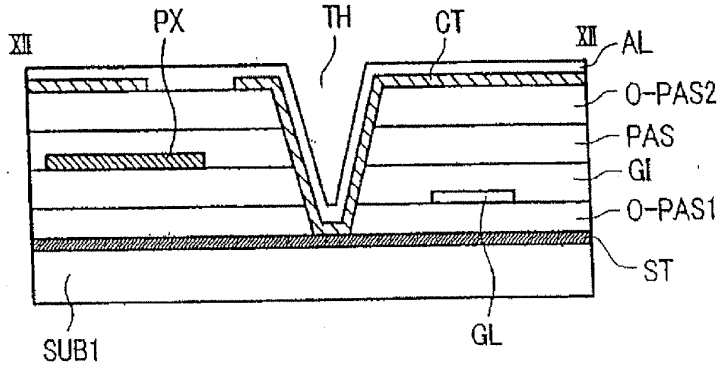

XII
PX
TH
CT
XII
AL
O-PAS2
PAS
GI
O-PAS1
ST
SUB1
GL

FIG. 76

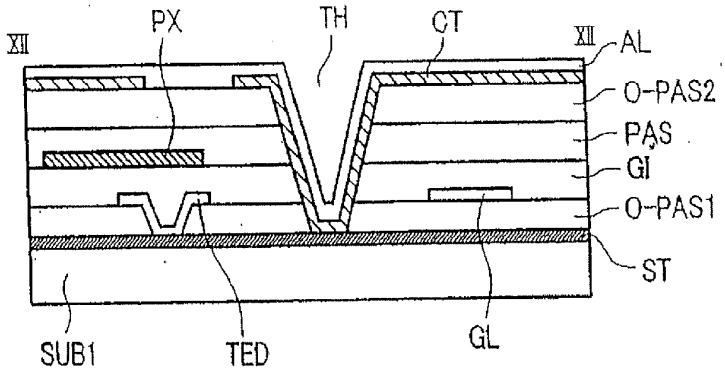

XII
PX
TH
CT
XII
AL
O-PAS2
PAS
GI
O-PAS1
ST
SUB1
TED
GL

FIG. 77

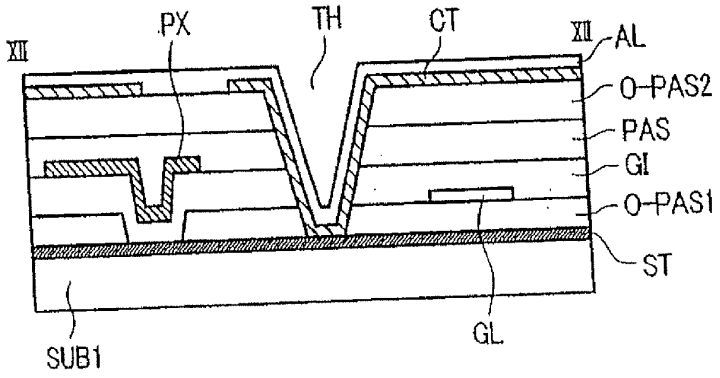

XII
PX
TH
CT
XII
AL
O-PAS2
PAS
GI
O-PAS1
ST
SUB1
GL

FIG. 78

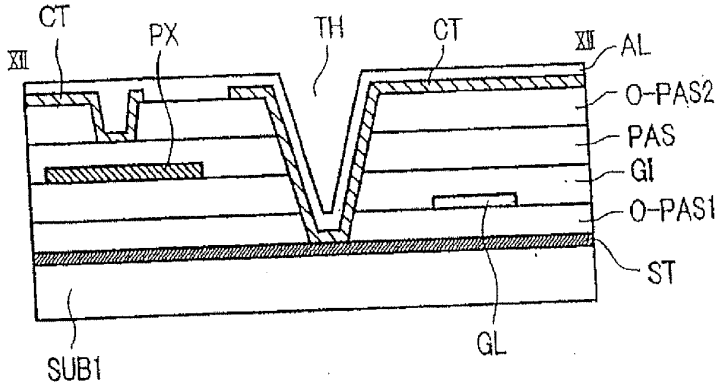

CT
XII
PX
TH
CT
XII
AL
O-PAS2
PAS
GI
O-PAS1
ST
SUB1
GL

FIG. 79

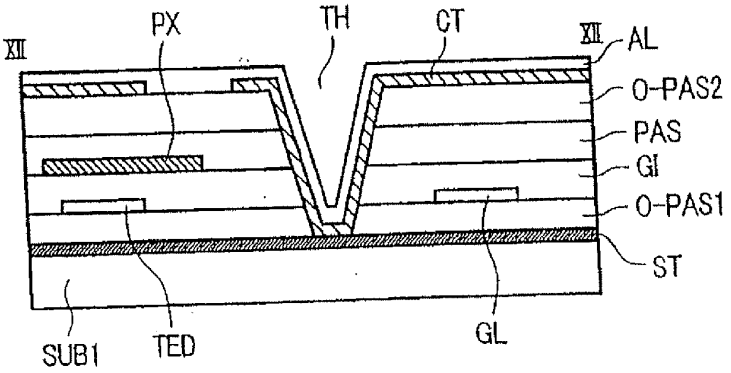

XII
PX
TH
CT
XII
AL
O-PAS2
PAS
GI
O-PAS1
ST
SUB1
TED
GL

FIG. 80

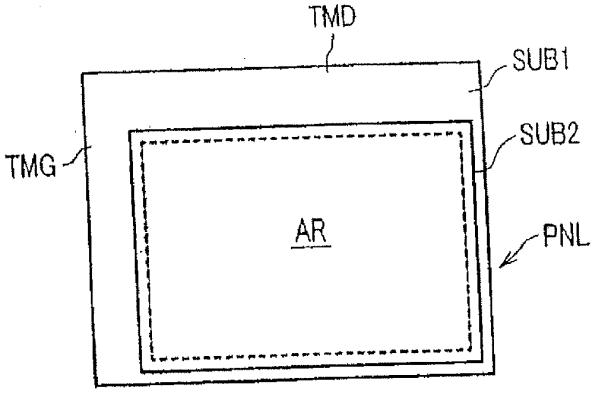

TMD
SUB1
SUB2
TMG
AR
PNL

FIG. 81

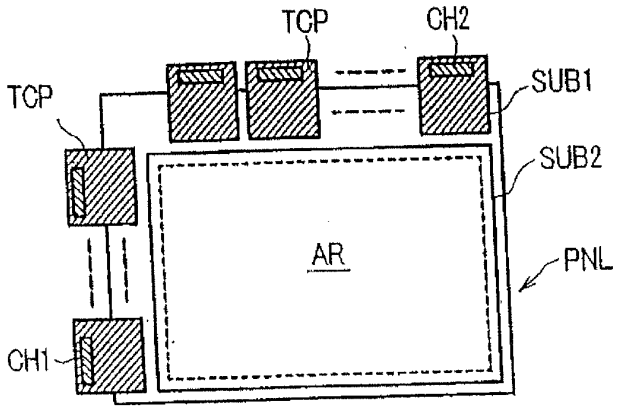


FIG. 82

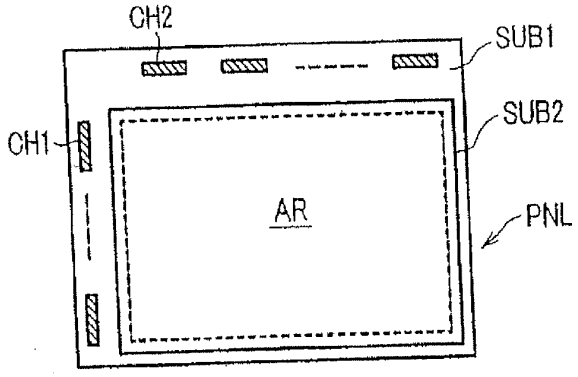


FIG. 83

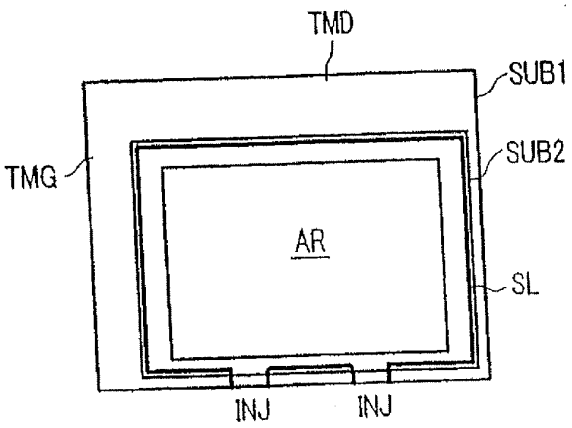


FIG. 84

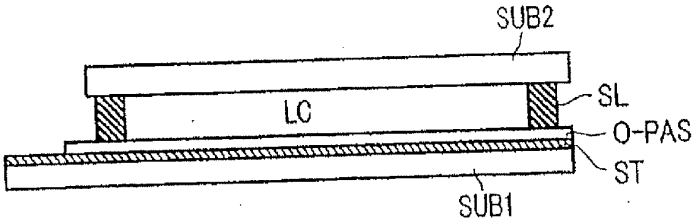


FIG. 85A

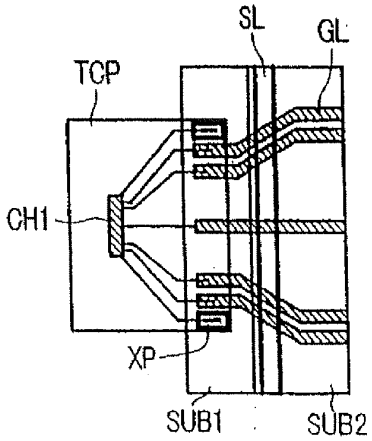


FIG. 85B

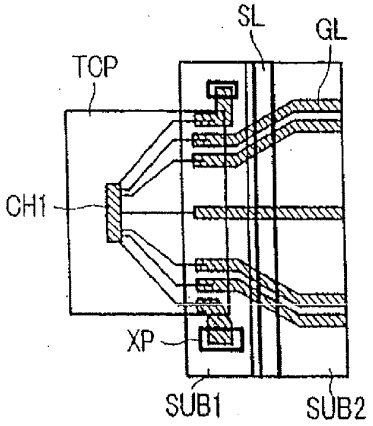


FIG. 85C

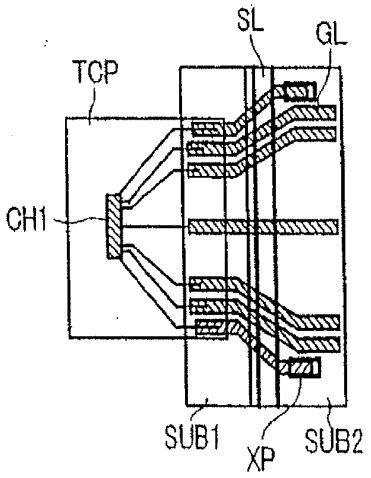


FIG. 86A

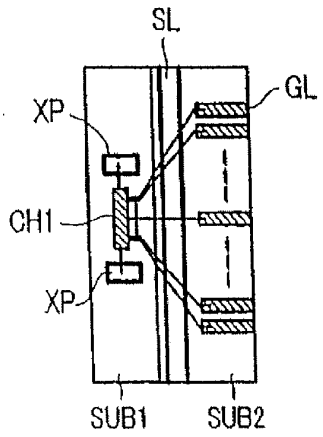


FIG. 86B

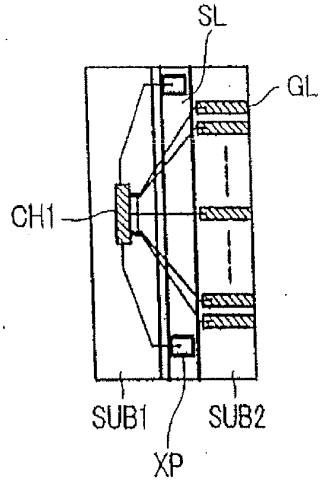


FIG. 87A

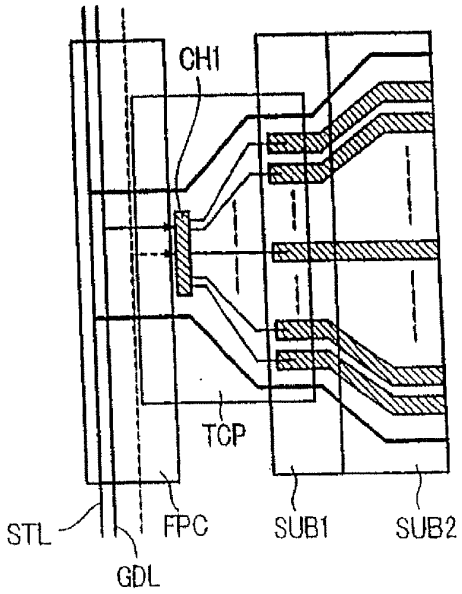


FIG. 87B

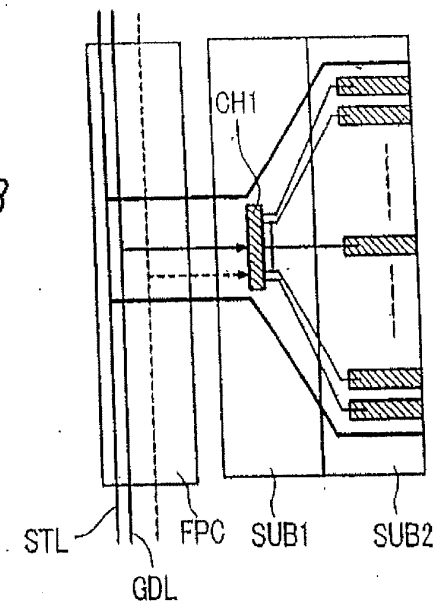


FIG. 88

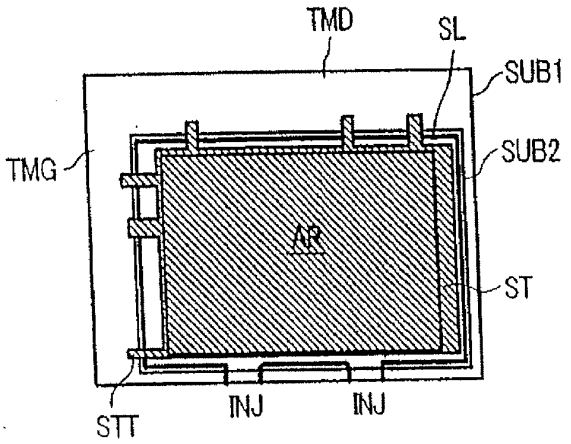

TMD
SL
SUB1
SUB2
TMG
AR
ST
STT
INJ
INJ

FIG. 89

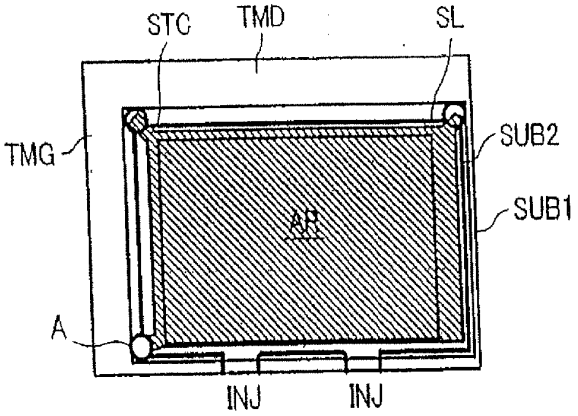

STC
TMD
SL
SUB2
TMG
AR
SUB1
A
INJ
INJ

FIG. 90

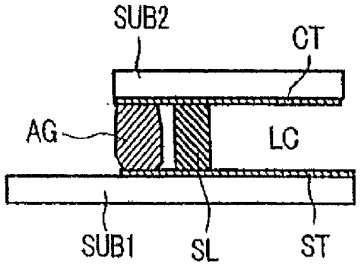


FIG. 91

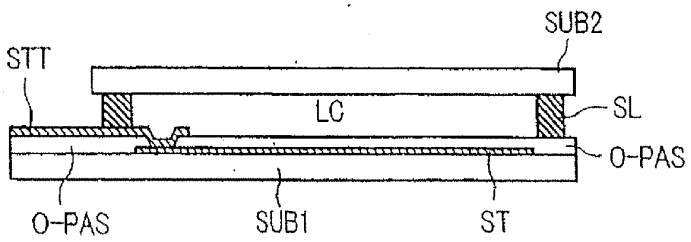


FIG. 92

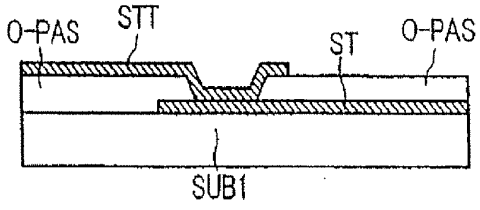


FIG. 93

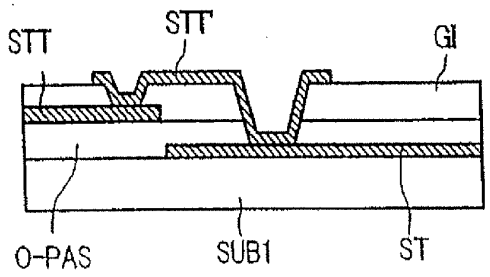


FIG. 94

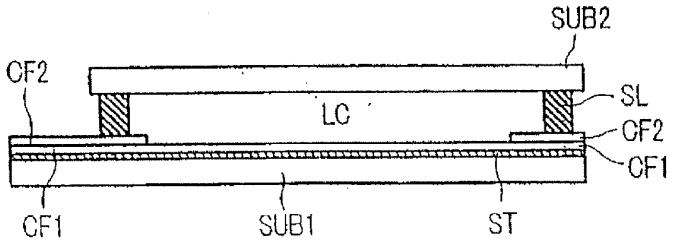


FIG. 95

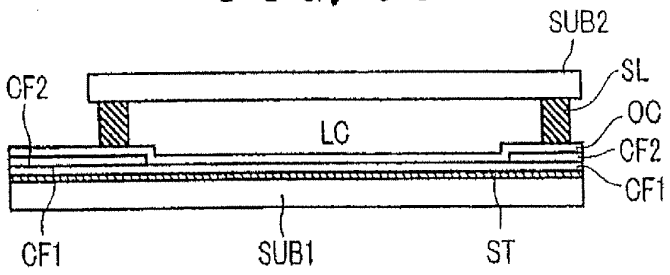


FIG. 96

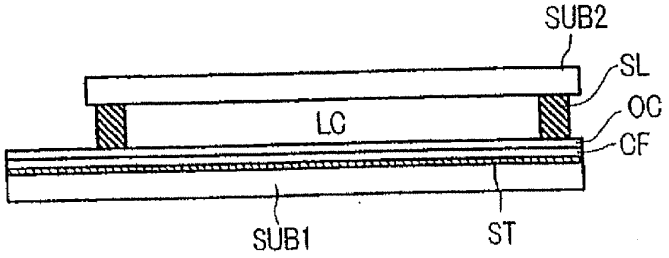


FIG. 97A

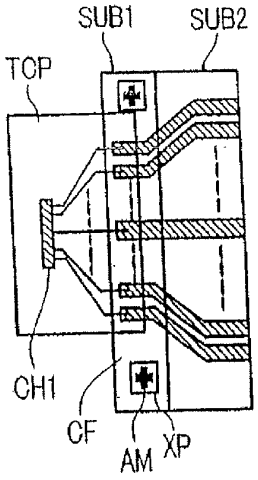


FIG. 97B

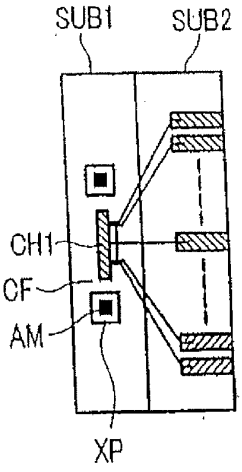


FIG. 98

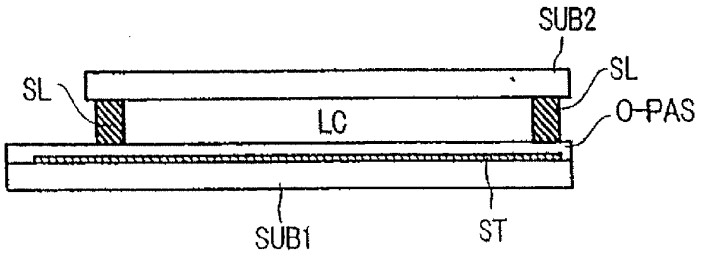


FIG. 99

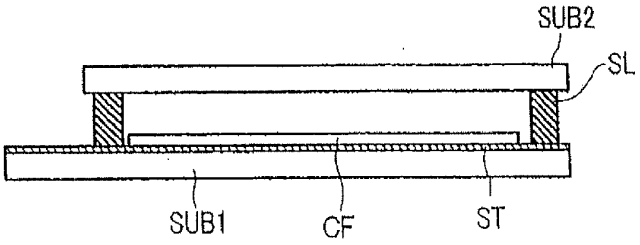


FIG. 100

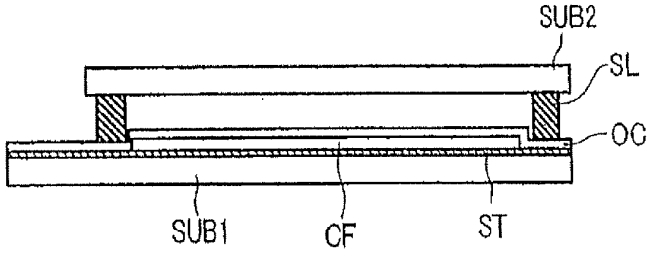


FIG. 101

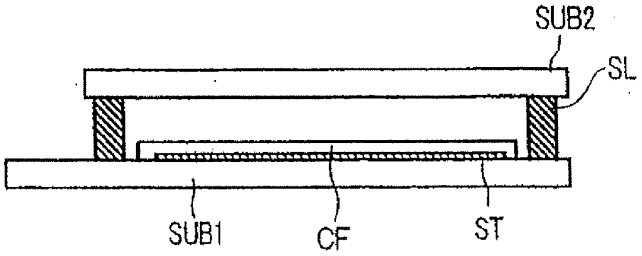


FIG. 102

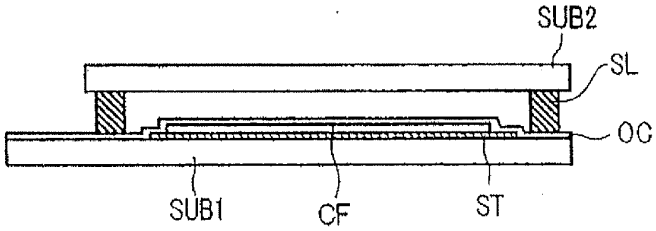


FIG. 103

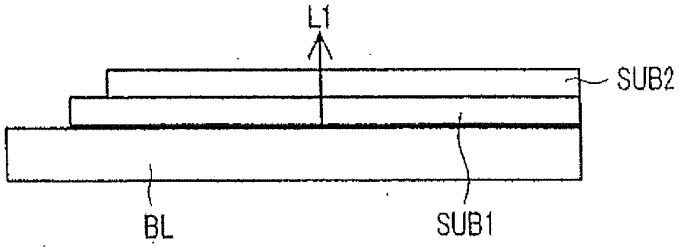


FIG. 104

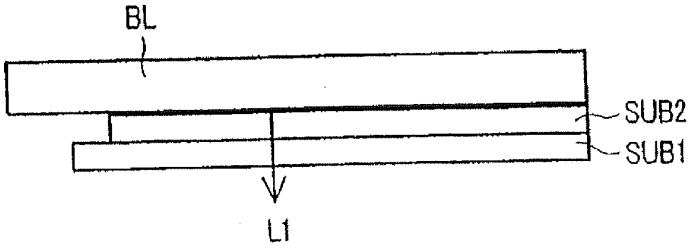


FIG. 105

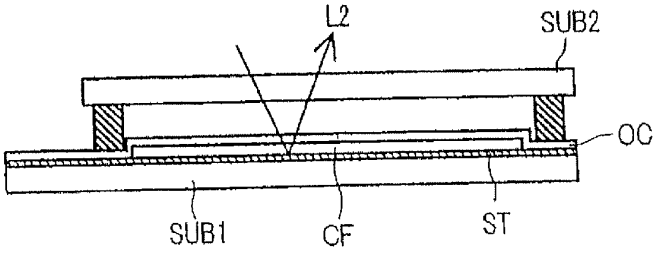


FIG. 106

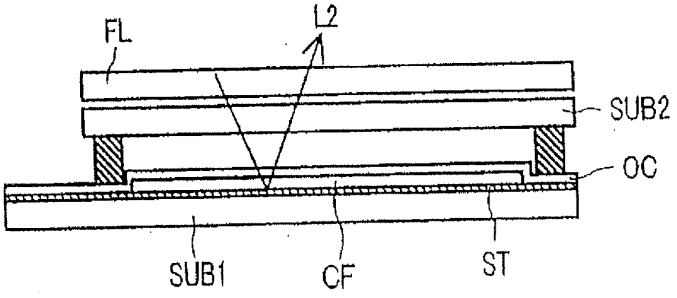


FIG. 107

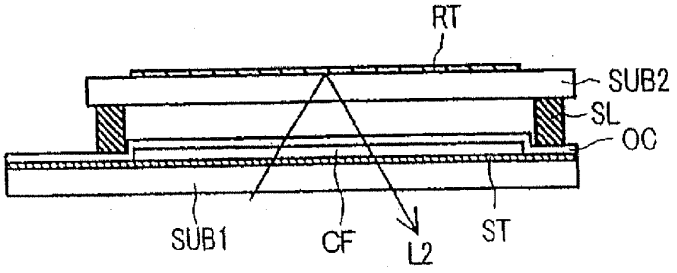


FIG. 108

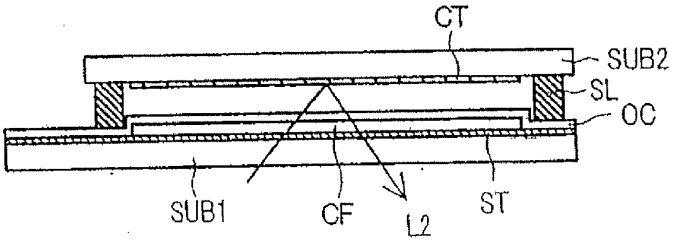


FIG. 109

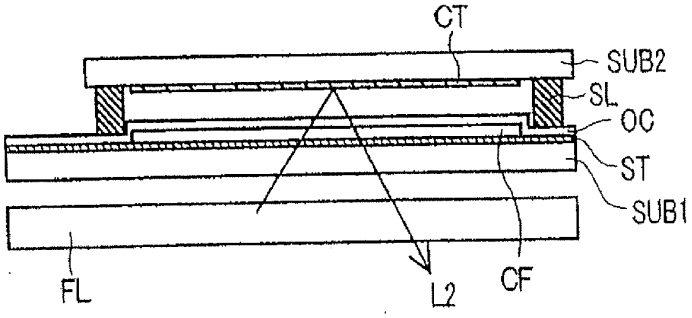


FIG. 110

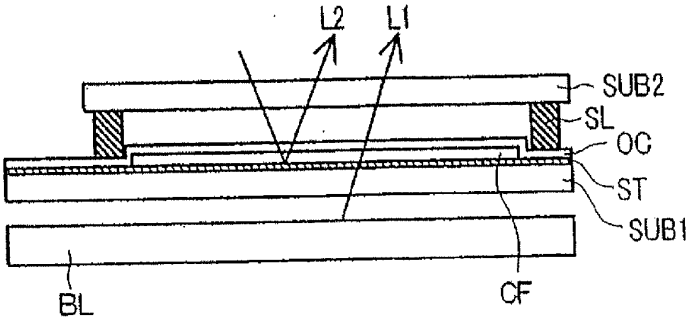
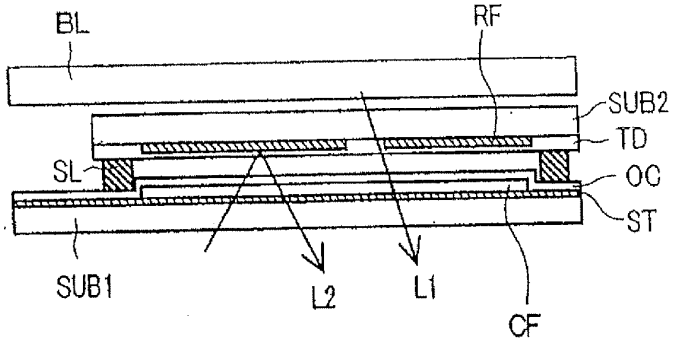


FIG. 111



PTO/AIA/01 (06-12)
Approved for use through 01/31/2014. OMB 0651-0032
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE

DECLARATION (37 CFR 1.63) FOR UTILITY OR DESIGN APPLICATION USING AN APPLICATION DATA SHEET (37 CFR 1.76)

Title of Invention	LIQUID CRYSTAL DISPLAY DEVICE, DISPLAY DEVICE AND MANUFACTURING METHOD THEREOF

As the below named inventor, I hereby declare that:

This declaration is directed to:

- ☐ The attached application, or
- ☐ United States application or PCT international application number _____ filed on _____

The above-identified application was made or authorized to be made by me.

I believe that I am the original inventor or an original joint inventor of a claimed invention in the application.

I hereby acknowledge that any willful false statement made in this declaration is punishable under 18 U.S.C. 1001 by fine or imprisonment of not more than five (5) years, or both.

WARNING:

Petitioner/applicant is cautioned to avoid submitting personal information in documents filed in a patent application that may contribute to identity theft. Personal information such as social security numbers, bank account numbers, or credit card numbers (other than a check or credit card authorization form PTO-2038 submitted for payment purposes) is never required by the USPTO to support a petition or an application. If this type of personal information is included in documents submitted to the USPTO, petitioners/applicants should consider redacting such personal information from the documents before submitting them to the USPTO. Petitioner/applicant is advised that the record of a patent application is available to the public after publication of the application (unless a non-publication request in compliance with 37 CFR 1.213(a) is made in the application) or issuance of a patent. Furthermore, the record from an abandoned application may also be available to the public if the application is referenced in a published application or an issued patent (see 37 CFR 1.14). Checks and credit card authorization forms PTO-2038 submitted for payment purposes are not retained in the application file and therefore are not publicly available.

LEGAL NAME OF INVENTOR

Inventor: Yoshiaki NAKAYOSHI Date (Optional): _____

Signature: Yoshiaki Nakayoshi

Note: An application data sheet (PTO/AIA/14 or equivalent), including naming the entire inventive entity, must accompany this form. Use an additional PTO/SB/A/A01 form for each additional inventor.

PTO/AIA/01 (06-12)
Approved for use through 01/31/2014. OMB 0651-0032
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE

DECLARATION (37 CFR 1.63) FOR UTILITY OR DESIGN APPLICATION USING AN APPLICATION DATA SHEET (37 CFR 1.76)

Title of Invention	LIQUID CRYSTAL DISPLAY DEVICE, DISPLAY DEVICE AND MANUFACTURING METHOD THEREOF

As the below named inventor, I hereby declare that:

This declaration is directed to:

- ☐ The attached application, or
- ☐ United States application or PCT international application number _____
  filed on _____

The above-identified application was made or authorized to be made by me.

I believe that I am the original inventor or an original joint inventor of a claimed invention in the application.

I hereby acknowledge that any willful false statement made in this declaration is punishable under 18 U.S.C. 1001 by fine or imprisonment of not more than five (5) years, or both.

WARNING:

Petitioner/applicant is cautioned to avoid submitting personal information in documents filed in a patent application that may contribute to identity theft. Personal information such as social security numbers, bank account numbers, or credit card numbers (other than a check or credit card authorization form PTO-2038 submitted for payment purposes) is never required by the USPTO to support a petition or an application. If this type of personal information is included in documents submitted to the USPTO, petitioners/applicants should consider redacting such personal information from the documents before submitting them to the USPTO. Petitioner/applicant is advised that the record of a patent application is available to the public after publication of the application (unless a non-publication request in compliance with 37 CFR 1.213(a) is made in the application) or issuance of a patent. Furthermore, the record from an abandoned application may also be available to the public if the application is referenced in a published application or an issued patent (see 37 CFR 1.14). Checks and credit card authorization forms PTO-2038 submitted for payment purposes are not retained in the application file and therefore are not publicly available.

LEGAL NAME OF INVENTOR

Inventor: Kazuhiko YANAGAWA Date (Optional): _____

Signature: Kazuhiko Yanagawa

Note: An application data sheet (PTO/AIA/14 or equivalent), including naming the entire inventive entity, must accompany this form. Use an additional PTO/SB/AIA01 form for each additional inventor.

Electronic Patent Application Fee Transmittal

Application Number:	
Filing Date:	
Title of Invention:	LIQUID CRYSTAL DISPLAY DEVICE, DISPLAY DEVICE AND MANUFACTURING METHOD THEREOF
First Named Inventor/Applicant Name:	Yoshiaki NAKAYOSHI
Filer:	Juan Carlos A. Marquez/Lily Niu
Attorney Docket Number:	HARU-0126

Filed as Large Entity

Filing Fees for Utility under 35 USC 111(a)

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Basic Filing:				
UTILITY APPLICATION FILING	1011	1	280	280
UTILITY SEARCH FEE	1111	1	600	600
UTILITY EXAMINATION FEE	1311	1	720	720
Pages:				
Claims:				
Miscellaneous-Filing:				
Petition:				
Patent-Appeals-and-Interference:				

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Post-Allowance-and-Post-Issuance:				
Extension-of-Time:				
Miscellaneous:				
		Total in USD ($)		**1600**

Electronic Acknowledgement Receipt	
EFS ID:	26988955
Application Number:	15271422
International Application Number:	
Confirmation Number:	2686
Title of Invention:	LIQUID CRYSTAL DISPLAY DEVICE, DISPLAY DEVICE AND MANUFACTURING METHOD THEREOF
First Named Inventor/Applicant Name:	Yoshiaki NAKAYOSHI
Customer Number:	38327
Filer:	Juan Carlos A. Marquez/Lily Niu
Filer Authorized By:	Juan Carlos A. Marquez
Attorney Docket Number:	HARU-0126
Receipt Date:	21-SEP-2016
Filing Date:	
Time Stamp:	12:14:21
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	yes
Payment Type	Credit Card
Payment was successfully received in RAM	$1600
RAM confirmation Number	9637
Deposit Account	
Authorized User	
The Director of the USPTO is hereby authorized to charge indicated fees and credit any overpayment as follows:	

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Transmittal of New Application	HARU-126-Continuation_transmittal.pdf	212146 88421166dbef1b12ff9f1284614bc49482c9f946	no	1
Warnings:					
Information:					
2	Application Data Sheet	HARU-126-ADS.pdf	1824109 054a0fd9e7e50aa9b634d79cd739f3c76715161c	no	10
Warnings:					
Information:					
3	Specification	HARU-126-SPECIFICATION.pdf	389931 2ed783256d5f47d89d2cdd36885b5cf28752cb2d	no	59
Warnings:					
Information:					
4	Claims	HARU-126-CLAIMS.pdf	78151 a755fdb0d74e1670b08d5fc443d560fa15c33c53	no	3
Warnings:					
Information:					
5	Abstract	HARU-126-Abstract.pdf	39683 3ed08f495506b5018efed3ee155b8439e49323b2	no	1
Warnings:					
The page size in the PDF is too large. The pages should be 8.5 x 11 or A4. If this PDF is submitted, the pages will be resized upon entry into the Image File Wrapper and may affect subsequent processing					
Information:					
6	Drawings-only black and white line drawings	HARU-126-Drawings.pdf	3124276 355a2d9dced6cfe8a9fcc74a9310300836cc320f	no	63
Warnings:					

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Information:					
7	Oath or Declaration filed	HARU-126-Declarations.pdf	278354 dbe344f81488f8d6a90454704ffebd1109e51589	no	2
Warnings:					
The page size in the PDF is too large. The pages should be 8.5 x 11 or A4. If this PDF is submitted, the pages will be resized upon entry into the Image File Wrapper and may affect subsequent processing					
Information:					
8	Fee Worksheet (SB06)	fee-info.pdf	35092 9ecf9e8ea7cbc59b6086902ca2fc8d3cf2797a0f	no	2
Warnings:					
Information:					
			Total Files Size (in bytes):	5981742	

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111
If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371
If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office
If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

Doc Code: PA..
Document Description: Power of Attorney

PTO/AIA/82A (07-13)
Approved for use through 11/30/2014. OMB 0651-0051
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

TRANSMITTAL FOR POWER OF ATTORNEY TO ONE OR MORE REGISTERED PRACTITIONERS

NOTE: This form is to be submitted with the Power of Attorney by Applicant form (PTO/AIA/82B) to identify the application to which the Power of Attorney is directed, in accordance with 37 CFR 1.5, unless the application number and filing date are identified in the Power of Attorney by Applicant form. If neither form PTO/AIA/82A nor form PTO/AIA82B identifies the application to which the Power of Attorney is directed, the Power of Attorney will not be recognized in the application.

Application Number	15/271,422
Filing Date	September 21, 2016
First Named Inventor	Yoshiaki NAKAYOSHI
Title	LIQUID CRYSTAL DISPLAY DEVICE, DISPLAY DEVICE AND MANUFACTURING METHOD THEREOF
Art Unit	
Examiner Name	
Attorney Docket Number	HARU-0126

SIGNATURE of Applicant or Patent Practitioner

Signature	/juan.carlos.a.marquez/	Date (Optional)	09-21-2016
Name	Juan Carlos A. Marquez	Registration Number	34,072
Title (if Applicant is a juristic entity)	Attorney of Record		
Applicant Name (if Applicant is a juristic entity)			

NOTE: This form must be signed in accordance with 37 CFR 1.33. See 37 CFR 1.4(d) for signature requirements and certifications. If more than one applicant, use multiple forms.

☐ *Total of _____ forms are submitted.

This collection of information is required by 37 CFR 1.131, 1.32, and 1.33. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.11 and 1.14. This collection is estimated to take 3 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

Doc Code: PA...
Document Description: Power of Attorney

PTO/AIA/82B (07-13)
Approved for use through 11/30/2014. OMB 0651-0051
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number

POWER OF ATTORNEY BY APPLICANT

I hereby revoke all previous powers of attorney given in the application identified in either the attached transmittal letter or the boxes below.

Application Number	Filing Date

(Note: The boxes above may be left blank if information is provided on form PTO/AIA/82A.)

☑ I hereby appoint the Patent Practitioner(s) associated with the following Customer Number as my/our attorney(s) or agent(s), and to transact all business in the United States Patent and Trademark Office connected therewith for the application referenced in the attached transmittal letter (form PTO/AIA/82A) or identified above: 38327

OR

☐ I hereby appoint Practitioner(s) named in the attached list (form PTO/AIA/82C) as my/our attorney(s) or agent(s), and to transact all business in the United States Patent and Trademark Office connected therewith for the patent application referenced in the attached transmittal letter (form PTO/AIA/82A) or identified above. (Note: Complete form PTO/AIA/82C.)

Please recognize or change the correspondence address for the application identified in the attached transmittal letter or the boxes above to:

☑ The address associated with the above-mentioned Customer Number

OR

☐ The address associated with Customer Number:

OR

Firm or Individual Name					
Address					
City		State		Zip	
Country					
Telephone		Email			

I am the Applicant (if the Applicant is a juristic entity, list the Applicant name in the box):

☐ Inventor or Joint Inventor (title not required below)

☐ Legal Representative of a Deceased or Legally Incapacitated Inventor (title not required below)

☑ Assignee or Person to Whom the Inventor is Under an Obligation to Assign (provide signer's title if applicant is a juristic entity)

☐ Person Who Otherwise Shows Sufficient Proprietary Interest (e.g., a petition under 37 CFR 1.46(b)(2) was granted in the application or is concurrently being filed with this document) (provide signer's title if applicant is a juristic entity)

SIGNATURE of Applicant for Patent

The undersigned (whose title is supplied below) is authorized to act on behalf of the applicant (e.g., where the applicant is a juristic entity).

Signature	/Kei Nakashima/	Date (Optional)	
Name	Kei NAKASHIMA		
Title	Group Manager, Japan Display Inc.		

NOTE: Signature - This form must be signed by the applicant in accordance with 37 CFR 1.33. See 37 CFR 1.4 for signature requirements and certifications. If more than one applicant, use multiple forms.

☐ Total of forms are submitted.

Customized PTO/AIA/80 (07-12)

POWER OF ATTORNEY TO PROSECUTE APPLICATIONS BEFORE THE USPTO

I hereby revoke all previous powers of attorney given in the application identified in the attached statement under 37 CFR 3.73(c).

I hereby **appoint:**

The Practitioner(s) associated with the Customer Number: **38327**

as attorney(s) or agent(s) to represent the undersigned before the United States Patent and Trademark Office (USPTO) in connection with the application identified in the attached statement under 37 CFR 3.73(c).

Please recognize or change the **correspondence address** for the application identified in the attached statement under 37 CFR 3.73(c) to:

The address associated with Customer Number: **38327**

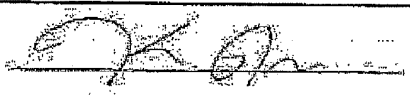
Assignee Name and Address:

Panasonic Liquid Crystal Display Co., Ltd.
1-6 Megahida-cho, Shikama-ku, Himeji-shi,
Hyogo, 672-8033 Japan

A copy of this form, together with a statement under 37 CFR 3.73(c) (Form PTO/SB/96 or equivalent) is required to be filed in each application in which this form is used. The statement under 37 CFR 3.73(c) may be completed by one of the practitioners appointed in this form, and must identify the application in which this Power of Attorney is to be filed.

SIGNATURE of Assignee of Record

The individual whose signature and title is supplied below is authorized to act on behalf of the assignee.

Signature  Date: Nov. 30, 2012

Name Kazuhiko Ishimaru

Title Manager of Intellectual Property Team

STITES & HARBISON PLLC • 1199 North Fairfax St. • Suite 900 • Alexandria, VA 22314
TEL: 703-739-4900 • FAX: 703-739-9577 • CUSTOMER NO. 38327

PTO/AIA/96 (08-12)
Approved for use through 01/31/2013. OMB 0651-0031
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE

STATEMENT UNDER 37 CFR 3.73(c)

Applicant/Patent Owner: Japan Display Inc.

Application No./Patent No.: 15/271,422 Filed/Issue Date: September 21, 2016

Titled: LIQUID CRYSTAL DISPLAY DEVICE, DISPLAY DEVICE AND MANUFACTURING METHOD THEREOF

Japan Display Inc., a corporation

(Name of Assignee) (Type of Assignee, e.g., corporation, partnership, university, government agency, etc.)

states that, for the patent application/patent identified above, it is (choose **one** of options 1, 2, 3 or 4 below):

1. ☐ The assignee of the entire right, title, and interest.

2. ☑ An assignee of less than the entire right, title, and interest (check applicable box):

   ☐ The extent (by percentage) of its ownership interest is 50 %. Additional Statement(s) by the owners holding the balance of the interest must be submitted to account for 100% of the ownership interest.

   ☐ There are unspecified percentages of ownership. The other parties, including inventors, who together own the entire right, title and interest are:

   Additional Statement(s) by the owner(s) holding the balance of the interest must be submitted to account for the entire right, title, and interest.

3. ☐ The assignee of an undivided interest in the entirety (a complete assignment from one of the joint inventors was made). The other parties, including inventors, who together own the entire right, title, and interest are:

   Additional Statement(s) by the owner(s) holding the balance of the interest must be submitted to account for the entire right, title, and interest.

4. ☐ The recipient, via a court proceeding or the like (*e.g.*, bankruptcy, probate), of an undivided interest in the entirety (a complete transfer of ownership interest was made). The certified document(s) showing the transfer is attached.

The interest identified in option 1, 2 or 3 above (not option 4) is evidenced by either (choose **one** of options A or B below):

A. ☐ An assignment from the inventor(s) of the patent application/patent identified above. The assignment was recorded in the United States Patent and Trademark Office at Reel _____, Frame _____, or for which a copy thereof is attached.

B. ☑ A chain of title from the inventor(s), of the patent application/patent identified above, to the current assignee as follows:

1. From: Yoshiaki NAKAYOSHI and Kazuhiko YANAGAWA To: Hitachi, Ltd.

   The document was recorded in the United States Patent and Trademark Office at

   Reel 035604, Frame 0582, or for which a copy thereof is attached.

2. From: Hitachi, Ltd. To: Hitachi Displays, Ltd.

   The document was recorded in the United States Patent and Trademark Office at

   Reel 035604, Frame 0628, or for which a copy thereof is attached.

PTO/AIA/96 (08-12)
Approved for use through 01/31/2013. OMB 0651-0031
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE

STATEMENT UNDER 37 CFR 3.73(c)

3. From: Hitachi Displays, Ltd. To: Hitachi Displays, Ltd. and IPS Alpha Support Co., Ltd.

The document was recorded in the United States Patent and Trademark Office at
Reel 035604, Frame 0765, or for which a copy thereof is attached.

4. From: IPS Alpha Support Co., Ltd. To: Panasonic Liquid Crystal Display Co., Ltd.

The document was recorded in the United States Patent and Trademark Office at
Reel 035605, Frame 0190, or for which a copy thereof is attached.

5. From: Hitachi Displays, Ltd. To: Japan Display East. Inc.

The document was recorded in the United States Patent and Trademark Office at
Reel 035625, Frame 0197, or for which a copy thereof is attached.

6. From: Japan Display East, Inc. To: Japan Display Inc.

The document was recorded in the United States Patent and Trademark Office at
Reel 035625, Frame 0381, or for which a copy thereof is attached.

☐ Additional documents in the chain of title are listed on a supplemental sheet(s).

☐ As required by 37 CFR 3.73(c)(1)(i), the documentary evidence of the chain of title from the original owner to the assignee was, or concurrently is being, submitted for recordation pursuant to 37 CFR 3.11.

[NOTE: A separate copy (i.e., a true copy of the original assignment document(s)) must be submitted to Assignment Division in accordance with 37 CFR Part 3, to record the assignment in the records of the USPTO. See MPEP 302.08]

The undersigned (whose title is supplied below) is authorized to act on behalf of the assignee.

/juan.carlos.a.marquez/	September 21, 2016
Signature	Date
Juan Carlos A. Marquez	34,072
Printed or Typed Name	Title or Registration Number

Privacy Act Statement

The **Privacy Act of 1974 (P.L. 93-579)** requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether disclosure of these records is required by the Freedom of Information Act.
2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.
3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.
4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).
5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.
6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).
7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (*i.e.*, GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.
8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspection or an issued patent.
9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

PTO/AIA/96 (08-12)
Approved for use through 01/31/2013. OMB 0651-0031
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE

STATEMENT UNDER 37 CFR 3.73(c)

Applicant/Patent Owner: Panasonic Liquid Crystal Display Co., Ltd.

Application No./Patent No.: 15/271,422 Filed/Issue Date: September 21, 2016

Titled: LIQUID CRYSTAL DISPLAY DEVICE, DISPLAY DEVICE AND MANUFACTURING METHOD THEREOF

Panasonic Liquid Crystal Display Co., Ltd., a corporation

(Name of Assignee) (Type of Assignee, e.g., corporation, partnership, university, government agency, etc.)

states that, for the patent application/patent identified above, it is (choose **one** of options 1, 2, 3 or 4 below):

1. ☐ The assignee of the entire right, title, and interest.

2. ☑ An assignee of less than the entire right, title, and interest (check applicable box):

   ☐ The extent (by percentage) of its ownership interest is 50 %. Additional Statement(s) by the owners holding the balance of the interest must be submitted to account for 100% of the ownership interest.

   ☐ There are unspecified percentages of ownership. The other parties, including inventors, who together own the entire right, title and interest are:

   Additional Statement(s) by the owner(s) holding the balance of the interest must be submitted to account for the entire right, title, and interest.

3. ☐ The assignee of an undivided interest in the entirety (a complete assignment from one of the joint inventors was made). The other parties, including inventors, who together own the entire right, title, and interest are:

   Additional Statement(s) by the owner(s) holding the balance of the interest must be submitted to account for the entire right, title, and interest.

4. ☐ The recipient, via a court proceeding or the like (*e.g.*, bankruptcy, probate), of an undivided interest in the entirety (a complete transfer of ownership interest was made). The certified document(s) showing the transfer is attached.

The interest identified in option 1, 2 or 3 above (not option 4) is evidenced by either (choose **one** of options A or B below):

A. ☐ An assignment from the inventor(s) of the patent application/patent identified above. The assignment was recorded in the United States Patent and Trademark Office at Reel _____, Frame _____, or for which a copy thereof is attached.

B. ☑ A chain of title from the inventor(s), of the patent application/patent identified above, to the current assignee as follows:

1. From: Yoshiaki NAKAYOSHI and Kazuhiko YANAGAWA To: Hitachi, Ltd.

   The document was recorded in the United States Patent and Trademark Office at
   Reel 035604, Frame 0582, or for which a copy thereof is attached.

2. From: Hitachi, Ltd. To: Hitachi Displays, Ltd.

   The document was recorded in the United States Patent and Trademark Office at
   Reel 035604, Frame 0628, or for which a copy thereof is attached.

STATEMENT UNDER 37 CFR 3.73(c)

3. From: Hitachi Displays, Ltd. To: Hitachi Displays, Ltd. and IPS Alpha Support Co., Ltd.

The document was recorded in the United States Patent and Trademark Office at
Reel 035604, Frame 0765, or for which a copy thereof is attached.

4. From: IPS Alpha Support Co., Ltd. To: Panasonic Liquid Crystal Display Co., Ltd.

The document was recorded in the United States Patent and Trademark Office at
Reel 035605, Frame 0190, or for which a copy thereof is attached.

5. From: Hitachi Displays, Ltd. To: Japan Display East. Inc.

The document was recorded in the United States Patent and Trademark Office at
Reel 035625, Frame 0197, or for which a copy thereof is attached.

6. From: Japan Display East, Inc. To: Japan Display Inc.

The document was recorded in the United States Patent and Trademark Office at
Reel 035625, Frame 0381, or for which a copy thereof is attached.

☐ Additional documents in the chain of title are listed on a supplemental sheet(s).

☐ As required by 37 CFR 3.73(c)(1)(i), the documentary evidence of the chain of title from the original owner to the assignee was, or concurrently is being, submitted for recordation pursuant to 37 CFR 3.11.

[NOTE: A separate copy (i.e., a true copy of the original assignment document(s)) must be submitted to Assignment Division in accordance with 37 CFR Part 3, to record the assignment in the records of the USPTO. See MPEP 302.08]

The undersigned (whose title is supplied below) is authorized to act on behalf of the assignee.

/juan.carlos.a.marquez/	September 21, 2016
Signature	Date
Juan Carlos A. Marquez	34,072
Printed or Typed Name	Title or Registration Number

Privacy Act Statement

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9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

Electronic Acknowledgement Receipt	
EFS ID:	26989288
Application Number:	15271422
International Application Number:	
Confirmation Number:	2686
Title of Invention:	LIQUID CRYSTAL DISPLAY DEVICE, DISPLAY DEVICE AND MANUFACTURING METHOD THEREOF
First Named Inventor/Applicant Name:	Yoshiaki NAKAYOSHI
Customer Number:	38327
Filer:	Juan Carlos A. Marquez/Lily Niu
Filer Authorized By:	Juan Carlos A. Marquez
Attorney Docket Number:	HARU-0126
Receipt Date:	21-SEP-2016
Filing Date:	
Time Stamp:	12:32:52
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	no

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Power of Attorney	HARU-126-POA_transmittal.pdf	161772 151d795ba82388c4bfa21ea8403cf054391d2fd1	no	1

Warnings:

Information:					
2	Power of Attorney	HARU-126-POAs.pdf	288468 2ea44fc819685b1e82b6ea84bff7712e9546acfd	no	2
Warnings:					
The page size in the PDF is too large. The pages should be 8.5 x 11 or A4. If this PDF is submitted, the pages will be resized upon entry into the Image File Wrapper and may affect subsequent processing					
Information:					
3	Assignee showing of ownership per 37 CFR 3.73	HARU-126-Assignee_statement_1.pdf	125205 108ea08153f177694e362917a56e90f5767f8c4d	no	3
Warnings:					
Information:					
4	Assignee showing of ownership per 37 CFR 3.73	HARU-126-Assignee_statement_2.pdf	125288 423f573a51cc7f77ffb4c431cb2b9b29702d95bf	no	3
Warnings:					
Information:					
		Total Files Size (in bytes):	700733		

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111
If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371
If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office
If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re U.S. Patent Application of	)	
	)	
NAKAYOSHI et al.	)	**Confirmation No. 2686**
	)	
Application Number: 15/271,422	)	
	)	
Filed: September 21, 2016	)	
	)	
For: LIQUID CRYSTAL DISPLAY DEVICE, DISPLAY DEVICE AND MANUFACTURING METHOD THEREOF	)	
	)	
Attorney Docket No. HARU-0126	)	

Commissioner of Patents
P.O. Box 1450
Alexandria, VA 22313-1450

INFORMATION DISCLOSURE STATEMENT

Sir:

This application is a Continuation of U.S. Application Serial No. 14/942,120 filed on November 16, 2015 which is a Continuation of U.S. Application Serial No. 14/708,348 filed on May 11, 2015, which is a Continuation of U.S. Application No. 14/285,006 filed on May 22, 2014, which is a continuation of U.S. Application No. 13/927,539 filed on June 26, 2013, which is a Continuation of U.S. Application No. 13/650,203 filed on October 12, 2012, which is a Continuation of U.S. Application No. 13/364,092 filed on February 1, 2012, which is a Continuation of U.S. Application Serial No. 12/926,735 filed December 7, 2010, which is a Continuation of U.S. Application Serial No. 12/292,728 filed November 25, 2008, which is a Divisional of U.S. Application Serial No. 11/976,884 filed October 29, 2007, which is a Divisional of U.S. Application No. 11/409,076 filed April 24, 2006, which is a Divisional of U.S. Application Serial No. 11/211,574 filed August 26, 2005, which is a Divisional of U.S. Application Serial No. 10/237,911 filed September 10, 2002.

Pursuant to 37 C.F.R. §§ 1.56 and 1.97, this Information Disclosure Statement is being submitted in connection with the above-identified patent application. A listing of documents to be published on the face of any patent granted from this application is submitted herewith on the accompanying Form PTO-1449. Any other documents or information submitted for consideration by the Examiner are listed in this paper. A copy of each non-US or foreign patent or non-patent publication or any portion thereof listed or herein identified is submitted herewith.

CERTIFICATION

1. This Information Disclosure Statement is being submitted:

   [X] **(a)** Concurrently with the new Continuation Application, whereby it is believed that no fee is due; OR

   [ ] **(b)** After three months from the filing date of the above-identified U.S. patent application but before the mailing date of the first Office Action on the merits of the above-identified application, whereby it is believed that no fee is due; OR

   [ ] **(c)** After three months from the filing date of the above-identified U.S. patent application and after the mailing date of the first Office Action on the merits of the above-identified application, but prior to the issuance of any Final Action or Notice of Allowance sent in such application, whereby Applicant(s) hereby submit the requisite certification hereinbelow, or authorization for the payment of the requisite fee is set forth hereinbelow; OR

   [ ] **(d)** After the issuance of a Final Action or Notice of Allowance, but before the payment of the Issue Fee, whereby Applicant(s) hereby submit the requisite certification hereinbelow, and authorization for the payment of the requisite fee is set forth hereinbelow.

2. In accordance with the requirements of 37 C.F.R. §1.97, and the above, Applicant(s) hereby certify that:

   [ ] Each item of information contained in this Information Disclosure Statement was first cited in any communication from a foreign patent office in a counterpart foreign application not more than three months prior to the filing of this Information Disclosure Statement; OR

   [ ] No item of information contained in this Information Disclosure Statement was cited in a communication from a foreign patent office in a counterpart foreign application, and, to the knowledge of the person signing the certification after making reasonable inquiry, no

item of information contained in the information disclosure statement was known to any individual designated in §1.56(c) more than three months prior to the filing of this Information Disclosure Statement.

3. Payment of any fees associated with this communication and submission is as follows:

   [ ] Payment for $____ to cover the fee is being submitted via the EFS payment procedure.

   [X] The Commissioner is hereby authorized to charge payment of any fees associated with this communication, including fees under 37 C.F.R. § 1.16 and 1.17, or credit any overpayment to Deposit Account Number 60-0155.

4. The Examiner is requested to acknowledge receipt and consideration of the information provided in this paper in accordance with prescribed procedures. Should there be any outstanding issues requiring discussion that would further the prosecution and allowance of the above-captioned application, the Examiner is invited to contact the undersigned representative at the address and phone number indicated below.

Respectfully submitted,

/juan.carlos.a.marquez/

_____

Juan Carlos A. Marquez
Registration Number 34,072

MARQUEZ IP LAW OFFICE, PLLC
1629 K Street, NW, Suite 300
Washington, DC 20006
Phone: (202) 349-1690
Fax: (202) 754-9829
Customer No. 38327

September 21, 2016

PTO/SB/08a (07-09)
Approved for use through 07/31/2016. OMB 0651-0031
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE

Substitute for form 1449/PTO

INFORMATION DISCLOSURE STATEMENT BY APPLICANT

(Use as many sheets as necessary)

Sheet 1 of 1

Complete if Known	
Application Number	15
Filing Date	2016-09-21
First Named Inventor	NAKAYOSHI
Art Unit	
Examiner Name	
Attorney Docket Number	HARU-0126

U. S. PATENT DOCUMENTS

Examiner Initials*	Cite No.[1]	Document Number Number-Kind Code[2] *(if known)*	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
	1	US- 6,069,678	05-30-2000	Sakamoto et al.	
	2	US- 6,650,389 B1	11-18-2003	Sakamoto	
	3	US- 6,462,800 B1	10-08-2002	Kim et al.	
	4	US- 6,552,770 B2	04-22-2003	Yanagawa et al.	
	5	US- 6,633,360 B2	10-14-2003	Okada et al.	
	6	US- 6,771,342 B1	08-03-2004	Hirakata et al.	
	7	US- 6,985,194	01-10-2006	Kawano, et al.	
	8	US- 2007/0153203	07-05-2007	Kim et al.	
	9	US- 6,621,545	09-16-2003	Park et al.	
	10	US- 5,892,562	04-06-1999	Yamazaki et al.	
	11	US- 2005/0105034	05-19-2005	Ono et al.	
	12	US- 6,259,502	07-10-2001	Komatsu	
	13	US- 5,668,379	09-16-1997	Ono et al.	
	14	US- 5,742,365	04-21-1998	Seo	
	15	US- 6,600,541	07-29-2003	Kurahashi et al.	
	16	US- 5,668,379	09-16-1997	Ono et al.	
	17	US- 6,580,487	06-17-2003	Kim et al.	
	18	US-			
	19	US-			

FOREIGN PATENT DOCUMENTS

Examiner Initials*	Cite No.[1]	Foreign Patent Document Country Code[3]-Number[4]-Kind Code[5] *(if known)*	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages Or Relevant Figures Appear	T[6]
	1					
	2					
	3					
	4					

Examiner Signature		Date Considered	

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant. [1] Applicant's unique citation designation number (optional). [2] See Kinds Codes of USPTO Patent Documents at www.uspto.gov or MPEP 901.04. [3] Enter Office that issued the document, by the two-letter code (WIPO Standard ST.3). [4] For Japanese patent documents, the indication of the year of the reign of the Emperor must precede the serial number of the patent document. [5] Kind of document by the appropriate symbols as indicated on the document under WIPO Standard ST.16 if possible. [6] Applicant is to place a check mark here if English language Translation is attached.

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PTO/SB/08a (07-09)
Approved for use through 07/31/2016. OMB 0651-0031
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Substitute for form 1449/PTO

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Sheet 1 of 1

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First Named Inventor	NAKAYOSHI
Art Unit	
Examiner Name	
Attorney Docket Number	HARU-0126

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Examiner Initials*	Cite No.[1]	Document Number Number-Kind Code[2] *(if known)*	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
	1	US- 6,469,765 B1	10-22-2002	Matsuyama et al.	
	2	US- 6,580,487 B1	06-17-2003	Kim et al.	
	3	US- 6,600,542 B2	07-29-2003	Kim et al.	
	4	US- 6,611,310 B2	08-26-2003	Kurahashi et al.	
	5	US- 6,646,707 B2	11-11-2003	Noh et al.	
	6	US- 6,667,790 B2	12-23-2003	Yanagawa et al.	
	7	US- 6,671,019 B1	12-30-2003	Petschek et al.	
	8	US- 6,721,028 B2	04-13-2004	Kim et al.	
	9	US- 6,784,964 B2	08-31-2004	Nakayoshi et al.	
	10	US- 2002/0041354 A1	04-11-2002	Noh et al.	
	11	US- 2003/0086045 A1	05-08-2003	Ono et al.	
	12	US- 2003/0071952 A1	04-17-2003	Yoshida et al.	
	13	US- 2002/0048500 A1	04-25-2002	Hermann et al.	
	14	US- 6,639,640 B1	10-28-2003	Matsuoka et al.	
	15	US- 6,335,148 B2	01-01-2002	Lee et al.	
	16	US- 6,380,672 B1	04-30-2002	Yudasaka	
	17	US- 5,686,980	11-11-1997	Hirayama et al.	
	18	US- 6,724,444 B2	04-20-2004	Ashizawa et al.	
	19	US- 6,337,726 B1	01-08-2002	Kawano et al.	

FOREIGN PATENT DOCUMENTS

Examiner Initials*	Cite No.[1]	Foreign Patent Document Country Code[3]-Number[4]-Kind Code[5] *(if known)*	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages Or Relevant Figures Appear	T[6]
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	2					
	3					
	4					

Examiner Signature		Date Considered	

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	2	US- 6233034 B1	05-15-2011	Lee et al.	
	3	US- 6456351 B1	09-24-2002	Kim et al.	
	4	US- 6256081 B1	07-03-2001	Lee et al.	
	5	US- 5,745,207	04-28-1998	Asada et al.	
	6	US- 6,266,116 B1	07-24-2001	OHTA et al,	
	7	US- 5,946,066	08-31-1999	Lee et al.	
	8	US- 6,597,413 B2	07-22-2003	Kurashina	
	9	US- 6,661,476 B1	12-09-2003	Abe et al.	
	10	US- 6,587,162 B1	07-01-2003	Kaneko et al.	
	11	US- 6,556,265 B1	04-29-2003	Murade	
	12	US- 6,493,046 B1	12-10-2002	Ueda	
	13	US- 5,060,036	10-22-1991	Choi	
	14	US- 6,356,330 B1	03-12-2002	Ando et al.	
	15	US- 5,185,601	02-09-1993	Takeda et al.	
	16	US- 5,771,082	06-23-1998	Chaudet et al.	
	17	US- 6,285,429 B1	09-04-2001	Nishida et al.	
	18	US- 6,362,858 B1	03-26-2002	Jeon et al.	
	19	US- 6,404,470 B1	06-11-2002	Kim et al.	

FOREIGN PATENT DOCUMENTS

Examiner Initials*	Cite No.[1]	Foreign Patent Document Country Code[3]-Number[4]-Kind Code[5] *(if known)*	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages Or Relevant Figures Appear	T[6]
	1	JP 2001-228493	08-24-2001	Hynix Semiconductor Inc.	Abstract	✔
	2	JP 2000-08408	09-24-1998			✔
	3	JP 3591513	04-19-2001	Seiko Epson Corporation		
	4	CN 1242854A	03-04-1999	Seiko Epson Corporation		

Examiner Signature		Date Considered	

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant. [1] Applicant's unique citation designation number (optional). [2] See Kinds Codes of USPTO Patent Documents at www.uspto.gov or MPEP 901.04. [3] Enter Office that issued the document, by the two-letter code (WIPO Standard ST.3). [4] For Japanese patent documents, the indication of the year of the reign of the Emperor must precede the serial number of the patent document. [5] Kind of document by the appropriate symbols as indicated on the document under WIPO Standard ST.16 if possible. [6] Applicant is to place a check mark here if English language Translation is attached.

Privacy Act Statement

The Privacy Act of 1974 (P.L. 93-579) requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether disclosure of these records is required by the Freedom of Information Act.
2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.
3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.
4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).
5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.
6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).
7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.
8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspection or an issued patent.
9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

PTO/SB/08b (07-09)
Approved for use through 07/31/2012. OMB 0651-0031
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE

Substitute for form 1449/PTO

INFORMATION DISCLOSURE STATEMENT BY APPLICANT

(Use as many sheets as necessary)

Sheet 1 of 1

	Complete if Known
Application Number	15
Filing Date	2016-09-21
First Named Inventor	NAKAYOSHI
Art Unit	
Examiner Name	
Attorney Docket Number	HARU-0126

NON PATENT LITERATURE DOCUMENTS

Examiner Initials*	Cite No.[1]	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T[2]
		JPO Office Action dated April 8, 2018, in Japanese	
		Chinese Office Action dated May 9, 2008 regarding Chinese Patent Application No. 2007100057283, in Chinese	

Examiner Signature		Date Considered	

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

[1] Applicant's unique citation designation number (optional). [2] Applicant is to place a check mark here if English language Translation is attached.

Privacy Act Statement

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The information provided by you in this form will be subject to the following routine uses:

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2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.
3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.
4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).
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9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

Electronic Acknowledgement Receipt	
EFS ID:	26989489
Application Number:	15271422
International Application Number:	
Confirmation Number:	2686
Title of Invention:	LIQUID CRYSTAL DISPLAY DEVICE, DISPLAY DEVICE AND MANUFACTURING METHOD THEREOF
First Named Inventor/Applicant Name:	Yoshiaki NAKAYOSHI
Customer Number:	38327
Filer:	Juan Carlos A. Marquez/Lily Niu
Filer Authorized By:	Juan Carlos A. Marquez
Attorney Docket Number:	HARU-0126
Receipt Date:	21-SEP-2016
Filing Date:	
Time Stamp:	12:43:47
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	no

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Transmittal Letter	HARU-126-IDS_transmittal.pdf	145540 1bfaa5643932dc229263f3845efa31ec8c1c2541	no	1

Warnings:

Information:					
2	Information Disclosure Statement (IDS) Form (SB08)	HARU-126-IDS_statement.pdf	132665 a2df2861efbc6e18450692e11007ad9fe1411e2d	no	3
Warnings:					
Information:					
This is not an USPTO supplied IDS fillable form					
3	Information Disclosure Statement (IDS) Form (SB08)	HARU-126-Form_SB08a1.pdf	260534 bb4ebd165575baa89832d36ad95a659ed0ef045b	no	2
Warnings:					
Information:					
This is not an USPTO supplied IDS fillable form					
4	Information Disclosure Statement (IDS) Form (SB08)	HARU-126-Form_SB08a2.pdf	259668 8185ab4f5f05023b951e198bc31cc53799ed196c	no	2
Warnings:					
Information:					
This is not an USPTO supplied IDS fillable form					
5	Information Disclosure Statement (IDS) Form (SB08)	HARU-126-Form_SB08a3.pdf	257361 ac26b3a8289a063e9635071c5947866f2d5dedb1	no	2
Warnings:					
Information:					
This is not an USPTO supplied IDS fillable form					
6	Information Disclosure Statement (IDS) Form (SB08)	HARU-126-Form_sb08b_new_form.pdf	320466 1a15232f4c86ab16038972d8073cedd6cd13a4d1	no	2
Warnings:					
Information:					
This is not an USPTO supplied IDS fillable form					
		Total Files Size (in bytes):	1376234		

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111
If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371
If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office
If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re U.S. Patent Application of	)	
	)	
NAKAYOSHI et al.	)	**Confirmation No. 2686**
	)	
Application Number: 15/271,422	)	
	)	
Filed: September 21, 2016	)	
	)	
For: LIQUID CRYSTAL DISPLAY DEVICE, DISPLAY DEVICE AND MANUFACTURING METHOD THEREOF	)	
	)	
Attorney Docket No. HARU-0126	)	

Commissioner of Patents
P.O. Box 1450
Alexandria, VA 22313-1450

LETTER

Sir:

The below-identified communications are submitted in the above-captioned application or proceeding:

(X) Information Disclosure Statement with PTO Form SB/08a (3 pages), SB/08b
( ) $_____ deposit account charge via EFS payment system

☒ The Commissioner is hereby authorized to charge payment of any fees associated with this Communication including fees under 37 C.F.R. § 1.16 and 1.17 or credit any overpayment to **Deposit Account Number 60-0155.**

Respectfully submitted,

/juan.carlos.a.marquez/

Juan Carlos A. Marquez
Registration Number 34,072

Marquez IP Law Office, PLLC
1629 K Street, NW, Suite 300
Washington, DC 20006
Tel. No. 202-349-1690
Fax No. 202-754-9829
Customer No. 38327

September 21, 2016

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NUMBER	FILING or 371(c) DATE	GRP ART UNIT	FIL FEE REC'D	ATTY.DOCKET.NO	TOT CLAIMS	IND CLAIMS
15/271,422	09/21/2016	2871	1600	HARU-0126	13	1

CONFIRMATION NO. 2686

FILING RECEIPT

38327
Juan Carlos A. Marquez
Marquez Intellectual Property Law Office PLLC
1629 K Street, NW
Suite 300
Washington, DC 20006

OC000000086194353

Date Mailed: 10/04/2016

Receipt is acknowledged of this non-provisional patent application. The application will be taken up for examination in due course. Applicant will be notified as to the results of the examination. Any correspondence concerning the application must include the following identification information: the U.S. APPLICATION NUMBER, FILING DATE, NAME OF APPLICANT, and TITLE OF INVENTION. Fees transmitted by check or draft are subject to collection. Please verify the accuracy of the data presented on this receipt. **If an error is noted on this Filing Receipt, please submit a written request for a Filing Receipt Correction. Please provide a copy of this Filing Receipt with the changes noted thereon. If you received a "Notice to File Missing Parts" for this application, please submit any corrections to this Filing Receipt with your reply to the Notice. When the USPTO processes the reply to the Notice, the USPTO will generate another Filing Receipt incorporating the requested corrections**

Inventor(s)

Yoshiaki NAKAYOSHI, Ooamishirasato, JAPAN;
Kazuhiko YANAGAWA, Mobara, JAPAN;

Applicant(s)

Japan Display Inc., Tokyo, JAPAN;
Panasonic Liquid Crystal Display Co., Ltd., Hyogo-ken, JAPAN;

Power of Attorney: The patent practitioners associated with Customer Number 38327

Domestic Priority data as claimed by applicant

This application is a CON of 14/942,120 11/16/2015
which is a CON of 14/708,348 05/11/2015 PAT 9213204
which is a CON of 14/285,006 05/22/2014 PAT 9086600
which is a CON of 13/927,539 06/26/2013 PAT 8760609
which is a CON of 13/650,203 10/12/2012 PAT 8493522
which is a CON of 13/364,092 02/01/2012 PAT 8310641
which is a CON of 12/926,735 12/07/2010 PAT 8248549
which is a CON of 12/292,728 11/25/2008 PAT 7872696
which is a DIV of 11/976,884 10/29/2007 PAT 7605876
which is a DIV of 11/409,076 04/24/2006 PAT 7307673
which is a DIV of 11/211,574 08/26/2005 PAT 7423701
which is a DIV of 10/237,911 09/10/2002 PAT 6970222

Foreign Applications (You may be eligible to benefit from the **Patent Prosecution Highway** program at the USPTO. Please see http://www.uspto.gov for more information.)
JAPAN 2001-317149 10/15/2001

Permission to Access Application via Priority Document Exchange: Yes

Permission to Access Search Results: Yes

Applicant may provide or rescind an authorization for access using Form PTO/SB/39 or Form PTO/SB/69 as appropriate.

Request to Retrieve - This application either claims priority to one or more applications filed in an intellectual property Office that participates in the Priority Document Exchange (PDX) program or contains a proper **Request to Retrieve Electronic Priority Application(s)** (PTO/SB/38 or its equivalent). Consequently, the USPTO will attempt to electronically retrieve these priority documents.

If Required, Foreign Filing License Granted: 09/30/2016

The country code and number of your priority application, to be used for filing abroad under the Paris Convention, is **US 15/271,422**

Projected Publication Date: 01/12/2017

Non-Publication Request: No

Early Publication Request: No

Title

LIQUID CRYSTAL DISPLAY DEVICE, DISPLAY DEVICE AND MANUFACTURING METHOD THEREOF

Preliminary Class

349

Statement under 37 CFR 1.55 or 1.78 for AIA (First Inventor to File) Transition Applications: No

PROTECTING YOUR INVENTION OUTSIDE THE UNITED STATES

Since the rights granted by a U.S. patent extend only throughout the territory of the United States and have no effect in a foreign country, an inventor who wishes patent protection in another country must apply for a patent in a specific country or in regional patent offices. Applicants may wish to consider the filing of an international application under the Patent Cooperation Treaty (PCT). An international (PCT) application generally has the same effect as a regular national patent application in each PCT-member country. The PCT process **simplifies** the filing of patent applications on the same invention in member countries, but **does not result** in a grant of "an international patent" and does not eliminate the need of applicants to file additional documents and fees in countries where patent protection is desired.

Almost every country has its own patent law, and a person desiring a patent in a particular country must make an application for patent in that country in accordance with its particular laws. Since the laws of many countries differ in various respects from the patent law of the United States, applicants are advised to seek guidance from specific foreign countries to ensure that patent rights are not lost prematurely.

Applicants also are advised that in the case of inventions made in the United States, the Director of the USPTO must issue a license before applicants can apply for a patent in a foreign country. The filing of a U.S. patent application serves as a request for a foreign filing license. The application's filing receipt contains further information and guidance as to the status of applicant's license for foreign filing.

Applicants may wish to consult the USPTO booklet, "General Information Concerning Patents" (specifically, the section entitled "Treaties and Foreign Patents") for more information on timeframes and deadlines for filing foreign patent applications. The guide is available either by contacting the USPTO Contact Center at 800-786-9199, or it can be viewed on the USPTO website at http://www.uspto.gov/web/offices/pac/doc/general/index.html.

For information on preventing theft of your intellectual property (patents, trademarks and copyrights), you may wish to consult the U.S. Government website, http://www.stopfakes.gov. Part of a Department of Commerce initiative, this website includes self-help "toolkits" giving innovators guidance on how to protect intellectual property in specific countries such as China, Korea and Mexico. For questions regarding patent enforcement issues, applicants may call the U.S. Government hotline at 1-866-999-HALT (1-866-999-4258).

LICENSE FOR FOREIGN FILING UNDER

Title 35, United States Code, Section 184

Title 37, Code of Federal Regulations, 5.11 & 5.15

GRANTED

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This license is to be retained by the licensee and may be used at any time on or after the effective date thereof unless it is revoked. This license is automatically transferred to any related applications(s) filed under 37 CFR 1.53(d). This license is not retroactive.

The grant of a license does not in any way lessen the responsibility of a licensee for the security of the subject matter as imposed by any Government contract or the provisions of existing laws relating to espionage and the national security or the export of technical data. Licensees should apprise themselves of current regulations especially with respect to certain countries, of other agencies, particularly the Office of Defense Trade Controls, Department of State (with respect to Arms, Munitions and Implements of War (22 CFR 121-128)); the Bureau of Industry and Security, Department of Commerce (15 CFR parts 730-774); the Office of Foreign AssetsControl, Department of Treasury (31 CFR Parts 500+) and the Department of Energy.

NOT GRANTED

No license under 35 U.S.C. 184 has been granted at this time, if the phrase "IF REQUIRED, FOREIGN FILING LICENSE GRANTED" DOES NOT appear on this form. Applicant may still petition for a license under 37 CFR 5.12, if a license is desired before the expiration of 6 months from the filing date of the application. If 6 months has lapsed from the filing date of this application and the licensee has not received any indication of a secrecy order under 35 U.S.C. 181, the licensee may foreign file the application pursuant to 37 CFR 5.15(b).

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The United States represents the largest, most dynamic marketplace in the world and is an unparalleled location for business investment, innovation, and commercialization of new technologies. The U.S. offers tremendous resources and advantages for those who invest and manufacture goods here. Through SelectUSA, our nation works to promote and facilitate business investment. SelectUSA provides information assistance to the international investor community; serves as an ombudsman for existing and potential investors; advocates on behalf of U.S. cities, states, and regions competing for global investment; and counsels U.S. economic development organizations on investment attraction best practices. To learn more about why the United States is the best country in the world to develop technology, manufacture products, deliver services, and grow your business, visit http://www.SelectUSA.gov or call +1-202-482-6800.

PATENT APPLICATION FEE DETERMINATION RECORD

Substitute for Form PTO-875

Application or Docket Number: 15/271,422

APPLICATION AS FILED - PART I

FOR	(Column 1) NUMBER FILED	(Column 2) NUMBER EXTRA	SMALL ENTITY RATE($)	SMALL ENTITY FEE($)	OR	OTHER THAN SMALL ENTITY RATE($)	OTHER THAN SMALL ENTITY FEE($)
BASIC FEE (37 CFR 1.16(a), (b), or (c))	N/A	N/A	N/A			N/A	280
SEARCH FEE (37 CFR 1.16(k), (i), or (m))	N/A	N/A	N/A			N/A	600
EXAMINATION FEE (37 CFR 1.16(o), (p), or (q))	N/A	N/A	N/A			N/A	720
TOTAL CLAIMS (37 CFR 1.16(i))	13 minus 20 =	*			OR	x 80 =	0.00
INDEPENDENT CLAIMS (37 CFR 1.16(h))	1 minus 3 =	*				x 420 =	0.00
APPLICATION SIZE FEE (37 CFR 1.16(s))	If the specification and drawings exceed 100 sheets of paper, the application size fee due is $310 ($155 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).						0.00
MULTIPLE DEPENDENT CLAIM PRESENT (37 CFR 1.16(j))							0.00
* If the difference in column 1 is less than zero, enter "0" in column 2.			TOTAL			TOTAL	1600

APPLICATION AS AMENDED - PART II

		(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA	SMALL ENTITY RATE($)	SMALL ENTITY ADDITIONAL FEE($)	OR	OTHER THAN SMALL ENTITY RATE($)	OTHER THAN SMALL ENTITY ADDITIONAL FEE($)
AMENDMENT A	Total (37 CFR 1.16(i))	*	Minus	**	=	x =		OR	x =	
	Independent (37 CFR 1.16(h))	*	Minus	***	=	x =		OR	x =	
	Application Size Fee (37 CFR 1.16(s))									
	FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))							OR		
						TOTAL ADD'L FEE		OR	TOTAL ADD'L FEE	

		(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA	SMALL ENTITY RATE($)	SMALL ENTITY ADDITIONAL FEE($)	OR	OTHER THAN SMALL ENTITY RATE($)	OTHER THAN SMALL ENTITY ADDITIONAL FEE($)
AMENDMENT B	Total (37 CFR 1.16(i))	*	Minus	**	=	x =		OR	x =	
	Independent (37 CFR 1.16(h))	*	Minus	***	=	x =		OR	x =	
	Application Size Fee (37 CFR 1.16(s))									
	FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))							OR		
						TOTAL ADD'L FEE		OR	TOTAL ADD'L FEE	

* If the entry in column 1 is less than the entry in column 2, write "0" in column 3.
** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20".
*** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3".
The "Highest Number Previously Paid For" (Total or Independent) is the highest found in the appropriate box in column 1.

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re U.S. Patent Application of	)	**Confirmation No. 2686**
	)	
NAKAYOSHI et al.	)	
	)	
Application Number: 15/271,422	)	
	)	
Filed: September 21, 2016	)	
	)	
For: LIQUID CRYSTAL DISPLAY DEVICE, DISPLAY DEVICE AND MANUFACTURING METHOD THEREOF	)	
	)	
Attorney Docket No. HARU-0126	)	

Commissioner of Patents
P.O. Box 1450
Alexandria, VA 22313-1450

PRELIMINARY AMENDMENT

Sir:

Prior to an examination on the merits, please amend the above-identified application as follows:

IN THE CLAIMS:

Claims 1-3 and 14-30 stand for consideration in this application, wherein claims 1-3 are being amended to more particularly point out and distinctly claim the subject invention; claims 4-13 are being canceled without prejudice or disclaimer; and new claims 14-30 are being submitted for consideration, all as follows:

1. (Currently Amended) A liquid crystal display device, comprising:

a first substrate;

a second substrate;

a liquid crystal layer between the first substrate and the second substrate, containing liquid crystal molecules;

a gate line and a drain line;

a pixel electrode and a counter electrode disposed between the first substrate and the liquid crystal layer;

a gate insulation layer formed on the gate line;

an organic insulation layer disposed between the first substrate and the liquid crystal layer;

~~a switching element, connected to the gate line, including a first electrode connected to the drain line and a second electrode connected to the pixel electrode;~~

wherein the liquid crystal layer is driven by an electric field generated between the pixel electrode and the counter electrode, and

wherein the pixel electrode is formed between the liquid crystal layer and the organic insulation layer, and wherein the counter electrode is a planar shape, and the pixel electrode comprises a slit having a first portion, and the first portion is not parallel with the gate line and the drain line.

2. (Currently Amended) A liquid crystal display device ~~according to claim 1, wherein the counter electrode is connected to a common layer and, wherein the organic insulation layer is formed between the counter electrode and the first substrate~~, comprising:

a first substrate;

a second substrate;

a liquid crystal layer between the first substrate and the second substrate, containing liquid crystal molecules;

a gate line and a drain line;

a pixel electrode and a counter electrode disposed between the first substrate and the liquid crystal layer;

a gate insulation layer formed on the gate line;

an organic insulation layer disposed between the first substrate and the liquid crystal layer;

wherein the liquid crystal layer is driven by an electric field generated between the pixel electrode and the counter electrode, and

wherein the pixel electrode is formed between the liquid crystal layer and the organic insulation layer, and wherein the counter electrode is a planar shape, and the pixel electrode comprises a slit having a first portion, and the first portion is not parallel with the gate line.

3. A liquid crystal display device ~~according to claim 2, wherein the counter electrode is connected to the common layer via a through hole within the organic insulation layer~~, comprising:

a first substrate;

a second substrate;

a liquid crystal layer between the first substrate and the second substrate, containing liquid crystal molecules;

a gate line and a drain line;

a pixel electrode and a counter electrode disposed between the first substrate and the liquid crystal layer;

a gate insulation layer formed on the gate line;

an organic insulation layer disposed between the first substrate and the liquid crystal layer;

wherein the liquid crystal layer is driven by an electric field generated between the pixel electrode and the counter electrode, and

wherein the pixel electrode is formed between the liquid crystal layer and the organic insulation layer, and wherein the counter electrode is a planar shape, and the pixel electrode comprises a slit having a first portion, and the first portion is not parallel with the drain line.

4-13. (Canceled).

14. (New) A liquid crystal display device according to claim 2, wherein the pixel electrode comprises a slit having a first portion, and the first portion is not parallel with the gate line and the drain line at least in a pixel.

15. (New) A liquid crystal display device according to claim 3, wherein the pixel electrode comprises a slit having a first portion, and the first portion is not parallel with the gate line and the drain line at least in a pixel.

16. (New) A liquid crystal display device according to claim 1, wherein the counter electrode is connected to a common layer and, wherein the organic insulation layer is formed between the counter electrode and the first substrate.

17. (New) A liquid crystal display device according to claim 16, wherein the counter electrode is connected to the common layer via a through hole within the organic insulation layer.

18. (New) A liquid crystal display device according to claim 17, wherein the common layer is a planer shape, and faces plural of the pixel electrode.

19. (New) A liquid crystal display device according to claim 1, wherein a passivation layer is formed between the liquid crystal layer and the pixel electrode contacting a second electrode, and wherein the passivation layer is formed between the liquid crystal layer and the drain line.

20. (New) A liquid crystal display device according to claim 2, wherein a passivation layer is formed between the liquid crystal layer and the pixel electrode contacting a second electrode, and wherein the passivation layer is formed between the liquid crystal layer and the drain line.

21. (New) A liquid crystal display device according to claim 3, wherein a passivation layer is formed between the liquid crystal layer and the pixel electrode contacting a second electrode, and wherein the passivation layer is formed between the liquid crystal layer and the drain line.

22. (New) A liquid crystal display device according to claim 1, wherein the counter electrode is a planer shape, and the pixel electrode comprises a slit having the first portion and a second portion, and both of the first portion and the second portion are not parallel with the gate line and the drain line.

23. (New) A liquid crystal display device according to claim 1, wherein the counter electrode is a planer shape, and the pixel electrode comprises a slit having the first portion and a second portion, and both of the first portion and the second portion are not parallel with the gate line.

24. (New) A liquid crystal display device according to claim 1, wherein the counter electrode is a planer shape, and the pixel electrode comprises a slit having the first portion and a second portion, and both of the first portion and the second portion are not parallel with the drain line.

25. (New) A liquid crystal display device according to claim 1, wherein the gate insulation layer is formed between the counter electrode and the drain line.

26. (New) A liquid crystal display device according to claim 1, wherein the counter electrode connects to a connection line.

27. (New) A liquid crystal display device according to claim 26, wherein the connection line is arranged parallel to the extension direction of the gate line.

28. (New) A liquid crystal display device according to claim 27, wherein the organic insulation layer is formed between the connection line and the first substrate.

29. (New) A liquid crystal display device according to claim 26, wherein the connection line is directly contacted to the counter electrode.

30. (New) A liquid crystal display device according to claim 29, wherein the common electrode is disposed between the connection line and the liquid crystal layer.

REMARKS

Prior to examination on the merits, the Examiner is respectfully requested to consider the above-outlined amendments, to proceed with examination of the application on the merits, and to indicate the allowability of the claim.

Status of the Claims

Claims 1-3 and 14-30 stand for consideration in this application, wherein claims 1-3 are being amended to more particularly point out and distinctly claim the subject invention; claims 4-13 are being canceled without prejudice or disclaimer; and new claims 14-30 are being submitted for consideration. Applicants submit that there is no new matter being added as a result of this Preliminary Amendment.

Support for the new claims submitted herewith may be found throughout the disclosure of the invention as filed.

Conclusion

In view of the above amendments and Applicants' comments stated herein, Applicants respectfully request an early and favorable action on the merits.

Respectfully submitted,

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November 11, 2016

Electronic Acknowledgement Receipt	
EFS ID:	27488259
Application Number:	15271422
International Application Number:	
Confirmation Number:	2686
Title of Invention:	LIQUID CRYSTAL DISPLAY DEVICE, DISPLAY DEVICE AND MANUFACTURING METHOD THEREOF
First Named Inventor/Applicant Name:	Yoshiaki NAKAYOSHI
Customer Number:	38327
Filer:	Juan Carlos A. Marquez
Filer Authorized By:	
Attorney Docket Number:	HARU-0126
Receipt Date:	11-NOV-2016
Filing Date:	21-SEP-2016
Time Stamp:	15:43:19
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	no

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Transmittal Letter	HARU-126-Claim_calculation_sheet_preliminary_amendment.pdf	93031 7e10f1b9693781e35090daf1ee8b9737b6aae7a8	no	2

Warnings:

Information:					
2	Preliminary Amendment	HARU-126_Preliminary_Amendment.pdf	104704 1b5d919967f0918ca6d8e08691deb36b3c984b53	no	7
Warnings:					
Information:					
			Total Files Size (in bytes):	197735	

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111
If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371
If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office
If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re U.S. Patent Application of	)	**Confirmation No. 2686**
	)	
NAKAYOSHI et al.	)	
	)	
Application Number: 15/271,422	)	
	)	
Filed: September 21, 2016	)	
	)	
For: LIQUID CRYSTAL DISPLAY DEVICE, DISPLAY DEVICE AND MANUFACTURING METHOD THEREOF	)	
	)	
Attorney Docket No. HARU-0126	)	

Mail Stop Amendment
Commissioner of Patents
P.O. Box 1450
Alexandria, VA 22313-1450

COVER LETTER

Sir:

[X] The fee for submission of claims is calculated as shown below:

FOR	TOTAL WITH NEW CLAIMS ADDED	TOTAL CURRENTLY ON FILE	CLAIMS ALREADY PAID	RATE	CALCULATION
Total Claims	20	13	(Over 20)	x $80	0
Independent Claims	3	1	(Over 3)	x $420	0
MULTIPLE DEPENDENT CLAIM(S)				+ 7860	0
REDUCTION FOR FILING BY SMALL ENTITY (note 37 C.F.R. §§ 1.9, 1.27, 1.28).				x ½	
			TOTAL		$0

In addition, the below-identified communications are submitted in the above-captioned application or proceeding:

[x] Preliminary Amendment (with claim amendments)
[ ] Substitute Abstract
[ ] Terminal Disclaimer
[ ] Information Disclosure Statement
[ ] __ sheet of replacement drawings
[ ] RCE
[ ] Other:

[ ] Applicant(s) hereby request and petition that the time for taking action in this case be extended pursuant to 37 C.F.R. § 1.136(a) for:
[ ] **one (1) month** [ ] **two (2) months** [ ] **three (3) months**

The fee set in 37 C.F.R. § 1.17 for the extension of time is **$**_____ for a large/small entity.

[ ] Payment of **$**_____ is made by credit card via the EFS payment system.

[x] The Commissioner is hereby authorized to charge any additional fees associated with this communication, including fees under 37 C.F.R. § 1.16 and 1.17, or credit any overpayment to **Deposit Account Number 60-0155**.

Respectfully submitted,

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November 11, 2016

PTO/SB/06 (09-11)
Approved for use through 1/31/2014. OMB 0651-0032
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE

PATENT APPLICATION FEE DETERMINATION RECORD Substitute for Form PTO-875	Application or Docket Number 15/271,422	Filing Date 09/21/2016	☐ To be Mailed

ENTITY: ☒ LARGE ☐ SMALL ☐ MICRO

APPLICATION AS FILED – PART I

	(Column 1)	(Column 2)		
FOR	NUMBER FILED	NUMBER EXTRA	RATE ($)	FEE ($)
☐ BASIC FEE (37 CFR 1.16(a), (b), or (c))	N/A	N/A	N/A	
☐ SEARCH FEE (37 CFR 1.16(k), (i), or (m))	N/A	N/A	N/A	
☐ EXAMINATION FEE (37 CFR 1.16(o), (p), or (q))	N/A	N/A	N/A	
TOTAL CLAIMS (37 CFR 1.16(i))	minus 20 =	*	X $ =	
INDEPENDENT CLAIMS (37 CFR 1.16(h))	minus 3 =	*	X $ =	
☐ APPLICATION SIZE FEE (37 CFR 1.16(s))	If the specification and drawings exceed 100 sheets of paper, the application size fee due is $310 ($155 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).			
☐ MULTIPLE DEPENDENT CLAIM PRESENT (37 CFR 1.16(j))				
* If the difference in column 1 is less than zero, enter "0" in column 2.			TOTAL	

APPLICATION AS AMENDED – PART II

		(Column 1)		(Column 2)	(Column 3)		
	11/11/2016	CLAIMS REMAINING AFTER AMENDMENT		HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA	RATE ($)	ADDITIONAL FEE ($)
AMENDMENT	Total (37 CFR 1.16(i))	* 19	Minus	** 20	= 0	X $80 =	0
	Independent (37 CFR 1.16(h))	* 1	Minus	***3	= 0	X $420 =	0
	☐ Application Size Fee (37 CFR 1.16(s))						
	☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))						
						TOTAL ADD'L FEE	0

		(Column 1)		(Column 2)	(Column 3)		
		CLAIMS REMAINING AFTER AMENDMENT		HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA	RATE ($)	ADDITIONAL FEE ($)
AMENDMENT	Total (37 CFR 1.16(i))	*	Minus	**	=	X $ =	
	Independent (37 CFR 1.16(h))	*	Minus	***	=	X $ =	
	☐ Application Size Fee (37 CFR 1.16(s))						
	☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))						
						TOTAL ADD'L FEE	

* If the entry in column 1 is less than the entry in column 2, write "0" in column 3.
** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20".
*** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3".
The "Highest Number Previously Paid For" (Total or Independent) is the highest number found in the appropriate box in column 1.

LIE
/LAMONT MCLAUCHLIN/

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NUMBER	FILING OR 371(C) DATE	FIRST NAMED APPLICANT	ATTY. DOCKET NO./TITLE
15/271,422	09/21/2016	Yoshiaki NAKAYOSHI	HARU-0126

CONFIRMATION NO. 2686

38327
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PUBLICATION NOTICE

OC00000088464743

Title:LIQUID CRYSTAL DISPLAY DEVICE, DISPLAY DEVICE AND MANUFACTURING METHOD THEREOF

Publication No.US-2017-0010509-A1
Publication Date:01/12/2017

NOTICE OF PUBLICATION OF APPLICATION

The above-identified application will be electronically published as a patent application publication pursuant to 37 CFR 1.211, et seq. The patent application publication number and publication date are set forth above.

The publication may be accessed through the USPTO's publically available Searchable Databases via the Internet at www.uspto.gov. The direct link to access the publication is currently http://www.uspto.gov/patft/.

The publication process established by the Office does not provide for mailing a copy of the publication to applicant. A copy of the publication may be obtained from the Office upon payment of the appropriate fee set forth in 37 CFR 1.19(a)(1). Orders for copies of patent application publications are handled by the USPTO's Office of Public Records. The Office of Public Records can be reached by telephone at (571) 272-3150 or (800) 972-6382, by facsimile at (571) 273-3250, by mail addressed to the United States Patent and Trademark Office, Office of Public Records, Alexandria, VA 22313-1450 or via the Internet.

In addition, information on the status of the application, including the mailing date of Office actions and the dates of receipt of correspondence filed in the Office, may also be accessed via the Internet through the Patent Electronic Business Center at www.uspto.gov using the public side of the Patent Application Information and Retrieval (PAIR) system. The direct link to access this status information is currently http://pair.uspto.gov/. Prior to publication, such status information is confidential and may only be obtained by applicant using the private side of PAIR.

Further assistance in electronically accessing the publication, or about PAIR, is available by calling the Patent Electronic Business Center at 1-866-217-9197.

Office of Data Managment, Application Assistance Unit (571) 272-4000, or (571) 272-4200, or 1-888-786-0101

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JAPAN PATENT OFFICE

別紙添付の書類に記載されている事項は下記の出願書類に記載されている事項と同一であることを証明する。
This is to certify that the annexed is a true copy of the following application as filed with this Office.

出願年月日 Date of Application:	２００１年１０月１５日
出願番号 Application Number:	特願２００１－３１７１４９
パリ条約による外国への出願に用いる優先権の主張の基礎となる出願の国コードと出願番号 The country code and number of your priority application, to be used for filing abroad under the Paris Convention, is	ＪＰ２００１－３１７１４９
出願人 Applicant(s):	株式会社ＰＦＵ

２０１７年　２月１４日

特許庁長官
Commissioner,
Japan Patent Office　小宮義則

【書類名】　特許願
【整理番号】　01P00040
【提出日】　平成13年10月15日
【あて先】　特許庁長官殿
【国際特許分類】　H04N　7/15
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　【予納台帳番号】　036397
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【提出物件の目録】
　【物件名】　明細書　1
　【物件名】　図面　1
　【物件名】　要約書　1
【プルーフの要否】　要

【書類名】　　明細書

【発明の名称】　　会議システムおよびその方法

【特許請求の範囲】

【請求項１】

ネットワークを介して実施する会議システムであって、他地点へ伝送した会議参加者が映された画像静止データをもとに、映された各参加者の画像位置付け処理を行なう画像処理手段と、その位置付け情報を各発言者が発言時に同時に入力装置にて他地点側会議システムに伝送する伝送手段と、他地点システム側では伝送された位置付け識別データ情報をもとに、表示装置に映し出されている他地点側の会議参加者が映された画像静止データの該当画像領域部分を変化させることで、容易に発言者の識別を行う画像処理手段を備えたことを特徴とした会議システム。

【請求項２】

発言者を特定するのに、予め登録しておいた声紋データベースと声紋認識手段を用いて、その情報をもとに他地点側の発言者の特定を行い、表示装置に映し出されている該当の画像領域部分を変化させることで、容易に発言者の識別を可能とすることを特徴とした会議方法。

【請求項３】

表示装置に映し出されている該当の画像領域部分を変化させる画像処理手段と連動して、予め登録しておいたデータベースからその発言者の情報も表示されることを特徴とした請求項１記載の会議システム。

【請求項４】

発言内容と合わせて、発言者名をも認識し、記録する手段を設け、議事録生成を行うことを特徴とした請求項１記載の会議システム。

【発明の詳細な説明】

【０００１】

【発明の属する技術分野】

本発明は、会議システム装置に関し、特に静止画映像によるＴＶ会議システムあるいは電話会議システム等に用いられ、静止画映像に変化を加えること等で、

動画を随時送受信するＴＶ会議システムと同等の使い勝手を実現し、かつ従来にない付帯の機能を実現する手段を備えた会議システムに関する。

【０００２】

【従来の技術】

従来、静止画映像をもとにした会議システムとしては、参加者が発言しても静止画映像はなんら変化をせず、音声だけで会議を進行していた。

【０００３】

【発明が解決しようとする課題】

しかしながら、上述のような会議システムにあたっては、発言者の特定が出来難いといった問題点があった。一方、随時の動画を伴ったＴＶ会議システムでは、上述の課題は解決される可能性もあるが、システムの価格が高価になることや回線のトラヒックも増大してしまう等の性能面での問題がある。また、静止画や動画のシステムとも、発言している人の名前や所属といった人事等の情報がわからないといった問題点もあった。

【０００４】

本発明は上記の問題を解決するために成されたものであって、その目的とするところは、システム構成が簡易であって、回線上のデータ量を動画を用いたＴＶ会議システムと比較して、データ量あるいは通信コスト等を各段に抑えながら、同等の使い勝手を実現し、かつ従来にない付帯の機能を備えた会議システムを提供することにある。

【０００５】

【課題を解決するための手段】

本発明は上記の問題点を解決するために、請求項１記載の発明にあっては、ネットワークを介して実施する会議システムであって、他地点へ伝送した会議参加者が映された画像静止データをもとに、映された各参加者の画像位置付け処理を行なう画像処理手段と、その位置付け情報を各発言者が発言時に同時に入力装置にて他地点側会議システムに伝送する伝送手段と、他地点システム側では伝送された位置付け識別データ情報をもとに表示装置に映し出されている他地点側の会議参加者が映された画像静止データの該当画像領域部分を変化させることで、容

易に発言者の識別を行う画像処理手段を備えたことを特徴とするものである。

【０００６】

請求項２記載の発明にあっては、表示装置に映し出されている該当の画像領域部分を変化させる機能と連動して、予め登録しておいたデータベースからその発言者の人事情報等も表示されることを特徴とするものである。

【０００７】

請求項３記載の発明にあっては、表示装置に映し出されている該当の画像領域部分を変化させる機能と連動して、予め登録しておいたデータベースからその発言者の人事情報等も表示されることを特徴とするものである。

【０００８】

請求項４記載の発明にあっては、発言内容と合わせて、発言者名をも認識し、記録することを可能とした議事録を自動で生成を行うことを特徴とするものである。

【０００９】

【発明の実施の形態】

本発明の実施の形態を図１～図３を用いて説明する。図１は、会議システムの構成を示す構成図である。図２は、表示装置に表示される例を示している。図３は、表示装置に表示される例を示している。

【００１０】

図１は本発明の構成図である。

【００１１】

図１において、１００は会議システムであり、１０１は会議参加者を会議に先立って撮影するカメラ、１０２は撮影した静止画を符号化して送信する静止画像符号化部、２０３は受信した静止画を復号化する静止画像復号化部、２０４は表示装置、２１０は静止画像に映っている人の領域を番号等で割り当てる画像解析部、２０９はそれら画像情報を格納するための記録装置、２１３は２１０での解析結果を符号化して送信するための画像解析結果送信部、１１５は２１３から送信された画像解析結果を復号化して受信する画像解析結果受信部である。

【００１２】

これと同様に、今度は他の会議システム側から会議参加者情報を送信することで、事前の準備を行う。手順及び図の説明は、以下の通りである。

【００１３】

図１において、２００は会議システムであり、２０１は会議参加者を会議に先立って撮影するカメラ、２０２は撮影した静止画を符号化して送信する静止画像符号化部、１０３は受信した静止画を復号化する静止画像復号化部、１０４は表示装置、１１０は静止画像に映っている人の領域を番号等で割り当てる画像解析部、１０９はそれら画像情報を格納するための記録装置、１１３は１１０での解析結果を符号化して送信するための画像解析結果送信部、２１５は１１３から送信された画像解析結果を復号化して受信する画像解析結果受信部である。

【００１４】

画像解析結果受信部１１５、２１５で得られた情報、例えば、Ａさんの識別番号は１番でＢさんの識別番号は２番といった情報に基づいて、実際に会議においてはその割り当てられた番号等をその発言する人が発言に先立ち、１１１や２１１の入力装置で入力することで、１１２や２１２の入力データ処理部で符号化して送信する。

【００１５】

１１２や２１２から送信されたデータは、それぞれ２１４、１１４で復号化し、その情報を２０８、１０８の表示画像変更処理部で該当の人の領域を変化させることで、実際に発言している人を容易に特定可能とすることを特徴とする。

【００１６】

また、１０５、２０５の音声入力装置から１０６、２０６を介して送信された音声を２０７、１０７の音声認識部にて誰が発言した音声かを、２０７、１０７にある音声認識ソフトウェアで、１０９、２０９に事前に格納されている声紋データにもとづき認識を行い、即座に１０８、２０８の表示画像変更処理部を介して、発言人の領域を変化させることで、実際に発言している人を容易に特定可能とすることを特徴とする。

【００１７】

図２は、表示装置１０４、２０４に表示される一例である。この例では、

参加者Ａ、参加者Ｂ、参加者Ｃの３名が、それぞれ、１番、２番、３番に割り当てられたことを示している。処理としては、他システム側から画像データを受信し、そのなかより、人物である画像領域を判断し、各人物別に番号を割り当てることで実現させる。

【００１８】

図３は、表示装置１０４、２０４に表示される一例である。この例では、参加者Ａが実施に発言を行っていることが、参加者Ａの背景部分の色が変化することで容易にわかる。処理としては、他システム側から発信者識別情報を受信後、該当番号の人物画像域の色を変化させることで実現させる。

【００１９】

図４は、画像データを受信する側の会議が運用されるまでの準備のフローチャートである。その流れは、他システム側から画像データを受信し、そのなかより、人物である画像領域を判断し、各人物別に番号を割り当てを実施する。その後、他システム側へ各人物画像と番号割り当て情報を送信する。

【００２０】

図５は、画像データを送信する側の会議が運用されるまでの準備のフローチャートである。その流れは、他システム側へ画像データを送信後、他システム側から各人物画像と番号割り当て情報を受信＆表示する。

【００２１】

図６は、画像データを受信する側の運用中のフローチャートである。その流れは、他システム側から発信者識別情報を受信後、該当番号の人物画像域の色を変化させる。

【００２２】

図７は、画像データを送信する側の運用中のフローチャートである。その流れは、入力装置から番号情報が入力されたら、他システム側へ発信者識別情報を送信する。

【００２３】

【発明の効果】

この発明により、以下に代表されるような効果が期待できる。

【００２４】

（１）簡単な設備で、誰が発言しているかを効果的かつ容易に識別が可能となる。

（２）従来の動画を基本としたＴＶ会議システムを構築することなく、同等のサービスを得ることが出きる。

（３）発言者の人事情報（プロフィール等）も同時に認識出きる。

（４）発言者の名前も含めた、正確な議事録の作成が可能となる。

【図面の簡単な説明】

【図１】

本発明の原理構成図である。

【図２】

本発明の一実施例の図である。

【図３】

本発明の一実施例の図である。

【図４】

本発明の画像データ受信側の準備フローチャートである。

【図５】

本発明の画像データ送信側の準備フローチャートである。

【図６】

本発明の画像データ受信側の運用中フローチャートである。

【図７】

本発明の画像データ送信側の運用中フローチャートである。

【符号の説明】

１００、２００：会議システム

１０１、２０１：カメラ

１０２、２０２：静止画像符号化部

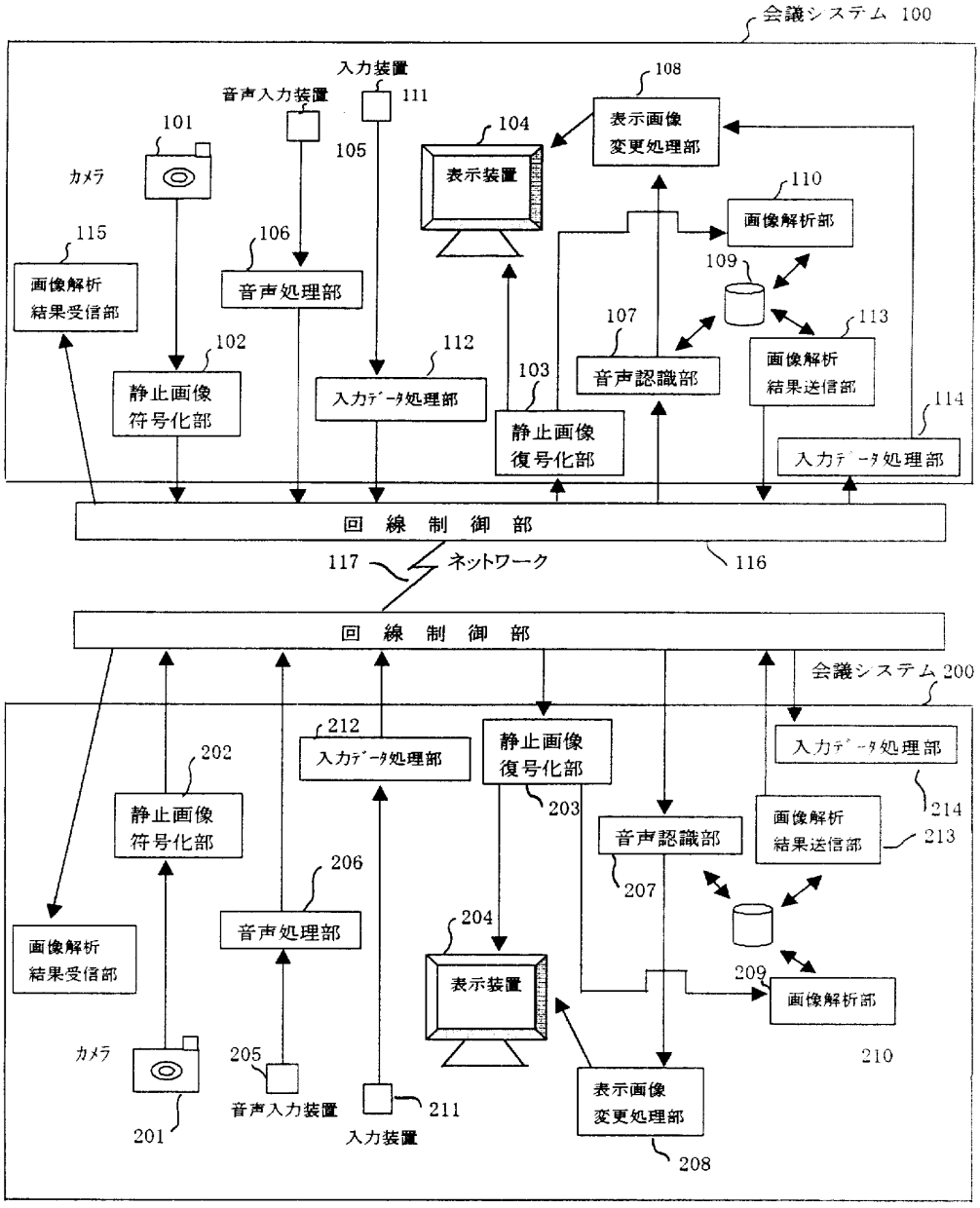
１０３、２０３：静止画像復号化部

１０４、２０４：表示装置

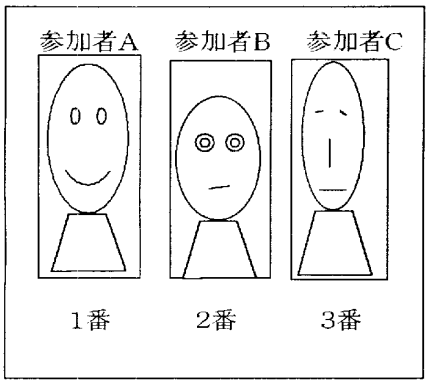
１０５、２０５：音声入力装置
１０６、２０６：音声処理部
１０７、２０７：音声認識部
１０８、２０８：表示画像変更処理部
１０９、２０９：データベース
１１０、２１０：画像解析部
１１１、２１１：入力装置
１１２、２１２：入力データ処理部
１１３、２１３：画像解析結果送信部
１１４、２１４：入力データ処理部
１１５、２１５：画像解析結果受信部
１１６、２１６：回線制御部
１１７：ネットワーク

【書類名】　　図面

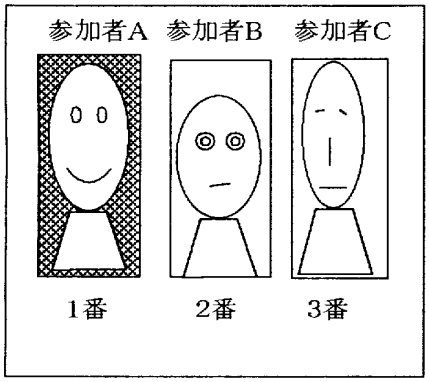
【図１】


会議システム 100
入力装置
音声入力装置
111
108
表示画像
変更処理部
101
104
105
表示装置
カメラ
110
画像解析部
115
106
109
画像解析
結果受信部
音声処理部
107
113
102
112
103
音声認識部
画像解析
結果送信部
静止画像
符号化部
入力ﾃﾞｰﾀ処理部
静止画像
復号化部
114
入力ﾃﾞｰﾀ処理部
回　線　制　御　部
117
ネットワーク
116
回　線　制　御　部
会議システム 200
212
入力ﾃﾞｰﾀ処理部
静止画像
復号化部
入力ﾃﾞｰﾀ処理部
202
203
214
静止画像
符号化部
音声認識部
画像解析
結果送信部
213
206
207
画像解析
結果受信部
音声処理部
204
209
表示装置
画像解析部
カメラ
205
210
音声入力装置
211
表示画像
変更処理部
201
入力装置
208

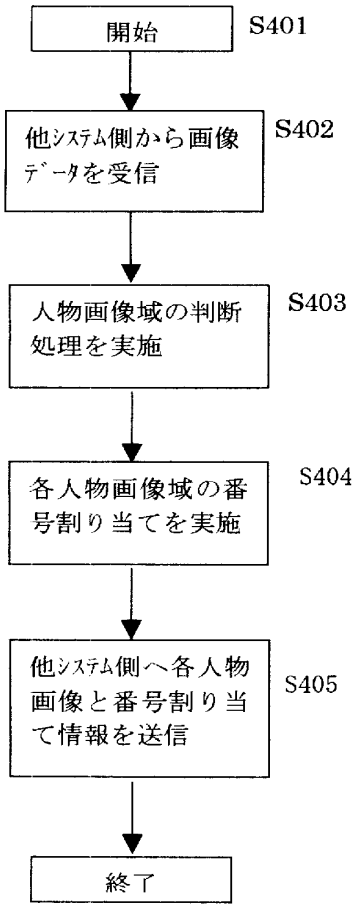
【図２】



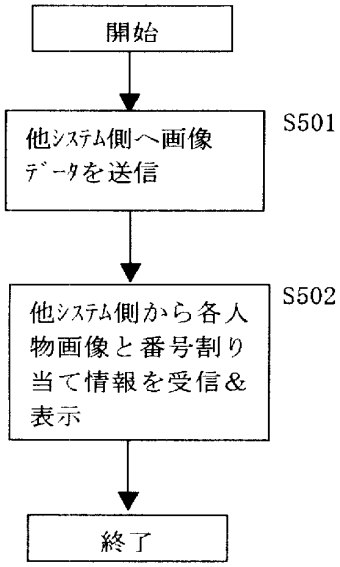
【図３】



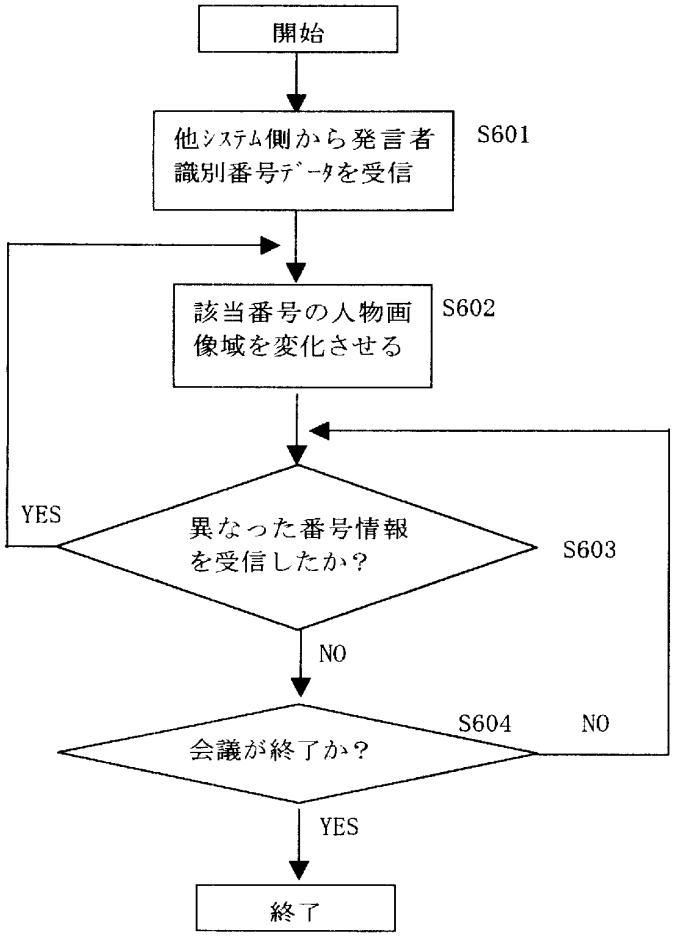
【図４】


開始
S401
他ｼｽﾃﾑ側から画像ﾃﾞｰﾀを受信
S402
人物画像域の判断処理を実施
S403
各人物画像域の番号割り当てを実施
S404
他ｼｽﾃﾑ側へ各人物画像と番号割り当て情報を送信
S405
終了

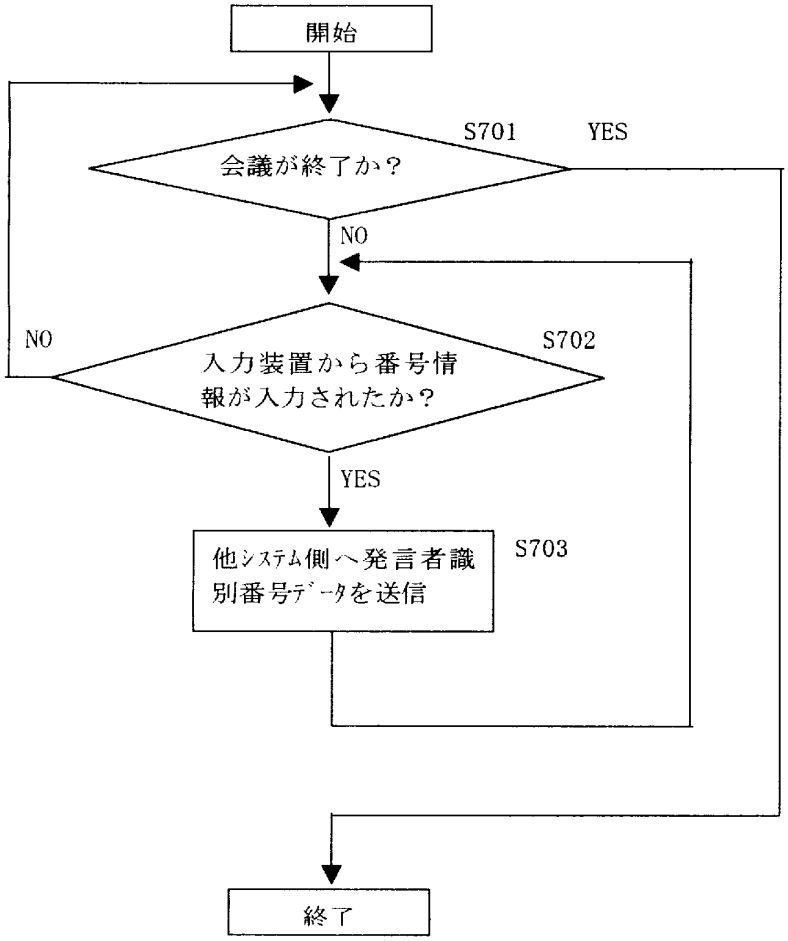
【図５】


開始
他ｼｽﾃﾑ側へ画像ﾃﾞｰﾀを送信
S501
他ｼｽﾃﾑ側から各人物画像と番号割り当て情報を受信＆表示
S502
終了

【図６】


開始
他ｼｽﾃﾑ側から発言者識別番号ﾃﾞｰﾀを受信
S601
該当番号の人物画像域を変化させる
S602
異なった番号情報を受信したか？
S603
YES
NO
会議が終了か？
S604
NO
YES
終了

【図７】


開始
S701
YES
会議が終了か？
NO
NO
S702
入力装置から番号情報が入力されたか？
YES
S703
他ｼｽﾃﾑ側へ発言者識別番号ﾃﾞｰﾀを送信
終了

【書類名】　　要約書

【要約】

【課題】　本発明は、会議システム装置に関し、特に静止画映像によるＴＶ会議システムあるいは電話会議システム等に用いられ、静止画映像に変化を加えること等で、動画を随時送受信するＴＶ会議システムと同等の使い勝手を実現し、かつ従来にない付帯の機能を実現する手段を備えた会議システムを提供する。

【解決手段】　ネットワークを介して実施する会議システムであって、他地点へ伝送した会議参加者が映された画像静止データをもとに、映された各参加者の画像位置付け処理を行なう画像処理手段と、その位置付け情報を各発言者が発言時に同時に入力装置にて他地点側会議システムに伝送する伝送手段と、他地点システム側では伝送された位置付け識別データ情報をもとに、表示装置に映し出されている他地点側の会議参加者が映された画像静止データの該当画像領域部分を変化させることで、容易に発言者の識別を可能とする。

【選択図】　図１

出願人履歴

０００１３６１３６

19900831

新規登録

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０００１３６１３６

20030407

名称変更

石川県河北郡宇ノ気町字宇野気ヌ９８番地の２

株式会社ＰＦＵ

０００１３６１３６

20040308

住所変更

石川県かほく市宇野気ヌ９８番地の２

株式会社ＰＦＵ

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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
15/271,422	09/21/2016	Yoshiaki NAKAYOSHI	HARU-0126	2686

38327 7590 09/17/2018

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EXAMINER	
CHIEN, LUCY P	

ART UNIT	PAPER NUMBER
2871	

NOTIFICATION DATE	DELIVERY MODE
09/17/2018	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

USPTO@dockettrak.com
lniu@marqueziplaw.com
mail@marqueziplaw.com

Office Action Summary	Application No. 15/271,422	Applicant(s) NAKAYOSHI et al.	
	Examiner LUCY P CHIEN	Art Unit 2871	AIA Status No

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTHS FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☑ Responsive to communication(s) filed on 9/21/2016.

☐ A declaration(s)/affidavit(s) under **37 CFR 1.130(b)** was/were filed on _____.

2a)☐ This action is **FINAL.** 2b) ☑ This action is non-final.

3)☐ An election was made by the applicant in response to a restriction requirement set forth during the interview on _____; the restriction requirement and election have been incorporated into this action.

4)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims*

5) ☑ Claim(s) 1-3 and 14-30 is/are pending in the application.

5a) Of the above claim(s) _____ is/are withdrawn from consideration.

6) ☐ Claim(s) _____ is/are allowed.

7) ☑ Claim(s) 1-3,14-16 and 19-30 is/are rejected.

8) ☑ Claim(s) 17-18 is/are objected to.

9) ☐ Claim(s) _____ are subject to restriction and/or election requirement

* If any claims have been determined allowable, you may be eligible to benefit from the **Patent Prosecution Highway** program at a participating intellectual property office for the corresponding application. For more information, please see http://www.uspto.gov/patents/init_events/pph/index.jsp or send an inquiry to **PPHfeedback@uspto.gov.**

Application Papers

10)☐ The specification is objected to by the Examiner.

11)☑ The drawing(s) filed on 9/21/2016 is/are: a)☑ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

Priority under 35 U.S.C. § 119

12)☑ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

Certified copies:

a)☑ All b)☐ Some** c)☐ None of the:

1.☑ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

** See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☑ Notice of References Cited (PTO-892)

2) ☑ Information Disclosure Statement(s) (PTO/SB/08a and/or PTO/SB/08b) Paper No(s)/Mail Date See Continuation Sheet.

3) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date _____.

4) ☐ Other: _____.

Continuation of Attachment(s) 2) Information Disclosure Statement(s) (PTO/SB/08a and/or PTO/SB/08b)
Paper No(s)/Mail Date: 9/21/2016,9/21/2016,9/21/2016,9/21/2016,9/21/2016

Notice of Pre-AIA or AIA Status

1. The present application is being examined under the pre-AIA first to invent provisions.

Claim Rejections - 35 USC § 103

2. In the event the determination of the status of the application as subject to AIA 35 U.S.C. 102 and 103 (or as subject to pre-AIA 35 U.S.C. 102 and 103) is incorrect, any correction of the statutory basis for the rejection will not be considered a new ground of rejection if the prior art relied upon, and the rationale supporting the rejection, would be the same under either status.

3. **Claim 1-3,14-16,19-30** is/are rejected under pre-AIA 35 U.S.C. 103(a) as being unpatentable over Min et al (US 6449026) in view of Lyu et al (US 6001539) in view of Kaneko et al (US 20010030717)

Regarding Claim 1-3

Min et al discloses (Fig. 1 and Fig. 2) a liquid crystal display device, comprising: a first substrate (11); a second substrate; a liquid crystal layer between the first substrate and the second substrate, containing liquid crystal molecules (column 4, lines 1-8); a gate line (31) and a drain line (36); a pixel electrode (21) and a counter electrode (12) disposed between the first substrate and the liquid crystal layer; a gate insulation layer (15) formed on the gate line; a insulation layer (20) disposed between the first substrate (11) and the liquid crystal layer; a switching element (where 13 is located), connected to the gate line, including a first electrode (19a) connected to the drain line and a second electrode (19b) connected to the pixel electrode (21); wherein the liquid crystal layer is driven by an electric field generated between the pixel electrode and the

counter electrode, and wherein the pixel electrode (21) is formed between the liquid crystal layer and the insulation layer (20), and wherein the counter electrode (12) is a planar shape, and the pixel electrode comprises a slit having a first portion (21),

Min et al does not disclose an organic insulation layer and the first portion is not parallel with the gate line and the drain line.

Lyu et al discloses (abstract) an organic insulation layer (110).

Kaneko et al discloses (Fig. 2) first portion is not parallel with the gate line and the drain line.

It would have been obvious to one of ordinary skill in the art to modify Min et al to include Lyu et al's organic insulation layer motivated by the desire to create a buffer between the TFT and pixel electrode to further include Kaneko et al's first portion of the pixel electrode not parallel with the gate line and drain line motivated by the desire tilt the liquid crystal a certain direction.

Regarding Claim 14,

In addition to Min et al, Lyu et al, and Kaneko et al, Min et al discloses (Fig. 1 and Fig. 2) wherein the pixel electrode (21)comprises a slit having a first portion, and the first portion is not parallel with the gate line and the drain line at least in a pixel (taught by Kaneko et al Fig. 2).

Regarding Claim 15,

In addition to Min et al, Lyu et al, and Kaneko et al, Min et al discloses (Fig. 1 and Fig. 2) wherein the pixel electrode (21) comprises a slit having a first portion, and the

first portion is not parallel with the gate line and the drain line at least in a pixel. (taught by Kaneko et al Fig. 2).

Regarding Claim 16,

In addition to Min et al, Lyu et al, and Kaneko et al, Min et al discloses (Fig. 1 and Fig. 2) wherein the counter electrode is connected to a common layer and, wherein the organic insulation layer is formed between the counter electrode and the first substrate. (column 1, lines 63-67).

Regarding Claim 19,

In addition to Min et al, Lyu et al, and Kaneko et al, Min et al discloses (Fig. 1 and Fig. 2) wherein a passivation layer (20) is formed between the liquid crystal layer and the pixel electrode (21) contacting a second electrode (19b), and wherein the passivation layer (20) is formed between the liquid crystal layer and the drain line (19a).

Regarding Claim 20,

In addition to Min et al, Lyu et al, and Kaneko et al, Min et al discloses (Fig. 1 and Fig. 2) wherein a passivation layer (20) is formed between the liquid crystal layer and the pixel electrode (21) contacting a second electrode (19b), and wherein the passivation layer (20) is formed between the liquid crystal layer and the drain line (19a).

Regarding Claim 21,

In addition to Min et al, Lyu et al, and Kaneko et al, Min et al discloses (Fig. 1 and Fig. 2) wherein a passivation layer (20) is formed between the liquid crystal layer and

the pixel electrode (21) contacting a second electrode (19b), and wherein the passivation layer is formed between the liquid crystal layer and the drain line.

Regarding Claim 22,

In addition to Min et al, Lyu et al, and Kaneko et al, Min et al discloses (Fig. 1 and Fig. 2)wherein the counter electrode (12)is a planer shape, and the pixel electrode (21) comprises a slit having the first portion and a second portion, and both of the first portion and the second portion are not parallel with the gate line and the drain line. (taught by Kaneko et al Fig. 2).

Regarding Claim 23,

In addition to Min et al, Lyu et al, and Kaneko et al, Min et al discloses (Fig. 1 and Fig. 2) wherein the counter electrode (12) is a planer shape, and the pixel electrode (21) comprises a slit having the first portion and a second portion, and both of the first portion and the second portion are not parallel with the gate line. (taught by Kaneko et al Fig. 2).

Regarding Claim 24,

In addition to Min et al, Lyu et al, and Kaneko et al, Min et al discloses (Fig. 1 and Fig. 2) wherein the counter electrode (12) is a planer shape, and the pixel electrode (21) comprises a slit having the first portion and a second portion, and both of the first portion and the second portion are not parallel with the drain line. (taught by Kaneko et al Fig. 2).

Regarding Claim 25,

In addition to Min et al, Lyu et al, and Kaneko et al, Min et al discloses (Fig. 1 and Fig. 2) wherein the gate insulation layer (15) is formed between the counter electrode (12) and the drain line (19a).

Regarding Claim 26,

In addition to Min et al, Lyu et al, and Kaneko et al, Min et al discloses (Fig. 1 and Fig. 2) wherein the counter electrode (12) connects to a connection line. (column 1, lines 63-67).

Regarding Claim 27,

In addition to Min et al, Lyu et al, and Kaneko et al, Min et al discloses (Fig. 1 and Fig. 2) wherein the connection line is arranged parallel to the extension direction of the gate line. (column 1, lines 63-67).

Regarding Claim 28,

In addition to Min et al, Lyu et al, and Kaneko et al, Min et al discloses (Fig. 1 and Fig. 2) wherein the organic insulation layer (20) is formed between the connection line and the first substrate (11).

Regarding Claim 29,

In addition to Min et al, Lyu et al, and Kaneko et al, Min et al discloses (Fig. 1 and Fig. 2) wherein the connection line is directly contacted to the counter electrode. (column 1, lines 63-67).

Regarding Claim 30,

In addition to Min et al, Lyu et al, and Kaneko et al, Min et al discloses (Fig. 1 and Fig. 2) wherein the common electrode (12) is disposed between the connection line and the liquid crystal layer. (column 1, lines 63-67).

Allowable Subject Matter

4. **Claim 17,18** are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Regarding Claim 17,

The prior art does not disclose nor would it be obvious to one of ordinary skill in the art to include another reference to disclose wherein the counter electrode is connected to the common layer via a through hole within the organic insulation layer. Claim 18 depends on Claim 17, therefore is objected.

Conclusion

5. Any inquiry concerning this communication or earlier communications from the examiner should be directed to LUCY P CHIEN whose telephone number is (571)272-8579. The examiner can normally be reached on 9AM-5PM PST M-F.

Examiner interviews are available via telephone, in-person, and video conferencing using a USPTO supplied web-based collaboration tool. To schedule an interview, applicant is encouraged to use the USPTO Automated Interview Request (AIR) at http://www.uspto.gov/interviewpractice.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Michael Caley can be reached on 571-272-2286. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/LUCY P CHIEN/
Primary Examiner, Art Unit 2871

Notice of References Cited	Application/Control No. 15/271,422	Applicant(s)/Patent Under Reexamination NAKAYOSHI et al.	
	Examiner LUCY P CHIEN	Art Unit 2871	Page 1 of 1

U.S. PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Name	CPC Classification	US Classification
*	A	US-6449026-B1	09-2002	Min; Tae Yup	G02F1/134363	349/141
*	B	US-6001539-A	12-1999	Lyu; Ki-Hyun	H01L27/1214	430/317
*	C	US-20010030717-A1	10-2001	Kaneko, Toshiki	G02F1/134363	349/43
	D					
	E					
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FOREIGN PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Country	Name	CPC Classification
	N					
	O					
	P					
	Q					
	R					
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	T					

NON-PATENT DOCUMENTS

*		Include as applicable: Author, Title Date, Publisher, Edition or Volume, Pertinent Pages)
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	X	

*A copy of this reference is not being furnished with this Office action. (See MPEP § 707.05(a).)
Dates in MM-YYYY format are publication dates. Classifications may be US or foreign.

Search Notes	Application/Control No.	Applicant(s)/Patent Under Reexamination
	15/271,422	NAKAYOSHI et al.
	Examiner	Art Unit
	LUCY P CHIEN	2871

CPC - Searched*		
Symbol	Date	Examiner

CPC Combination Sets - Searched*		
Symbol	Date	Examiner

US Classification - Searched*			
Class	Subclass	Date	Examiner

* See search history printout included with this form or the SEARCH NOTES box below to determine the scope of the search.

Search Notes		
Search Notes	Date	Examiner
see search notes from EAST	09/12/2018	LC

Interference Search			
US Class/CPC Symbol	US Subclass/CPC Group	Date	Examiner

/LUCY P CHIEN/ Primary Examiner, Art Unit 2871	

PTO/SB/08a (07-09)
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INFORMATION DISCLOSURE STATEMENT BY APPLICANT

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Sheet 1 of 1

Complete if Known	
Application Number	15
Filing Date	2016-09-21
First Named Inventor	NAKAYOSHI
Art Unit	
Examiner Name	
Attorney Docket Number	HARU-0126

U. S. PATENT DOCUMENTS

Examiner Initials*	Cite No.[1]	Document Number Number-Kind Code[2] *(if known)*	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
	1	US- 6,469,765 B1	10-22-2002	Matsuyama et al.	
	2	US- 6,580,487 B1	06-17-2003	Kim et al.	
	3	US- 6,600,542 B2	07-29-2003	Kim et al.	
	4	US- 6,611,310 B2	08-26-2003	Kurahashi et al.	
	5	US- 6,646,707 B2	11-11-2003	Noh et al.	
	6	US- 6,667,790 B2	12-23-2003	Yanagawa et al.	
	7	US- 6,671,019 B1	12-30-2003	Petschek et al.	
	8	US- 6,721,028 B2	04-13-2004	Kim et al.	
	9	US- 6,784,964 B2	08-31-2004	Nakayoshi et al.	
	10	US- 2002/0041354 A1	04-11-2002	Noh et al.	
	11	US- 2003/0086045 A1	05-08-2003	Ono et al.	
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	13	US- 2002/0048500 A1	04-25-2002	Hermann et al.	
	14	US- 6,639,640 B1	10-28-2003	Matsuoka et al.	
	15	US- 6,335,148 B2	01-01-2002	Lee et al.	
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	17	US- 5,686,980	11-11-1997	Hirayama et al.	
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7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.
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	1	US- 6,069,678	05-30-2000	Sakamoto et al.	
	2	US- 6,650,389 B1	11-18-2003	Sakamoto	
	3	US- 6,462,800 B1	10-08-2002	Kim et al.	
	4	US- 6,552,770 B2	04-22-2003	Yanagawa et al.	
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	10	US- 5,892,562	04-06-1999	Yamazaki et al.	
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	12	US- 6,259,502	07-10-2001	Komatsu	
	13	US- 5,668,379	09-16-1997	Ono et al.	
	14	US- 5,742,365	04-21-1998	Seo	
	15	US- 6,600,541	07-29-2003	Kurahashi et al.	
	16	US- 5,668,379	09-16-1997	Ono et al.	
	17	US- 6,580,487	06-17-2003	Kim et al.	
	18	US-			
	19	US-			

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EAST Search History

EAST Search History (Prior Art)

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L1	188	"5668379"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2018/09/12 15:48
L2	55	G02F1/134309.cpc. and pixel adj3 electrode near8 slit$2 near9 ((common counter) adj2 electrode$2) near9 planar	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2018/09/12 15:52
L3	20	L2 and organic adj3 insulat$4	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2018/09/12 15:52
L4	180	pixel adj3 electrode near8 slit$2 near9 ((common counter) adj2 electrode$2) near9 planar	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2018/09/12 15:59
L5	38	L4 and organic adj3 insulat$4	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2018/09/12 15:59
L6	1989	G02F2001/134372.cpc. and G02F1/134309.cpc.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2018/09/12 16:08
L7	328	L6 and pixel adj3 electrode$2 near8 slit$2	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2018/09/12 16:08
L8	79	L7 and organic near3 insulat$4	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2018/09/12 16:08
L9	6643	G02F2001/134372.cpc.	US-PGPUB; USPAT; USOCR;	OR	OFF	2018/09/12 16:10

			FPRS; EPO; JPO; DERWENT; IBM_TDB			
L10	1392	L9 and pixel adj3 electrode$2 near8 (cut adj3 outs cutt adj3 outs comb slit$2)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2018/09/12 16:10
L11	13	("4542960" | "4643533" | "5162933" | "5309264" | "5576862" | "5598285" | "5836797" | "5959706" | "5959708" | "5977562" | "6124915" | "6177970" | "6233034").PN.	US-PGPUB; USPAT; USOCR	OR	OFF	2018/09/12 16:21
L12	34	"6580487"	US-PGPUB; USPAT; USOCR	OR	OFF	2018/09/12 16:27
L13	1	US20170010509A1	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2018/09/12 17:22
L14	5	"20170010509"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2018/09/12 17:22
L15	201	G02F2001/134372.cpc. and passivation near3 organic	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2018/09/12 17:24
L16	1601	(TFT transistor) near9 passivation near3 organic	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2018/09/12 17:25
L20	750	pixel adj3 electrode near8 (zig zag zigzag$4)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2018/09/12 17:29

EAST Search History (Interference)

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Attorney Docket Number	HARU-0126

NON PATENT LITERATURE DOCUMENTS

Examiner Initials*	Cite No.[1]	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T[2]
		JPO Office Action dated April 8, 2018, in Japanese	
		Chinese Office Action dated May 9, 2008 regarding Chinese Patent Application No. 2007100057283, in Chinese	

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2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.
3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.
4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).
5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.
6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).
7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (*i.e.*, GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.
8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspection or an issued patent.
9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /L.P.C/

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re U.S. Patent Application of	)	
	)	
NAKAYOSHI et al.	)	**Confirmation No. 2686**
	)	
Application Number: 15/271,422	)	
	)	
Filed: September 21, 2016	)	
	)	
For: LIQUID CRYSTAL DISPLAY DEVICE, DISPLAY DEVICE AND MANUFACTURING METHOD THEREOF	)	
	)	
Attorney Docket No. HARU-0126	)	

Commissioner of Patents
P.O. Box 1450
Alexandria, VA 22313-1450

INFORMATION DISCLOSURE STATEMENT

Sir:

This application is a Continuation of U.S. Application Serial No. 14/942,120 filed on November 16, 2015 which is a Continuation of U.S. Application Serial No. 14/708,348 filed on May 11, 2015, which is a Continuation of U.S. Application No. 14/285,006 filed on May 22, 2014, which is a continuation of U.S. Application No. 13/927,539 filed on June 26, 2013, which is a Continuation of U.S. Application No. 13/650,203 filed on October 12, 2012, which is a Continuation of U.S. Application No. 13/364,092 filed on February 1, 2012, which is a Continuation of U.S. Application Serial No. 12/926,735 filed December 7, 2010, which is a Continuation of U.S. Application Serial No. 12/292,728 filed November 25, 2008, which is a Divisional of U.S. Application Serial No. 11/976,884 filed October 29, 2007, which is a Divisional of U.S. Application No. 11/409,076 filed April 24, 2006, which is a Divisional of U.S. Application Serial No. 11/211,574 filed August 26, 2005, which is a Divisional of U.S. Application Serial No. 10/237,911 filed September 10, 2002.

ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /L.P.C/

Pursuant to 37 C.F.R. §§ 1.56 and 1.97, this Information Disclosure Statement is being submitted in connection with the above-identified patent application. A listing of documents to be published on the face of any patent granted from this application is submitted herewith on the accompanying Form PTO-1449. Any other documents or information submitted for consideration by the Examiner are listed in this paper. A copy of each non-US or foreign patent or non-patent publication or any portion thereof listed or herein identified is submitted herewith.

CERTIFICATION

1. This Information Disclosure Statement is being submitted:
   - **[X] (a)** Concurrently with the new Continuation Application, whereby it is believed that no fee is due; OR
   - **[ ] (b)** After three months from the filing date of the above-identified U.S. patent application but before the mailing date of the first Office Action on the merits of the above-identified application, whereby it is believed that no fee is due; OR
   - **[ ] (c)** After three months from the filing date of the above-identified U.S. patent application and after the mailing date of the first Office Action on the merits of the above-identified application, but prior to the issuance of any Final Action or Notice of Allowance sent in such application, whereby Applicant(s) hereby submit the requisite certification hereinbelow, or authorization for the payment of the requisite fee is set forth hereinbelow; OR
   - **[ ] (d)** After the issuance of a Final Action or Notice of Allowance, but before the payment of the Issue Fee, whereby Applicant(s) hereby submit the requisite certification hereinbelow, and authorization for the payment of the requisite fee is set forth hereinbelow.

2. In accordance with the requirements of 37 C.F.R. §1.97, and the above, Applicant(s) hereby certify that:
   - [ ] Each item of information contained in this Information Disclosure Statement was first cited in any communication from a foreign patent office in a counterpart foreign application not more than three months prior to the filing of this Information Disclosure Statement; OR
   - [ ] No item of information contained in this Information Disclosure Statement was cited in a communication from a foreign patent office in a counterpart foreign application, and, to the knowledge of the person signing the certification after making reasonable inquiry, no

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item of information contained in the information disclosure statement was known to any individual designated in §1.56(c) more than three months prior to the filing of this Information Disclosure Statement.

3. Payment of any fees associated with this communication and submission is as follows:

[ ] Payment for $____ to cover the fee is being submitted via the EFS payment procedure.

[X] The Commissioner is hereby authorized to charge payment of any fees associated with this communication, including fees under 37 C.F.R. § 1.16 and 1.17, or credit any overpayment to Deposit Account Number 60-0155.

4. The Examiner is requested to acknowledge receipt and consideration of the information provided in this paper in accordance with prescribed procedures. Should there be any outstanding issues requiring discussion that would further the prosecution and allowance of the above-captioned application, the Examiner is invited to contact the undersigned representative at the address and phone number indicated below.

Respectfully submitted,

/juan.carlos.a.marquez/

_____

Juan Carlos A. Marquez
Registration Number 34,072

MARQUEZ IP LAW OFFICE, PLLC
1629 K Street, NW, Suite 300
Washington, DC 20006
Phone: (202) 349-1690
Fax: (202) 754-9829
Customer No. 38327

September 21, 2016

/LUCY P CHIEN/ 09/12/2018

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PTO/SB/08a (07-09)
Approved for use through 07/31/2016. OMB 0651-0031
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Substitute for form 1449/PTO

INFORMATION DISCLOSURE STATEMENT BY APPLICANT

(Use as many sheets as necessary)

Sheet 1 of 1

Complete if Known	
Application Number	15
Filing Date	2016-09-21
First Named Inventor	NAKAYOSHI
Art Unit	
Examiner Name	
Attorney Docket Number	HARU-0126

U. S. PATENT DOCUMENTS

Examiner Initials*	Cite No.[1]	Document Number Number-Kind Code[2] *(if known)*	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
	1	US- 5914762	06-22-1999	Lee et al.	
	2	US- 6233034 B1	05-15-2011	Lee et al.	
	3	US- 6456351 B1	09-24-2002	Kim et al.	
	4	US- 6256081 B1	07-03-2001	Lee et al.	
	5	US- 5,745,207	04-28-1998	Asada et al.	
	6	US- 6,266,116 B1	07-24-2001	OHTA et al,	
	7	US- 5,946,066	08-31-1999	Lee et al.	
	8	US- 6,597,413 B2	07-22-2003	Kurashina	
	9	US- 6,661,476 B1	12-09-2003	Abe et al.	
	10	US- 6,587,162 B1	07-01-2003	Kaneko et al.	
	11	US- 6,556,265 B1	04-29-2003	Murade	
	12	US- 6,493,046 B1	12-10-2002	Ueda	
	13	US- 5,060,036	10-22-1991	Choi	
	14	US- 6,356,330 B1	03-12-2002	Ando et al.	
	15	US- 5,185,601	02-09-1993	Takeda et al.	
	16	US- 5,771,082	06-23-1998	Chaudet et al.	
	17	US- 6,285,429 B1	09-04-2001	Nishida et al.	
	18	US- 6,362,858 B1	03-26-2002	Jeon et al.	
	19	US- 6,404,470 B1	06-11-2002	Kim et al.	

FOREIGN PATENT DOCUMENTS

Examiner Initials*	Cite No.[1]	Foreign Patent Document Country Code[3]-Number[4]-Kind Code[5] *(if known)*	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages Or Relevant Figures Appear	T[6]
	1	JP 2001-228493	08-24-2001	Hynix Semiconductor Inc.	Abstract	✔
	2	JP 2000-08408	09-24-1998			✔
	3	JP 3591513	04-19-2001	Seiko Epson Corporation		
	4	CN 1242854A	03-04-1999	Seiko Epson Corporation		

Examiner Signature	/LUCY P CHIEN/	Date Considered	09/12/2018

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant. [1] Applicant's unique citation designation number (optional). [2] See Kinds Codes of USPTO Patent Documents at www.uspto.gov or MPEP 901.04. [3] Enter Office that issued the document, by the two-letter code (WIPO Standard ST.3). [4] For Japanese patent documents, the indication of the year of the reign of the Emperor must precede the serial number of the patent document. [5] Kind of document by the appropriate symbols as indicated on the document under WIPO Standard ST.16 if possible. [6] Applicant is to place a check mark here if English language Translation is attached.

ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /L.P.C/

Privacy Act Statement

The Privacy Act of 1974 (P.L. 93-579) requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether disclosure of these records is required by the Freedom of Information Act.
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6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).
7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.
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ALEXANDRIA VA 22313-1451

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Juan Carlos A. Marquez
Marquez Intellectual Property Law Office PLLC
1629 K Street, NW
Suite 300
Washington, DC 20006

Courtesy Reminder for
Application Serial No: 15/271,422

Attorney Docket No: HARU-0126
Customer Number: 38327
Date of Electronic Notification: 09/17/2018

This is a courtesy reminder that new correspondence is available for this application. If you have not done so already, please review the correspondence. The official date of notification of the outgoing correspondence will be indicated on the form PTOL-90 accompanying the correspondence.

An email notification regarding the correspondence was sent to the following email address(es) associated with your customer number:

USPTO@dockettrak.com
mail@marqueziplaw.com
lniu@marqueziplaw.com

To view your correspondence online or update your email addresses, please visit us anytime at **https://sportal.uspto.gov/secure/myportal/privatepair.** If you have any questions, please email the Electronic Business Center (EBC) at EBC@uspto.gov or call 1-866-217-9197.

Electronic Acknowledgement Receipt	
EFS ID:	34605534
Application Number:	15271422
International Application Number:	
Confirmation Number:	2686
Title of Invention:	LIQUID CRYSTAL DISPLAY DEVICE, DISPLAY DEVICE AND MANUFACTURING METHOD THEREOF
First Named Inventor/Applicant Name:	Yoshiaki NAKAYOSHI
Customer Number:	38327
Filer:	Juan Carlos A. Marquez
Filer Authorized By:	
Attorney Docket Number:	HARU-0126
Receipt Date:	17-DEC-2018
Filing Date:	21-SEP-2016
Time Stamp:	14:14:45
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	no

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Transmittal Letter	HARU-126-Claim_calculation_sheet_Response_09172018.pdf	172716 0b1a2baa4997614af9471aa485566ae8661bc200	no	2

Warnings:

Information:					
2	Amendment/Req. Reconsideration-After Non-Final Reject	HARU-126_Response_to_OA_09172018.pdf	161836 9a4b39fba325ba405fd0cc17fcd7cd72b0242199	no	5
Warnings:					
Information:					
			Total Files Size (in bytes):	334552	

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111
If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.
National Stage of an International Application under 35 U.S.C. 371
If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.
New International Application Filed with the USPTO as a Receiving Office
If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re U.S. Patent Application of	)	**Confirmation No. 2686**
	)	
NAKAYOSHI et al.	)	
	)	**Art Unit 2871**
Application Number: 15/271,422	)	
	)	
Filed: September 21, 2016	)	**Examiner: Lucy P. Chien**
	)	
For: LIQUID CRYSTAL DISPLAY DEVICE, DISPLAY DEVICE AND MANUFACTURING METHOD THEREOF	)	
	)	
Attorney Docket No. HARU-0126	)	

Mail Stop Amendment
Commissioner of Patents
P.O. Box 1450
Alexandria, VA 22313-1450

COVER LETTER

Sir:

[X] The fee for submission of claims is calculated as shown below:

FOR	TOTAL WITH NEW CLAIMS ADDED	TOTAL CURRENTLY ON FILE	CLAIMS ALREADY PAID	RATE	CALCULATION
Total Claims	2	20	(Over 20)	x $100	0
Independent Claims	1	3	(Over 3)	x $460	0
MULTIPLE DEPENDENT CLAIM(S)				+ 820	0
REDUCTION FOR FILING BY SMALL ENTITY (note 37 C.F.R. §§ 1.9, 1.27, 1.28).				x ½	
			TOTAL		$0

In addition, the below-identified communications are submitted in the above-captioned application or proceeding:

[x] Response to Non-Final Office Action (with claim amendments)
[ ] Substitute Abstract
[ ] Terminal Disclaimer
[ ] Information Disclosure Statement
[ ] __ sheet of replacement drawings
[ ] RCE
[ ] Other:

[ ] Applicant(s) hereby request and petition that the time for taking action in this case be extended pursuant to 37 C.F.R. § 1.136(a) for:
[ ] **one (1) month** [ ] **two (2) months** [ ] **three (3) months**

The fee set in 37 C.F.R. § 1.17 for the extension of time is **$**_____ for a large/small entity.

[ ] Payment of **$**_____ is made by credit card via the EFS payment system.

[x] The Commissioner is hereby authorized to charge any additional fees associated with this communication, including fees under 37 C.F.R. § 1.16 and 1.17, or credit any overpayment to **Deposit Account Number 60-0155**.

Respectfully submitted,

/juan.carlos.a.marquez/

Juan Carlos A. Marquez
Registration Number 34,072

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Customer No. 38327

December 17, 2018

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re U.S. Patent Application of	)	**Confirmation No. 2686**
NAKAYOSHI et al.	)	**Art Unit 2871**
Application Number: 15/271,422	)	
Filed: September 21, 2016	)	**Examiner: Lucy P. Chien**
For: LIQUID CRYSTAL DISPLAY DEVICE, DISPLAY DEVICE AND MANUFACTURING METHOD THEREOF	)	
Attorney Docket No. HARU-0126	)	

Commissioner of Patents
P.O. Box 1450
Alexandria, VA 22313-1450

RESPONSE AND AMENDMENT UNDER 37 C.F.R. § 1.111

Sir:

This is in response to the Office Action mailed on September 17, 2018, the period of response to which is set to expire on December 17, 2018. Please amend the above-referenced application as follows:

IN THE CLAIMS:

Claims 17-18 stand for consideration in this application, wherein claim 17 is being amended to more particularly point out and distinctly claim the subject invention; claims 1-3, 14-16 and 19-30 are being canceled without prejudice or disclaimer, all as follows:

1-16. (Canceled).

17. (Currently Amended) A liquid crystal display device ~~according to claim 16~~, comprising:

a first substrate;

a second substrate;

a liquid crystal layer between the first substrate and the second substrate, containing liquid crystal molecules;

a gate line and a drain line;

a pixel electrode and a counter electrode disposed between the first substrate and the liquid crystal layer;

a gate insulation layer formed on the gate line; and

an organic insulation layer disposed between the first substrate and the liquid crystal layer,

wherein the liquid crystal layer is driven by an electric field generated between the pixel electrode and the counter electrode,

wherein the pixel electrode is formed between the liquid crystal layer and the organic insulation layer,

wherein the counter electrode is a planer shape, and the pixel electrode comprises a slit having a first portion, and the first portion is not parallel with the gate line and the drain line,

wherein the counter electrode is connected to a common layer,

wherein the organic insulation layer is formed between the counter electrode and the first substrate, and

wherein the counter electrode is connected to the common layer via a through hole within the organic insulation layer.

18. (Previously Presented) A liquid crystal display device according to claim 17, wherein the common layer is a planer shape, and faces plural of the pixel electrode.

19-30. (Canceled).

REMARKS

The above amendments to the above-captioned application along with the following remarks are being submitted as a full and complete response to the Office Action dated September 17, 2018 (USPTO Paper No. 20180912). In view of the above amendments and the following remarks, the Examiner is respectfully requested to give due reconsideration to this application, to indicate the allowability of the claims, and to pass this case to issue.

Status of the Claims

As outlined above, claims 17-18 stand for consideration in this application, wherein claim 17 is being amended to more particularly point out and distinctly claim the subject invention; claims 1-3, 14-16 and 19-30 are being canceled without prejudice or disclaimer. In particular, claim 17 is being amended to incorporate the substance of claims 1 and 16 therein. Any and all amendments to the specification and/or to the claims are fully supported throughout the disclosure of the invention. Applicants submit that no new matter is being introduced into this application through the submission of this response.

Prior Art Rejection

The Examiner rejected claims 1-3, 14-16 and 19-30 under 35 U.S.C. §103(a) as being unpatentable over US Patent No. 6,001,539 to Min et al., in view of US Publication No. 2001/0030717 to Kaneko et al. Applicants have reviewed the above-noted rejection and hereby respectfully traverse.

Allowable Subject Matter

In the Office Action, the Examiner only objected to claims 17-18 as being dependent on a rejected base claim, but would allow the claims if they are amended to add all the limitations of their base claim and any intervening claims. As outlined above, claim 17 is being amended to more particularly point out and distinctly claim the subject invention as suggested by the Examiner, wherein claim 17 incorporates the substance of claims 1 and 16 therein. In view of the above amendments, Applicants will submit that the claims are now in condition for allowance.

Conclusion

In view of all the above, Applicants respectfully submit that certain clear and distinct differences as discussed exist between the present invention as now claimed and the prior art as a whole. These differences are more than sufficient that the present invention as now claimed would not have been anticipated nor rendered obvious given the prior art. Rather, the present invention as a whole is distinguishable, and thereby allowable over the prior art.

Favorable reconsideration of this application as amended is respectfully solicited. Should there be any outstanding issues requiring discussion that would further the prosecution and allowance of the above-captioned application, the Examiner is invited to contact the Applicants' undersigned representative at the address and phone number indicated below.

Respectfully submitted,

/juan.carlos.a.marquez/

Juan Carlos A. Marquez
Registration Number 34,072

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Suite 300
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Fax: (202) 754-9829
Customer No. 38327

December 17, 2018

PTO/SB/06 (09-11)
Approved for use through 1/31/2014. OMB 0651-0032
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

PATENT APPLICATION FEE DETERMINATION RECORD Substitute for Form PTO-875	Application or Docket Number 15/271,422	Filing Date 09/21/2016	☐ To be Mailed

ENTITY: ☒ LARGE ☐ SMALL ☐ MICRO

APPLICATION AS FILED – PART I

	(Column 1)	(Column 2)		
FOR	NUMBER FILED	NUMBER EXTRA	RATE ($)	FEE ($)
☐ BASIC FEE (37 CFR 1.16(a), (b), or (c))	N/A	N/A	N/A	
☐ SEARCH FEE (37 CFR 1.16(k), (i), or (m))	N/A	N/A	N/A	
☐ EXAMINATION FEE (37 CFR 1.16(o), (p), or (q))	N/A	N/A	N/A	
TOTAL CLAIMS (37 CFR 1.16(i))	minus 20 =	*	X $ =	
INDEPENDENT CLAIMS (37 CFR 1.16(h))	minus 3 =	*	X $ =	
☐ APPLICATION SIZE FEE (37 CFR 1.16(s))	If the specification and drawings exceed 100 sheets of paper, the application size fee due is $310 ($155 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).			
☐ MULTIPLE DEPENDENT CLAIM PRESENT (37 CFR 1.16(j))				
* If the difference in column 1 is less than zero, enter "0" in column 2.			TOTAL	

APPLICATION AS AMENDED – PART II

		(Column 1)		(Column 2)	(Column 3)		
	12/17/2018	CLAIMS REMAINING AFTER AMENDMENT		HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA	RATE ($)	ADDITIONAL FEE ($)
AMENDMENT	Total (37 CFR 1.16(i))	* 2	Minus	** 20	= 0	X $100 =	0
	Independent (37 CFR 1.16(h))	* 1	Minus	***3	= 0	X $460 =	0
	☐ Application Size Fee (37 CFR 1.16(s))						
	☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))						
						TOTAL ADD'L FEE	0

		(Column 1)		(Column 2)	(Column 3)		
		CLAIMS REMAINING AFTER AMENDMENT		HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA	RATE ($)	ADDITIONAL FEE ($)
AMENDMENT	Total (37 CFR 1.16(i))	*	Minus	**	=	X $ =	
	Independent (37 CFR 1.16(h))	*	Minus	***	=	X $ =	
	☐ Application Size Fee (37 CFR 1.16(s))						
	☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))						
						TOTAL ADD'L FEE	

* If the entry in column 1 is less than the entry in column 2, write "0" in column 3.
** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20".
*** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3".
The "Highest Number Previously Paid For" (Total or Independent) is the highest number found in the appropriate box in column 1.

SLIE
NICOL D. SCOTT

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
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P.O. Box 1450
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www.uspto.gov

NOTICE OF ALLOWANCE AND FEE(S) DUE

38327 7590 02/13/2019

Juan Carlos A. Marquez
Marquez Intellectual Property Law Office PLLC
1629 K Street, NW
Suite 300
Washington, DC 20006

EXAMINER
CHIEN, LUCY P

ART UNIT	PAPER NUMBER
2871	

DATE MAILED: 02/13/2019

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
15/271,422	09/21/2016	Yoshiaki NAKAYOSHI	HARU-0126	2686

TITLE OF INVENTION: LIQUID CRYSTAL DISPLAY DEVICE, DISPLAY DEVICE AND MANUFACTURING METHOD THEREOF

APPLN. TYPE	ENTITY STATUS	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	UNDISCOUNTED	$1000	$0.00	$0.00	$1000	05/13/2019

THE APPLICATION IDENTIFIED ABOVE HAS BEEN EXAMINED AND IS ALLOWED FOR ISSUANCE AS A PATENT. PROSECUTION ON THE MERITS IS CLOSED. THIS NOTICE OF ALLOWANCE IS NOT A GRANT OF PATENT RIGHTS. THIS APPLICATION IS SUBJECT TO WITHDRAWAL FROM ISSUE AT THE INITIATIVE OF THE OFFICE OR UPON PETITION BY THE APPLICANT. SEE 37 CFR 1.313 AND MPEP 1308.

THE ISSUE FEE AND PUBLICATION FEE (IF REQUIRED) MUST BE PAID WITHIN THREE MONTHS FROM THE MAILING DATE OF THIS NOTICE OR THIS APPLICATION SHALL BE REGARDED AS ABANDONED. THIS STATUTORY PERIOD CANNOT BE EXTENDED. SEE 35 U.S.C. 151. THE ISSUE FEE DUE INDICATED ABOVE DOES NOT REFLECT A CREDIT FOR ANY PREVIOUSLY PAID ISSUE FEE IN THIS APPLICATION. IF AN ISSUE FEE HAS PREVIOUSLY BEEN PAID IN THIS APPLICATION (AS SHOWN ABOVE), THE RETURN OF PART B OF THIS FORM WILL BE CONSIDERED A REQUEST TO REAPPLY THE PREVIOUSLY PAID ISSUE FEE TOWARD THE ISSUE FEE NOW DUE.

HOW TO REPLY TO THIS NOTICE:

I. Review the ENTITY STATUS shown above. If the ENTITY STATUS is shown as SMALL or MICRO, verify whether entitlement to that entity status still applies.

If the ENTITY STATUS is the same as shown above, pay the TOTAL FEE(S) DUE shown above.

If the ENTITY STATUS is changed from that shown above, on PART B - FEE(S) TRANSMITTAL, complete section number 5 titled "Change in Entity Status (from status indicated above)".

For purposes of this notice, small entity fees are 1/2 the amount of undiscounted fees, and micro entity fees are 1/2 the amount of small entity fees.

II. PART B - FEE(S) TRANSMITTAL, or its equivalent, must be completed and returned to the United States Patent and Trademark Office (USPTO) with your ISSUE FEE and PUBLICATION FEE (if required). If you are charging the fee(s) to your deposit account, section "4b" of Part B - Fee(s) Transmittal should be completed and an extra copy of the form should be submitted. If an equivalent of Part B is filed, a request to reapply a previously paid issue fee must be clearly made, and delays in processing may occur due to the difficulty in recognizing the paper as an equivalent of Part B.

III. All communications regarding this application must give the application number. Please direct all communications prior to issuance to Mail Stop ISSUE FEE unless advised to the contrary.

IMPORTANT REMINDER: Maintenance fees are due in utility patents issuing on applications filed on or after Dec. 12, 1980. It is patentee's responsibility to ensure timely payment of maintenance fees when due. More information is available at www.uspto.gov/PatentMaintenanceFees.

PART B - FEE(S) TRANSMITTAL

Complete and send this form, together with applicable fee(s), by mail or fax, or via EFS-Web.

By mail, send to: Mail Stop ISSUE FEE
Commissioner for Patents
P.O. Box 1450
Alexandria, Virginia 22313-1450

By fax, send to: (571)-273-2885

INSTRUCTIONS: This form should be used for transmitting the ISSUE FEE and PUBLICATION FEE (if required). Blocks 1 through 5 should be completed where appropriate. All further correspondence including the Patent, advance orders and notification of maintenance fees will be mailed to the current correspondence address as indicated unless corrected below or directed otherwise in Block 1, by (a) specifying a new correspondence address; and/or (b) indicating a separate "FEE ADDRESS" for maintenance fee notifications.

CURRENT CORRESPONDENCE ADDRESS (Note: Use Block 1 for any change of address)

38327 7590 02/13/2019
Juan Carlos A. Marquez
Marquez Intellectual Property Law Office PLLC
1629 K Street, NW
Suite 300
Washington, DC 20006

Note: A certificate of mailing can only be used for domestic mailings of the Fee(s) Transmittal. This certificate cannot be used for any other accompanying papers. Each additional paper, such as an assignment or formal drawing, must have its own certificate of mailing or transmission.

Certificate of Mailing or Transmission

I hereby certify that this Fee(s) Transmittal is being deposited with the United States Postal Service with sufficient postage for first class mail in an envelope addressed to the Mail Stop ISSUE FEE address above, or being transmitted to the USPTO via EFS-Web or by facsimile to (571) 273-2885, on the date below.

(Typed or printed name)
(Signature)
(Date)

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
15/271,422	09/21/2016	Yoshiaki NAKAYOSHI	HARU-0126	2686

TITLE OF INVENTION: LIQUID CRYSTAL DISPLAY DEVICE, DISPLAY DEVICE AND MANUFACTURING METHOD THEREOF

APPLN. TYPE	ENTITY STATUS	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	UNDISCOUNTED	$1000	$0.00	$0.00	$1000	05/13/2019

EXAMINER	ART UNIT	CLASS-SUBCLASS
CHIEN, LUCY P	2871	349-141000

1. Change of correspondence address or indication of "Fee Address" (37 CFR 1.363).

❑ Change of correspondence address (or Change of Correspondence Address form PTO/SB/122) attached.

❑ "Fee Address" indication (or "Fee Address" Indication form PTO/SB/47; Rev 03-09 or more recent) attached. **Use of a Customer Number is required.**

2. For printing on the patent front page, list
(1) The names of up to 3 registered patent attorneys or agents OR, alternatively,
(2) The name of a single firm (having as a member a registered attorney or agent) and the names of up to 2 registered patent attorneys or agents. If no name is listed, no name will be printed.

1 _____
2 _____
3 _____

3. ASSIGNEE NAME AND RESIDENCE DATA TO BE PRINTED ON THE PATENT (print or type)

PLEASE NOTE: Unless an assignee is identified below, no assignee data will appear on the patent. If an assignee is identified below, the document must have been previously recorded, or filed for recordation, as set forth in 37 CFR 3.11 and 37 CFR 3.81(a). Completion of this form is NOT a substitute for filing an assignment.

(A) NAME OF ASSIGNEE (B) RESIDENCE: (CITY and STATE OR COUNTRY)

Please check the appropriate assignee category or categories (will not be printed on the patent) : ❑ Individual ❑ Corporation or other private group entity ❑ Government

4a. Fees submitted: ❑Issue Fee ❑Publication Fee (if required) ❑Advance Order - # of Copies _____

4b. Method of Payment: *(Please first reapply any previously paid fee shown above)*

❑ Electronic Payment via EFS-Web ❑ Enclosed check ❑ Non-electronic payment by credit card (Attach form PTO-2038)

❑ The Director is hereby authorized to charge the required fee(s), any deficiency, or credit any overpayment to Deposit Account No. _____

5. **Change in Entity Status** (from status indicated above)

❑ Applicant certifying micro entity status. See 37 CFR 1.29

❑ Applicant asserting small entity status. See 37 CFR 1.27

❑ Applicant changing to regular undiscounted fee status.

NOTE: Absent a valid certification of Micro Entity Status (see forms PTO/SB/15A and 15B), issue fee payment in the micro entity amount will not be accepted at the risk of application abandonment.
NOTE: If the application was previously under micro entity status, checking this box will be taken to be a notification of loss of entitlement to micro entity status.
NOTE: Checking this box will be taken to be a notification of loss of entitlement to small or micro entity status, as applicable.

NOTE: This form must be signed in accordance with 37 CFR 1.31 and 1.33. See 37 CFR 1.4 for signature requirements and certifications.

Authorized Signature _____ Date _____

Typed or printed name _____ Registration No. _____

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
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P.O. Box 1450
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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
15/271,422	09/21/2016	Yoshiaki NAKAYOSHI	HARU-0126	2686

38327 7590 02/13/2019

Juan Carlos A. Marquez
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1629 K Street, NW
Suite 300
Washington, DC 20006

EXAMINER	
CHIEN, LUCY P	
ART UNIT	**PAPER NUMBER**
2871	

DATE MAILED: 02/13/2019

Determination of Patent Term Adjustment under 35 U.S.C. 154 (b)
(Applications filed on or after May 29, 2000)

The Office has discontinued providing a Patent Term Adjustment (PTA) calculation with the Notice of Allowance.

Section 1(h)(2) of the AIA Technical Corrections Act amended 35 U.S.C. 154(b)(3)(B)(i) to eliminate the requirement that the Office provide a patent term adjustment determination with the notice of allowance. See Revisions to Patent Term Adjustment, 78 Fed. Reg. 19416, 19417 (Apr. 1, 2013). Therefore, the Office is no longer providing an initial patent term adjustment determination with the notice of allowance. The Office will continue to provide a patent term adjustment determination with the Issue Notification Letter that is mailed to applicant approximately three weeks prior to the issue date of the patent, and will include the patent term adjustment on the patent. Any request for reconsideration of the patent term adjustment determination (or reinstatement of patent term adjustment) should follow the process outlined in 37 CFR 1.705.

Any questions regarding the Patent Term Extension or Adjustment determination should be directed to the Office of Patent Legal Administration at (571)-272-7702. Questions relating to issue and publication fee payments should be directed to the Customer Service Center of the Office of Patent Publication at 1-(888)-786-0101 or (571)-272-4200.

OMB Clearance and PRA Burden Statement for PTOL-85 Part B

The Paperwork Reduction Act (PRA) of 1995 requires Federal agencies to obtain Office of Management and Budget approval before requesting most types of information from the public. When OMB approves an agency request to collect information from the public, OMB (i) provides a valid OMB Control Number and expiration date for the agency to display on the instrument that will be used to collect the information and (ii) requires the agency to inform the public about the OMB Control Number's legal significance in accordance with 5 CFR 1320.5(b).

The information collected by PTOL-85 Part B is required by 37 CFR 1.311. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 30 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, Virginia 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, Virginia 22313-1450. Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

Privacy Act Statement

The Privacy Act of 1974 (P.L. 93-579) requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether disclosure of these records is required by the Freedom of Information Act.
2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.
3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.
4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).
5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.
6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).
7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.
8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspection or an issued patent.
9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

Notice of Allowability	Application No. 15/271,422	Applicant(s) NAKAYOSHI et al.	
	Examiner LUCY P CHIEN	Art Unit 2871	AIA Status No

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☑ This communication is responsive to 12/17/2018.
   ☐ A declaration(s)/affidavit(s) under **37 CFR 1.130(b)** was/were filed on _____.

2. ☐ An election was made by the applicant in response to a restriction requirement set forth during the interview on _____; the restriction requirement and election have been incorporated into this action.

3. ☑ The allowed claim(s) is/are 17-18 . As a result of the allowed claim(s), you may be eligible to benefit from the **Patent Prosecution Highway** program at a participating intellectual property office for the corresponding application. For more information, please see **http://www.uspto.gov/patents/init_events/pph/index.jsp** or send an inquiry to **PPHfeedback@uspto.gov.**

4. ☑ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

   Certified copies:

   a) ☑ All b) ☐ Some *c) ☐ None of the:

   1. ☑ Certified copies of the priority documents have been received.
   2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
   3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

   * Certified copies not received: _____ .

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file areply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

5. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
   ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____ .

   Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).

6. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☐ Notice of References Cited (PTO-892)
2. ☐ Information Disclosure Statements (PTO/SB/08), Paper No./Mail Date _____.
3. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material _____.
4. ☐ Interview Summary (PTO-413), Paper No./Mail Date. _____.
5. ☐ Examiner's Amendment/Comment
6. ☑ Examiner's Statement of Reasons for Allowance
7. ☐ Other _____.

/LUCY P CHIEN/
Primary Examiner, Art Unit 2871

Notice of Pre-AIA or AIA Status

1. The present application is being examined under the pre-AIA first to invent provisions.

Reasons for Allowance

2. The following is an examiner's statement of reasons for allowance:

Claim 17,18 are allowed.

Regarding Claim 17,

Min et al discloses (Fig. 1 and Fig. 2) a liquid crystal display device, comprising: a first substrate (11); a second substrate; a liquid crystal layer between the first substrate and the second substrate, containing liquid crystal molecules (column 4, lines 1-8); a gate line (31) and a drain line (36); a pixel electrode (21) and a counter electrode (12) disposed between the first substrate and the liquid crystal layer; a gate insulation layer (15) formed on the gate line; a insulation layer (20) disposed between the first substrate (11) and the liquid crystal layer; a switching element (where 13 is located), connected to the gate line, including a first electrode (19a) connected to the drain line and a second electrode (19b) connected to the pixel electrode (21); wherein the liquid crystal layer is driven by an electric field generated between the pixel electrode and the counter electrode, and wherein the pixel electrode (21) is formed between the liquid crystal layer and the insulation layer (20), and wherein the counter electrode (12) is a planar shape, and the pixel electrode comprises a slit having a first portion (21),

Min et al does not disclose an organic insulation layer and the first portion is not parallel with the gate line and the drain line.

Lyu et al discloses (abstract) an organic insulation layer (110).

Kaneko et al discloses (Fig. 2) first portion is not parallel with the gate line and the drain line.

The prior art does not disclose nor would it be obvious to one of ordinary skill in the art to include another reference to disclose wherein the counter electrode is connected to the common layer via a through hole within the organic insulation layer.

Claim 18 depends on Claim 17, therefore is allowable.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Conclusion

3. Any inquiry concerning this communication or earlier communications from the examiner should be directed to LUCY P CHIEN whose telephone number is (571)272-8579. The examiner can normally be reached on 9AM-5PM PST M-TH.

Examiner interviews are available via telephone, in-person, and video conferencing using a USPTO supplied web-based collaboration tool. To schedule an interview, applicant is encouraged to use the USPTO Automated Interview Request (AIR) at http://www.uspto.gov/interviewpractice.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Michael Caley can be reached on 571-272-2286. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/LUCY P CHIEN/
Primary Examiner, Art Unit 2871

Issue Classification	Application/Control No.	Applicant(s)/Patent Under Reexamination
	15/271,422	NAKAYOSHI et al.
	Examiner	**Art Unit**
	LUCY P CHIEN	2871

CPC								
Symbol							**Type**	**Version**
G02F	/	1	/	134309			F	2013-01-01
G02F	/	1	/	136213			I	2013-01-01
G02F	/	1	/	136286			I	2013-01-01
G02F	/	1	/	1343			I	2013-01-01
G02F	/	1	/	133345			I	2013-01-01
G02F	/	1	/	13439			I	2013-01-01
G02F	/	1	/	1368			I	2013-01-01
G02F	/	2201	/	40			A	2013-01-01
G02F	/	1	/	13			A	2013-01-01
G02F	/	2201	/	123			A	2013-01-01

CPC Combination Sets								
Symbol					**Type**	**Set**	**Ranking**	**Version**
	/		/					

NONE		Total Claims Allowed:	
(Assistant Examiner)	(Date)	2	
/LUCY P CHIEN/ Primary Examiner, Art Unit 2871	06 February 2019	O.G. Print Claim(s)	O.G. Print Figure
(Primary Examiner)	(Date)	17	54

U.S. Patent and Trademark Office — Part of Paper No.: 20190206

Issue Classification	Application/Control No.	Applicant(s)/Patent Under Reexamination
	15/271,422	NAKAYOSHI et al.
	Examiner	**Art Unit**
	LUCY P CHIEN	2871

INTERNATIONAL CLASSIFICATION				
CLAIMED				
G02F1/13	/	1	/	13
G02F1/1333	/	1	/	1333
G02F1/1343	/	1	/	1343
G02F1/1362	/	1	/	1362
G02F1/1368	/	1	/	1368

NON-CLAIMED				
	/		/	

US ORIGINAL CLASSIFICATION	
CLASS	**SUBCLASS**

CROSS REFERENCES(S)						
CLASS	**SUBCLASS (ONE SUBCLASS PER BLOCK)**					

NONE		Total Claims Allowed:	
(Assistant Examiner)	(Date)	2	
/LUCY P CHIEN/ Primary Examiner, Art Unit 2871	06 February 2019	O.G. Print Claim(s)	O.G. Print Figure
(Primary Examiner)	(Date)	17	54

U.S. Patent and Trademark Office — Part of Paper No.: 20190206

Issue Classification	Application/Control No.	Applicant(s)/Patent Under Reexamination
	15/271,422	NAKAYOSHI et al.
	Examiner	**Art Unit**
	LUCY P CHIEN	2871

☐ Claims renumbered in the same order as presented by applicant ☐ CPA ☐ T.D. ☐ R.1.47

CLAIMS

Final	Original	Final	Original	Final	Original	Final	Original	Final	Original	Final	Original	Final	Original	Final	Original
	1		10		19		28								
	2		11		20		29								
	3		12		21		30								
	4		13		22										
	5		14		23										
	6		15		24										
	7		16		25										
	8	1	17		26										
	9	2	18		27										

NONE		**Total Claims Allowed:**	
(Assistant Examiner)	(Date)	2	
/LUCY P CHIEN/ Primary Examiner, Art Unit 2871	06 February 2019	O.G. Print Claim(s)	O.G. Print Figure
(Primary Examiner)	(Date)	17	54

U.S. Patent and Trademark Office Part of Paper No.: 20190206

Search Notes	Application/Control No.	Applicant(s)/Patent Under Reexamination
	15/271,422	NAKAYOSHI et al.
	Examiner	Art Unit
	LUCY P CHIEN	2871

CPC - Searched*		
Symbol	Date	Examiner
G02F 1/134309	02/06/2019	LC
G02F 1/133345	02/06/2019	LC
G02F 1/1343	02/06/2019	LC

CPC Combination Sets - Searched*		
Symbol	Date	Examiner

US Classification - Searched*			
Class	Subclass	Date	Examiner

* See search history printout included with this form or the SEARCH NOTES box below to determine the scope of the search.

Search Notes		
Search Notes	Date	Examiner
see search notes from EAST	02/06/2019	LC
G02F 1/134309	02/06/2019	LC
G02F 1/133345	02/06/2019	LC
G02F 1/1343	02/06/2019	LC

/LUCY P CHIEN/ Primary Examiner, Art Unit 2871	/LUCY P CHIEN/ Primary Examiner, Art Unit 2871

Search Notes	Application/Control No.	Applicant(s)/Patent Under Reexamination
	15/271,422	NAKAYOSHI et al.
	Examiner	Art Unit
	LUCY P CHIEN	2871

Interference Search			
US Class/CPC Symbol	US Subclass/CPC Group	Date	Examiner
349	141	02/06/2019	LC
G02F 1/134309		02/06/2019	LC
G02F 1/133345		02/06/2019	LC
G02F 1/1343		02/06/2019	LC

/LUCY P CHIEN/ Primary Examiner, Art Unit 2871	/LUCY P CHIEN/ Primary Examiner, Art Unit 2871

EAST Search History

EAST Search History (Prior Art)

< This search history is empty>

EAST Search History (Interference)

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L9	1863	349/141.ccls.	USPAT	OR	OFF	2019/02/06 18:58
L8	432	G02F1/1343.cpc.	USPAT	OR	OFF	2019/02/06 18:57
L7	2059	G02F1/133345.cpc.	USPAT	OR	OFF	2019/02/06 18:30
L6	2578	G02F1/134309.cpc.	USPAT	OR	OFF	2019/02/06 18:05
L5	672	L1 and L2 and L3 and L4	USPAT	OR	OFF	2019/02/06 17:51
L4	20330	(counter common) adj3 electrode.clm.	USPAT	OR	OFF	2019/02/06 17:51
L3	233590	organic.clm.	USPAT	OR	OFF	2019/02/06 17:51
L2	17268	pixel adj3 electrode.clm.	USPAT	OR	OFF	2019/02/06 17:51
L1	67508	liquid adj3 crystal.clm.	USPAT	OR	OFF	2019/02/06 17:51

2/ 6/ 2019 6:58:49 PM
C:\ Users\ lchien\ Documents\ EAST\ Workspaces\ 15271422.wsp

Bibliographic Data

Application No: 15/271,422

Foreign Priority claimed: (•) Yes ( ) No

35 USC 119 (a-d) conditions met: [✓] Yes [ ] No [ ] Met After Allowance

Verified and Acknowledged: /LUCY P CHIEN/ Examiner's Signature | Initials

Title: LIQUID CRYSTAL DISPLAY DEVICE, DISPLAY DEVICE AND MANUFACTURING METHOD THEREOF

FILING or 371(c) DATE	CLASS	GROUP ART UNIT	ATTORNEY DOCKET NO.
09/21/2016	349	2871	HARU-0126
RULE			

APPLICANTS

Japan Display Inc., Tokyo, JAPAN

Panasonic Liquid Crystal Display Co., Ltd., Hyogo-ken, JAPAN

INVENTORS

Yoshiaki NAKAYOSHI Ooamishirasato, JAPAN

Kazuhiko YANAGAWA Mobara, JAPAN

CONTINUING DATA

This application is a CON of 14942120 11/16/2015 PAT 9488880

14942120 is a CON of 14708348 05/11/2015 PAT 9213204

14708348 is a CON of 14285006 05/22/2014 PAT 9086600

14285006 is a CON of 13927539 06/26/2013 PAT 8760609

13927539 is a CON of 13650203 10/12/2012 PAT 8493522

13650203 is a CON of 13364092 02/01/2012 PAT 8310641

13364092 is a CON of 12926735 12/07/2010 PAT 8248549

12926735 is a CON of 12292728 11/25/2008 PAT 7872696

12292728 is a DIV of 11976884 10/29/2007 PAT 7605876

11976884 is a DIV of 11409076 04/24/2006 PAT 7307673

11409076 is a DIV of 11211574 08/26/2005 PAT 7423701

11211574 is a DIV of 10237911 09/10/2002 PAT 6970222

FOREIGN APPLICATIONS

JAPAN 2001-317149 10/15/2001

IF REQUIRED, FOREIGN LICENSE GRANTED**

09/30/2016

STATE OR COUNTRY

JAPAN

ADDRESS

Juan Carlos A. Marquez
Marquez Intellectual Property Law Office PLLC
1629 K Street, NW
Suite 300
Washington, DC 20006
UNITED STATES

FILING FEE RECEIVED

$1,600

PART B - FEE(S) TRANSMITTAL

Complete and send this form, together with applicable fee(s), by mail or fax, or via EFS-Web.

By mail, send to: Mail Stop ISSUE FEE
Commissioner for Patents
P.O. Box 1450
Alexandria, Virginia 22313-1450

By fax, send to: (571)-273-2885

INSTRUCTIONS: This form should be used for transmitting the ISSUE FEE and PUBLICATION FEE (if required). Blocks 1 through 5 should be completed where appropriate. All further correspondence including the Patent, advance orders and notification of maintenance fees will be mailed to the current correspondence address as indicated unless corrected below or directed otherwise in Block 1, by (a) specifying a new correspondence address; and/or (b) indicating a separate "FEE ADDRESS" for maintenance fee notifications.

CURRENT CORRESPONDENCE ADDRESS (Note: Use Block 1 for any change of address)

38327 7590 02/13/2019
Juan Carlos A. Marquez
Marquez Intellectual Property Law Office PLLC
1629 K Street, NW
Suite 300
Washington, DC 20006

Note: A certificate of mailing can only be used for domestic mailings of the Fee(s) Transmittal. This certificate cannot be used for any other accompanying papers. Each additional paper, such as an assignment or formal drawing, must have its own certificate of mailing or transmission.

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I hereby certify that this Fee(s) Transmittal is being deposited with the United States Postal Service with sufficient postage for first class mail in an envelope addressed to the Mail Stop ISSUE FEE address above, or being transmitted to the USPTO via EFS-Web or by facsimile to (571) 273-2885, on the date below.

(Typed or printed name)
(Signature)
(Date)

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
15/271,422	09/21/2016	Yoshiaki NAKAYOSHI	HARU-0126	2686

TITLE OF INVENTION: LIQUID CRYSTAL DISPLAY DEVICE, DISPLAY DEVICE AND MANUFACTURING METHOD THEREOF

APPLN. TYPE	ENTITY STATUS	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	UNDISCOUNTED	$1000	$0.00	$0.00	$1000	05/13/2019

EXAMINER	ART UNIT	CLASS-SUBCLASS
CHIEN, LUCY P	2871	349-141000

1. Change of correspondence address or indication of "Fee Address" (37 CFR 1.363).

☐ Change of correspondence address (or Change of Correspondence Address form PTO/SB/122) attached.

☐ "Fee Address" indication (or "Fee Address" Indication form PTO/SB/47; Rev 03-09 or more recent) attached. **Use of a Customer Number is required.**

2. For printing on the patent front page, list
(1) The names of up to 3 registered patent attorneys or agents OR, alternatively,
(2) The name of a single firm (having as a member a registered attorney or agent) and the names of up to 2 registered patent attorneys or agents. If no name is listed, no name will be printed.

1 Juan Carlos A. Marquez
2 Marquez IP Law Office, PLLC
3

3. ASSIGNEE NAME AND RESIDENCE DATA TO BE PRINTED ON THE PATENT (print or type)

PLEASE NOTE: Unless an assignee is identified below, no assignee data will appear on the patent. If an assignee is identified below, the document must have been previously recorded, or filed for recordation, as set forth in 37 CFR 3.11 and 37 CFR 3.81(a). Completion of this form is NOT a substitute for filing an assignment.

(A) NAME OF ASSIGNEE	(B) RESIDENCE: (CITY and STATE OR COUNTRY)
JAPAN DISPLAY INC.	TOKYO, JAPAN
PANASONIC LIQUID CRYSTAL DISPLAY CO., LTD.	HYOGO-KEN, JAPAN

Please check the appropriate assignee category or categories (will not be printed on the patent) : ☐ Individual ☒ Corporation or other private group entity ☐ Government

4a. Fees submitted: ☒ Issue Fee ☐ Publication Fee (if required) ☐ Advance Order - # of Copies _____

4b. Method of Payment: *(Please first reapply any previously paid fee shown above)*

☒ Electronic Payment via EFS-Web ☐ Enclosed check ☐ Non-electronic payment by credit card (Attach form PTO-2038)

☒ The Director is hereby authorized to charge the required fee(s), any deficiency, or credit any overpayment to Deposit Account No. 60-155

5. **Change in Entity Status** (from status indicated above)

☐ Applicant certifying micro entity status. See 37 CFR 1.29

☐ Applicant asserting small entity status. See 37 CFR 1.27

☐ Applicant changing to regular undiscounted fee status.

NOTE: Absent a valid certification of Micro Entity Status (see forms PTO/SB/15A and 15B), issue fee payment in the micro entity amount will not be accepted at the risk of application abandonment.
NOTE: If the application was previously under micro entity status, checking this box will be taken to be a notification of loss of entitlement to micro entity status.
NOTE: Checking this box will be taken to be a notification of loss of entitlement to small or micro entity status, as applicable.

NOTE: This form must be signed in accordance with 37 CFR 1.31 and 1.33. See 37 CFR 1.4 for signature requirements and certifications.

Authorized Signature /juan.carlos.a.marquez/ Date May 7, 2019

Typed or printed name Juan Carlos A. Marquez Registration No. 34,072

Electronic Patent Application Fee Transmittal

Application Number:	15271422
Filing Date:	21-Sep-2016
Title of Invention:	LIQUID CRYSTAL DISPLAY DEVICE, DISPLAY DEVICE AND MANUFACTURING METHOD THEREOF
First Named Inventor/Applicant Name:	Yoshiaki NAKAYOSHI
Filer:	Juan Carlos A. Marquez/Lily Niu
Attorney Docket Number:	HARU-0126

Filed as Large Entity

Filing Fees for Utility under 35 USC 111(a)

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Basic Filing:				
Pages:				
Claims:				
Miscellaneous-Filing:				
Petition:				
Patent-Appeals-and-Interference:				
Post-Allowance-and-Post-Issuance:				
UTILITY APPL ISSUE FEE	1501	1	1000	1000

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Extension-of-Time:				
Miscellaneous:				
			Total in USD ($)	**1000**

Electronic Acknowledgement Receipt	
EFS ID:	35937123
Application Number:	15271422
International Application Number:	
Confirmation Number:	2686
Title of Invention:	LIQUID CRYSTAL DISPLAY DEVICE, DISPLAY DEVICE AND MANUFACTURING METHOD THEREOF
First Named Inventor/Applicant Name:	Yoshiaki NAKAYOSHI
Customer Number:	38327
Filer:	Juan Carlos A. Marquez/Lily Niu
Filer Authorized By:	Juan Carlos A. Marquez
Attorney Docket Number:	HARU-0126
Receipt Date:	07-MAY-2019
Filing Date:	21-SEP-2016
Time Stamp:	12:40:21
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	yes
Payment Type	CARD
Payment was successfully received in RAM	$1000
RAM confirmation Number	050719INTEFSW12410200
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Authorized User	
The Director of the USPTO is hereby authorized to charge indicated fees and credit any overpayment as follows:	

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Issue Fee Payment (PTO-85B)	HARU-0126-Issue_fee_form.pdf	146140 b0784bd80c473afbb5aee8ba87c30362f3516152	no	1
Warnings:					
Information:					
2	Fee Worksheet (SB06)	fee-info.pdf	30363 a7b0b338c3a62c1773fc3b07fa041b677233df1a	no	2
Warnings:					
Information:					
		Total Files Size (in bytes):	176503		

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New Applications Under 35 U.S.C. 111
If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.
National Stage of an International Application under 35 U.S.C. 371
If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.
New International Application Filed with the USPTO as a Receiving Office
If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

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www.uspto.gov

APPLICATION NO.	ISSUE DATE	PATENT NO.	ATTORNEY DOCKET NO.	CONFIRMATION NO.
15/271,422	06/25/2019	10330989	HARU-0126	2686

38327 7590 06/05/2019

Juan Carlos A. Marquez
Marquez Intellectual Property Law Office PLLC
1629 K Street, NW
Suite 300
Washington, DC 20006

ISSUE NOTIFICATION

The projected patent number and issue date are specified above.

Determination of Patent Term Adjustment under 35 U.S.C. 154 (b)
(application filed on or after May 29, 2000)

The Patent Term Adjustment is 300 day(s). Any patent to issue from the above-identified application will include an indication of the adjustment on the front page.

If a Continued Prosecution Application (CPA) was filed in the above-identified application, the filing date that determines Patent Term Adjustment is the filing date of the most recent CPA.

Applicant will be able to obtain more detailed information by accessing the Patent Application Information Retrieval (PAIR) WEB site (http://pair.uspto.gov).

Any questions regarding the Patent Term Extension or Adjustment determination should be directed to the Office of Patent Legal Administration at (571)-272-7702. Questions relating to issue and publication fee payments should be directed to the Application Assistance Unit (AAU) of the Office of Data Management (ODM) at (571)-272-4200.

APPLICANT(s) (Please see PAIR WEB site http://pair.uspto.gov for additional applicants):

Yoshiaki NAKAYOSHI, Ooamishirasato, JAPAN;
Japan Display Inc., Tokyo, JAPAN;
Kazuhiko YANAGAWA, Mobara, JAPAN;
Panasonic Liquid Crystal Display Co., Ltd., Hyogo-ken, JAPAN;

IR103 (Rev. 10/09)