

UNITED STATES PATENT AND TRADEMARK OFFICE

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BEFORE THE PATENT TRIAL AND APPEAL BOARD

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TIANMA MICROELECTRONICS CO. LTD.,  
Petitioner,

v.

JAPAN DISPLAY INC. and PANASONIC LIQUID  
CRYSTAL DISPLAY CO., LTD.,  
Patent Owner.

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IPR2021-01060  
Patent 10,330,989 B2

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Before JO-ANNE M. KOKOSKI, KRISTINA M. KALAN, and  
ELIZABETH M. ROESEL, *Administrative Patent Judges*.

KOKOSKI, *Administrative Patent Judge*.

DECISION  
Denying Institution of *Inter Partes* Review  
*35 U.S.C. § 314, 37 C.F.R. § 42.4*

## I. INTRODUCTION

Tianma Microelectronics Co. Ltd. (“Petitioner”) filed a Petition to institute an *inter partes* review of claims 1 and 2 (the “challenged claims”) of U.S. Patent No. 10,330,989 B2 (“the ’989 patent,” Ex. 1001). Paper 2 (“Pet.”). Japan Display Inc. and Panasonic Liquid Crystal Display Co., Ltd. (collectively, “Patent Owner”) filed a Preliminary Response. Paper 7 (“Prelim. Resp.”). With Board authorization, Petitioner filed a Reply to the Preliminary Response (“Reply,” Paper 8), and Patent Owner filed a Sur-reply to Petitioner’s Reply (“Sur-reply,” Paper 10).

Institution of an *inter partes* review is authorized by statute when “the information presented in the petition . . . and any response . . . shows that there is a reasonable likelihood that the petitioner would prevail with respect to at least 1 of the claims challenged in the petition.” 35 U.S.C. § 314 (2018); *see also* 37 C.F.R. § 42.4 (2021). For the reasons set forth below, we deny the Petition and do not institute an *inter partes* review.

### A. Real Parties in Interest

Each party identifies itself as the real party-in-interest. Pet. 99; Paper 6, 1.

### B. Related Matters

The parties indicate that, pursuant to the district court’s order (Ex. 1022), the ’989 patent is no longer at issue in *Japan Display Inc. v. Tianma Microelectronics Co. Ltd.*, No. 2:20-cv-00283 (E.D. Tex.). Paper 12, 1; Paper 14, 3; Ex. 1023.

### C. The ’989 Patent

The ’989 patent, titled “Liquid Crystal Display Device, Display Device and Manufacturing Method Thereof,” is directed to “an active matrix type liquid crystal display device which can reduce holding capacity for

holding lighting of pixels for a given time and feeding resistance thereof thus enhancing numerical aperture.” Ex. 1001, code (54), 1:49–53.

The ’989 patent describes a liquid crystal display device that includes: liquid crystal sandwiched between a first substrate and a second substrate; a plurality of gate lines arranged parallel to each other that extend in a first direction; a plurality of drain lines arranged parallel to each other that extend in a second direction that crosses the gate lines; a plurality of switching elements arranged at the crossing portions of the gate lines and the drain lines; pixel electrodes, driven by the switching elements, formed on an inner surface of the first substrate; and pixel regions formed of a plurality of pixel electrodes. *Id.* at 9:2–13. A reference electrode layer that is insulated by a first insulation layer is formed in between an electrode forming layer “which is constituted of the gate lines, the drain lines, the switching elements and the pixel electrodes including the pixel regions of the first substrate and the first substrate side.” *Id.* at 9:14–20. The electrode forming layer includes a gate insulation layer, a passivation layer, and the pixel electrode “in this order over the first insulation layer and further includes a capacitive electrode layer” that is “connected to the pixel electrodes between the first insulation layer and the passivation layer.” *Id.* at 9:28–33. “[H]olding capacities of the pixels are formed among the pixel electrodes, the reference electrode layer, and the capacitive electrode layer.” *Id.* at 9:34–36.

Figure 61 of the '989 patent is reproduced below.

*FIG. 61*

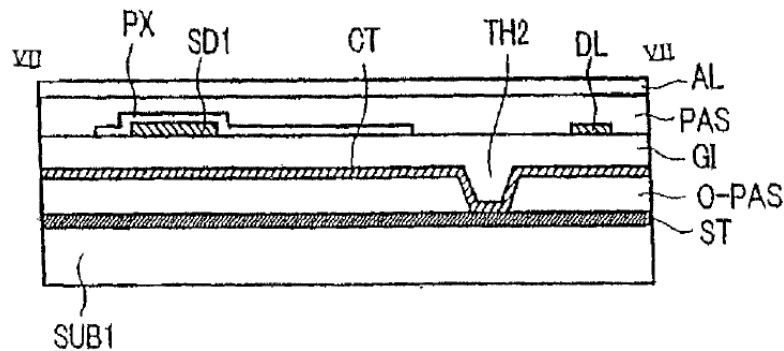


Figure 61 is a cross-section view of a portion of a modified liquid crystal display device described in the '989 patent. *Id.* at 39:41–45. Source electrode SD1 is formed over gate insulation layer GI, and pixel electrode PX overlaps source electrode SD1. *Id.* at 39:47–51. Counter electrode CT is formed over organic insulation layer O-PAS and is connected to reference electrode layer ST via through hole TH2, forming a holding capacity between counter electrode CT and pixel electrode PX. *Id.* at 39:51–55.

The '989 patent teaches that, “[d]ue to such a constitution, the numerical aperture of the pixels can be enhanced” and, because “the area of the reference electrode layer is large, the feeding resistance can be reduced.” *Id.* at 9:37–40. The '989 patent further teaches that the capacitive electrode layer can be formed over the gate insulation layer, and the capacitive electrode layer is connected to the reference electrode layer via through holes which penetrate the gate insulation layer. *Id.* at 10:32–35. In this way, “the holding capacity formed between the reference electrode and the pixel electrodes can be adjusted by changing the area of the capacitive electrode layer connected to the reference electrode layer.” *Id.* at 10:36–39.

*D. Illustrative Claim*

Petitioner challenges claims 1 and 2 of the '989 patent. Pet. 1. Claim 1, the only independent challenged claim, is illustrative of the claimed subject matter and is reproduced below.

1. A liquid crystal display device, comprising:
  - [a] a first substrate;
  - [b] a second substrate;
  - [c] a liquid crystal layer between the first substrate and the second substrate, containing liquid crystal molecules;
  - [d] a gate line and a drain line;
  - [e] a pixel electrode and a counter electrode disposed between the first substrate and the liquid crystal layer;
  - [f] a gate insulation layer formed on the gate line; and
  - [g] an organic insulation layer disposed between the first substrate and the liquid crystal layer,
  - [h] wherein the liquid crystal layer is driven by an electric field generated between the pixel electrode and the counter electrode,
  - [i] wherein the pixel electrode is formed between the liquid crystal layer and the organic insulation layer,
  - [j] wherein the counter electrode is a planar shape, and
  - [k] the pixel electrode comprises a slit having a first portion, and the first portion is not parallel with the gate line and the drain line,
  - [l] wherein the counter electrode is connected to a common layer,
  - [m] wherein the organic insulation layer is formed between the counter electrode and the first substrate, and
  - [n] wherein the counter electrode is connected to the common layer via a through hole within the organic insulation layer.

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