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Lee et al.

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(54) **THIN FILM TRANSISTOR ARRAY PANEL AND A METHOD FOR MANUFACTURING THE SAME**

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(*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 476 days.

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Primary Examiner—Sarah Song

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(74) Attorney, Agent, or Firm—F. Chau & Associates, LLC

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(30) **Foreign Application Priority Data**

(57) **ABSTRACT**

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A thin film transistor array panel includes a substrate; a plurality of gate lines that are formed on the substrate; a plurality of data lines that intersect the gate lines; a plurality of thin film transistors that are connected to the gate lines and the data lines; a plurality of color filters that are formed on upper parts of the gate lines, the data lines, and the thin film transistors; a common electrode that is formed on the color filters and that includes a transparent conductor; a passivation layer that is formed on an upper part of the common electrode; and a plurality of pixel electrodes that are formed on an upper part of the passivation layer and that are connected to a drain electrode of each of the thin film transistors.

(51) **Int. Cl.**

G02F 1/136 (2006.01)

(52) **U.S. Cl.** 349/43

(58) **Field of Classification Search** 349/42,
349/43, 139, 141, 143, 148

See application file for complete search history.

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17 Claims, 14 Drawing Sheets

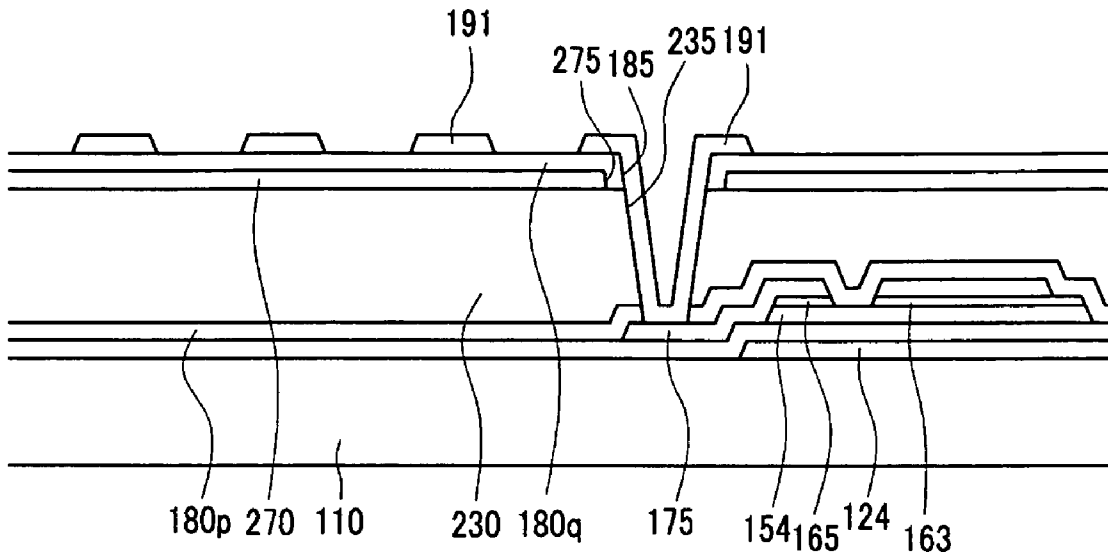


FIG. 1

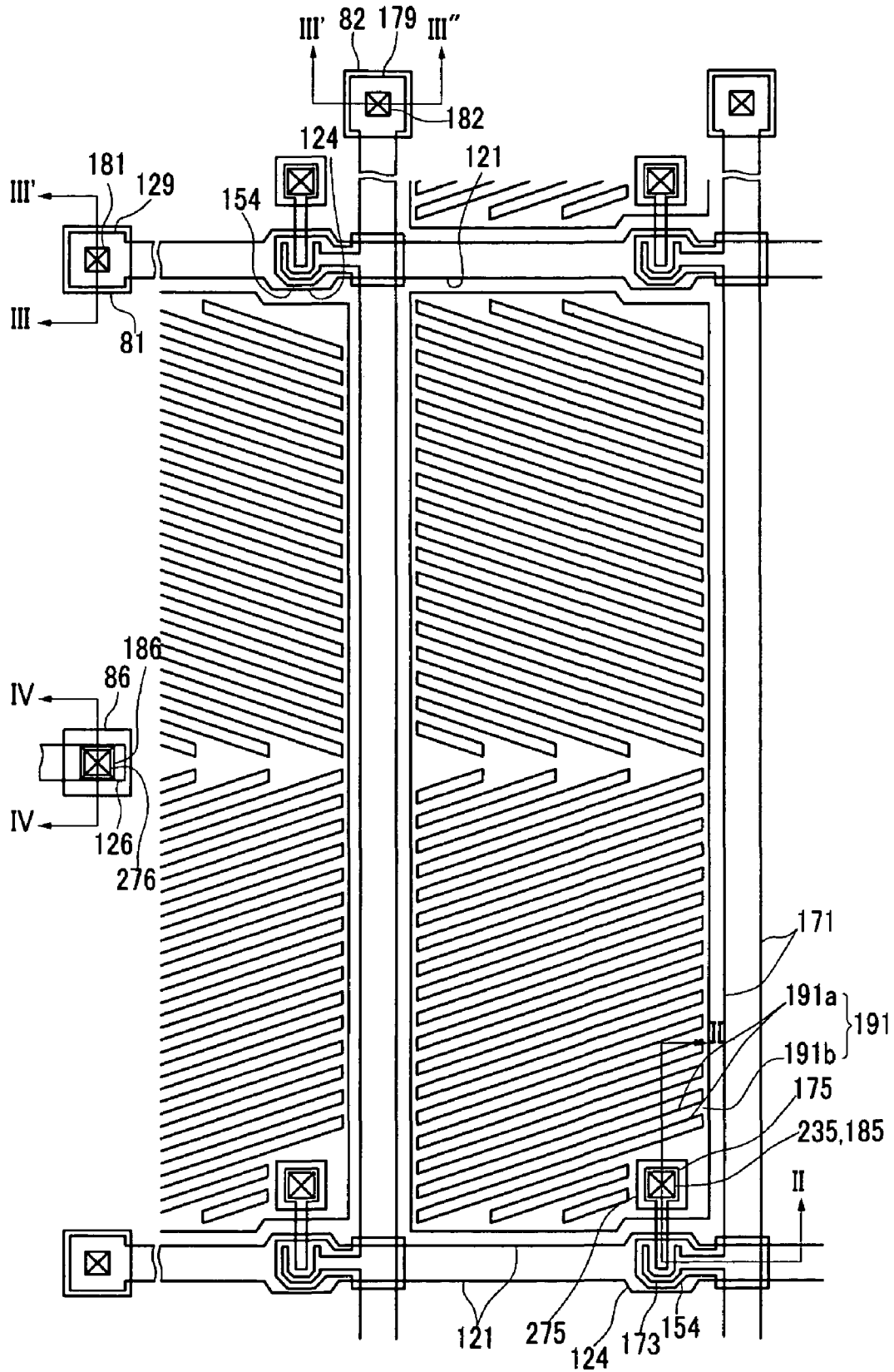


FIG.2

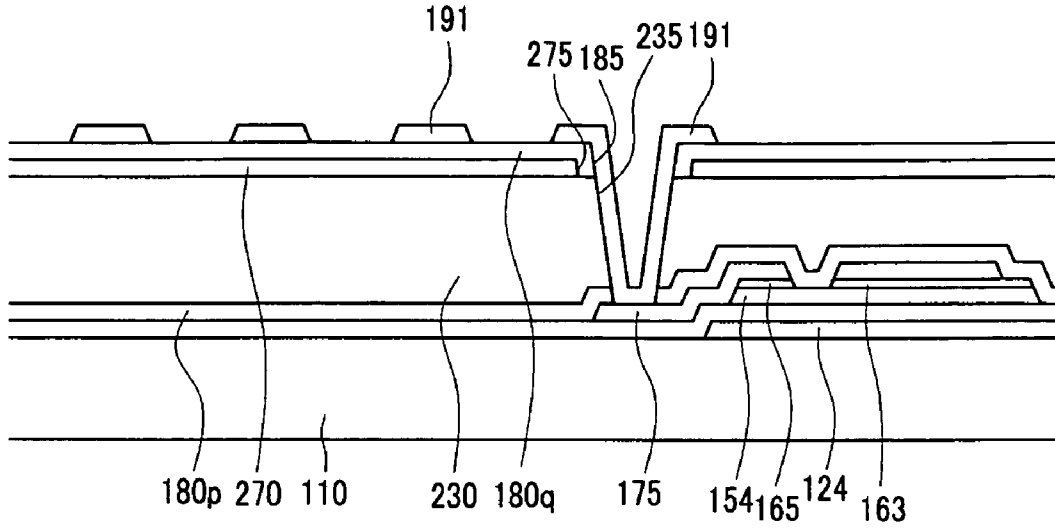


FIG.3

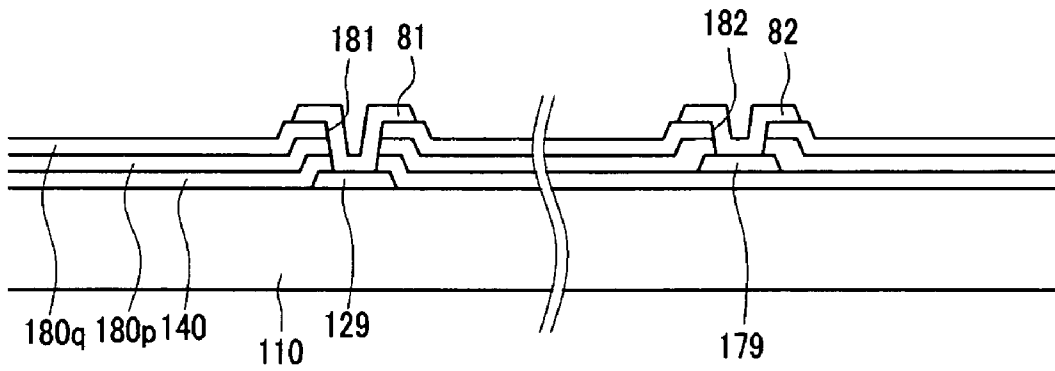


FIG.4

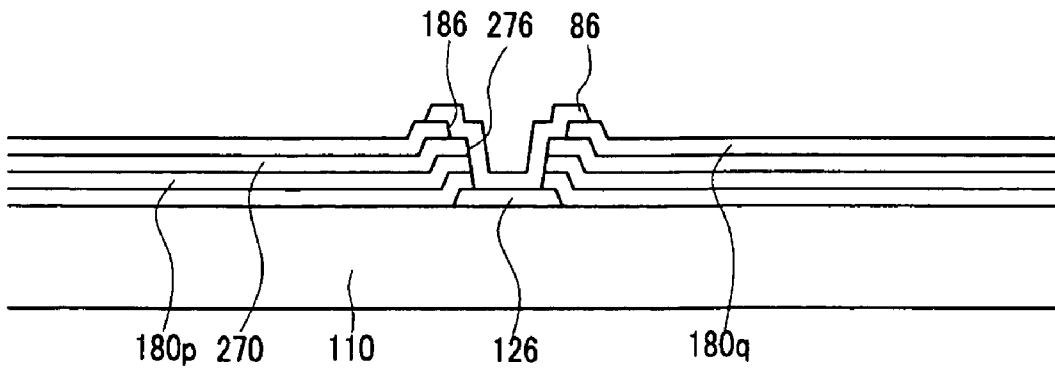


FIG. 5

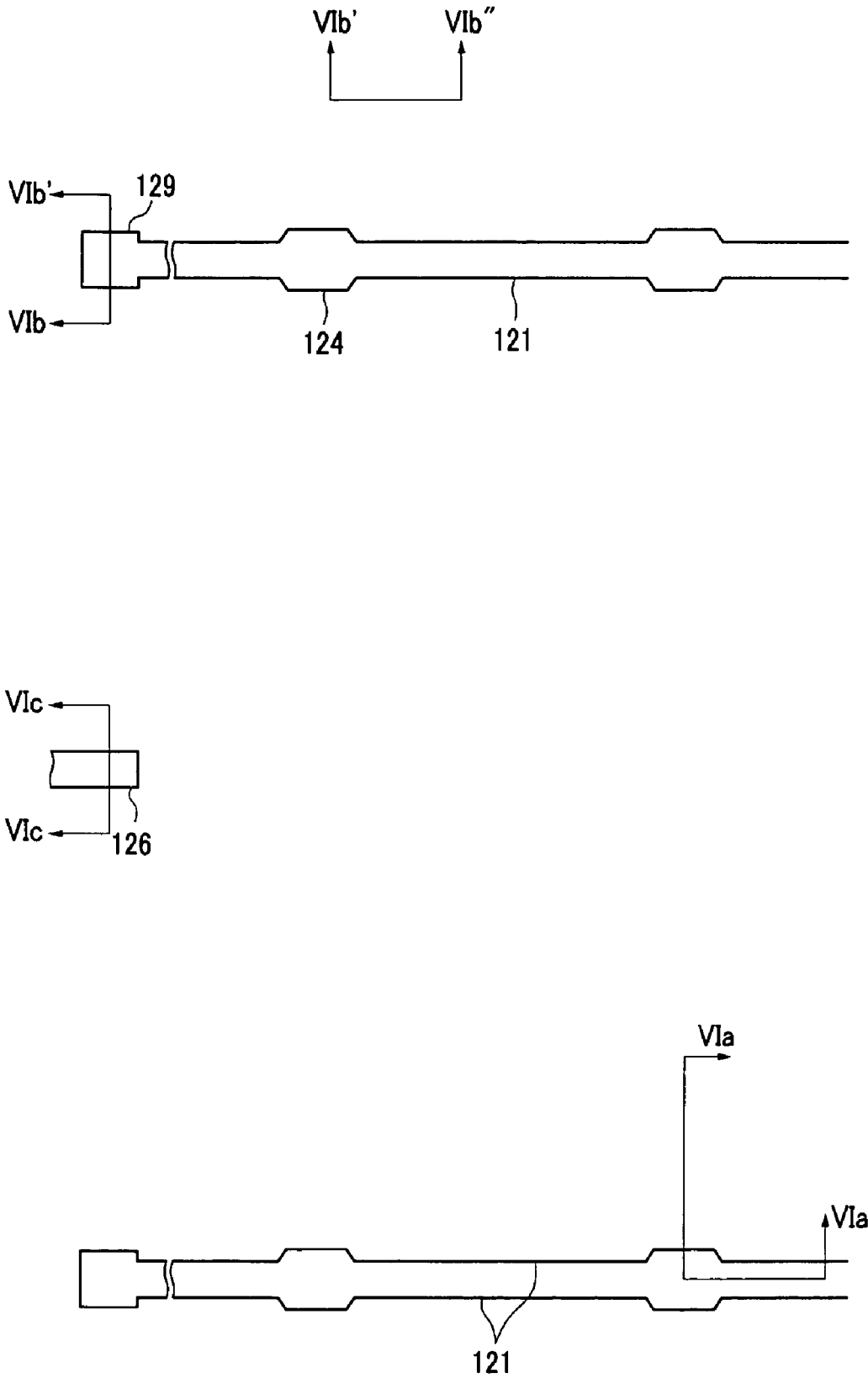


FIG.6A

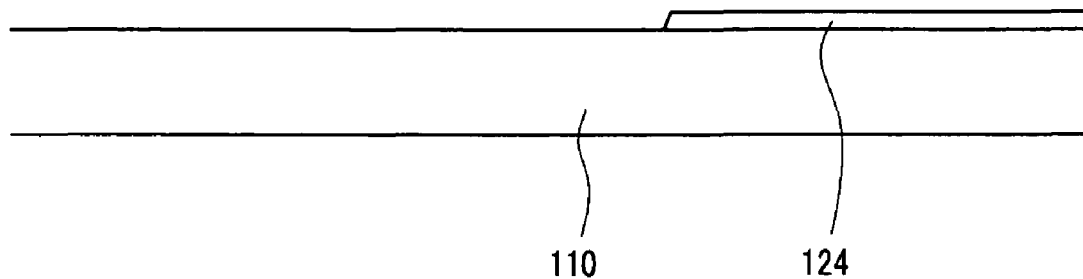


FIG.6B

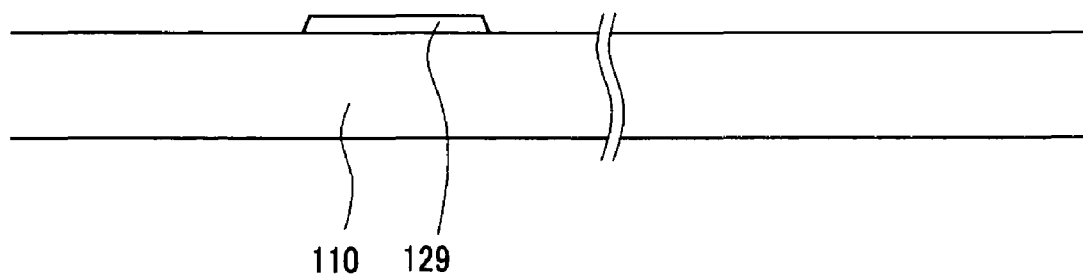
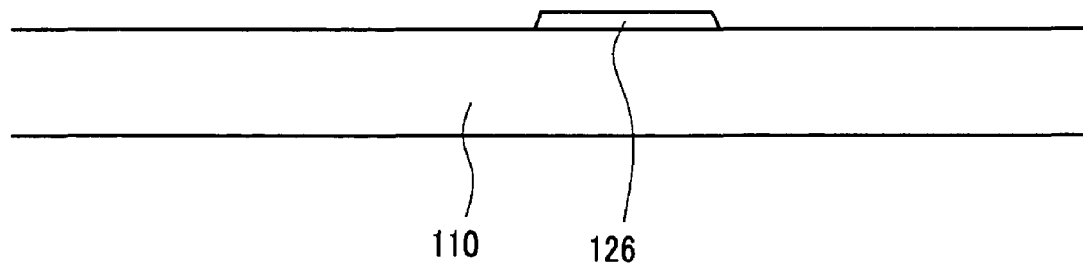


FIG.6C



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