Petitioner's Oral Hearing Demonstratives

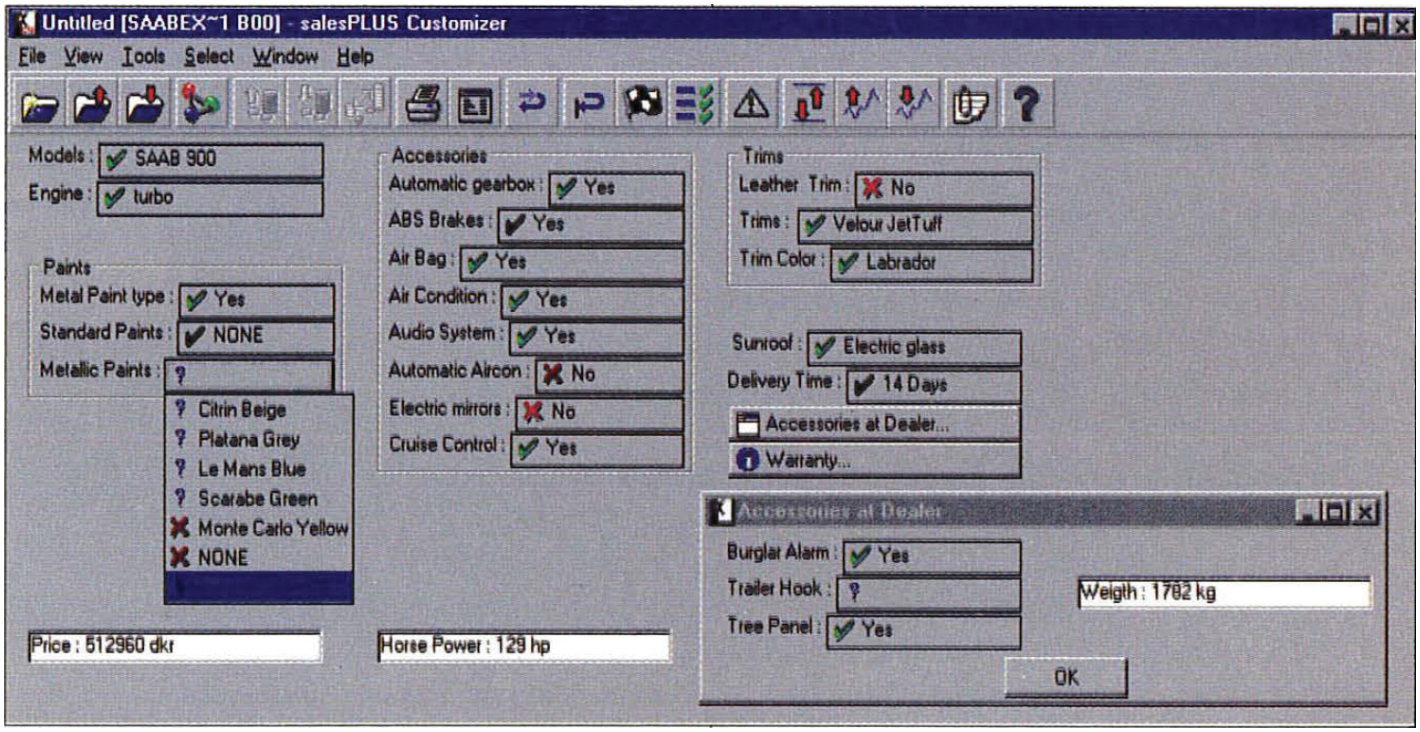
Configit A/S (Petitioner)
v.
Versata Development Group, Inc. (Patent Owner)

Case Nos. IPR2021-01055
U.S. Patent No. 6,836,766

Demonstrative Exhibit

FISH.

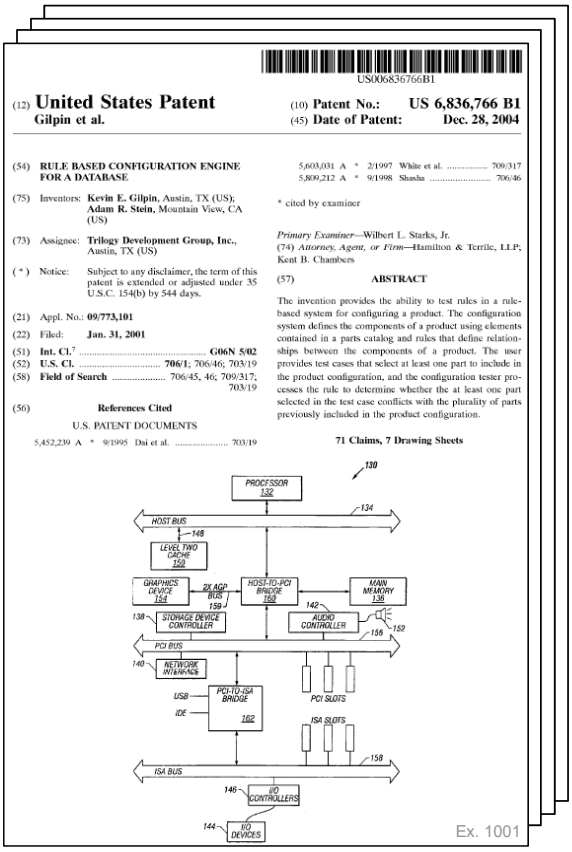
Prior Art: Product Configurators



Ex. 1006, 6; Ex. 1002 ¶¶ 36-37; Pet., 9

The ’766 Patent

The ’766 Patent



US006836766B1

(12) **United States Patent**
Gilpin et al.

(10) **Patent No.: US 6,836,766 B1**
(45) **Date of Patent: Dec. 28, 2004**

(54) **RULE BASED CONFIGURATION ENGINE FOR A DATABASE**

(75) Inventors: **Kevin E. Gilpin**, Austin, TX (US); **Adam R. Stein**, Mountain View, CA (US)

(73) Assignee: **Trilogy Development Group, Inc.**, Austin, TX (US)

(*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 544 days.

(21) Appl. No.: **09/773,101**

(22) Filed: **Jan. 31, 2001**

(51) **Int. Cl.**[7] **G06N 5/02**
(52) **U.S. Cl.** **706/1**; 706/46; 703/19
(58) **Field of Search** 706/45, 46; 709/317; 703/19

(56) **References Cited**

U.S. PATENT DOCUMENTS

5,452,239 A * 9/1995 Dai et al. 703/19
5,603,031 A * 2/1997 White et al. 709/317
5,809,212 A * 9/1998 Shasha 706/46

* cited by examiner

Primary Examiner—Wilbert L. Starks, Jr.
(74) *Attorney, Agent, or Firm*—Hamilton & Terrile, LLP; Kent B. Chambers

(57) **ABSTRACT**

The invention provides the ability to test rules in a rule-based system for configuring a product. The configuration system defines the components of a product using elements contained in a parts catalog and rules that define relationships between the components of a product. The user provides test cases that select at least one part to include in the product configuration, and the configuration tester processes the rule to determine whether the at least one part selected in the test case conflicts with the plurality of parts previously included in the product configuration.

71 Claims, 7 Drawing Sheets

Ex. 1001

1. A method of using a computer system to test a product configuration for configuration errors, wherein the product configuration is stored as electronic data in a computer system for generating product configurations, the computer system including at least one rule defining a relationship between at least two parts, the product configuration including a plurality of parts, the method comprising:

entering a test case into the computer system to detect configuration errors in the product configuration, wherein the test case includes data to change the product configuration;

processing the test case with the computer system in accordance with the at least one rule to detect whether the change in the product configuration, as a result of processing the test case in accordance with the at least one rule, produced a configuration error in the product configuration; and

generating explanation data with the computer system to provide an explanation of any detected configuration error in the product configuration.

Ex. 1001, cl. 1

The ’766 Patent

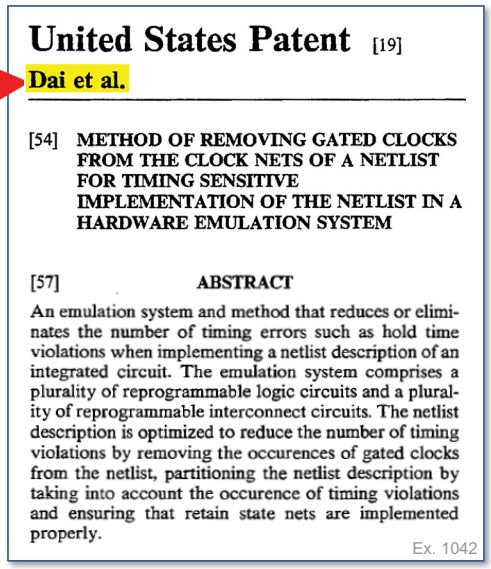
The examiner did not consider the correct prior art

The following is an Examiner's statement of reasons for allowance:

The cited prior art taken alone or in combination fails to teach the claimed invention of a rule based configuration engine, as claimed by Applicant. Specifically, independent claims 1, 14, 27, and 70 disclose the use of a computer system to test an electronically stored product configuration for errors.

The closest prior art of Dai et al (U.S. Patent Number 5,542,239; dated 19 September 1995; class 703; subclass 019) teaches the implementation of a netlist but fails to teach or suggest the use of a computer system to test an electronically stored product configuration for errors. To the extent that this feature is not found in the prior art cited by Examiner, the present case is held allowable over the art of record.

Ex. 1011 at 205



United States Patent [19]

Dai et al.

[54] **METHOD OF REMOVING GATED CLOCKS FROM THE CLOCK NETS OF A NETLIST FOR TIMING SENSITIVE IMPLEMENTATION OF THE NETLIST IN A HARDWARE EMULATION SYSTEM**

[57] **ABSTRACT**

An emulation system and method that reduces or eliminates the number of timing errors such as hold time violations when implementing a netlist description of an integrated circuit. The emulation system comprises a plurality of reprogrammable logic circuits and a plurality of reprogrammable interconnect circuits. The netlist description is optimized to reduce the number of timing violations by removing the occurences of gated clocks from the netlist, partitioning the netlist description by taking into account the occurence of timing violations and ensuring that retain state nets are implemented properly.

Ex. 1042

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