



[54] METHOD OF REMOVING GATED CLOCKS FROM THE CLOCK NETS OF A NETLIST FOR TIMING SENSITIVE IMPLEMENTATION OF THE NETLIST IN A HARDWARE EMULATION SYSTEM

[58] Field of Search 364/578-580, 364/232.3, 927.81; 371/16.2, 22.1, 22.2, 23, 27; 340/825.22, 825.06, 825.88, 825.89, 825.83, 825.84; 307/465, 468, 219, 303; 357/45; 395/500; 365/201; 370/13, 14, 17

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[21] Appl. No.: 844

[57] ABSTRACT

An emulation system and method that reduces or eliminates the number of timing errors such as hold time violations when implementing a netlist description of an integrated circuit. The emulation system comprises a plurality of reprogrammable logic circuits and a plurality of reprogrammable interconnect circuits. The netlist description is optimized to reduce the number of timing violations by removing the occurrences of gated clocks from the netlist, partitioning the netlist description by taking into account the occurrence of timing violations and ensuring that retain state nets are implemented properly.

[22] Filed: Feb. 26, 1993

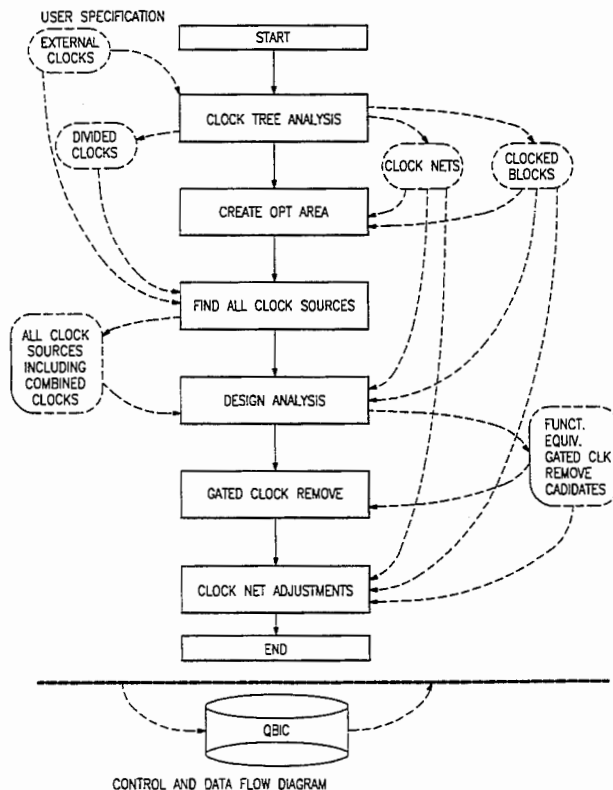
Related U.S. Application Data

[63] Continuation-in-part of Ser. No. 13,025, Jan. 29, 1993, abandoned.

[51] Int. Cl.⁶ G06G 7/48; G06F 17/00

[52] U.S. Cl. 364/578; 364/580; 371/222

2 Claims, 78 Drawing Sheets



CONTROL AND DATA FLOW DIAGRAM

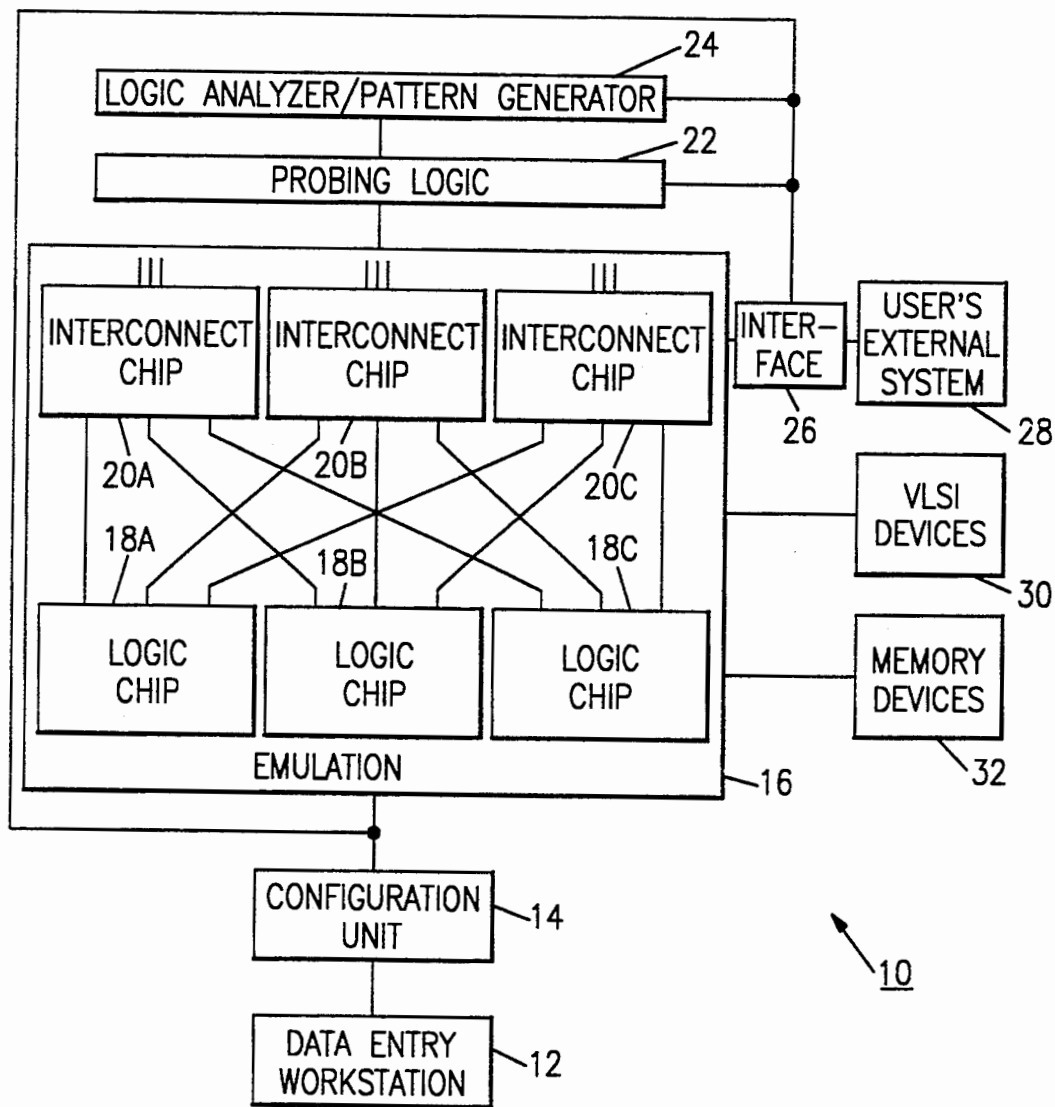


FIG. 1

CONNECTIONS TO EXTERNAL SIGNALS

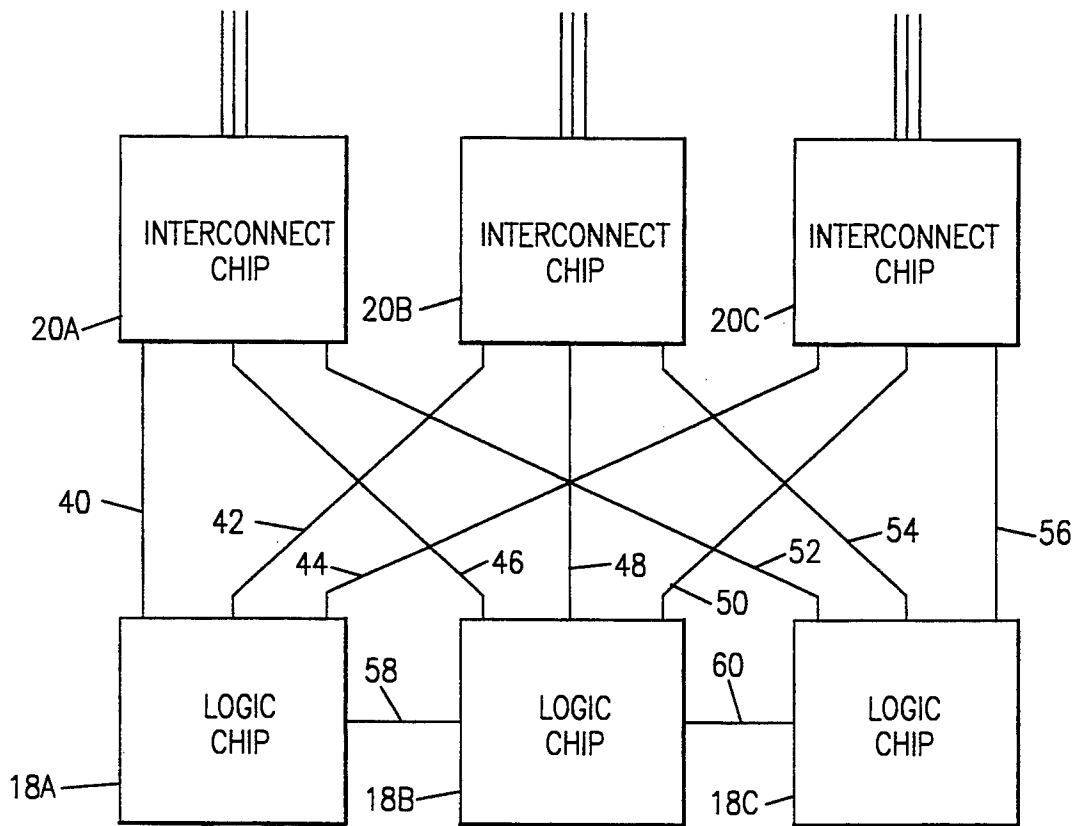
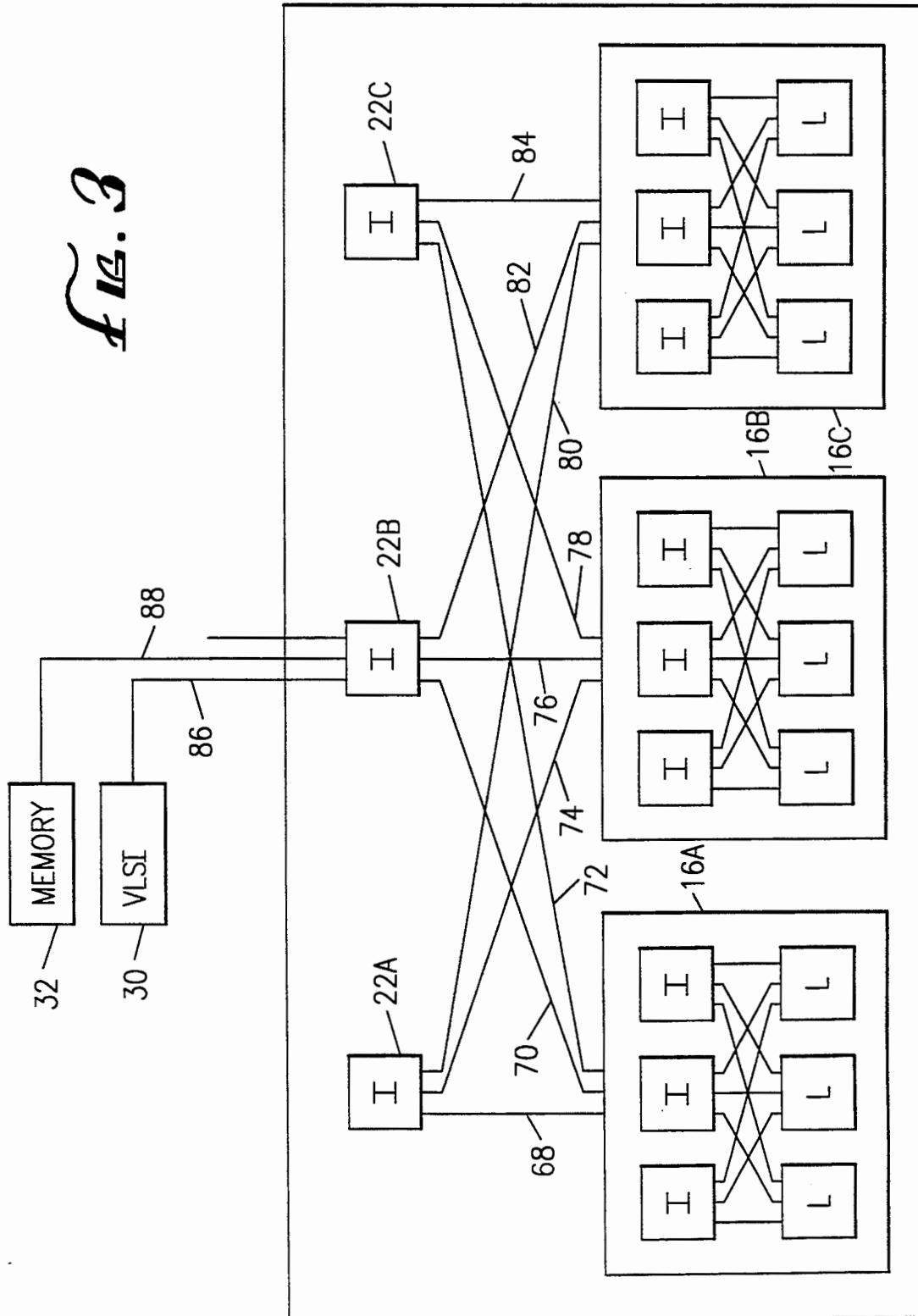


FIG. 2

FIG. 3



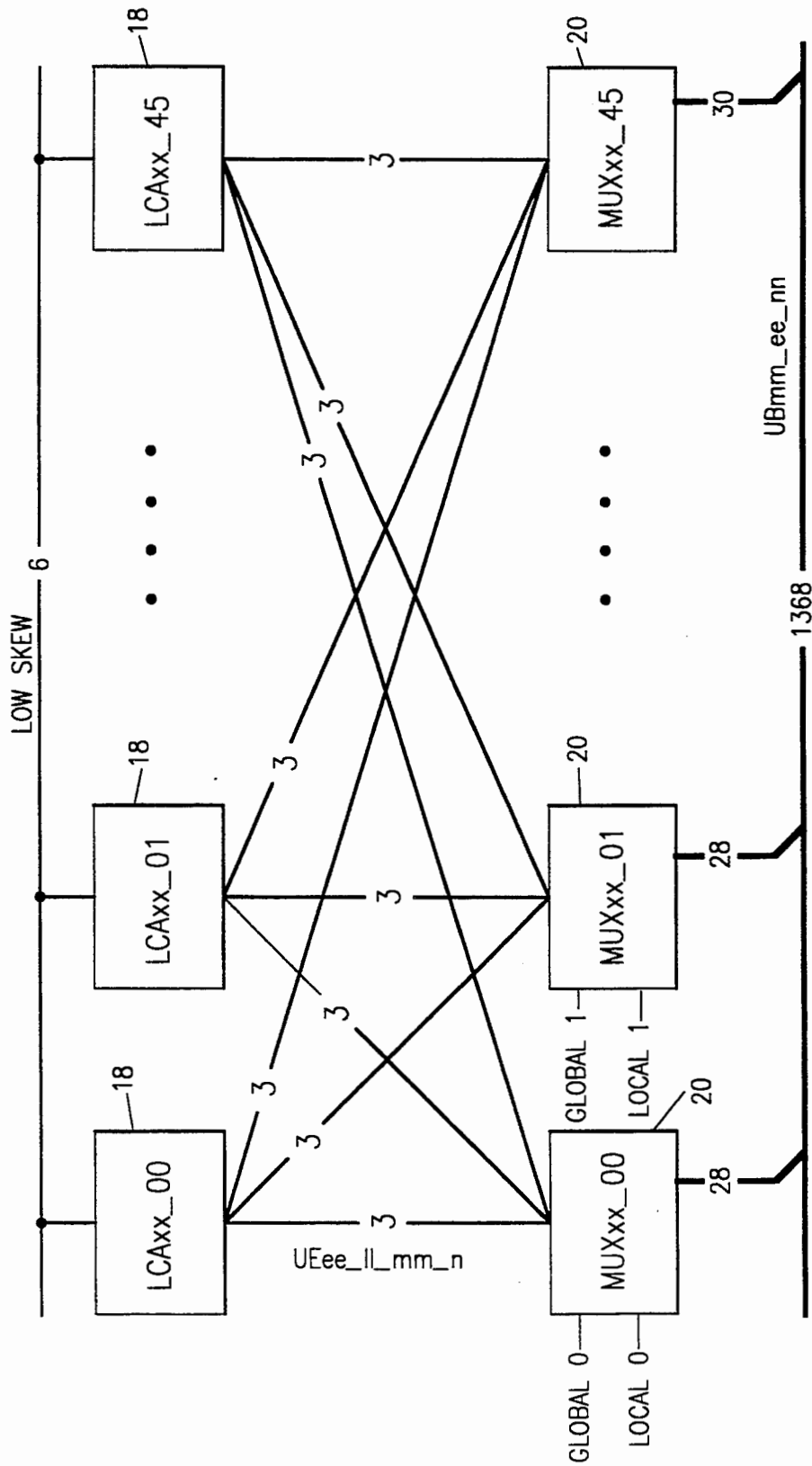


FIG. 4

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