COMPUTER

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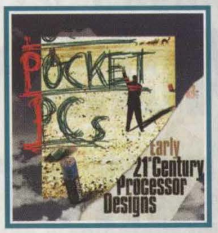

While transaction processing and Web servers dominate the high-end computing market, multimedia and DSP applications are beginning to prevail in the desktop and mobile-computing markets. These applications exhibit behavioral characteristics that are quite different from traditional general-purpose applications and require a new set of design constraints, such as very specialized performance at very low power and cost. This special issue captures some of these exciting trends in processor architecture.

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NEXT MONTH

Software Engineering on Internet Time

BPA INTERNATIONAL

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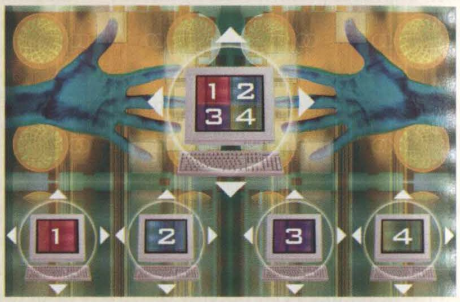
Itsy: Stretching the Bounds of Mobile Computing

A prototype pocket computer that has enough processing power and memory capacity to run cycle-hungry applications such as continuous-speech recognition and real-time MPEG-1 movie decoding has proved to be a useful experimental tool for interesting applications, systems work, and power studies.



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The advent of fast, power-thrifty microprocessors has made possible pocket-size computers with performance approaching that of desktop PCs. This new class of mobile computers enables applications and user-interface modalities not feasible with traditional personal digital assistants and cell phones, while placing new demands on batteries and power management. We built Compaq's Itsy pocket computer research prototype to explore the possibilities, demands, and limitations of mobile computing.

Our primary hardware goals were to attain high performance with minimal power consumption, size, and weight. At the same time, we needed a rich feature set to support user-interface and applications research and the flexibility to easily add new capabilities. To meet these goals, we used daughtercards to provide Itsy with comprehensive expansion capability. Fine-grain hardware control supports flexible power management and monitoring. Developers can use the Linux operating system with extensions for a flash file system, resource sharing, and power management to rapidly prototype operating system extensions and new applications. Itsy has sufficient processing power and memory capacity to run cycle-hungry applications such as continuous speech recognition, a full-fledged Java virtual machine, and real-time MPEG-1 movie decoding.

HARDWARE

We began our hardware effort by constructing 75 systems that we used to start software development.[1] The experience we gained in building and using these systems influenced our subsequent design, Itsy v2. Figure 1 shows this design's general architecture, and Table 1 lists its primary specifications.

Our design focused on two goals: packing maximum performance into a unit that people can comfortably carry all day in a pocket or purse and enabling easy customization and extension of the system hardware and software. Itsy is only slightly larger than a credit card, but it incorporates these other desirable features. Criteria such as cost or suitability for volume manufacturing, which are critical for commercial products, played no significant role.

A small system's battery and display are generally its largest and heaviest components, so they establish a lower bound on the system's size and weight. For Itsy, we selected a lithium-ion cell just large enough to provide a full day of intermittent use, and the smallest available LCD with sufficient resolution for a rich graphical interface.

We ruthlessly excluded any features or components that would bloat the system. For example, version 1 users wanted a thumbwheel encoder, a cursor button, a good speaker, and a stylus slot, but because all four of these features would not fit within our space budget, we excluded the stylus slot. Similar considerations led us to omit a bulky stereo headphone jack and codec in favor of a smaller monaural headset jack and a monaural codec that includes a touch-screen controller. Finally, a radio transceiver was clearly desirable, but we found no obvious best choice to include in the base system. Therefore, we relegated experimental radios to the daughtercard or serial interfaces. As a result of these choices, the complete Itsy is only 70 percent larger in volume than it would be if it contained only the battery and display.

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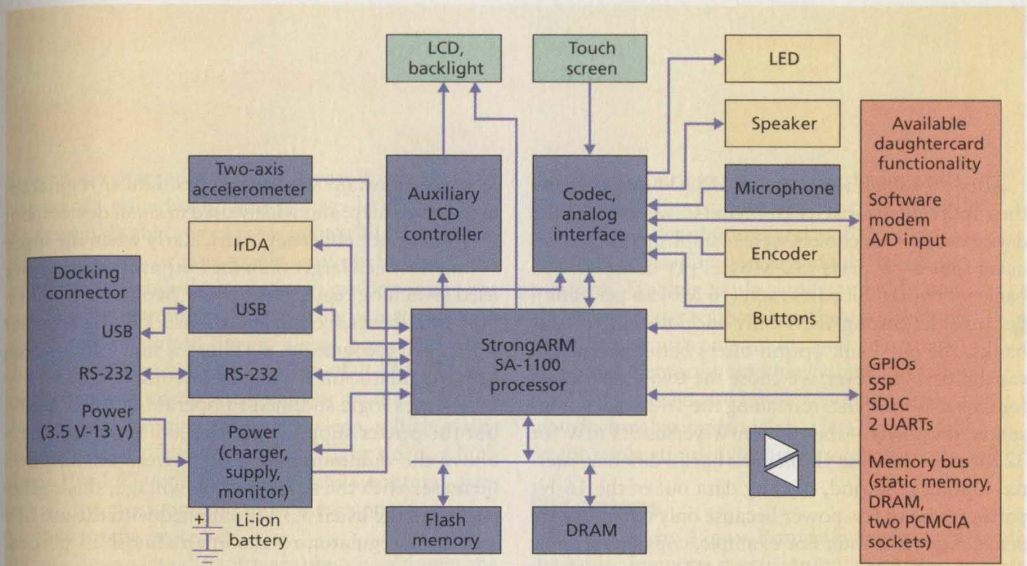

Figure 1. Itsy v2 architecture. Most of the hardware is implemented on the motherboard (depicted in blue). The LCD and the touch screen attach to the motherboard via dedicated connectors. Other parts of the hardware (shown in yellow) are implemented on a separate flexible circuit board. A daughtercard connector is available to interface with additional hardware. Daughtercards can use any of the features listed in the red box.

Processor

The StrongARM SA-1100 is a low-power 32-bit microprocessor that implements the ARM instruction set.[2,3] This processor was a clear choice because its integer performance approaches that of desktop processors, but it uses an order of magnitude less power. It also provides a useful collection of peripheral devices, as well as power-saving features that researchers can exploit. To minimize energy use, the StrongARM supports software-controllable clock frequency and two low-power modes: idle and sleep. In idle mode, the clock to the processor core is gated off, saving power due to the CMOS circuit technology, while the rest of the chip remains powered and all peripherals remain enabled. In sleep mode, most of the processor is unpowered, and only the real-time clock and the wake-up circuit remain enabled. Optionally, the system clock can remain enabled for faster wake-up.

Display

In contrast to the usual power-saving passive-matrix displays developers commonly choose for small systems, Itsy's LCD has some particularly useful characteristics. Its 0.18-mm pixel pitch is 25 to 30 percent smaller than the typical pitch of small matrix displays, permitting dense text and crisp graphics. Its multiline addressing technology provides higher contrast than is typical of a passive display. Finally, the LCD's built-in 1-bit-per-pixel memory and a programmable-logic-device (PLD) auxiliary controller make it possible to display a static monochrome image while the processor is in sleep mode.

Memory

The most frequent complaint from Itsy v1 prototype users was the limitation of having only 4 Mbytes of flash memory, so we started the v2 motherboard design with the memory system. As Figure 2 shows, we chose a micro-ball-grid array package for the flash instead of a peripheral lead package. Although the micro-BGA calls for a more complicated assembly process, it offers three times the mounting density. We chose the motherboard width to allow dense tiling of the flash across the board's full width. We arranged the DRAMs on the opposite side to match the flash tiling. Itsy v2 has twice as much DRAM and eight times as much flash as Itsy v1, with only a 3 percent increase in board area.

Table 1. Itsy v2 specifications (without daughtercard).

Component or characteristic	Specification
Processor	StrongARM SA-1100 (59 MHz–191 MHz)*
Dynamic RAM (DRAM)	32 Mbytes (50 ns, extended data out)
Flash memory	32 Mbytes (90 ns)
Processor-core voltage	1.5 V or 1.23 V (selectable)
Main voltage	3.05 V
LCD	320 × 200 pixels, 15 gray levels
Battery	Rechargeable Li-ion (2.2 W × h)
Size	118 mm × 65 mm × 16 mm
Weight	130 gm

*The processor's manual guarantees operation up to a 191-MHz core frequency at 1.5 V, but all Itsy systems built to date function correctly at 206 MHz and even higher.

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After choosing the number of DRAM chips (4) and their individual capacity (64 Mbits), we selected the device width. Our choices were to implement one bank using four 8-bit parts (32 Mbytes per bank) or two banks of two 16-bit parts each (16 Mbytes per bank). Because the StrongARM only supports up to four banks, the one-bank option offers better expansion capabilities. However, we chose the two-bank design for two reasons. First, refreshing the 16-bit parts consumes less power—about 5.2 mW versus 9.5 mW for 32 Mbytes—because 16-bit parts have a different internal topology. Second, reading data out of the 16-bit parts consumes less power because only two parts are active instead of four. For example, copying memory using eight-word bursts at 206 MHz requires about 490 mW rather than 630 mW.

Power system

Our DRAM selection demonstrates how we used architectural decisions and component selection to stretch battery life. However, to make the best use of limited battery energy, we had to consider both power supply and consumption.

Because battery voltage varies widely during use, the design needs voltage regulators to provide the system with constant supply voltages. Linear regulators are small, cheap, and widely used in small devices, but they have poor efficiency, particularly when the input voltage is much larger than the output. Therefore, we used switching regulators for our two main supplies. However, because clean audio was a key requirement for speech recognition, we chose a small, low-noise, linear regulator for the analog circuitry.

Itsy uses logic specified to operate at 3.3 ± 0.3 V, but the power supply is set to 3.05 V, only slightly above the minimum. Because power consumption increases with the square of the voltage, this reduction from the usual 3.3 V, combined with the use of a switching regulator, results in an almost 15 percent power savings. Although a lower system voltage reduces noise margins, test systems have operated reliably at as low as 2.7 V, indicating that this design point was a reasonable trade-off.

Power-saving mechanisms

These power strategies were necessary but not sufficient, so we developed additional hardware features that allow the software to make the best use of available energy. The hardware does not automatically disable external peripherals when the processor enters

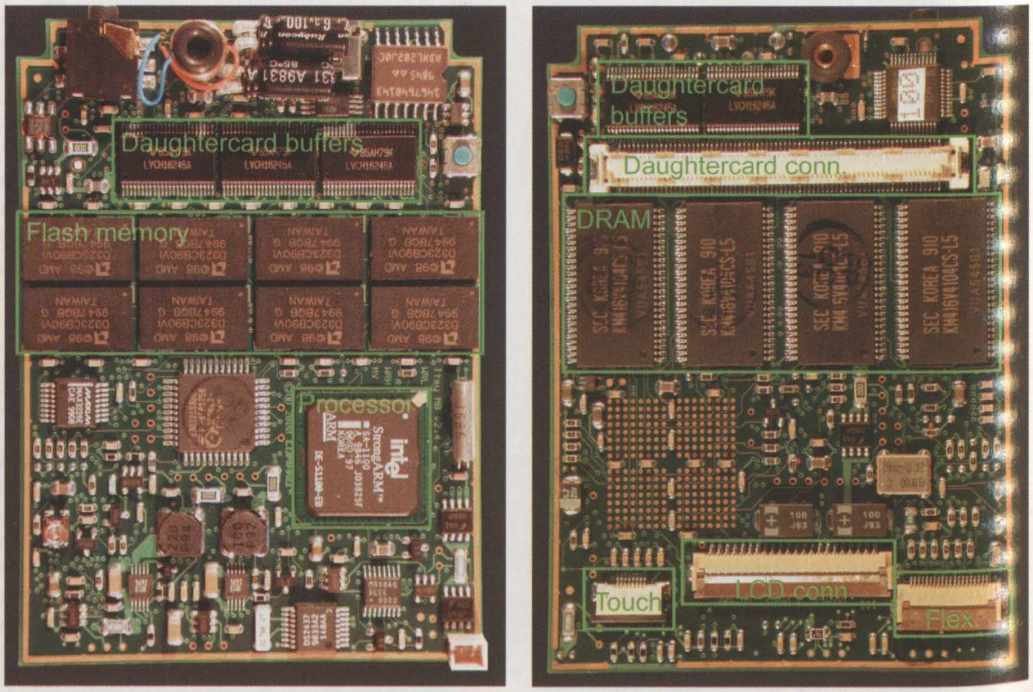

Figure 2. The (a) top and (b) bottom sides of the Itsy v2 motherboard. Using micro-ball-grid array packages for the processor and flash memory offers a very high mounting density.

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